IRHYS9A97230CM, IRHYB9A97230CM

PD-97960B

Radiation Hardened Power MOSFET
Thru-Hole (Low-Ohmic TO-257AA)
-200V, -14A, P-channel, R9 Superjunction Technology

Features

- Single event effect (SEE) hardened
  (up to LET of 90.5 MeV·cm^2/mg)
- Improved SOA for linear mode operation
- Low $R_{DS(on)}$
- Improved avalanche energy
- Simple drive requirements
- Hermetically sealed
- Electrically isolated
- Ceramic eyelets
- ESD rating: class 2 per MIL-STD-750, Method 1020

Product Summary

- **BV_{DSS}:** -200V
- **I_D :** -14A
- **$R_{DS(on),max}$:** 175mΩ
- **$Q_{G,max}$:** 49nC
- **REF:** MIL-PRF-19500/780

Low – Ohmic TO-257AA

Tabless TO-257AA

Potential Applications

- Motor drives
- DC-DC converter
- Latching current limiter

Product Validation

Qualified according to MIL-PRF-19500 for space applications

Description

IR HiRel R9 technology provides superior power MOSFETs for space applications. This family of p-channel MOSFETs are the first radiation hardened devices that are based on a superjunction technology. These devices have improved immunity to Single Event Effect (SEE) and have been characterized for useful performance with Linear Energy Transfer (LET) up to 90.5 MeV·cm^2/mg. Their combination of low $R_{DS(on)}$ and improved SOA allows for better performance in applications such as Latching Current Limiters (LCL), Solid-State Power Controllers (SSPC) or DC-DC converters. These devices retain all of the well-established advantages of MOSFETs such as voltage control, fast switching and temperature stability of electrical parameters.

Ordering Information

Table 1 Ordering options

Part number	Package	Screening Level	TID Level
IRHYS9A97230CM	Low-Ohmic TO-257AA	COTS	100 krad(Si)
JANSR2N7661T3	Low-Ohmic TO-257AA	JANS	100 krad(Si)
IRHYS9A93230CM	Low-Ohmic TO-257AA	COTS	300 krad(Si)
JANSF2N7661T3	Low-Ohmic TO-257AA	JANS	300 krad(Si)
IRHYB9A97230CM	Tabless TO-257AA	COTS	100 krad(Si)
JANSR2N7661D5	Tabless TO-257AA	JANS	100 krad(Si)
IRHYB9A93230CM	Tabless TO-257AA	COTS	300 krad(Si)
JANSF2N7661D5	Tabless TO-257AA	JANS	300 krad(Si)

Table of contents

1 Absolute Maximum Ratings

Table 2 Absolute Maximum Ratings (Pre-Irradiation)

Symbol	Parameter	Value	Unit
I_{D1} @ V_{GS} = -12V, T_C = 25°C	Continuous Drain Current	-14	A
I_{D2} @ V_{GS} = -12V, T_C = 100°C	Continuous Drain Current	-9.0	A
I_{DM} @ T_C = 25°C	Pulsed Drain Current [1]	-56	A
P_D @ T_C = 25°C	Maximum Power Dissipation	75	W
	Linear Derating Factor	0.6	W/°C
V_{GS}	Gate-to-Source Voltage	± 20	V
E_{AS}	Single Pulse Avalanche Energy [2]	770	mJ
I_{AR}	Avalanche Current [1]	-9.0	A
E_{AR}	Repetitive Avalanche Energy [1]	7.5	mJ
dv/dt	Peak Diode Reverse Recovery [3]	-20	V/ns
T_J T_{STG}	Operating Junction and Storage Temperature Range	-55 to +150	°C
	Lead Temperature	300 (0.063in./1.6mm from case for 10s)	°C
	Weight	4.3 (Typical)	g

[1] Repetitive Rating; Pulse width limited by maximum junction temperature.

[2] V_{DD} = -125V, starting T_J = 25°C, L = 19mH, Peak I_L = -9A, V_{GS} = -20V

[3] $I_{SD} \leq$ -14A, di/dt $\leq$ -905A/µs, $V_{DD} \leq$ -200V, $T_J \leq$ 150°C

2 Device Characteristics

2.1 Electrical Characteristics (Pre-Irradiation)

Table 3 Static and Dynamic Electrical Characteristics @ T_j = 25°C (Unless Otherwise Specified)

Symbol	Parameter	Min.	Typ.	Max.	Unit	Test Conditions
BV_{DSS}	Drain-to-Source Breakdown Voltage	-200	—	—	V	V_{GS} = 0V, I_D = -1.0mA
$\Delta BV_{DSS}/\Delta T_J$	Breakdown Voltage Temp. Coefficient	—	-0.22	—	V/°C	Reference to 25°C, I_D = -1.0mA
$R_{DS(on)}$	Static Drain-to-Source On-State Resistance	—	—	175	mΩ	V_{GS} = -12V, I_{D2} = -9A [1]
$V_{GS(th)}$	Gate Threshold Voltage	-2.0	—	-4.0	V	$V_{DS} \geq V_{GS}$, I_D = -1mA
$\Delta V_{GS(th)}/\Delta T_J$	Gate Threshold Voltage Coefficient	—	5.0	—	mV/°C	
Gfs	Forward Transconductance	5.4	—	—	S	V_{DS} = -15V, I_{D2} = -9A [1]
I_{DSS}	Zero Gate Voltage Drain Current	—	—	-10	µA	V_{DS} = -160V, V_{GS} = 0V
		—	—	-25		V_{DS} = -160V, V_{GS} = 0V, T_J = 125°C
I_{GSS}	Gate-to-Source Leakage Forward	—	—	-100	nA	V_{GS} = -20V
	Gate-to-Source Leakage Reverse	—	—	100		V_{GS} = 20V
Q_G	Total Gate Charge	—	—	49	nC	I_{D1} = -14A V_{DS} = -100V V_{GS} = -12V
Q_{GS}	Gate-to-Source Charge	—	—	16		
Q_{GD}	Gate-to-Drain ('Miller') Charge	—	—	12		
$t_{d(on)}$	Turn-On Delay Time	—	—	18	ns	I_{D1} = -14A ** V_{DD} = -100V R_G = 7.5Ω V_{GS} = -12V
t_r	Rise Time	—	—	30		
$t_{d(off)}$	Turn-Off Delay Time	—	—	84		
t_f	Fall Time	—	—	30		
$L_s + L_D$	Total Inductance	—	6.8	—	nH	Measured from Drain lead (6mm / 0.25in. from package) to Source lead (6mm / 0.25in. from package) with Source wires internally bonded from Source Pin to Drain Pad
C_{iss}	Input Capacitance	—	2215	—	pF	V_{GS} = 0V V_{DS} = -25V f = 1.0MHz
C_{oss}	Output Capacitance	—	270	—		
C_{rss}	Reverse Transfer Capacitance	—	6.0	—		
R_G	Gate Resistance	—	5.0	—	Ω	f = 1.0MHz, open drain

** Switching speed maximum limits are based on manufacturing test equipment and capability.

[1] Pulse width ≤ 300 µs; Duty Cycle ≤ 2%

2.2 Source-Drain Diode Ratings and Characteristics (Pre-Irradiation)

Table 4 Source-Drain Diode Characteristics

Symbol	Parameter	Min.	Typ.	Max.	Unit	Test Conditions
I_S	Continuous Source Current (Body Diode)	—	—	-14	A	
I_{SM}	Pulsed Source Current (Body Diode) [1]	—	—	-56	A	
V_{SD}	Diode Forward Voltage	—	—	-1.3	V	T_J = 25°C, I_S = -14A, V_{GS} = 0V [2]
t_{rr}	Reverse Recovery Time	—	159	239	ns	T_J = 25°C, I_F = -14A, V_{DD} ≤ -25V di/dt = -100A/µs
Q_{rr}	Reverse Recovery Charge	—	1.1	—	µC	
t_{on}	Forward Turn-On Time	Intrinsic turn-on time is negligible (turn-on is dominated by L_S+L_D)				

2.3 Thermal Characteristics

Table 5 Thermal Resistance

Symbol	Parameter	Min.	Typ.	Max.	Unit
$R_{\theta JC}$	Junction-to-Case	—	—	1.67	°C/W
$R_{\theta JA}$	Junction-to-Ambient	—	—	80	

2.4 Radiation Characteristics

IR HiRel Radiation Hardened MOSFETs are tested to verify their radiation hardness capability. The hardness assurance program at IR HiRel is comprised of two radiation environments. Every manufacturing lot is tested for total ionizing dose (per notes 3 and 4) using the TO-3 package. Both pre- and post-irradiation performance are tested and specified using the same drive circuitry and test conditions in order to provide a direct comparison.

2.4.1 Electrical Characteristics — Post Total Dose Irradiation

Table 6 Electrical Characteristics @ T_j = 25°C, Post Total Dose Irradiation [3, 4]

Symbol	Parameter	Up to 300krads (Si)[5]		Unit	Test Conditions
		Min.	Max.		
BV_{DSS}	Drain-to-Source Breakdown Voltage	-200	—	V	V_{GS} = 0V, I_D = -1mA
$V_{GS(th)}$	Gate Threshold Voltage	-2.0	-4.0	V	V_{DS} ≥ V_{GS}, I_D = -1mA
I_{GSS}	Gate-to-Source Leakage Forward	—	-100	nA	V_{GS} = -20V
	Gate-to-Source Leakage Reverse	—	100		V_{GS} = 20V
I_{DSS}	Zero Gate Voltage Drain Current	—	-10	µA	V_{DS} = -160V, V_{GS} = 0V
$R_{DS(on)}$	Static Drain-to-Source On-State Resistance (TO-3) [2]	—	175	mΩ	V_{GS} = -12V, I_{D2} = -9A
$R_{DS(on)}$	Static Drain-to-Source On-State Resistance (Low-Ohmic TO-257AA)[2]	—	175	m Ω	V_{GS} = -12V, I_{D2} = -9A
V_{SD}	Diode Forward Voltage	—	-1.3	V	V_{GS} = 0V, I_F = -14A

[1] Repetitive Rating; Pulse width limited by maximum junction temperature.
[2] Pulse width ≤ 300 µs; Duty Cycle ≤ 2%
[3] Total Dose Irradiation with V_{GS} Bias. V_{GS} =- 12V applied and V_{DS} = 0 during irradiation per MIL-STD-750, Method 1019, condition A.
[4] Total Dose Irradiation with V_{DS} Bias. V_{DS} = -160V applied and V_{GS} = 0 during irradiation per MIL-STD-750, Method 1019, condition A.
[5] Part numbers IRHYS9A97230CM (JANSR2N7661T3), IRHYS9A93230CM (JANSF2N7661T3), IRHYB9A97230CM (JANSR2N7661D5), and IRHYB9A93230CM (JANSF2N7661D5)

2.4.2 Single Event Effects — Safe Operating Area

IR HiRel radiation hardened MOSFETs have been characterized in heavy ion environment for Single Event Effects (SEE). Single Event Effects characterization is illustrated in Fig. 1 and Table 7.

Table 7 Typical Single Event Effects Safe Operating Area

LET ($MeV\cdot cm^2/mg$)	Energy (MeV)	Range (µm)	V_{DS} (V)			
			V_{GS} = 0V	V_{GS} = 3V	V_{GS} = 5V	V_{GS} = 10V
38.4 ± 5%	420± 7.5%	51.9 ± 7.5%	-200	-200	-200	-200
66.4 ± 5%	783 ± 7.5%	59.4 ± 7.5%	-200	-200	-200	—
90.5 ± 5%	1430 ± 7.5%	80.4± 7.5%	-200	-200	—	—

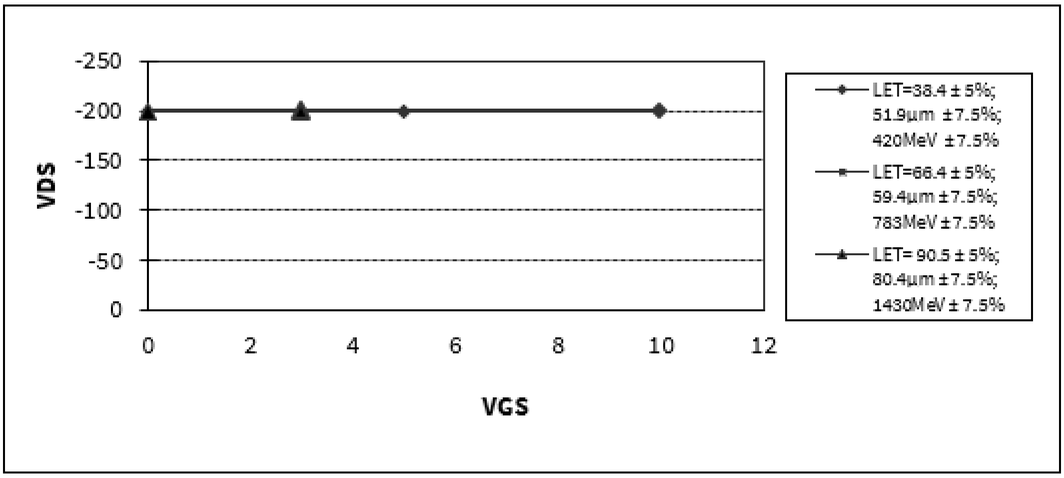


Figure 1 Typical Single Event Effect, Safe Operating Area

3 Electrical Characteristics Curves (Pre-irradiation)

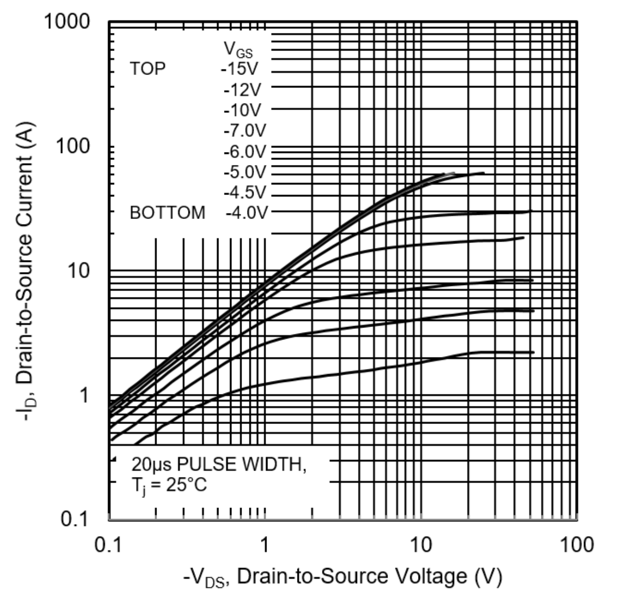


Figure 2 Typical Output Characteristics

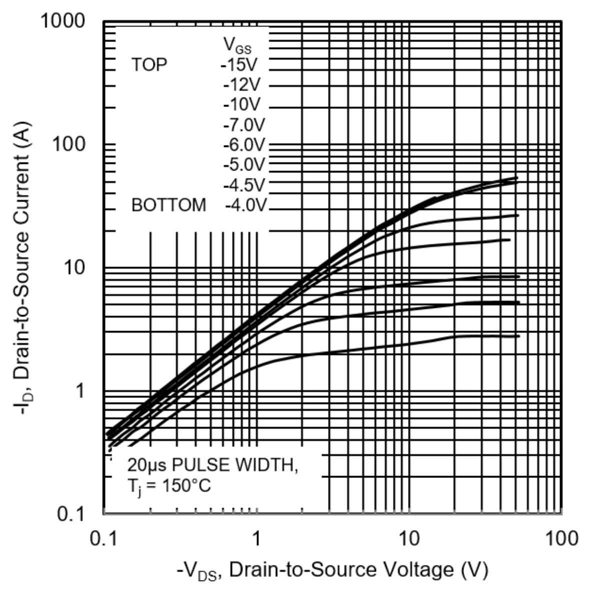


Figure 3 Typical Output Characteristics

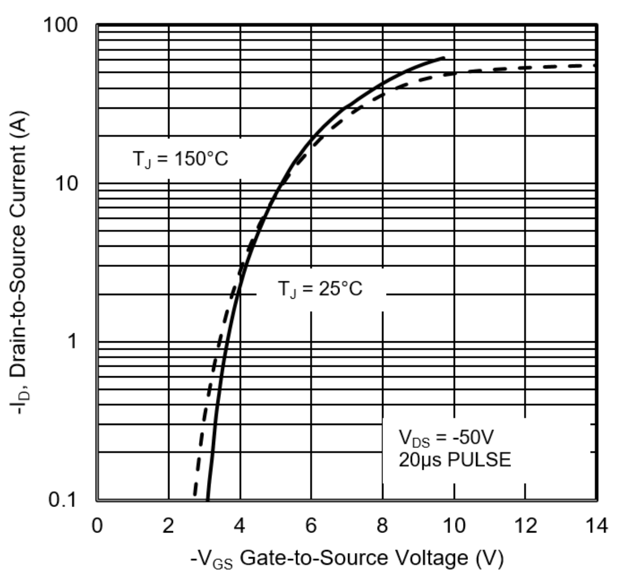


Figure 4 Typical Transfer Characteristics

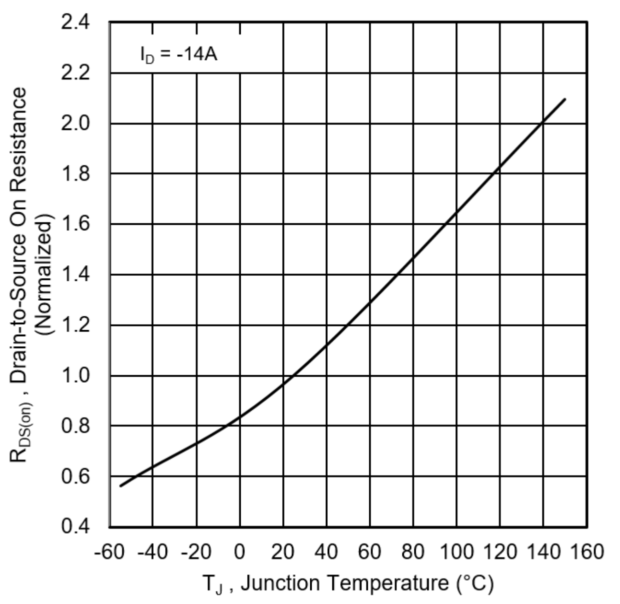


Figure 5 Normalized On-Resistance Vs. Temperature

Electrical Characteristics Curves (Pre-irradiation)

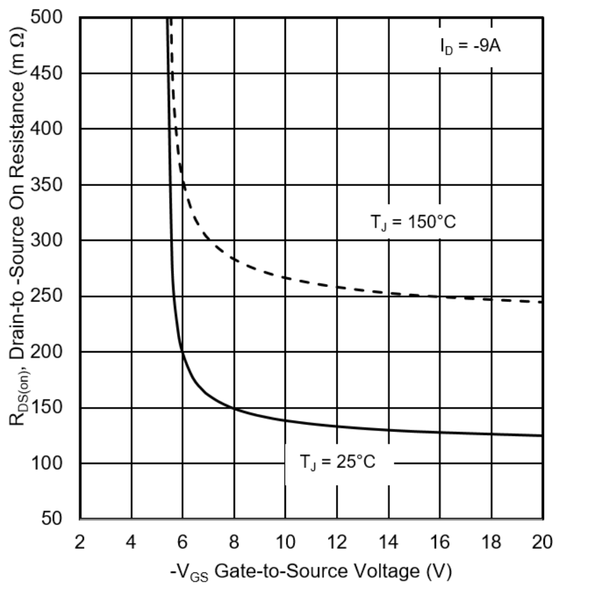


Figure 6 Typical On-Resistance Vs. Gate Voltage

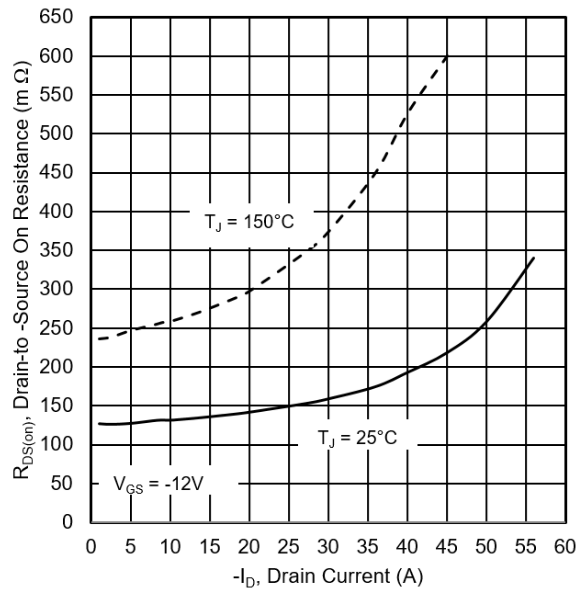


Figure 7 Typical On-Resistance Vs. Drain Current

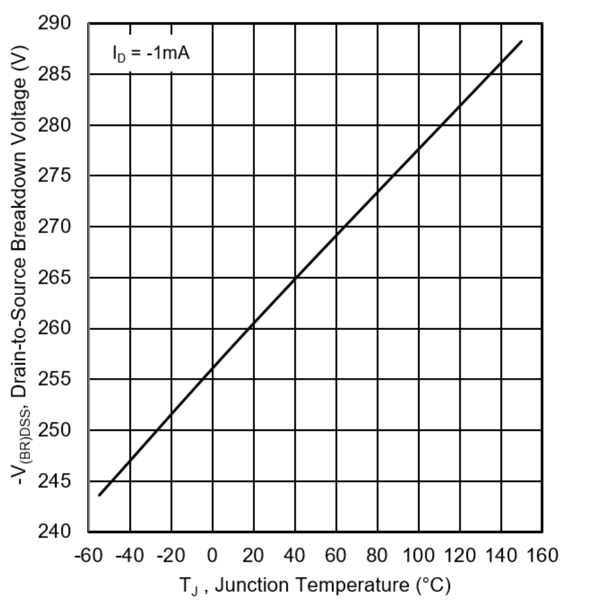


Figure 8 Typical Drain-to-Source Breakdown Voltage Vs. Temperature

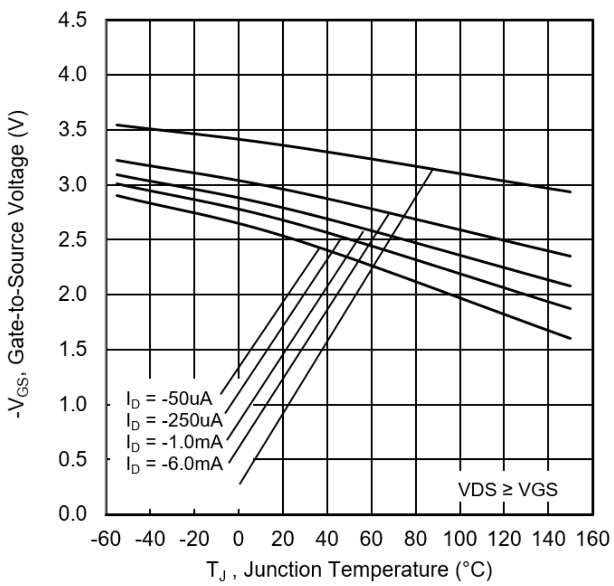


Figure 9 Typical Threshold Voltage Vs. Temperature

Electrical Characteristics Curves (Pre-irradiation)

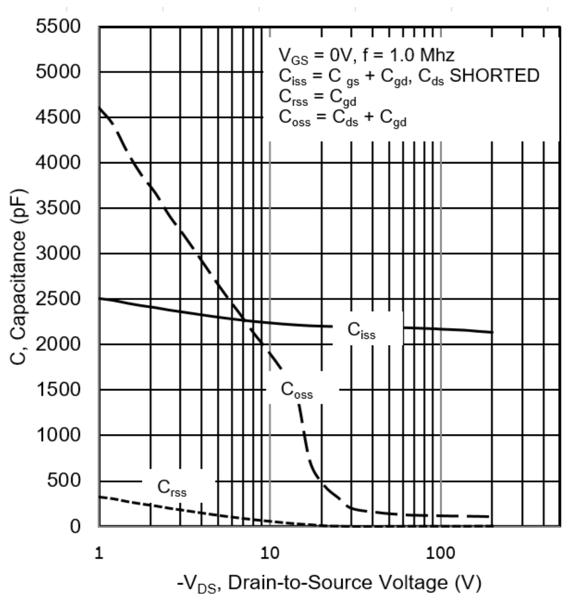


Figure 10 **Typical Capacitance Vs. Drain-to-Source Voltage**

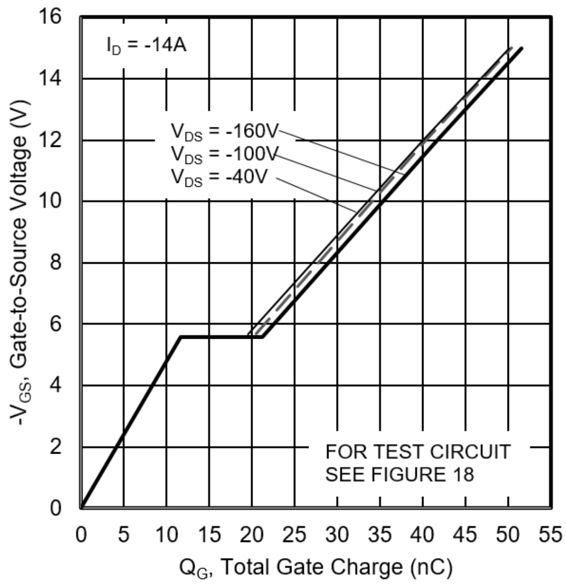


Figure 11 **Typical Gate-to-Source Voltage Vs. Gate Charge**

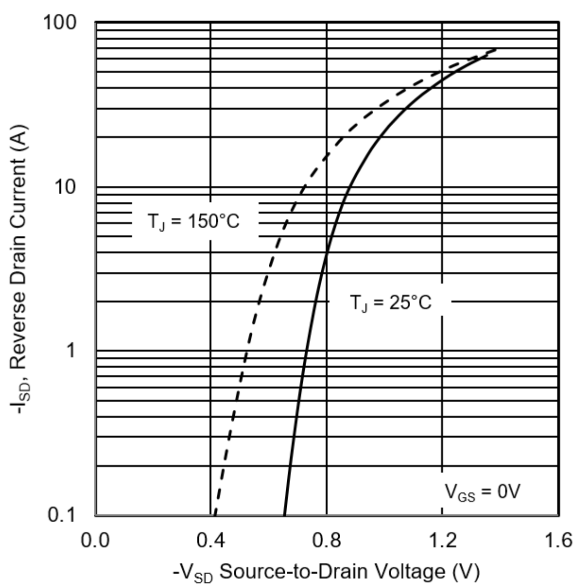


Figure 12 **Typical Source-Drain Current Vs. Diode Forward Voltage**

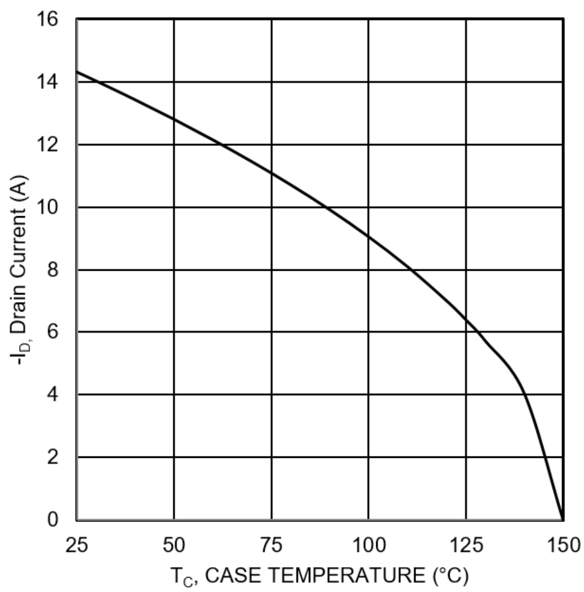


Figure 13 **Maximum Drain Current Vs. Case Temperature**

Electrical Characteristics Curves (Pre-irradiation)

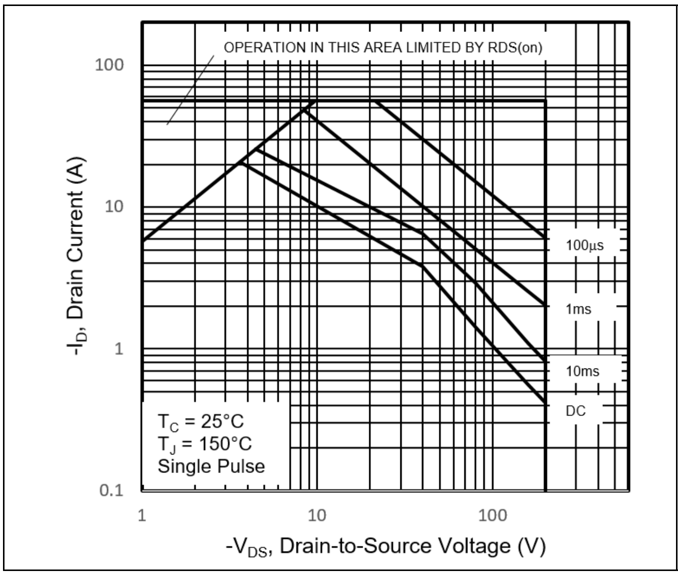


Figure 14 Maximum Safe Operating Area

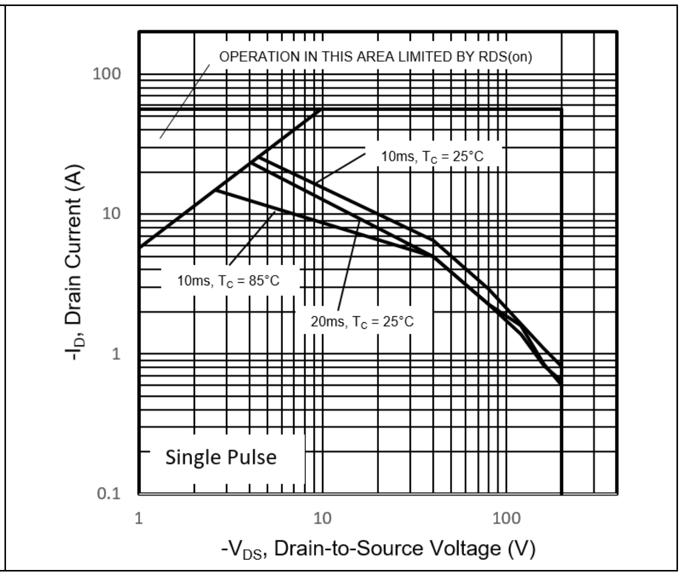


Figure 15 Maximum Safe Operating Area

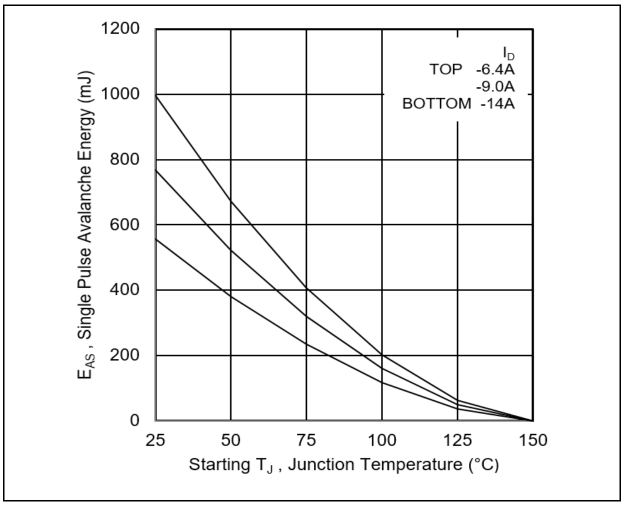


Figure 16 Maximum Avalanche Energy Vs. Junction Temperature

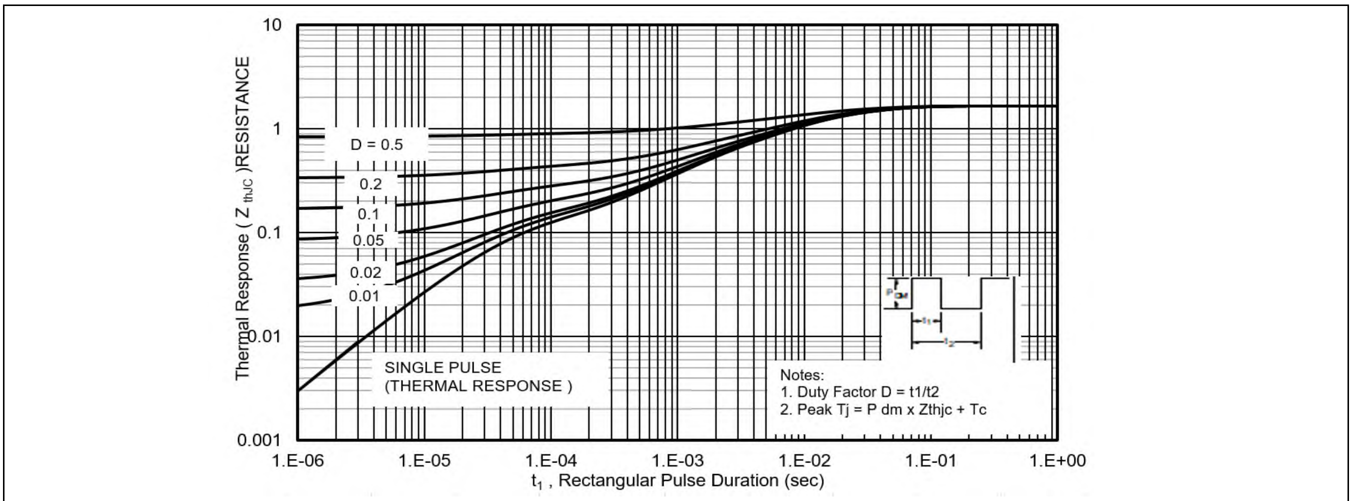


Figure 17 Maximum Effective Transient Thermal Impedance, Junction-to-Case

4 Test Circuits (Pre-irradiation)

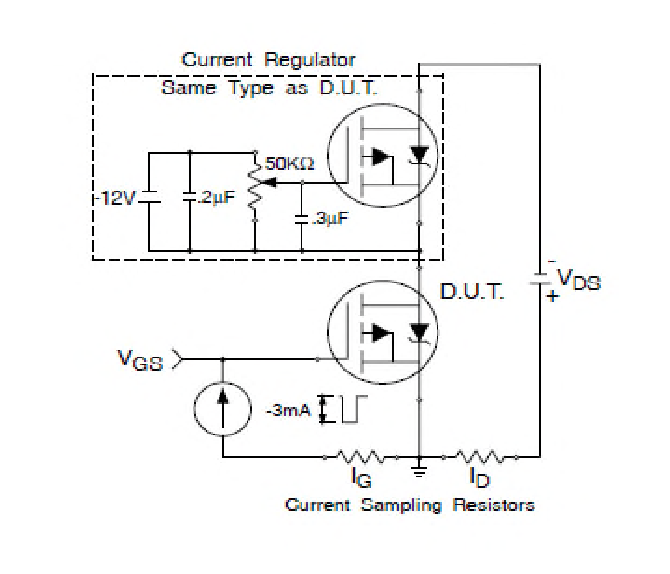


Figure 18 Gate Charge Test Circuit

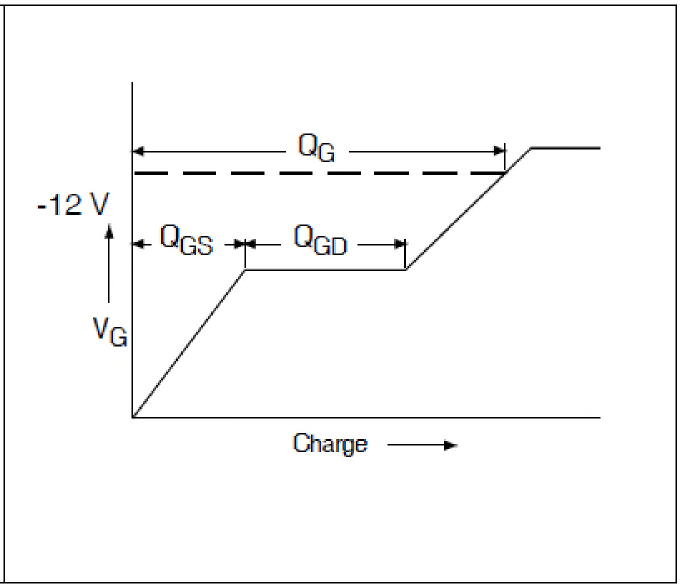


Figure 19 Gate Charge Waveform

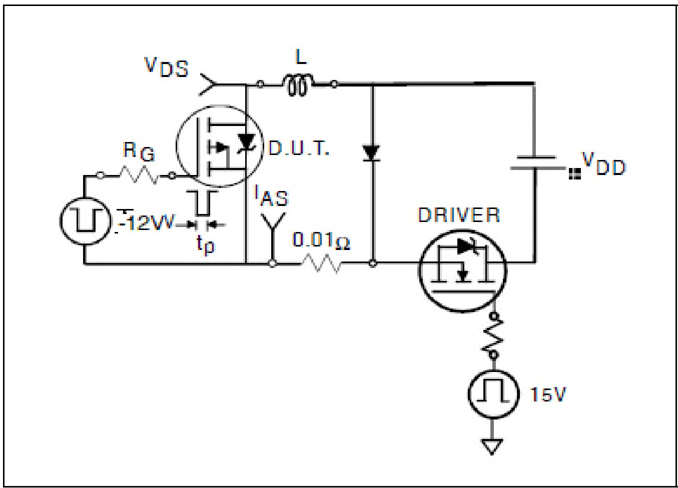


Figure 20 Unclamped Inductive Test Circuit

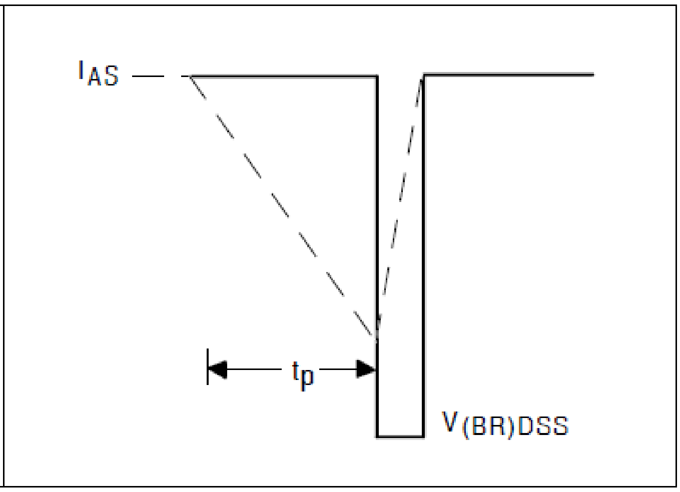


Figure 21 Unclamped Inductive Waveform

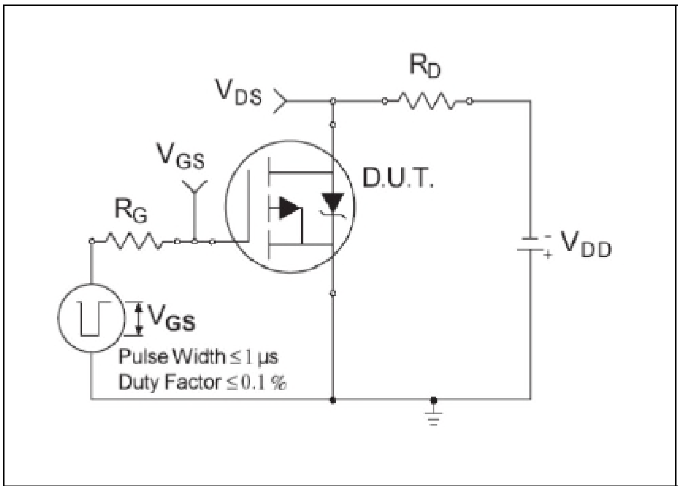


Figure 22 Switching Time Test Circuit

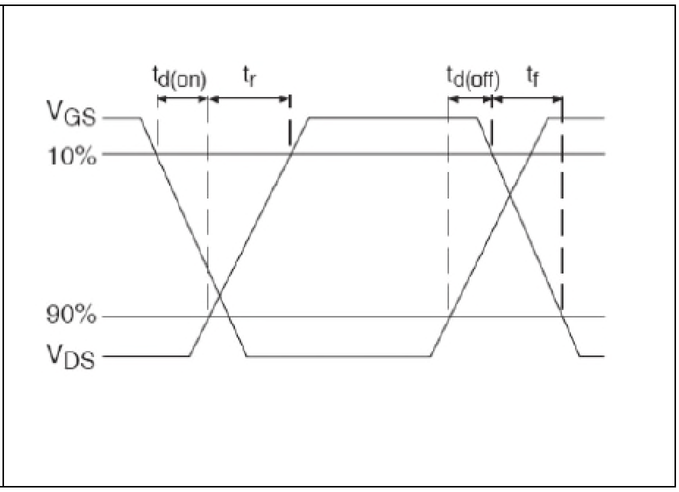
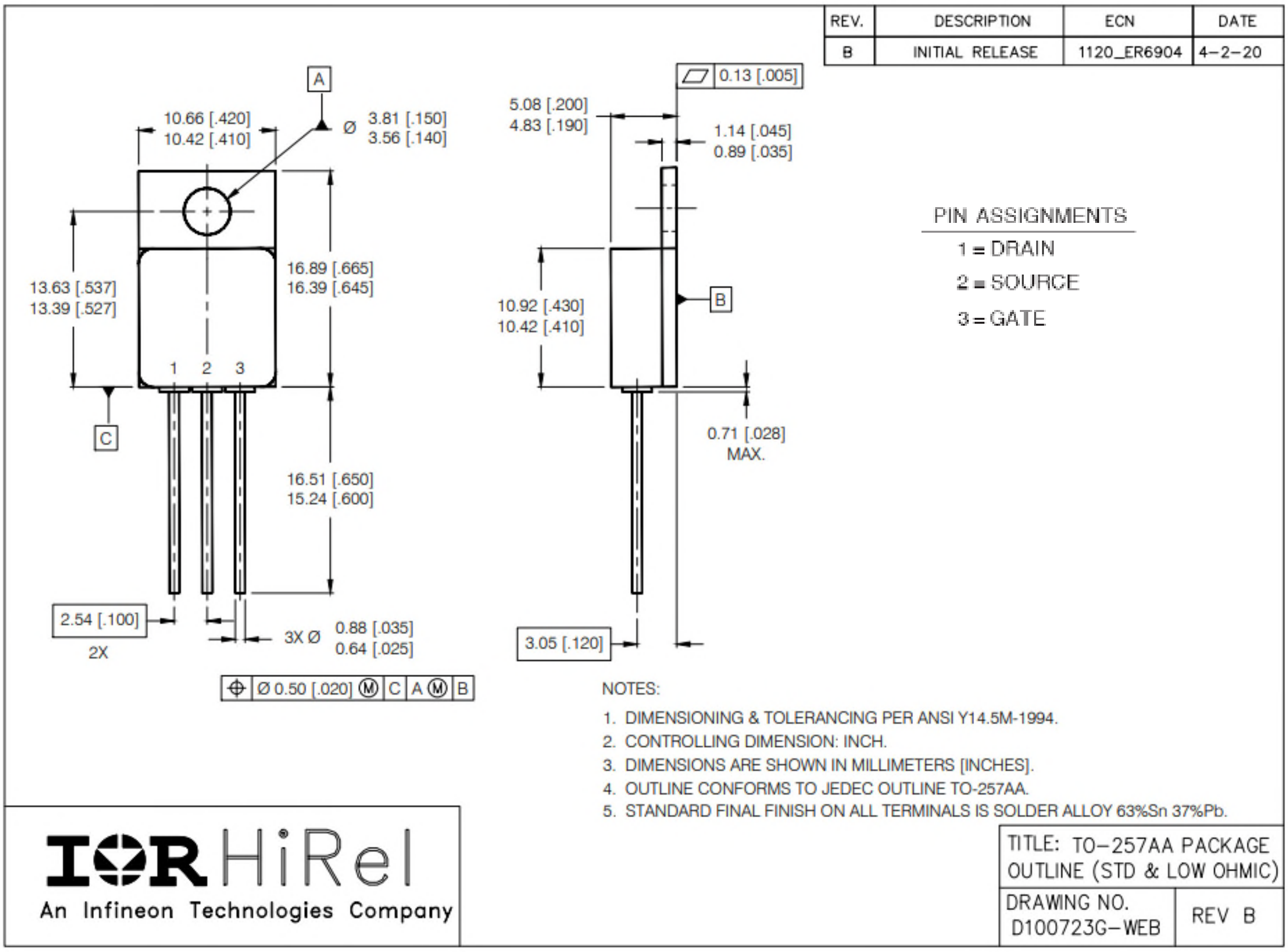


Figure 23 Switching Time Waveforms

5 Package Outline (Low-Ohmic TO-257AA)

Note: For the most updated package outline, please see the website: (Low-Ohmic TO-257AA)

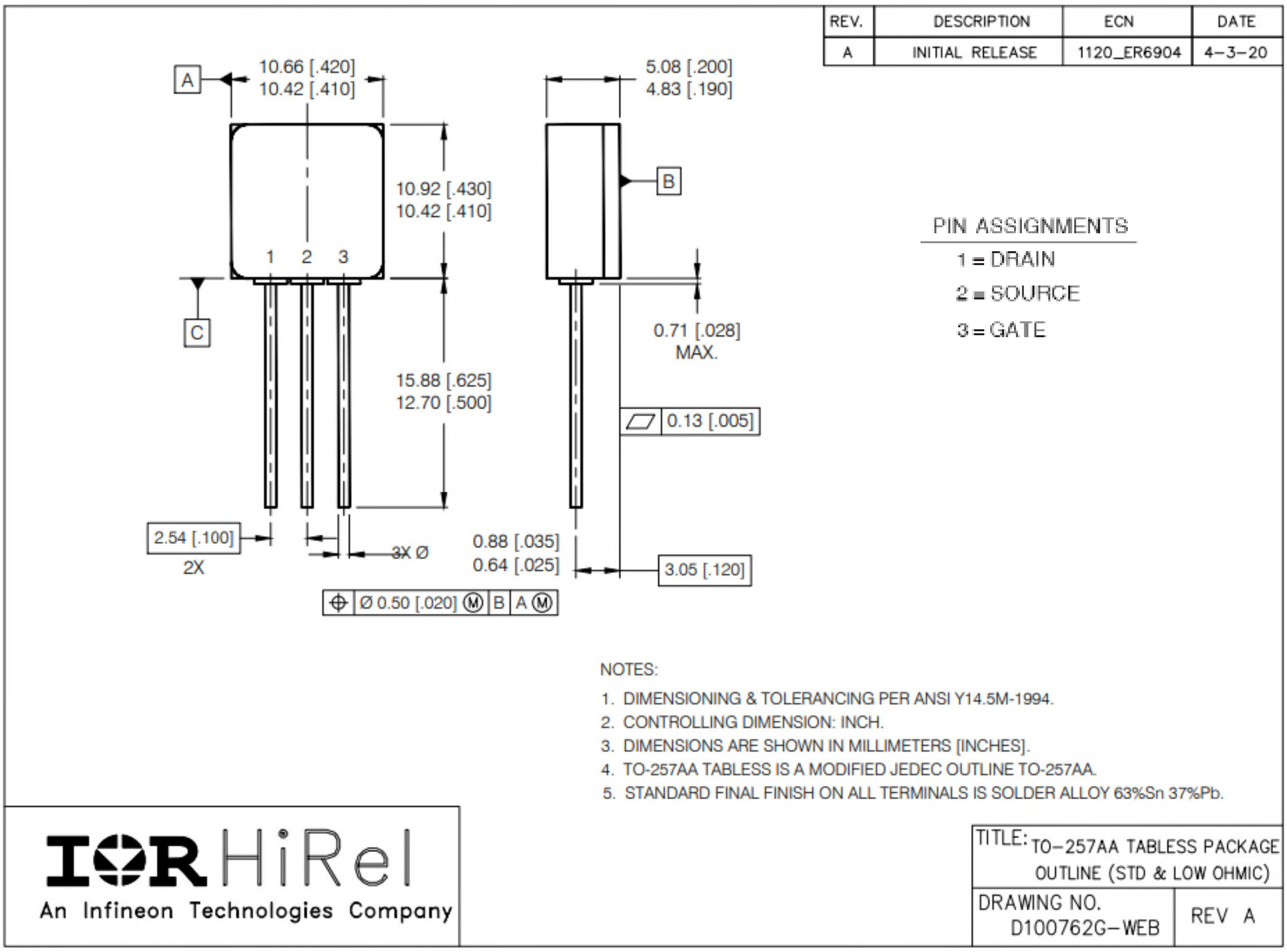


BERYLLIA WARNING PER MIL-PRF-19500

Package containing beryllia shall not be ground, sandblasted, machined, or have other operations performed on them which will produce beryllia or beryllium dust. Furthermore, beryllium oxide packages shall not be placed in acids that will produce fumes containing beryllium.

6 Package Outline (Tabless TO-257AA)

Note: For the most updated package outline, please see the website: Tabless TO-257AA



BERYLLIA WARNING PER MIL-PRF-19500

Package containing beryllia shall not be ground, sandblasted, machined, or have other operations performed on them which will produce beryllia or beryllium dust. Furthermore, beryllium oxide packages shall not be placed in acids that will produce fumes containing beryllium.

Revision history

Document version	Date of release	Description of changes
	10/19/2022	Preliminary datasheet with PPD number (PPD-97960A)
Rev B	12/13/2022	Final datasheet with PD number

Trademarks

All referenced product or service names and trademarks are the property of their respective owners.

Edition 2022-12-13

Published by

International Rectifier HiRel Products, Inc.

An Infineon Technologies company

El Segundo, California 90245 USA

Do you have a question about this document?

Email: erratum@infineon.com

Document reference