

IRL3302SPbF

HEXFET® Power MOSFET

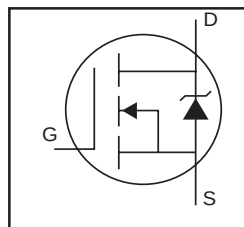
- Advanced Process Technology
- Surface Mount
- Optimized for 4.5V-7.0V Gate Drive
- Ideal for CPU Core DC-DC Converters
- Fast Switching

• Lead-Free

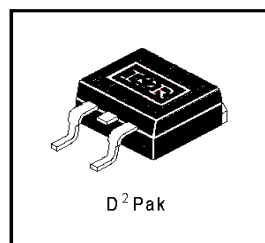
Description

These HEXFET Power MOSFETs were designed specifically to meet the demands of CPU core DC-DC converters. Advanced processing techniques combined with an optimized gate oxide design results in a die sized specifically to offer maximum efficiency at minimum cost.

The D²Pak is a surface mount power package capable of accommodating die sizes up to HEX-4. It provides the highest power capability and the lowest possible on-resistance in any existing surface mount package. The D²Pak is suitable for high current applications because of its low internal connection resistance and can dissipate up to 2.0W in a typical surface mount application.



$V_{DS} = 20V$
$R_{DS(on)} = 0.020\Omega$
$I_D = 39A$



Absolute Maximum Ratings

	Parameter	Max.	Units
$I_D @ T_C = 25^\circ C$	Continuous Drain Current, $V_{GS} @ 4.5V$ ⑤	39	A
$I_D @ T_C = 100^\circ C$	Continuous Drain Current, $V_{GS} @ 4.5V$ ⑤	25	
I_{DM}	Pulsed Drain Current ①⑤	160	
$P_D @ T_C = 25^\circ C$	Power Dissipation	57	W
	Linear Derating Factor	0.45	W/°C
V_{GS}	Gate-to-Source Voltage	± 10	V
E_{AS}	Single Pulse Avalanche Energy②⑤	130	mJ
I_{AR}	Avalanche Current①	23	A
E_{AR}	Repetitive Avalanche Energy①	5.7	mJ
dv/dt	Peak Diode Recovery dv/dt ③⑤	5.0	V/ns
T_J	Operating Junction and	-55 to + 150	°C
T_{STG}	Storage Temperature Range		
	Soldering Temperature, for 10 seconds	300 (1.6mm from case)	

Thermal Resistance

	Parameter	Typ.	Max.	Units
R_{gJC}	Junction-to-Case	—	2.2	°C/W
R_{gJA}	Junction-to-Ambient (PCB Mounted, steady-state)**	—	40	

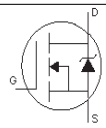
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Electrical Characteristics @ $T_J = 25^\circ\text{C}$ (unless otherwise specified)

	Parameter	Min.	Typ.	Max.	Units	Conditions
$V_{(BR)DSS}$	Drain-to-Source Breakdown Voltage	20	—	—	V	$V_{GS} = 0V$, $I_D = 250\mu A$
$DV_{(BR)DSS}/dT_J$	Breakdown Voltage Temp. Coefficient	—	0.022	—	V/ $^\circ\text{C}$	Reference to 25°C , $I_D = 1mA$ ⑤
$R_{DS(on)}$	Static Drain-to-Source On-Resistance	—	—	0.023	Ω	$V_{GS} = 4.5V$, $I_D = 23A$ ④
		—	—	0.020		$V_{GS} = 7.0V$, $I_D = 23A$ ④
$V_{GS(th)}$	Gate Threshold Voltage	0.70	—	—	V	$V_{DS} = V_{GS}$, $I_D = 250\mu A$
g_{fs}	Forward Transconductance	21	—	—	S	$V_{DS} = 10V$, $I_D = 23A$ ⑤
I_{DSS}	Drain-to-Source Leakage Current	—	—	25	μA	$V_{DS} = 20V$, $V_{GS} = 0V$
		—	—	250		$V_{DS} = 10V$, $V_{GS} = 0V$, $T_J = 150^\circ\text{C}$
I_{GSS}	Gate-to-Source Forward Leakage	—	—	100	nA	$V_{GS} = 10V$
	Gate-to-Source Reverse Leakage	—	—	-100		$V_{GS} = -10V$
Q_g	Total Gate Charge	—	—	31	nC	$I_D = 23A$
Q_{gs}	Gate-to-Source Charge	—	—	5.7		$V_{DS} = 16V$
Q_{gd}	Gate-to-Drain ("Miller") Charge	—	—	13		$V_{GS} = 4.5V$, See Fig. 6 ④⑤
$t_{d(on)}$	Turn-On Delay Time	—	7.2	—	ns	$V_{DD} = 10V$
t_r	Rise Time	—	110	—		$I_D = 23A$
$t_{d(off)}$	Turn-Off Delay Time	—	41	—		$R_G = 9.5\Omega$, $V_{GS} = 4.5V$
t_f	Fall Time	—	89	—		$R_D = 2.4\Omega$, ④⑤
L_S	Internal Source Inductance	—	7.5	—	nH	Between lead, and center of die contact
C_{iss}	Input Capacitance	—	1300	—	pF	$V_{GS} = 0V$
C_{oss}	Output Capacitance	—	520	—		$V_{DS} = 15V$
C_{rss}	Reverse Transfer Capacitance	—	190	—		$f = 1.0MHz$, See Fig. 5⑤

Source-Drain Ratings and Characteristics

	Parameter	Min.	Typ.	Max.	Units	Conditions
I_S	Continuous Source Current (Body Diode)	—	—	39	A	MOSFET symbol showing the integral reverse p-n junction diode. 
I_{SM}	Pulsed Source Current (Body Diode) ①⑤	—	—	160		
V_{SD}	Diode Forward Voltage	—	—	1.3	V	$T_J = 25^\circ\text{C}$, $I_S = 23A$, $V_{GS} = 0V$ ④
t_{rr}	Reverse Recovery Time	—	62	94	ns	$T_J = 25^\circ\text{C}$, $I_F = 23A$
Q_{rr}	Reverse Recovery Charge	—	—	110	160	nC $di/dt = 100A/\mu s$ ④⑤
t_{on}	Forward Turn-On Time	Intrinsic turn-on time is negligible (turn-on is dominated by $L_S + L_D$)				

Notes:

- ① Repetitive rating; pulse width limited by max. junction temperature.
- ② Starting $T_J = 25^\circ\text{C}$, $L = 0.49mH$
 $R_G = 25\Omega$, $I_{AS} = 23A$.
- ③ $I_{SD} \leq 23A$, $di/dt \leq 97A/\mu s$, $V_{DD} \leq V_{(BR)DSS}$,
 $T_J \leq 150^\circ\text{C}$
- ④ Pulse width $\leq 300\mu s$; duty cycle $\leq 2\%$.
- ⑤ Uses IRL3302 data and test conditions

** When mounted on FR-4 board using minimum recommended footprint.
For recommended footprint and soldering techniques refer to application note #AN-994.

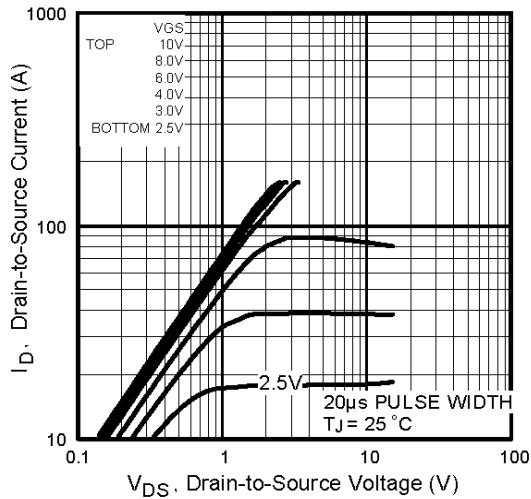


Fig 1. Typical Output Characteristics

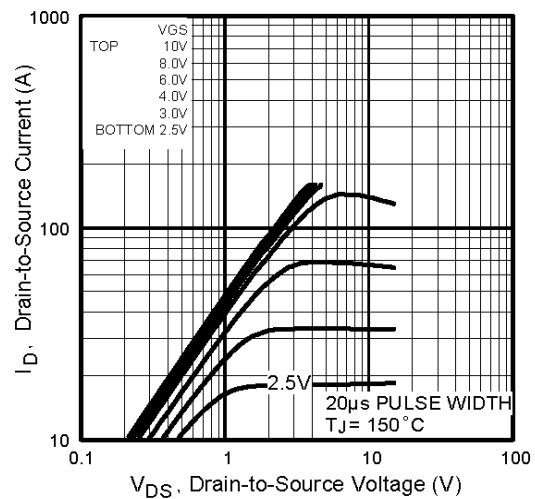


Fig 2. Typical Output Characteristics

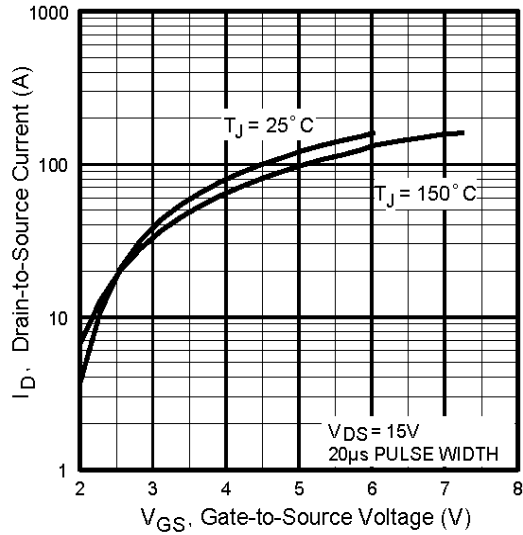


Fig 3. Typical Transfer Characteristics

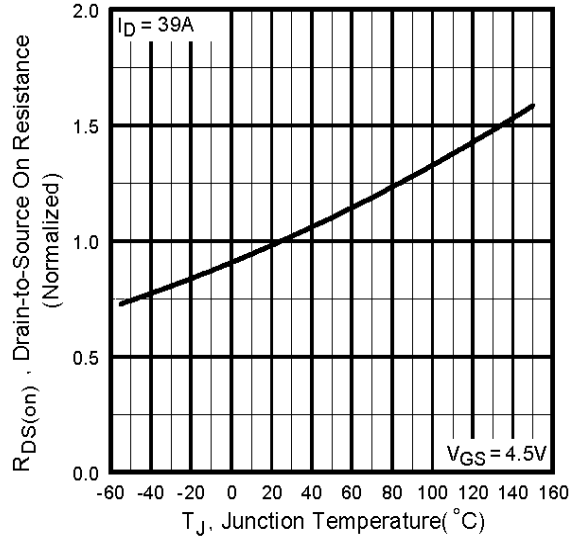
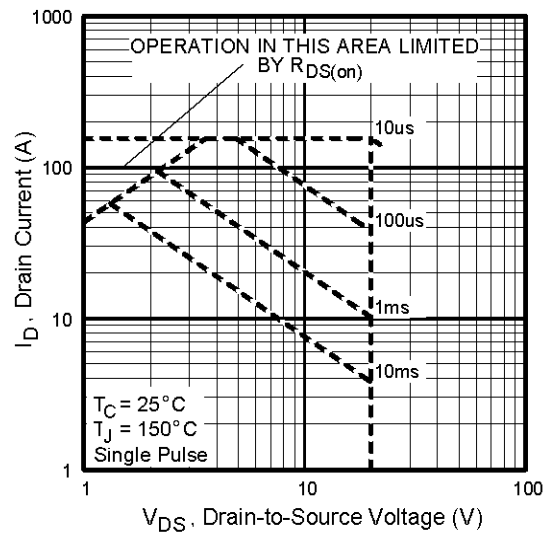
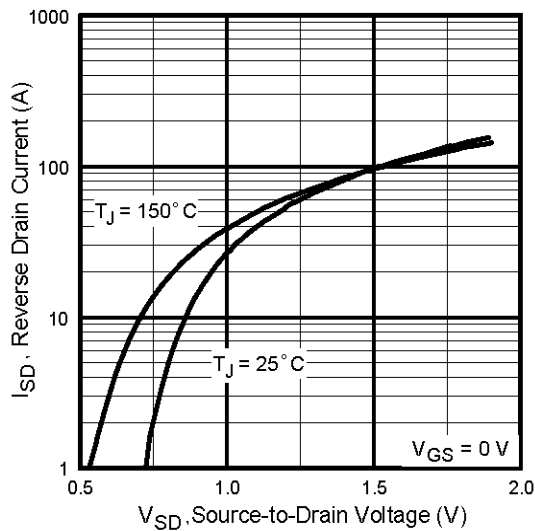
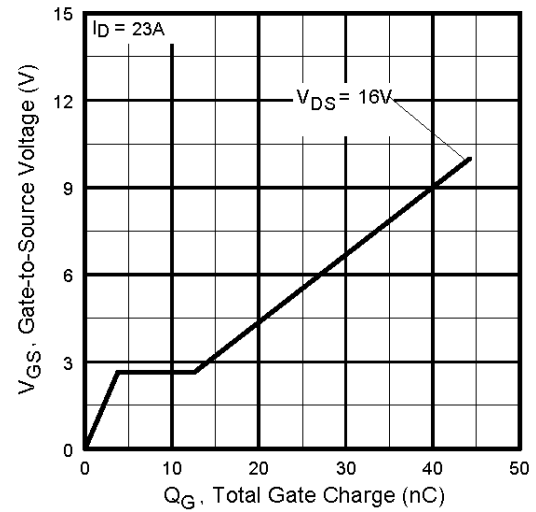
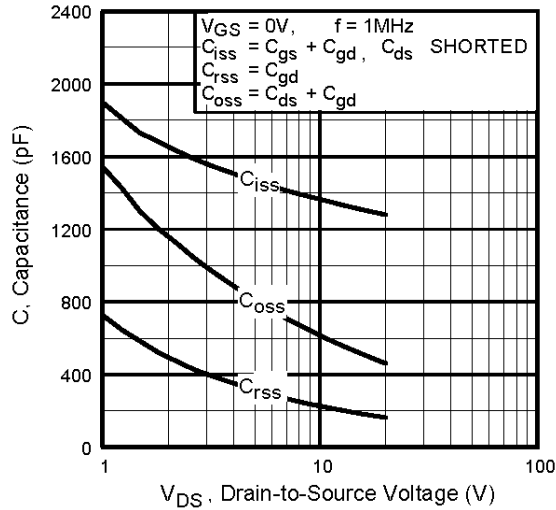


Fig 4. Normalized On-Resistance Vs. Temperature



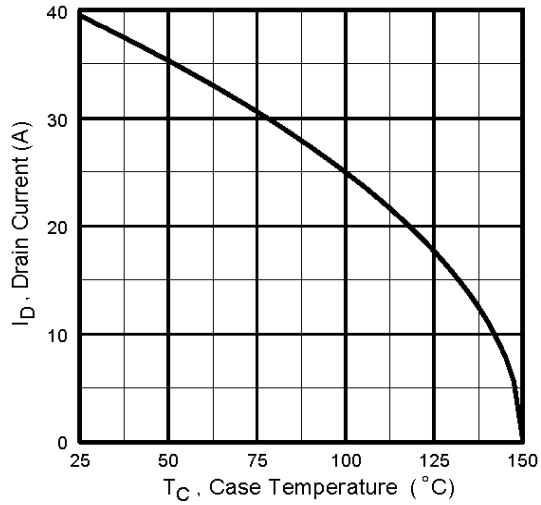


Fig 9. Maximum Drain Current Vs. Case Temperature

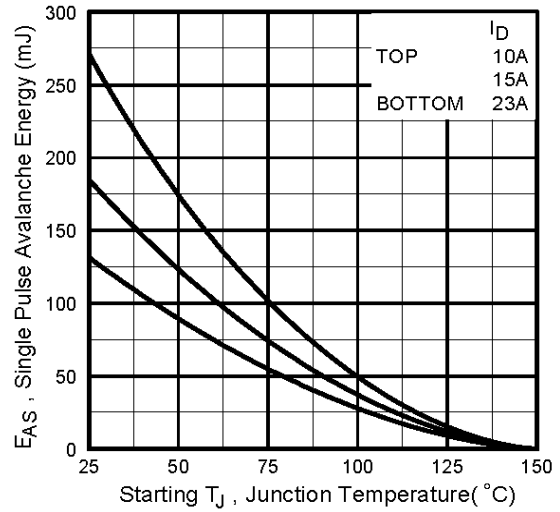


Fig 10. Maximum Avalanche Energy Vs. Drain Current

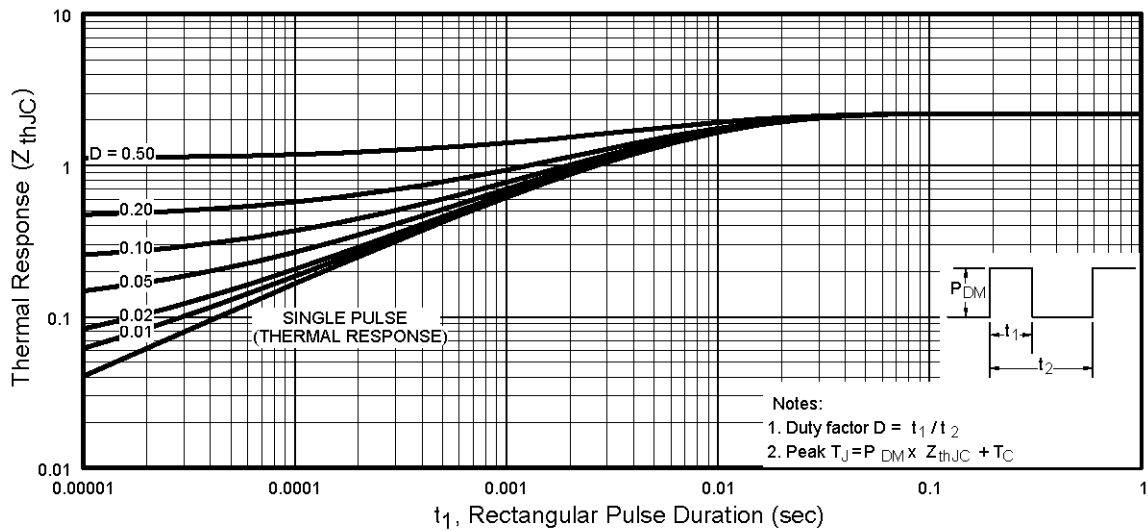


Fig 11. Maximum Effective Transient Thermal Impedance, Junction-to-Case

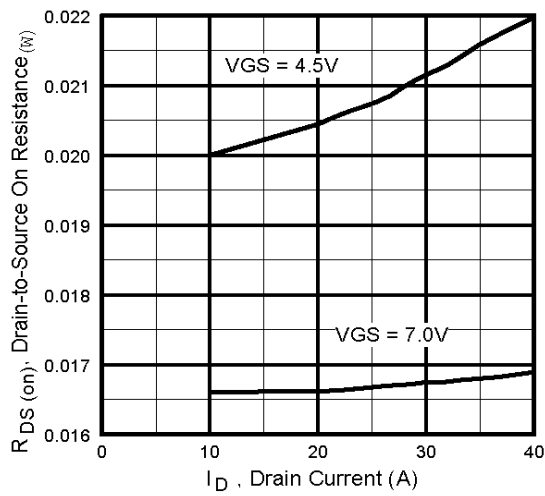


Fig 12. On-Resistance Vs. Drain Current

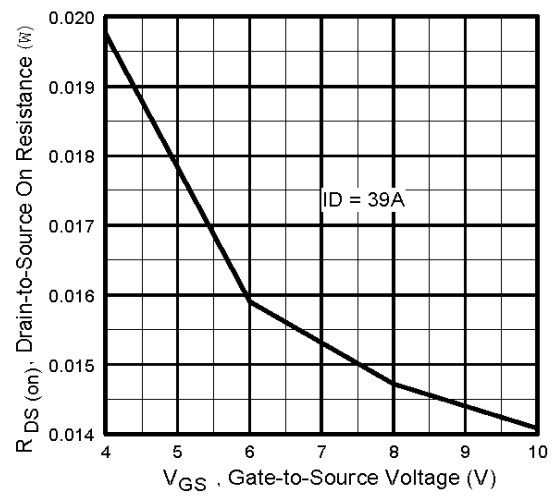
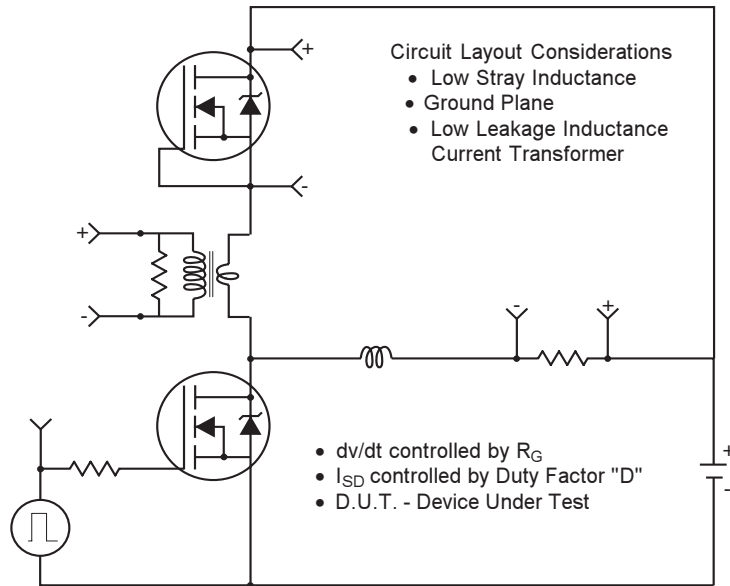


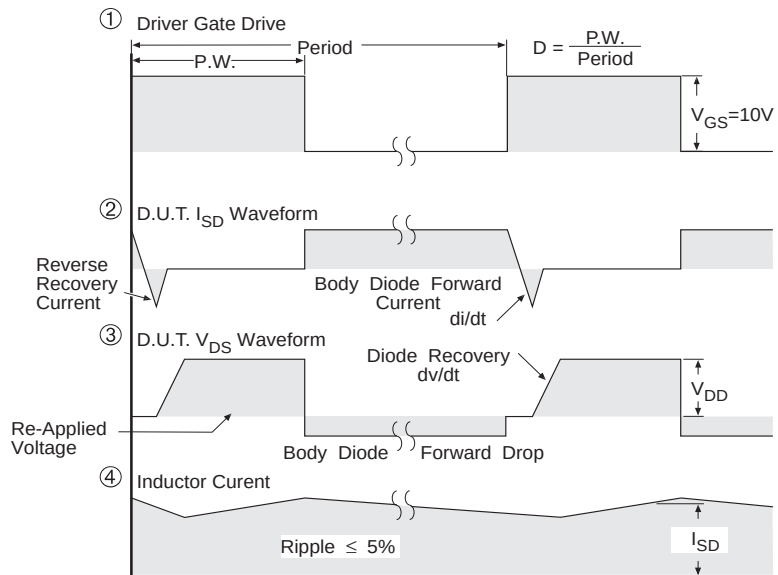
Fig 13. On-Resistance Vs. Gate Voltage

Peak Diode Recovery dv/dt Test Circuit



* Reverse Polarity for P-Channel

** Use P-Channel Driver for P-Channel Measurements



*** $V_{GS} = 5.0V$ for Logic Level and 3V Drive Devices

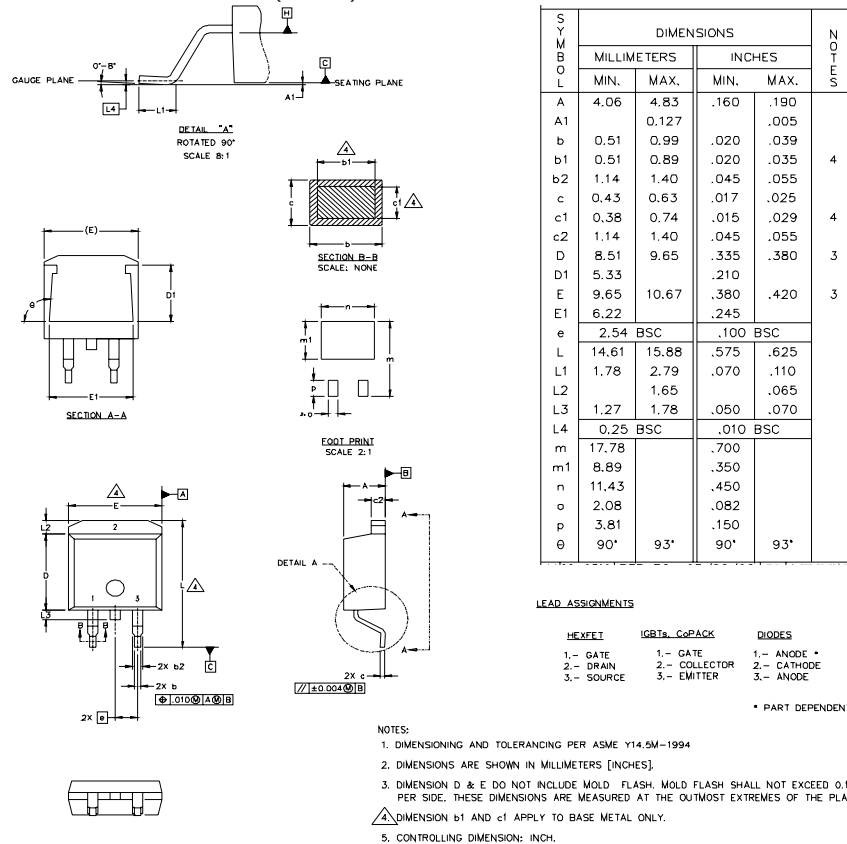
Fig 14 For N Channel HEXFETS

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D²Pak Package Outline

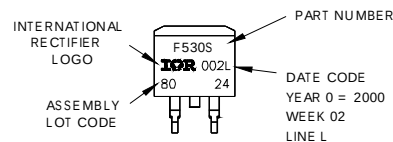
Dimensions are shown in millimeters (inches)



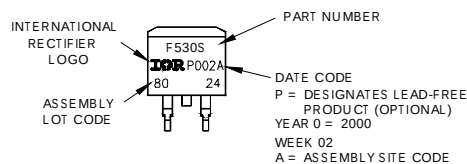
D²Pak Part Marking Information

EXAMPLE: THIS IS AN IRF530S WITH
LOT CODE 8024
ASSEMBLED ON WW 02, 2000
IN THE ASSEMBLY LINE "L"

Note: "P" in assembly line
position indicates "Lead-Free"

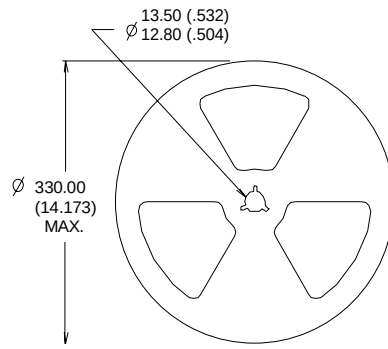
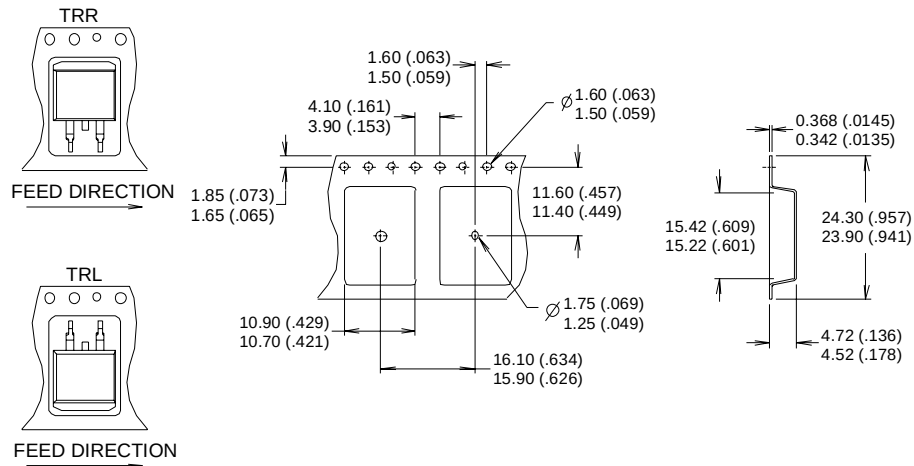


OR

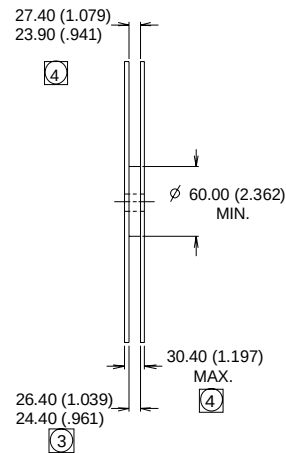


D²Pak Tape & Reel Information

Dimensions are shown in millimeters (inches)



- NOTES:
1. CONFORMS TO EIA-418.
 2. CONTROLLING DIMENSION: MILLIMETER.
 3. DIMENSION MEASURED @ HUB.
 4. INCLUDES FLANGE DISTORTION @ OUTER EDGE.



Data and specifications subject to change without notice.