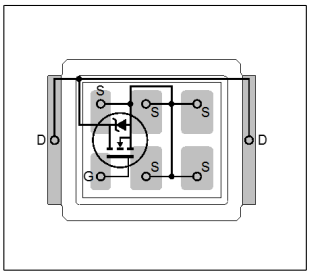
MOSFET

OptiMOS™5, 40 V

DirectFET ME



Features

Application

- Brushed Motor drive applications
- BLDC Motor drive applications
- Battery powered circuits
- Half-bridge and full-bridge topologies
- Synchronous rectifier applications
- Resonant mode power supplies
- OR-ing and redundant power switches
- DC/DC and AC/DC converters
- DC/AC Inverters

Product validation

Fully qualified according to JEDEC for Industrial Applications

Table 1 Key Performance Parameters

Parameter	Value	Unit
V_{DS}	40	V
Rds(on), max	0.82	mΩ
Id	231	A
Qoss	104	nC
Qg(0V..4.5V)	61	nC

Type / Ordering Code	Package	Marking	Related Links
IRL40DM247	MG-WDSON-8-904 (ME)	M247	-

Table of Contents

1 Maximum ratings

at T_A=25 °C, unless otherwise specified

Table 2 Maximum ratings

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Continuous drain current	I_D	- - -	- - -	231 147 43	A	V_{GS}=10 V, T_C=25 °C V_{GS}=10 V, T_C=100 °C V_{GS}=10 V, T_A=25 °C (silicon limited), R_{THJA}=45 °C/W[1]
Pulsed drain current[2]	$I_{D,pulse}$	-	-	926	A	T_C=25 °C
Avalanche energy, single pulse[3]	E_{AS}	-	-	85	mJ	I_D=50 A, R_{GS}=50 Ω
Gate source voltage	V_{GS}	-20	-	20	V	-
Power dissipation	P_{tot}	- -	- -	78 2.8	W	T_C=25 °C T_A=25 °C, R_{THJA}=45 °C/W[1]
Operating and storage temperature	T_j, T_{stg}	-55	-	150	°C	IEC climatic category; DIN IEC 68-1: 55/150/56

2 Thermal characteristics

Table 3 Thermal characteristics

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Thermal resistance, junction - case	R_{thJC}	-	-	1.6	°C/W	-
Thermal resistance, junction - Ambient, double sided cooling	R_{thJA}[4]	-	12.5	-	°C/W	-
Thermal resistance, junction - Ambient, mounted on minimum foot print	R_{thJA}[5]	-	20	-	°C/W	-
Thermal resistance, junction - Ambient	R_{thJA}[1]	-	-	45	°C/W	-
Device on PCB, 6 cm² cooling area	R_{thJA}[1]	-	0.75	-	°C/W	-
Soldering temperature, wave and reflow soldering are allowed	T_{sold}	-	-	260	°C	reflow MSL1

[1] Device on 40 mm x 40 mm x 1.5 mm epoxy PCB FR4 with 6 cm² (one layer, 70 µm thick) copper area for drain connection. PCB is vertical in still air.
[2] See Diagram 3 for more detailed information
[3] See Diagram 13 for more detailed information
[4] Used double sided cooling, mounting pad with large heat sink
[5] Mouted on minimum footprint full size board with metalized back with small clip heat sink

3 Electrical characteristics

at T_j=25 °C, unless otherwise specified

Table 4 Static characteristics

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Drain-source breakdown voltage	$V_{(BR)DSS}$	40	-	-	V	V_{GS}=0 V, I_D=1 mA
Breakdown voltage temperature coefficient	$dV_{(BR)DSS}/dT_j$	-	31	-	mV/°C	I_D=1 mA, referenced to 25 °C
Gate threshold voltage	$V_{GS(th)}$	1.2	1.6	2	V	V_{DS}=V_{GS}, I_D=250 µA
Zero gate voltage drain current	I_{DSS}	-	-	1	µA	V_{DS}=40 V, V_{GS}=0 V, T_j=25 °C
Gate-source leakage current	I_{GSS}	-	-	100	nA	V_{GS}=20 V, V_{DS}=0 V
Drain-source on-state resistance	$R_{DS(on)}$	- -	0.62 0.79	0.82 1.3	mΩ	V_{GS}=10 V, I_D=50 A V_{GS}=4.5 V, I_D=50 A
Gate resistance[1)]	R_G	-	1.2	-	Ω	-
Transconductance	g_{fs}	-	310	-	S	$\|V_{DS}\|\geq 2\|I_D\|R_{DS(on)max}$, I_D=50 A

Table 5 Dynamic characteristics

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Input capacitance[1)]	C_{iss}	-	8400	-	pF	V_{GS}=0 V, V_{DS}=20 V, f=1 MHz
Output capacitance[1)]	C_{oss}	-	2400	-	pF	V_{GS}=0 V, V_{DS}=20 V, f=1 MHz
Reverse transfer capacitance[1)]	C_{rss}	-	190	-	pF	V_{GS}=0 V, V_{DS}=20 V, f=1 MHz
Turn-on delay time	$t_{d(on)}$	-	25	-	ns	V_{DD}=20 V, V_{GS}=4.5 V, I_D=50 A, $R_{G,ext}$=1.8 Ω
Rise time	t_r	-	71	-	ns	V_{DD}=20 V, V_{GS}=4.5 V, I_D=50 A, $R_{G,ext}$=1.8 Ω
Turn-off delay time	$t_{d(off)}$	-	49	-	ns	V_{DD}=20 V, V_{GS}=4.5 V, I_D=50 A, $R_{G,ext}$=1.8 Ω
Fall time	t_f	-	50	-	ns	V_{DD}=20 V, V_{GS}=4.5 V, I_D=50 A, $R_{G,ext}$=1.8 Ω

[1)] Defined by design. Not subject to production test.

Table 6 Gate charge characteristics[1)]

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Gate to source charge	Q_{gs}	-	20	-	nC	V_{DD}=20 V, I_D=50 A, V_{GS}=0 to 4.5 V
Gate charge at threshold	$Q_{g(th)}$	-	13	-	nC	V_{DD}=20 V, I_D=50 A, V_{GS}=0 to 4.5 V
Gate to drain charge[2)]	Q_{gd}	-	19	-	nC	V_{DD}=20 V, I_D=50 A, V_{GS}=0 to 4.5 V
Switching charge	Q_{sw}	-	25	-	nC	V_{DD}=20 V, I_D=50 A, V_{GS}=0 to 4.5 V
Gate charge total[2)]	Q_g	-	61	85	nC	V_{DD}=20 V, I_D=50 A, V_{GS}=0 to 4.5 V
Gate plateau voltage	$V_{plateau}$	-	2.3	-	V	V_{DD}=20 V, I_D=50 A, V_{GS}=0 to 4.5 V
Gate charge total	Q_g	-	118	165	nC	V_{DD}=20 V, I_D=50 A, V_{GS}=0 to 10 V
Gate charge total, sync. FET	$Q_{g(sync)}$	-	99	-	nC	V_{DS}=0.1 V, V_{GS}=0 to 10 V
Output charge[1)]	Q_{oss}	-	104	-	nC	V_{DD}=20 V, V_{GS}=0 V

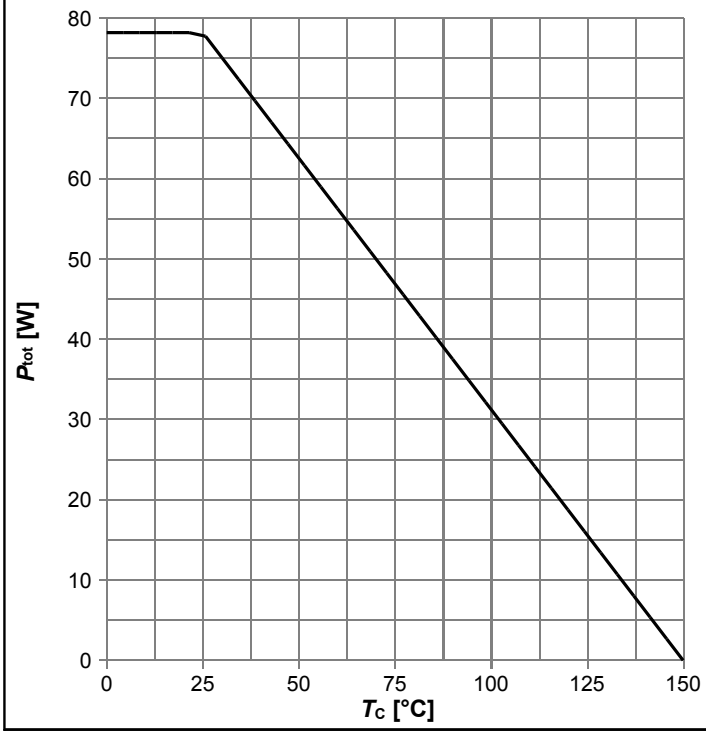
Table 7 Reverse diode

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Diode continuous forward current	I_S	-	-	78	A	T_C=25 °C
Diode pulse current	$I_{S,pulse}$	-	-	926	A	T_C=25 °C
Diode forward voltage	V_{SD}	-	-	1	V	V_{GS}=0 V, I_F=50 A, T_j=25 °C
Reverse recovery time[2)]	t_{rr}	-	53	-	ns	V_R=20 V, I_F=50 A, di_F/dt=100 A/µs
Reverse recovery charge[2)]	Q_{rr}	-	56	-	nC	V_R=20 V, I_F=50 A, di_F/dt=100 A/µs

[1)] See ″Gate charge waveforms″ for parameter definition
[2)] Defined by design. Not subject to production test.

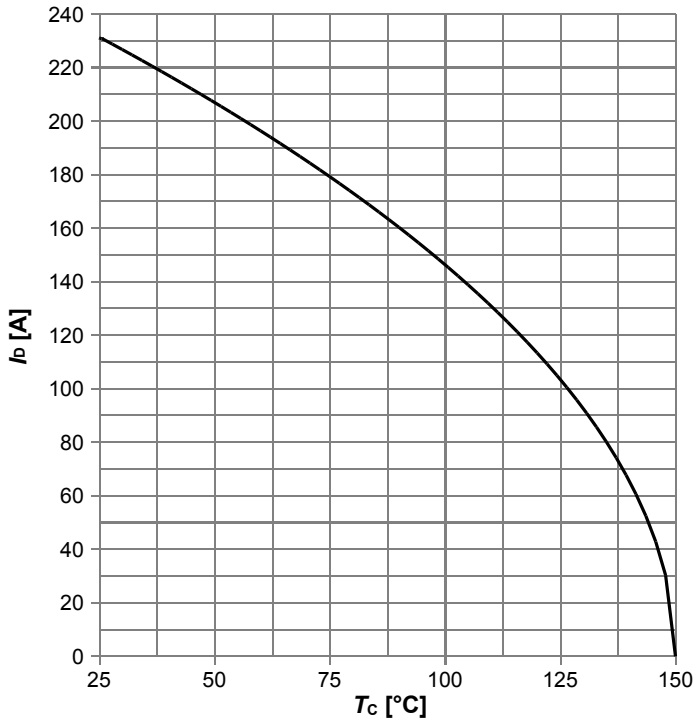
4 Electrical characteristics diagrams

Diagram 1: Power dissipation



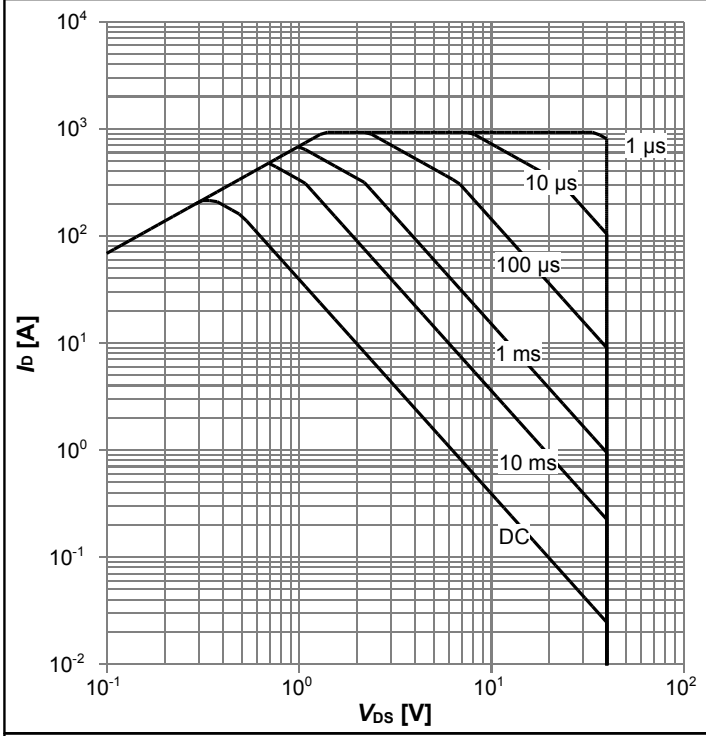
$P_{tot}=f(T_C)$

Diagram 2: Drain current



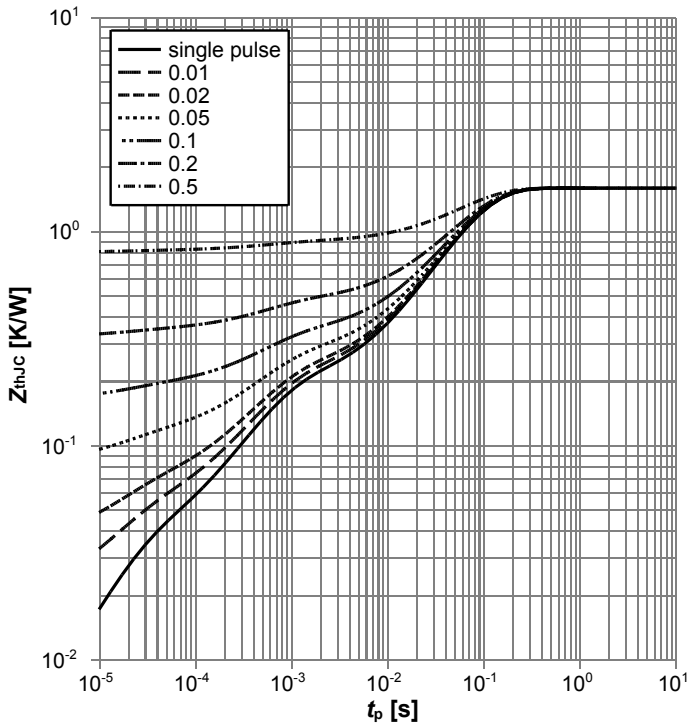
$I_D=f(T_C)$; $V_{GS}\geq 10$ V

Diagram 3: Safe operating area



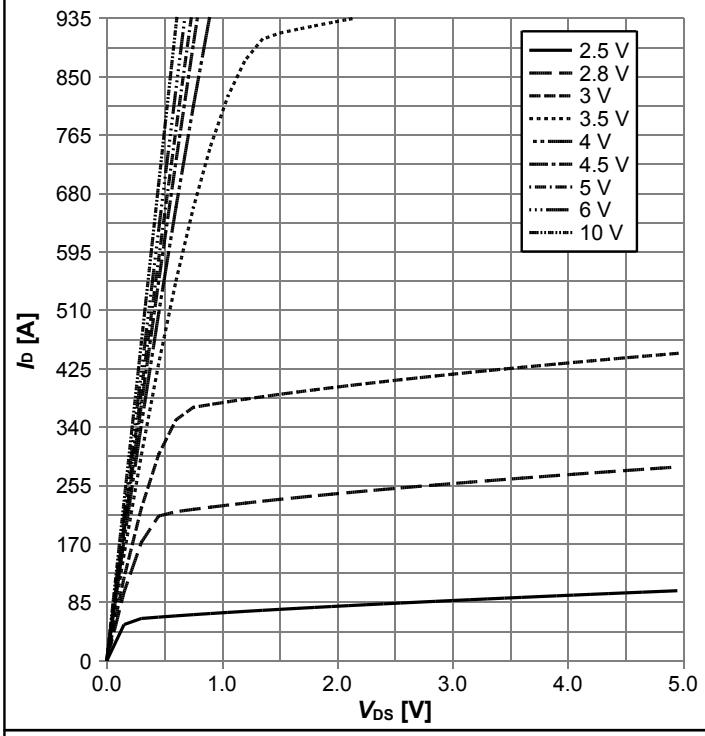
$I_D=f(V_{DS})$; T_C=25 °C; D=0; parameter: t_p

Diagram 4: Max. transient thermal impedance



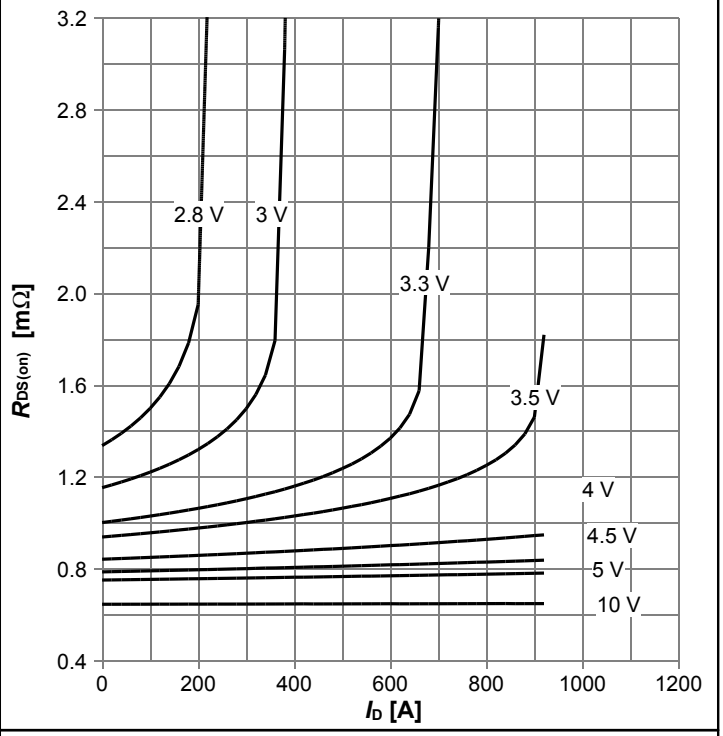
$Z_{thJC}=f(t_p)$; parameter: $D=t_p/T$

Diagram 5: Typ. output characteristics



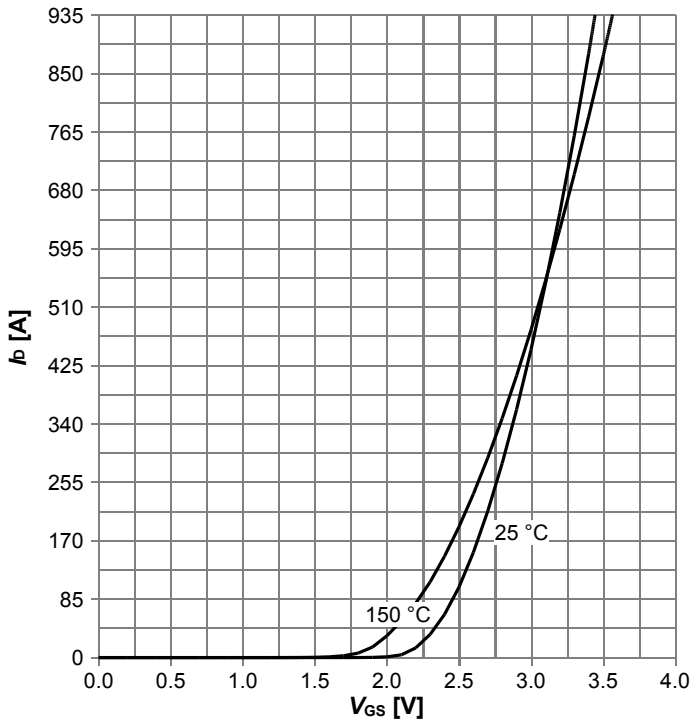
I_D=f(V_{DS}), T_j=25 °C; parameter: V_{GS}

Diagram 6: Typ. drain-source on resistance



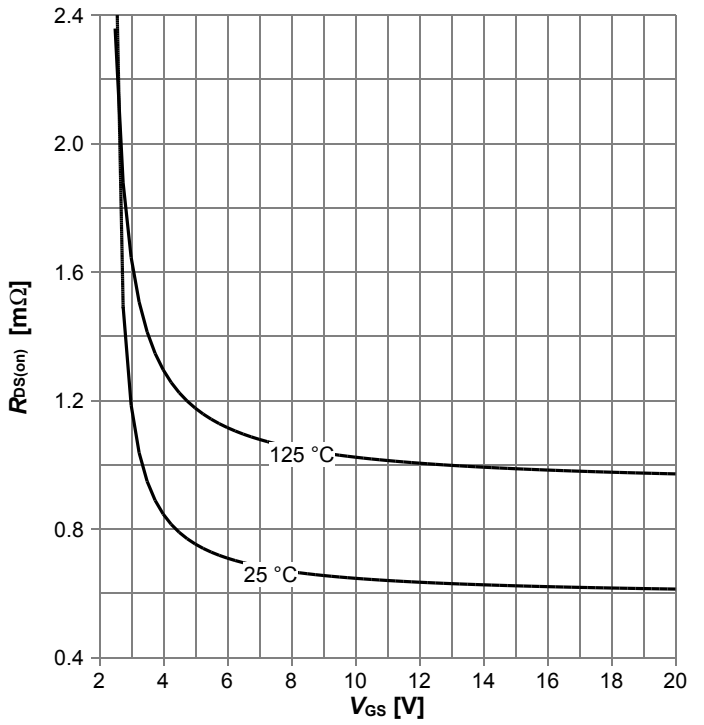
$R_{DS(on)}$=f(I_D), T_j=25 °C; parameter: V_{GS}

Diagram 7: Typ. transfer characteristics



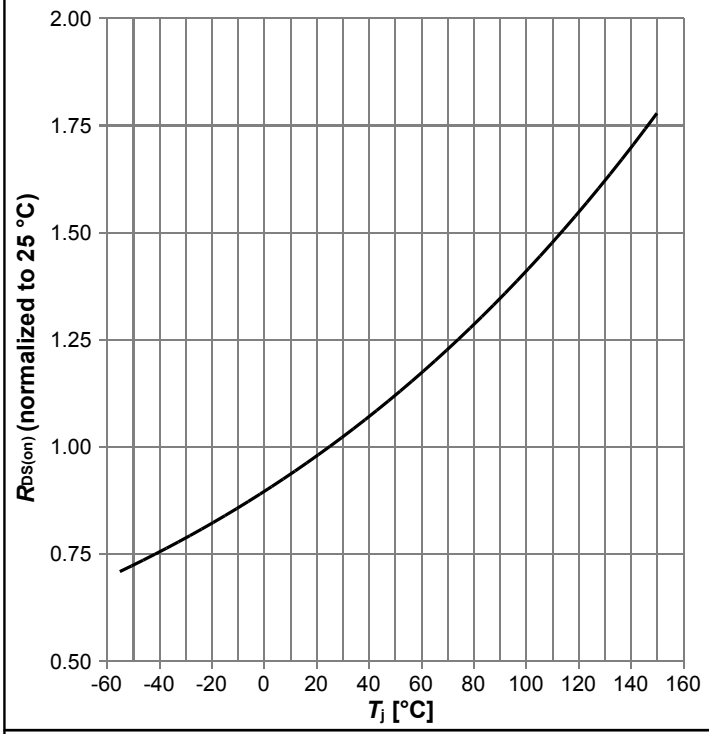
I_D=f(V_{GS}), |V_{DS}|>2|I_D|$R_{DS(on)max}$; parameter: T_j

Diagram 8: Typ. drain-source on resistance



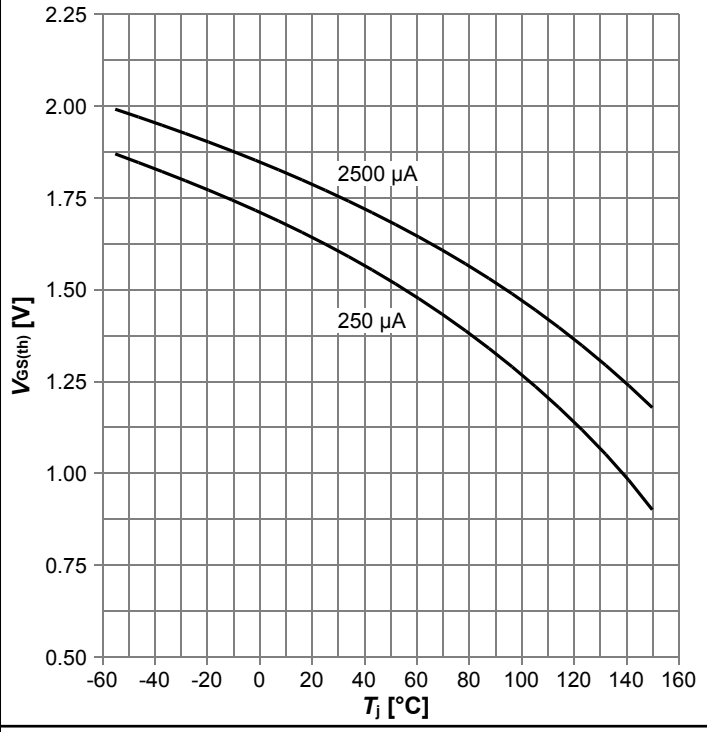
$R_{DS(on)}$=f(V_{GS}), I_D=50 A; parameter: T_j

Diagram 9: Normalized drain-source on resistance



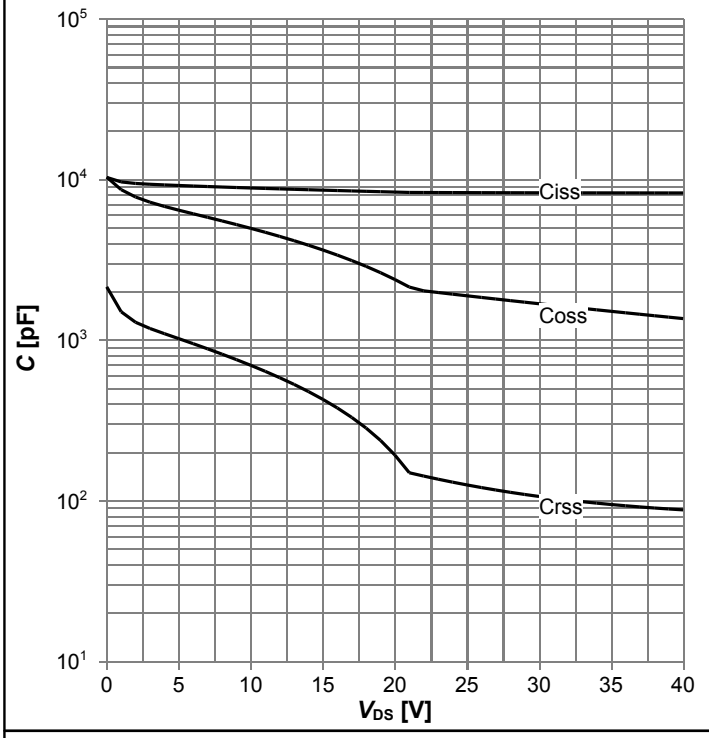
$R_{DS(on)}$=f(T_j), I_D=50 A, V_{GS}=10 V

Diagram 10: Typ. gate threshold voltage



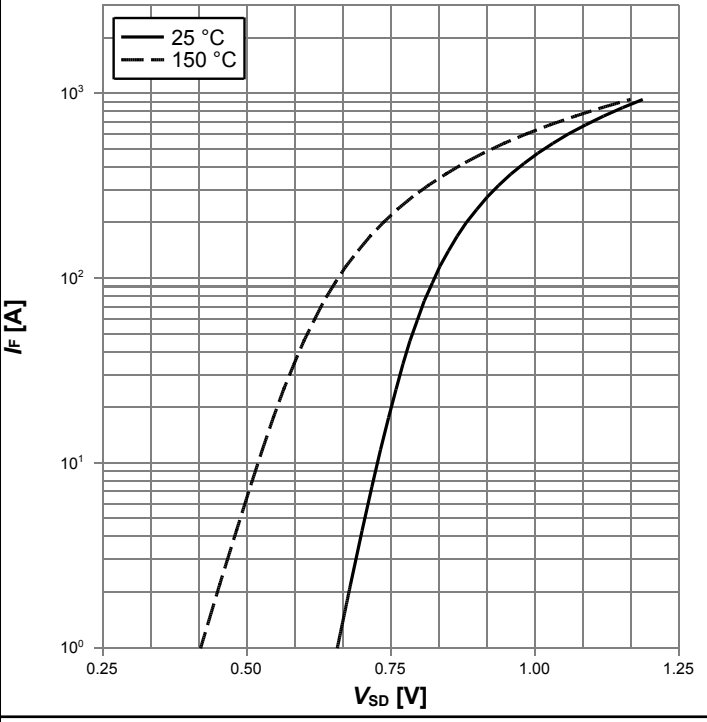
$V_{GS(th}$=f(T_j), V_{GS}=V_{DS}; parameter: I_D

Diagram 11: Typ. capacitances



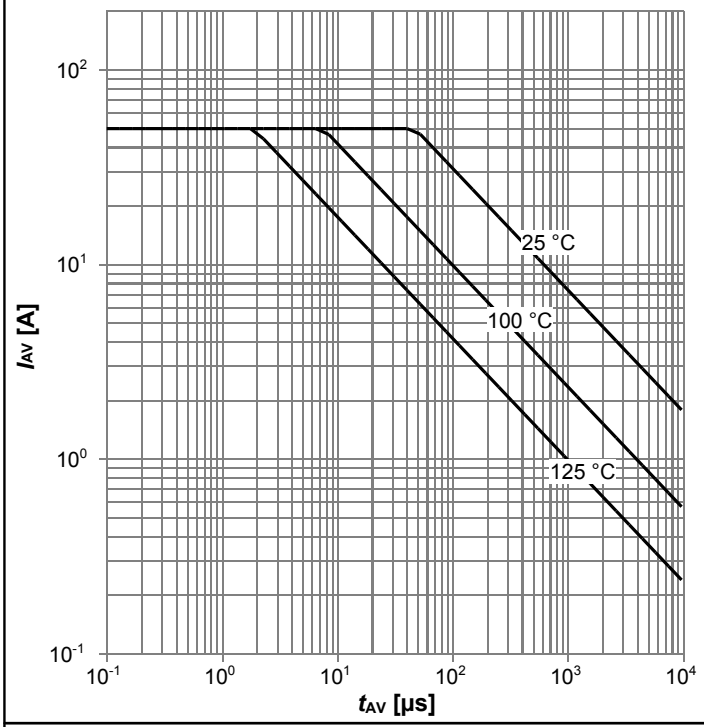
C=f(V_{DS}); V_{GS}=0 V; f=1 MHz

Diagram 12: Forward characteristics of reverse diode



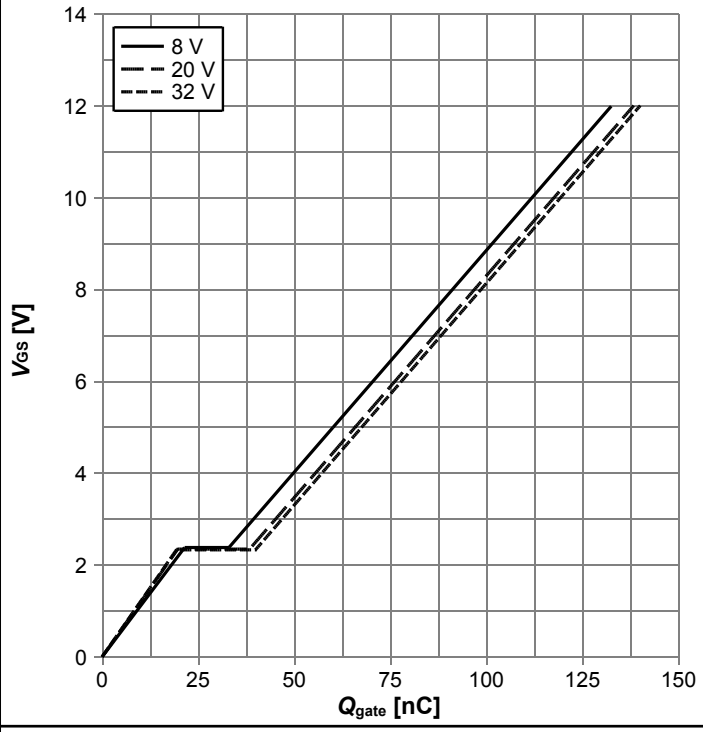
I_F=f(V_{SD}); parameter: T_j

Diagram 13: Avalanche characteristics



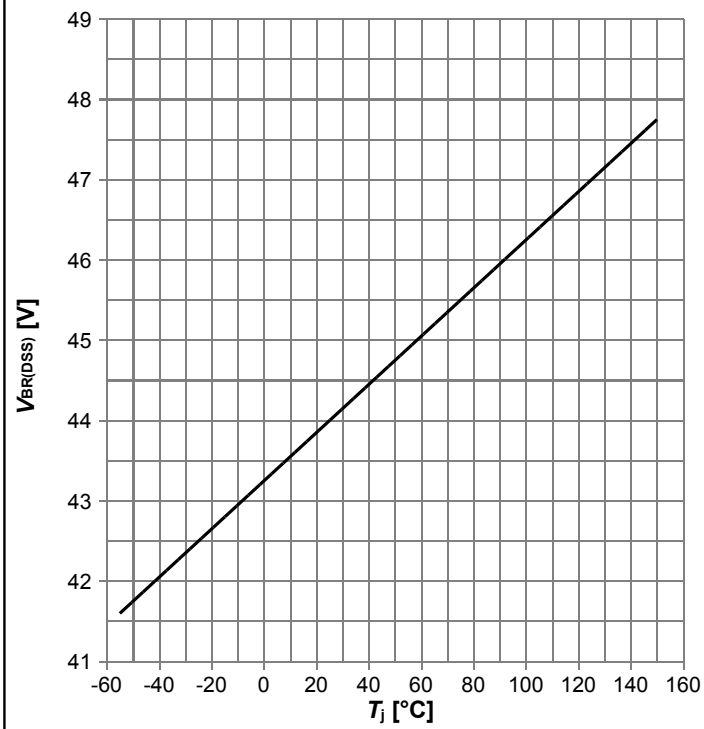
I_{AS}=f(t_{AV}); R_{GS}=25 Ω; parameter: $T_{j,start}$

Diagram 14: Typ. gate charge



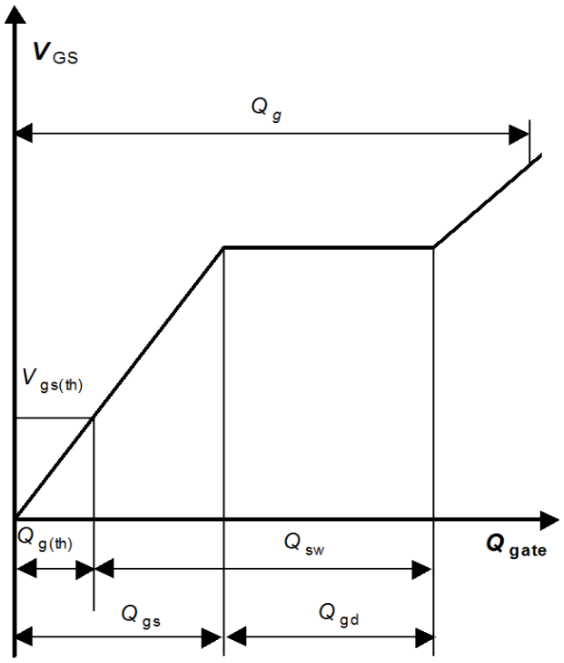
V_{GS}=f(Q_{gate}), I_D=50 A pulsed, T_j=25 °C; parameter: V_{DD}

Diagram 15: Drain-source breakdown voltage



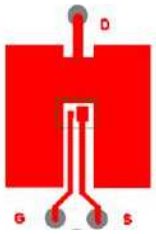
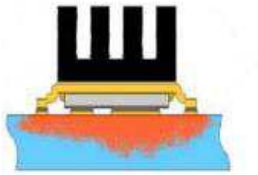
$V_{BR(DSS)}$=f(T_j); I_D=1 mA

Diagram Gate charge waveforms

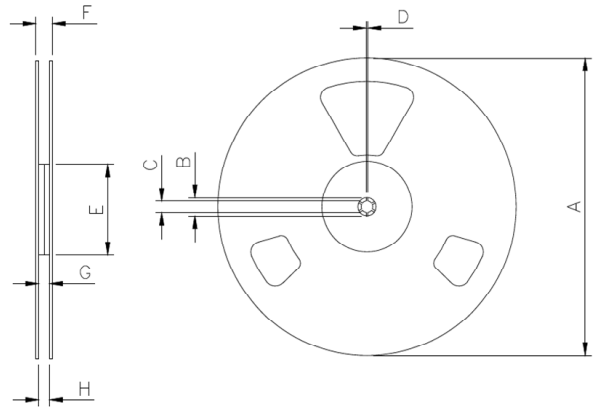


5 Test Circuits

Table 8 Rth/Zth measurement diagrams

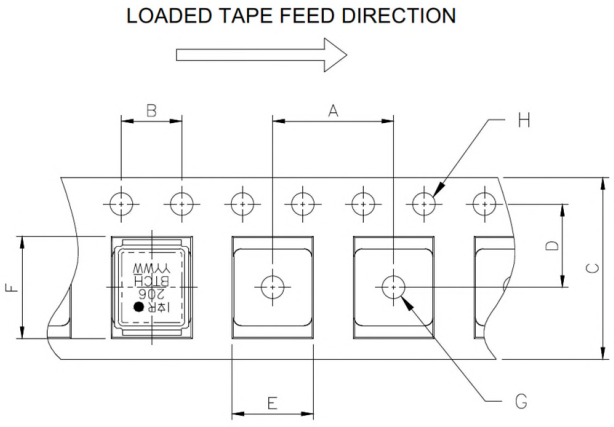
Rth/Zth measurement diagrams		
		
[1] Surface mounted on 1 in. square Cu board (still air).	[5] Mounted on minimum footprint full size board with metalized back and with small clip heatsink (still air)	

6 Package Outlines



NOTE: Controlling dimensions in mm
Std reel quantity is 4800 parts, ordered as IRL40DM247

REEL DIMENSIONS				
	METRIC		IMPERIAL	
CODE	MIN	MAX	MIN	MAX
A	330.0	N.C	12.992	N.C
B	20.2	N.C	0.795	N.C
C	12.8	13.2	0.504	0.520
D	1.5	N.C	0.059	N.C
E	100.0	N.C	3.937	N.C
F	N.C	18.4	N.C	0.724
G	12.4	14.4	0.488	0.567
H	11.9	15.4	0.469	0.606



NOTE: CONTROLLING
DIMENSIONS IN MM

DIMENSIONS				
	METRIC		IMPERIAL	
CODE	MIN	MAX	MIN	MAX
A	7.90	8.10	0.311	0.319
B	3.90	4.10	0.154	0.161
C	11.90	12.30	0.469	0.484
D	5.45	5.55	0.215	0.219
E	5.10	5.30	0.201	0.209
F	6.50	6.70	0.256	0.264
G	1.50	N.C	0.059	N.C
H	1.50	1.60	0.059	0.063

Figure 1 Outline Tape (MG-WDSON-8-904 (ME), dimensions in mm/inches

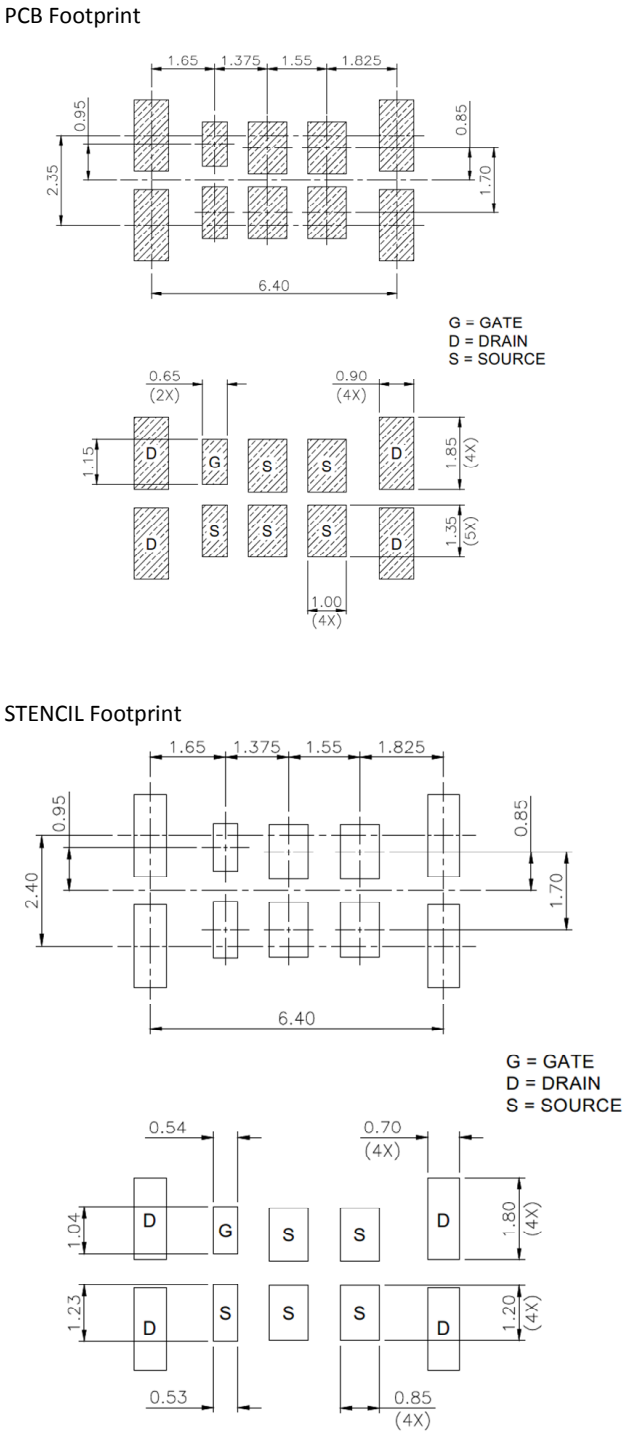
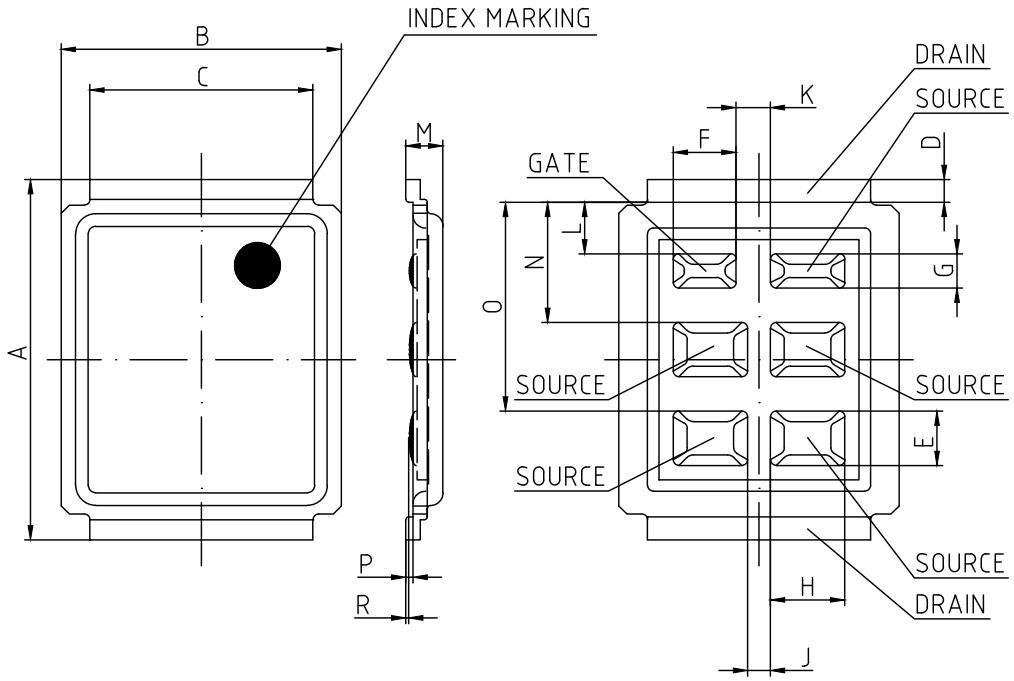


Figure 2 Outline Boardpad (MG-WDSON-8-904 (ME), dimensions in mm



DIMENSION	MILLIMETERS	
	MIN.	MAX.
A	6.25	6.35
B	4.80	5.05
C	3.85	3.95
D	0.35	0.45
E	0.93	0.97
F	1.08	1.12
G	0.58	0.62
H	1.28	1.32
J	0.38	0.42
K	0.58	0.62
L	0.83	0.97
M	-	0.70
N	2.03	2.17
O	3.58	3.72
P	0.08	0.17
R	0.00	0.10

DOCUMENT NO.	Z8B00188582
REVISION	01
SCALE 10:1	0 1 2mm
EUROPEAN PROJECTION	
ISSUE DATE	17.04.2018

Figure 3 Outline MG-WDSON-8-904 (ME), dimensions in mm/inches

Revision History

IRL40DM247

Revision: 2020-03-05, Rev. 2.2

Previous Revision

Revision	Date	Subjects (major changes since last revision)
0.9	2018-04-25	Release of target version
1.0	2018-12-04	Release of preliminary version
2.0	2019-10-30	Release of final version
2.1	2020-03-05	Update Max Qg- page 5
2.2	2020-03-05	Update Application

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