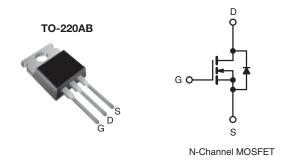


Vishay Siliconix

Power MOSFET

PRODUCT SUMMARY					
V _{DS} (V)	200				
R _{DS(on)} (Ω)	V _{GS} = 5.0 V 0.80				
Q _g (Max.) (nC)	16				
Q _{gs} (nC)	2.7				
Q _{gd} (nC)	9.6				
Configuration	Single				



FEATURES

- Dynamic dV/dt Rating
- Repetitive Avalanche Rated
- Logic-Level Gate Drive
- R_{DS(on)} Specified at V_{GS} = 4 V and 5 V
- Fast Switching
- · Ease of paralleling
- Simple Drive Requirements
- Compliant to RoHS Directive 2002/95/EC

DESCRIPTION

Third generation Power MOSFETs from Vishay provide the designer with the best combination of fast switching, ruggedized device design, low on-resistance and cost-effectiveness.

The TO-220AB package is universally preferred for all commercial-industrial applications at power dissipation levels to approximately 50 W. The low thermal resistance and low package cost of the TO-220AB contribute to its wide acceptance throughout the industry.

ORDERING INFORMATION	
Package	TO-220AB
Lead (Pb)-free	IRL620PbF
	SiHL620-E3
SnPb	IRL620
	SiHL620

ABSOLUTE MAXIMUM RATINGS ($T_{\mbox{\scriptsize C}}$	= 25 °C, unl	ess otherwis	se noted)			
PARAMETER			SYMBOL	LIMIT	UNIT	
Drain-Source Voltage			V _{DS}	200	V	
Gate-Source Voltage			V _{GS}	± 10	v	
Continuous Drain Current	V _{GS} at 5.0 V	T _C = 25 °C	1	5.2		
	V _{GS} at 5.0 V	T _C = 25 °C T _C = 100 °C	ID	3.3	А	
Pulsed Drain Current ^a			I _{DM}	21		
Linear Derating Factor				0.40	W/°C	
Single Pulse Avalanche Energy ^b			E _{AS}	125	mJ	
Repetitive Avalanche Current ^a			I _{AR}	5.2	А	
Repetitive Avalanche Energy ^a			E _{AR}	5.0	mJ	
Maximum Power Dissipation	aximum Power Dissipation $T_{\rm C} = 25 ^{\circ}{\rm C}$			50	W	
Peak Diode Recovery dV/dt ^c			dV/dt	5.0	V/ns	
Operating Junction and Storage Temperature Range			T _J , T _{stg}	- 55 to + 150	°C	
Soldering Recommendations (Peak Temperature)	emperature) for 10 s			300 ^d		
Mounting Torque	6.32 or 1	6-32 or M3 screw		10	lbf ∙ in	
	0-32 OF IMS SCIEW		Γ	1.1	N·m	

Notes

a. Repetitive rating; pulse width limited by maximum junction temperature (see fig. 11).

b. $V_{DD} = 50$ V, starting $T_J = 25$ °C, L = 6.9 mH, $R_q = 25 \Omega$, $I_{AS} = 5.2$ A (see fig. 12c).

c. $I_{SD} \le 5.2$ A, dV/dt ≤ 120 A/µs, $V_{DD} \le V_{DS}$, $T_J \le 150$ °C.

d. 1.6 mm from case.

* Pb containing terminations are not RoHS compliant, exemptions may apply

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$ \begin{array}{ c c c c c c c c c c c c c c c c c c c$	THERMAL RESISTANCE RATINGS								
Case-to-Sink, Flat, Greased Surface R_{hCS} 0.50 . C/W Maximum Junction-to-Case (Drain) R_{hUC} - 2.5 C/W SPECIFICATIONS (T _J = 25 °C, unless otherwise noted) PARAMETER SYMBOL TEST CONDITIONS Min. TYP. MAX. UN Specifications Min. TYP. MAX. UN Static Drain-Source Breakdown Voltage V _{DS} V _{OS} = 0.V, I _D = 250 µA 1.0 - 2.0 V Gate-Source Threshold Voltage V _{DS} /V _{DS} V _{DS} = 0.0, I _D = 250 µA 1.0 - 2.0 V Zero Gate Voltage Drain Current IDSS VDS = 200 V, V_SS = 0 V - - 4.100 n/2 Forward Transconductance g _B V _{DS} = 160 V, V _{DS} = 0 V, T _J = 125 °C - - 0.80 Q_{SS} Output Capacitance C _{Rs} V _{DS} = 5.0 V I _D = 3.1 A ^b 1.2 - 1.0 S Dirain-Source On-State Resistance C _{Rs} V _{DS} = 5.0 V I _D = 3.1 A ^b	PARAMETER	SYMBOL	TYP.		MAX.		UNIT		
Maximum Junction-to-Case (Drain) R_{HUC} - 2.5 SPECIFICATIONS (T _J = 25 °C, unless otherwise noted) Test conditions Min. TYP. MAX. UN Static Static Static Nin. TYP. MAX. UN Static Vos Test conditions Min. TYP. MAX. UN Static Vos Conditions Min. TYP. MAX. UN Static Vos Conditions Min. TYP. MAX. UN Gate-Source Coefficient AVps/TJ Reference to 25 °C, Ip = 1 mA 0.027 - V/ Case-Source Threshold Votage Vose = 100 - - ± 100 n./ - ± 100 n./ Zoro Gate Voltage Drain Current Ioss Vose = 100 V, Vose = 0 V, TJ = 125 °C - - 0.80 D Drain-Source On-State Resistance Ros(on) Vose = 50 V, Ip = 3.1 A ^D 1.2 - 1.0 Ω Dynamic Input Capacitance Coss Vose = 50 V, Ip = 3.1 A ^D 1.2 - 1.6 - 2.7 -<	Maximum Junction-to-Ambient	R _{thJA}	0.50 -						
$ \begin{array}{c c c c c c c c c c c c c c c c c c c $	Case-to-Sink, Flat, Greased Surface	R _{thCS}					°C/W		
$\begin{array}{ c c c c c c c c c c c c c c c c c c c$	Maximum Junction-to-Case (Drain)	R _{thJC}							
$\begin{array}{ c c c c c c c c c c c c c c c c c c c$									
Static VDS VDS VDS VDS Pain-Source Breakdown Voltage VDS VDS VDS Pain-Source Laskage 200 - - VV Stemperature Coefficient $\Delta V_{DS} T_{J}$ Reference to 25 °C, to = 1 mA - 0.27 - VV Gate-Source Leakage VDS = VDS, VDS = VDS, VDS = VDS, VDS = 250 µA 1.0 - 2.0 V Gate-Source Leakage ILSS VDS = VDS, VDS = 250 µA 1.0 - 2.0 V Gate-Source Leakage ILSS VDS = VDS, VDS = 0 V, TJ = 125 °C - - 250 µL Case Source On-State Resistance RDS(on) VDS = 50 V, VDS = 0 V, TJ = 125 °C - - 0.80 Ω Forward Transconductance Gis VDS = 50 V, ID = 3.1 A ^b - - 0.80 Ω Input Capacitance Cose VDS = 50 V, ID = 3.1 A ^b - - 0.10 Ω Reverse Transfer Capacitance Cose VDS = 50 V, ID = 3.1 A ^b - - 1.0 - - 1	SPECIFICATIONS ($T_J = 25 \ ^{\circ}C$, u	nless otherw	ise noted)						
$ \begin{array}{c c c c c c c c c c c c c c c c c c c $	PARAMETER	SYMBOL			MIN.	TYP.	MAX.	UNIT	
	Static								
$ \begin{array}{c c c c c c c c c c c c c c c c c c c $	Drain-Source Breakdown Voltage	V _{DS}	$V_{GS} = 0$	V, I _D = 2	50 µA	200	-	-	V
Gate-Source Leakage Loss VGS = ± 10 - + ± 100 n/A Zero Gate Voltage Drain Current IDSS $V_{DS} = 200 V, V_{GS} = 0 V$ - - 250 μ^{μ} Drain-Source On-State Resistance RDS(on) $V_{OS} = 5.0 V$ Ip = 3.1 A ^b - - 0.800 μ^{μ} Forward Transconductance gra V_{DS} = 50 V Ip = 3.1 A ^b - - 0.800 μ^{μ} Dynamic VOS = 50 V, Ip = 3.1 A ^b - - 0.800 μ^{μ} Duptati Capacitance Ciss VOS = 50 V, Ip = 3.1 A ^b - - 0.800 μ^{μ} Output Capacitance Ciss VOS = 50 V, Ip = 3.1 A ^b - - 0.800 μ^{μ} Output Capacitance Ciss VOS = 50 V, Ip = 3.1 A ^b - - 91 - 10 Gate-Charge Qg VOS = 50 V - 91 - 10 - 2.7 - 10 - 12.7 - 10 - -	V _{DS} Temperature Coefficient	$\Delta V_{DS}/T_{J}$	Reference t	o 25 °C,	I _D = 1 mA	-	0.27	-	V/°C
$ \begin{array}{c c c c c c c c c c c c c c c c c c c $	Gate-Source Threshold Voltage	V _{GS(th)}	$V_{DS} = V_{C}$	_{GS} , I _D = 2	50 μA	1.0	-	2.0	V
$ \begin{array}{ c c c c c c c c c c c c c c c c c c c$	Gate-Source Leakage	I _{GSS}	Vo	as = ± 10		-	-	± 100	nA
$\begin{array}{c c c c c c c c c c c c c c c c c c c $	Zour Ooto Maltana Duain Ourseat		V _{DS} = 20	00 V, V _{GS}	s = 0 V	-	-	25	μA
$\begin{array}{ c c c c c c c c c c c c c c c c c c c$	Zero Gate voltage Drain Current	IDSS	V _{DS} = 160 V, V	_{GS} = 0 V	, T _J = 125 °C	-	-	250	
$\begin{tabular}{ c c c c c c c } \hline V_{GS} = 4.0 \ V & _{D} = 2.6 \ A^{b} & - & - & 1.0 \ P_{A} & P_$	Drain-Source On-State Resistance	R _{DS(on)}	$V_{GS} = 5.0 V$	I	_D = 3.1 A ^b	-	-	0.80	0
DynamicInput CapacitanceCiss $V_{GS} = 0 V$, $V_{DS} = 25 V$, f = 1.0 MHz, see fig. 5-360-Output CapacitanceCoss $V_{GS} = 25 V$, f = 1.0 MHz, see fig. 591-pFReverse Transfer CapacitanceCrss $I_{D} = 5.2 A$, $V_{DS} = 160 V$, see fig. 6 and 13b1616Gate-Drain Charge Q_{gd} $V_{GS} = 5.0 V$ $I_{D} = 5.2 A$, $V_{DS} = 160 V$, see fig. 6 and 13b169.6Turn-On Delay Time $t_{d(on)}$ $V_{GS} = 5.0 V$ $I_{D} = 5.2 A$, $V_{DS} = 160 V$, see fig. 6 and 13b9.69.6Turn-On Delay Time $t_{d(onf)}$ $V_{GS} = 100 V$, $I_{D} = 9.0 A$, $R_{g} = 6.0 \Omega$, $R_{D} = 11 \Omega$, see fig. 10b-4.218-Fall Time t_{f} $V_{CS} = 100 V$, $I_{D} = 9.0 A$, $R_{g} = 6.0 \Omega$, $R_{D} = 11 \Omega$, see fig. 10b-1817-Internal Drain Inductance L_{D} Between lead, 6 mm (0.25") from package and center of die contact-4.516Pulsed Diode Forward Current* I_{S} MOSFET symbol showing the integral reverse $p - n$ junction diode5.2ABody Diode Voltage V_{SD} $T_{J} = 25 °C$, $I_{F} = 5.2 A$, $dI/dt = 100 A/\mu s^b$ -1.8VBody Diode Reverse Recovery Time t_{rr} $T_{J} = 25 °C$, $I_{F} = 5.2 A$, $dI/dt = 100 A/\mu s^b$ -<		()	$V_{GS} = 4.0 V$	I	_D = 2.6 A ^b	-	-	1.0	Ω
$ \begin{array}{ c c c c c c } \mbox{Input Capacitance} & C_{1ss} & V_{GS} = 0 \ V, & V_{DS} = 25 \ V, & f = 1.0 \ MHz, see fig. 5 & f = 1.0 \ MHz, see fig. 5 & f = 1.0 \ MHz, see fig. 5 & f = 1.0 \ MHz, see fig. 5 & f = 1.0 \ MHz, see fig. 5 & f = 1.0 \ MHz, see fig. 5 & f = 1.0 \ MHz, see fig. 5 & f = 1.0 \ MHz, see fig. 5 & f = 1.0 \ MHz, see fig. 5 & f = 1.0 \ MHz, see fig. 5 & f = 1.0 \ MHz, see fig. 6 \ and 13^b & f & - & 16 \ - & - & 2.7 & - & 0.6 \ \ - & - & 0.6 \ \ - & - & 0.6 \ \ - & - & 0.6 \ \ - & - & 0.6 \ \ - & - & 0.6 \ \ - & - & 0.6 \ \ - & - & 0.6 \ \ - & - & 0.6 \ \ \ - & - & 0.6 \ \ \ - & - & 0.6 \ \ \ - & - & 0.6 \ \ \ \ - & - & 0.6 \ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \$	Forward Transconductance	g fs	$V_{DS} = 50 \text{ V}, \text{ I}_{D} = 3.1 \text{ A}^{b}$		1.2	-	-	S	
Output Capacitance C_{oss} $r_{VDS} = 25 \text{ V}$, $f = 1.0 \text{ MHz}$, see fig. 5 r_{-} 91 r_{-} pF Reverse Transfer Capacitance C_{rss} $r_{DS} = 25 \text{ V}$, $f = 1.0 \text{ MHz}$, see fig. 5 r_{-} 91 r_{-} pF Total Gate Charge Q_{g} Q_{g} $V_{GS} = 5.0 \text{ V}$ $r_{D} = 5.2 \text{ A}, V_{DS} = 160 \text{ V},$ see fig. 6 and 13b r_{-} r_{-} 16 r_{-} <	Dynamic								
Output Capacitance C_{oss} $V_{DS} = 25 \text{ V}, f = 1.0 \text{ MHz}, see fig. 5$ $ 91$ $ 91$ $ pf$ Reverse Transfer Capacitance C_{rss} $f = 1.0 \text{ MHz}, see fig. 5$ $ 27$ $ 27$ $ 27$ $ 27$ $ 27$ $ 27$ $ 27$ $ 27$ $ 16$ 27 $ 27$ 7	Input Capacitance	C _{iss}	$V_{DS} = 25 V,$		-	360	-	pF	
Reverse transfer Capacitance C_{rss} $ 27$ $-$ Total Gate Charge Q_g Gate-Source Charge Q_{gs} Gate-Drain Charge Q_{gd} Turn-On Delay Time $t_{d(on)}$ Rise Time t_r Turn-Off Delay Time $t_{d(off)}$ Fall Time t_r Turn-Off Delay Time $t_{d(off)}$ Fall Time t_r Turn-Off Delay Time $t_{d(off)}$ Fall Time t_r Internal Drain Inductance L_D Between lead, 6 mm (0.25") from package and center of die contactOntinuous Source-Drain Diode Current l_S MOSFET symbol showing the integral reverse $p - n$ junction diodePulsed Diode Forward Currenta l_{SM} Body Diode Voltage V_{SD} $T_J = 25 °C$, $l_F = 5.2 A$, $dl/dt = 100 A/\mu s^b$ $T_J = 25 °C$, $l_F = 5.2 A$, $dl/dt = 100 A/\mu s^b$ $ 1.8$ $ 1.8$ $ 1.8$ $ 1.8$ $ -$ <t< td=""><td>Output Capacitance</td><td>C_{oss}</td><td>-</td><td>91</td><td>-</td></t<>	Output Capacitance	C _{oss}			-	91	-		
Gate-Source Charge Q_{gs} $V_{GS} = 5.0 \text{ V}$ $I_{D} = 5.2 \text{ A}, V_{DS} = 160 \text{ V}, see fig. 6 and 13b$ - - 2.7 nC Gate-Drain Charge Q_{gd} $V_{GS} = 5.0 \text{ V}$ $I_D = 5.2 \text{ A}, V_{DS} = 160 \text{ V}, see fig. 6 and 13b$ - - 9.6 Turn-On Delay Time $t_{d(on)}$ t_r $V_{DD} = 100 \text{ V}, I_D = 9.0 \text{ A}, R_g = 6.0 \Omega, R_D = 11 \Omega$, see fig. 10b - 4.2 - - 18 - - 18 - - 18 - - 17 - 18 0 0 0 0	Reverse Transfer Capacitance	C _{rss}			-	27	-		
Gate-Source Charge U_{gs} $V_{GS} = 3.0 \text{ V}$ see fig. 6 and 13b $ 2.7$ $1000000000000000000000000000000000000$	Total Gate Charge	Qg				-	-	16	
Gate-Drain Charge Q_{gd} 9.6Turn-On Delay Time $t_{d(on)}$ Rise Time t_r Turn-Off Delay Time $t_{d(off)}$ Fall Time t_r Internal Drain Inductance L_D Internal Source Inductance L_S Drain-Source Body Diode CharacteristicsContinuous Source-Drain Diode Current I_S Pulsed Diode Forward Current ^a I_{SM} Body Diode Reverse Recovery Time t_{rr} Turn-Off Delay Time t_{rr} Turn-Off Delay Time t_{gd} Turn-Off Delay Time t_{gd} Fall Time t_{gd} Internal Drain Inductance L_D Between lead, 6 mm (0.25") from package and center of die contact- t_{gd}	Gate-Source Charge	Q _{gs}			-	-	2.7	nC	
Rise TimetrVVUU	Gate-Drain Charge	Q _{gd}		000	ing. o and to	-	-	9.6	
$\begin{array}{c c c c c c c c c c c c c c c c c c c $	Turn-On Delay Time	t _{d(on)}			-	4.2	-	- ns	
$\begin{array}{c c c c c c c c c c c c c c c c c c c $	Rise Time				-	31	-		
Internal Drain Inductance L_D Between lead, 6 mm (0.25") from package and center of die contact-4.5-nHInternal Source Inductance L_S L_S MOSFET symbol showing the integral reverse p - n junction diode-7.5-nHPulsed Diode Forward Currenta I_S MOSFET symbol showing the integral reverse p - n junction diode5.2ABody Diode Voltage V_{SD} $T_J = 25$ °C, $I_S = 5.2$ A, $V_{GS} = 0$ Vb1.8VBody Diode Reverse Recovery Time t_{rr} $T_J = 25$ °C, $I_F = 5.2$ A, dI/dt = 100 A/µsb-1.80270nsBody Diode Reverse Recovery Charge Q_{rr} T-1.01.11.7µC	Turn-Off Delay Time	t _{d(off)}			-	18	-		
Internal Drain InductanceLD6 mm (0.25") from package and center of die contact-4.3-nHInternal Source InductanceLS6 mm (0.25") from package and center of die contact-7.5-nHDrain-Source Body Diode CharacteristicsMOSFET symbol showing the integral reverse p - n junction diode5.2APulsed Diode Forward CurrentaIsMOSFET symbol showing the integral reverse p - n junction diode5.2ABody Diode VoltageV_SDT_J = 25 °C, I_S = 5.2 A, V_{GS} = 0 Vb1.8VBody Diode Reverse Recovery TimetrrT_J = 25 °C, I_F = 5.2 A, dl/dt = 100 A/µs^b-1.11.7µC	Fall Time	t _f			-	17	-		
Internal Source InductanceLSpackage and center of die contactImage: Contact for the contact fo	Internal Drain Inductance	L _D	6 mm (0.25") from package and center of		-	4.5	-	nЦ	
Continuous Source-Drain Diode CurrentIsMOSFET symbol showing the integral reverse $p - n$ junction diode5.2APulsed Diode Forward CurrentaIsMIsM $T_J = 25 ^{\circ}C$, Is = 5.2 A, VGS = 0 Vb21ABody Diode VoltageVSD $T_J = 25 ^{\circ}C$, Is = 5.2 A, VGS = 0 Vb1.8VBody Diode Reverse Recovery Time t_{rr} $T_J = 25 ^{\circ}C$, IF = 5.2 A, dI/dt = 100 A/µsb-180270nsBody Diode Reverse Recovery Charge Q_{rr} 1.11.7µC	Internal Source Inductance	L _S			-	7.5	-	пн	
Continuous Source-Drain Diode OutrientIsshowing the integral reverse p - n junction diodeIII <td>Drain-Source Body Diode Characteristic</td> <td>cs</td> <td></td> <td></td> <td></td> <td></td> <td></td> <td></td> <td></td>	Drain-Source Body Diode Characteristic	cs							
Pulsed Diode Forward Current ^a I _{SM} Integral reverse p - n junction diode - - 21 Body Diode Voltage V _{SD} T _J = 25 °C, I _S = 5.2 A, V _{GS} = 0 V ^b - - 1.8 V Body Diode Reverse Recovery Time t_{rr} $T_J = 25 °C, I_F = 5.2 A, dI/dt = 100 A/\mu sb$ - 180 270 ns Body Diode Reverse Recovery Charge Q_{rr} T_J = 25 °C, I_F = 5.2 A, dI/dt = 100 A/\mu s ^b - 1.1 1.7 μ C	Continuous Source-Drain Diode Current	I _S	showing the integral reverse		-	-	5.2	А	
Body Diode Reverse Recovery Time t_{rr} $T_J = 25 \ ^{\circ}C$, $I_F = 5.2 \ A$, $dl/dt = 100 \ A/\mu s^b$ -180270nsBody Diode Reverse Recovery Charge Q_{rr} $T_J = 25 \ ^{\circ}C$, $I_F = 5.2 \ A$, $dl/dt = 100 \ A/\mu s^b$ -1.11.7 μC	Pulsed Diode Forward Current ^a	I _{SM}			-	-	21		
Body Diode Reverse Recovery Charge Q_{rr} $T_J = 25 \text{ °C}, I_F = 5.2 \text{ A}, dl/dt = 100 \text{ A}/\mu \text{s}^{\text{o}}$ $ 1.1$ 1.7 μC	Body Diode Voltage	V_{SD}	$T_J = 25 \ ^{\circ}C, \ I_S = 5.2 \ A, \ V_{GS} = 0 \ V^b$		-	-	1.8	V	
Body Diode Reverse Recovery Charge Q _{rr} - 1.1 1.7 μC	Body Diode Reverse Recovery Time	t _{rr}	$T_J = 25 \text{ °C}, I_F = 5.2 \text{ A}, dI/dt = 100 \text{ A}/\mu\text{s}^b$		-	180	270	ns	
Forward Turn-On Time ton Intrinsic turn-on time is negligible (turn-on is dominated by L _S and L _D)	Body Diode Reverse Recovery Charge	Q _{rr}			-	1.1	1.7	μC	
	Forward Turn-On Time	t _{on}	Intrinsic turn-	on time	is negligible (turn	-on is dor	minated b	y L _S and	L _D)

Notes

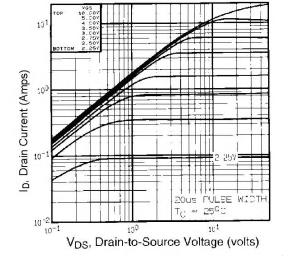
a. Repetitive rating; pulse width limited by maximum junction temperature (see fig. 11).

b. Pulse width $\leq 300~\mu s;$ duty cycle $\leq 2~\%.$

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TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)

Fig. 1 - Typical Output Characteristics, T_C = 25 °C

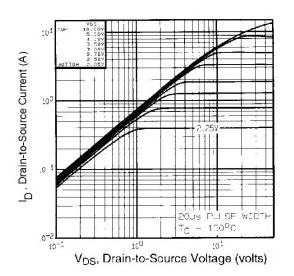


Fig. 2 - Typical Output Characteristics, T_C = 150 °C

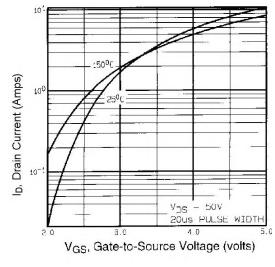


Fig. 3 - Typical Transfer Characteristics

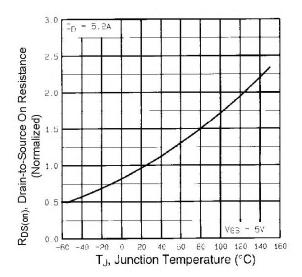


Fig. 4 - Normalized On-Resistance vs. Temperature

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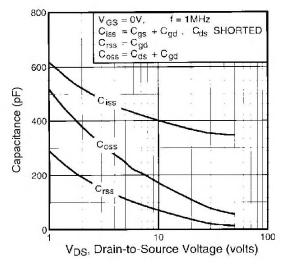


Fig. 5 - Typical Capacitance vs. Drain-to-Source Voltage

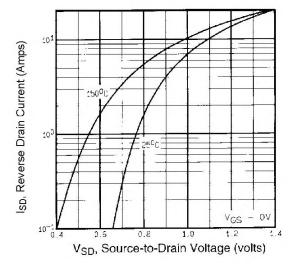


Fig. 7 - Typical Source-Drain Diode Forward Voltage

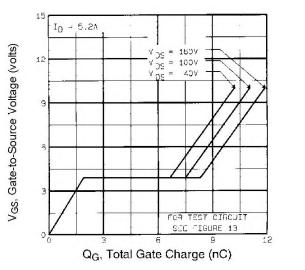


Fig. 6 - Typical Gate Charge vs. Gate-to-Source Voltage

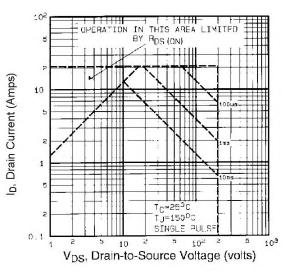


Fig. 8 - Maximum Safe Operating Area

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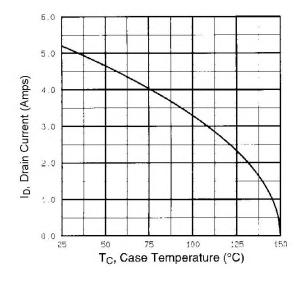


Fig. 9 - Maximum Drain Current vs. Case Temperature

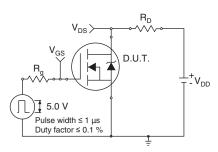


Fig. 10a - Switching Time Test Circuit

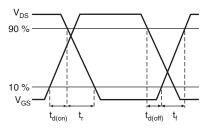


Fig. 10b - Switching Time Waveforms

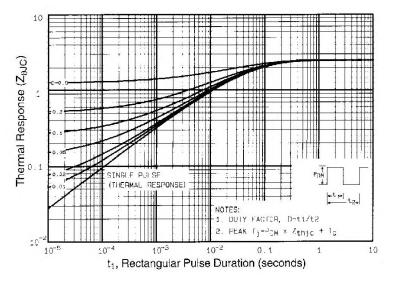


Fig. 11 - Maximum Effective Transient Thermal Impedance, Junction-to-Case

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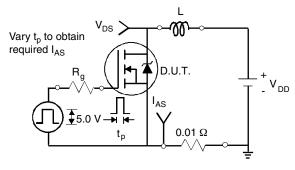


Fig. 12a - Unclamped Inductive Test Circuit

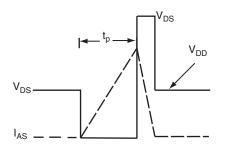


Fig. 12b - Unclamped Inductive Waveforms

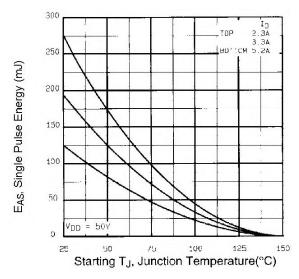


Fig. 12c - Maximum Avalanche Energy vs. Drain Current

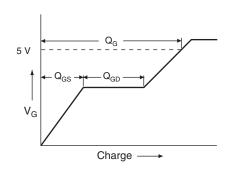


Fig. 13a - Basic Gate Charge Waveform

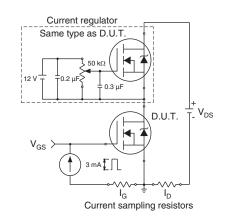
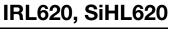


Fig. 13b - Gate Charge Test Circuit

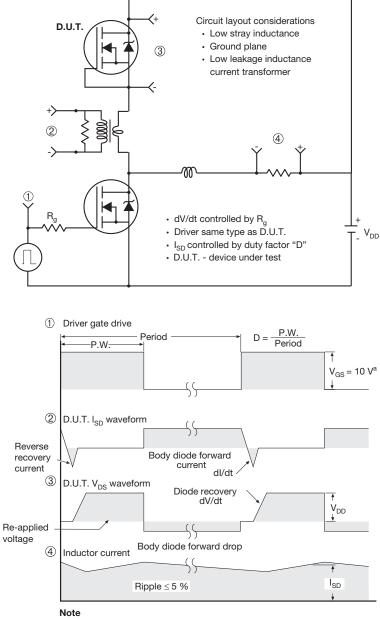
Document Number: 91301 S11-0519-Rev. C, 21-Mar-11



Vishay Siliconix



Peak Diode Recovery dV/dt Test Circuit



a. $V_{GS} = 5 V$ for logic level devices

Fig. 14 - For N-Channel

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TO-220-1



DIM.	MILLIN	IETERS	INCHES		
DIN.	MIN.	MAX.	MIN.	MAX.	
А	4.24	4.65	0.167	0.183	
b	0.69	1.02	0.027	0.040	
b(1)	1.14	1.78	0.045	0.070	
С	0.36	0.61	0.014	0.024	
D	14.33	15.85	0.564	0.624	
E	9.96	10.52	0.392	0.414	
е	2.41	2.67	0.095	0.105	
e(1)	4.88	5.28	0.192	0.208	
F	1.14	1.40	0.045	0.055	
H(1)	6.10	6.71	0.240	0.264	
J(1)	2.41	2.92	0.095	0.115	
L	13.36	14.40	0.526	0.567	
L(1)	3.33	4.04	0.131	0.159	
ØР	3.53	3.94	0.139	0.155	
Q	2.54	3.00	0.100	0.118	
ECN: X15-0364-Rev. C, 14-Dec-15 DWG: 6031					

Note

- M^{\star} = 0.052 inches to 0.064 inches (dimension including protrusion), heatsink hole for HVM

Package Picture					
AS	3E	Xi'an			
		IRF 9510 744K AB			

Revison: 14-Dec-15

1 For technical questions, contact: <u>hvm@vishay.com</u> Document Number: 66542

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