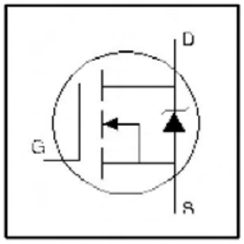
International
IOR Rectifier

PD- 95591

IRL620SPbF

HEXFET® Power MOSFET

- Surface Mount
- Available in Tape & Reel
- Dynamic dv/dt Rating
- Repetitive Avalanche Rated
- Logic-Level Gate Drive
- $R_{DS(on)}$ Specified at V_{GS}=4V & 5V
- Fast Switching
- Lead-Free



V_{DSS} = 200V

$R_{DS(on)}$ = 0.80Ω

I_D = 5.2A


SMD-220

Description

Third Generation HEXFETs from International Rectifier provide the designer with the best combination of fast switching, ruggedized device design, low on-resistance and cost-effectiveness.

The SMD-220 is a surface-mount power package capable of accommodating die sizes up to HEX-4. It provides the highest power capability and the lowest possible on-resistance in any existing surface-mount package. The SMD-220 is suitable for high current applications because of its low internal connection resistance and can dissipate up to 2.0W in a typical surface-mount application.

Absolute Maximum Ratings

	Parameter	Max.	Units
I_D @ T_C = 25°C	Continuous Drain Current, V_{GS} @ 5.0 V	5.2	A
I_D @ T_C = 100°C	Continuous Drain Current, V_{GS} @ 5.0 V	3.3	
I_{DM}	Pulsed Drain Current ①	21	
P_D @T_C = 25°C	Power Dissipation	50	W
P_D @T_A = 25°C	Power Dissipation (PCB Mount)**	3.1	
	Linear Derating Factor	0.40	W/°C
	Linear Derating Factor (PCB Mount)**	0.025	
V_{GS}	Gate-to-Source Voltage	±10	V
E_{AS}	Single Pulse Avalanche Energy ②	125	mJ
I_{AR}	Avalanche Current ①	5.2	A
E_{AR}	Repetitive Avalanche Energy ①	5.0	mJ
dv/dt	Peak Diode Recovery dv/dt ③	5.0	V/ns
T_J, T_{STG}	Junction and Storage Temperature Range	-55 to + 150	°C
	Soldering Temperature, for 10 seconds	300 (1.6mm from case)	

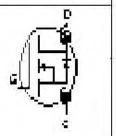
Thermal Resistance

	Parameter	Min.	Typ.	Max.	Units
$R_{θJC}$	Junction-to-Case	—	—	2.5	°C/W
$R_{θJA}$	Junction-to-Ambient (PCB Mount)**	—	—	40	
$R_{θJA}$	Junction-to-Ambient	—	—	62	

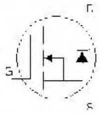
** When mounted on 1" square PCB (FR-4 or G-10 Material). For recommended footprint and soldering techniques, refer to Application Note AN-994.

07/21/04

Electrical Characteristics @ T_J = 25°C (unless otherwise specified)

	Parameter	Min.	Typ.	Max.	Units	Conditions
$V_{(BR)DSS}$	Drain-to-Source Breakdown Voltage	200	—	—	V	V_{GS} = 0V, ID = 250μA
$\Delta V_{(BR)DSS}/\Delta T_J$	Breakdown Voltage Temp. Coefficient	—	0.27	—	V/°C	Reference to 25°C, I_D = 1mA
$R_{DS(on)}$	Static Drain-to-Source On-Resistance	—	—	0.80	Ω	V_{GS} = 10.0V, I_D = 3.1A ④
		—	—	1.0		V_{GS} = 4.0V, I_D = 2.6A ④
$V_{GS(th)}$	Gate Threshold Voltage	1.0	—	2.0	V	V_{DS} = V_{GS}, I_D = 250μA
g_{fs}	Forward Transconductance	1.2	—	—	S	V_{DS} = 50V, I_D = 3.1A
I_{DSS}	Drain-to-Source Leakage Current	—	—	25	μA	V_{DS} = 200V, V_{GS} = 0V
		—	—	250		V_{DS} = 320V, V_{GS} = 0V, T_J = 125°C
I_{GSS}	Gate-to-Source Forward Leakage	—	—	100	nA	V_{GS} = 10V
	Gate-to-Source Reverse Leakage	—	—	-100		V_{GS} = -10V
Q_g	Total Gate Charge	—	—	16	nC	I_D = 5.2A
Q_{gs}	Gate-to-Source Charge	—	—	2.9		V_{DS} = 160V
Q_{gd}	Gate-to-Drain ("Miller") Charge	—	—	9.6		V_{GS} = 5.0V, See Fig. 6 and 13 ④
$t_{d(on)}$	Turn-On Delay Time	—	4.2	—	ns	V_{DD} = 100V
t_r	Rise Time	—	31	—		I_D = 5.2A
$t_{d(off)}$	Turn-Off Delay Time	—	18	—		R_G = 9.0Ω
t_f	Fall Time	—	17	—		R_D = 20Ω, See Fig. 10 ④
L_D	Internal Drain Inductance	—	4.5	—	nH	Between lead, 6mm (0.25in.) from package and center of die contact 
L_S	Internal Source Inductance	—	7.5	—		
C_{iss}	Input Capacitance	—	360	—	pF	V_{GS} = 0V
C_{oss}	Output Capacitance	—	91	—		V_{DS} = 25V
C_{rss}	Reverse Transfer Capacitance	—	27	—		ƒ = 1.0MHz, See Fig. 5

Source-Drain Ratings and Characteristics

	Parameter	Min.	Typ.	Max.	Units	Conditions
I_S	Continuous Source Current (Body Diode)	—	—	5.2	A	MOSFET symbol showing the integral reverse p-n junction diode. 
I_{SM}	Pulsed Source Current (Body Diode) ①	—	—	21		
V_{SD}	Diode Forward Voltage	—	—	1.8	V	T_J = 25°C, I_S = 5.2A, V_{GS} = 0V ④
t_{rr}	Reverse Recovery Time	—	180	270	ns	T_J = 25°C, I_F = 5.2A
Q_{rr}	Reverse RecoveryCharge	—	1.1	1.7	μC	di/dt = 100A/μs ④
t_{on}	Forward Turn-On Time	Intrinsic turn-on time is negligible (turn-on is dominated by L_S+L_D)				

Notes:

① Repetitive rating; pulse width limited by max. junction temperature. (See fig. 11)

② V_{DD} = 50V, starting T_J = 25°C, L = 6.9mH R_G = 25Ω, I_{AS} = 5.2A. (See Figure 12)

③ $I_{SD} \leq$ 5.2A, di/dt ≤ 95A/μs, $V_{DD} \leq V_{(BR)DSS}$, $T_J \leq$ 150°C

④ Pulse width ≤ 300μs; duty cycle ≤ 2%.

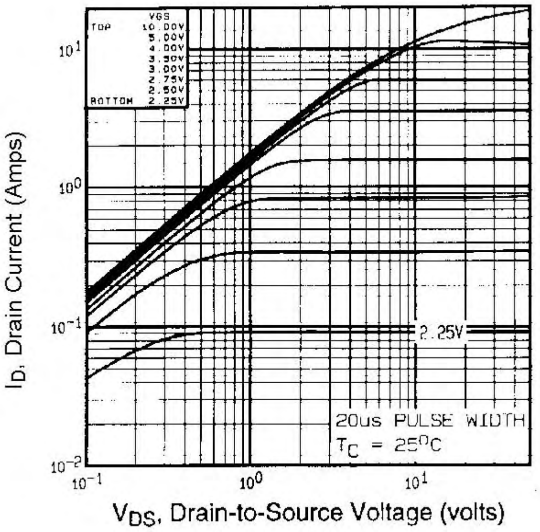


Fig 1. Typical Output Characteristics, T_C = 25ºC

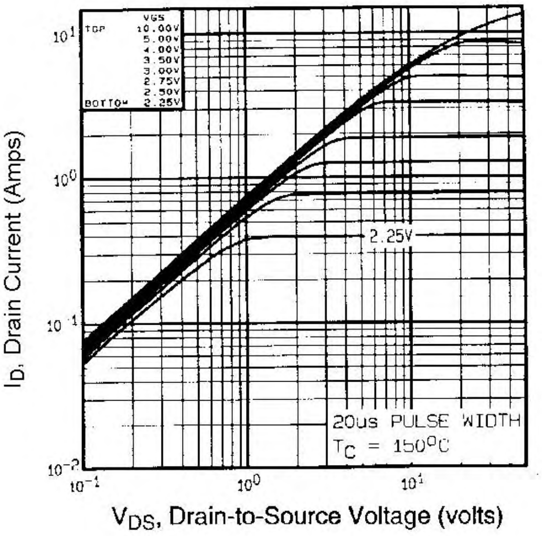


Fig 2. Typical Output Characteristics, T_C = 150ºC

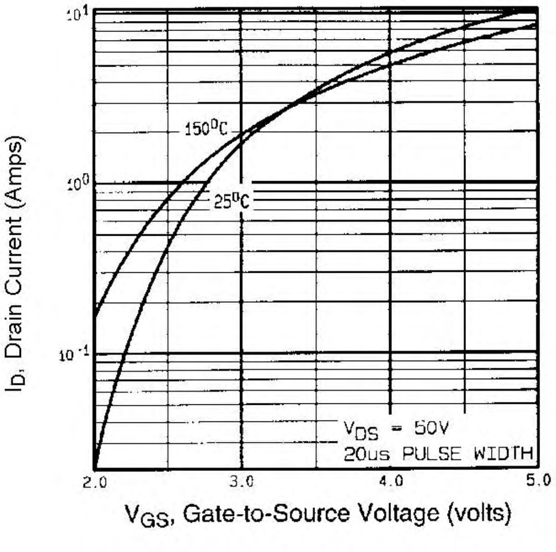


Fig 3. Typical Transfer Characteristics

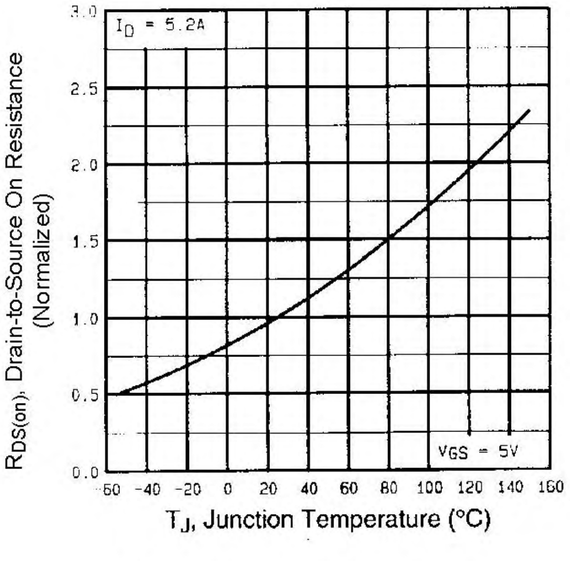


Fig 4. Normalized On-Resistance Vs. Temperature

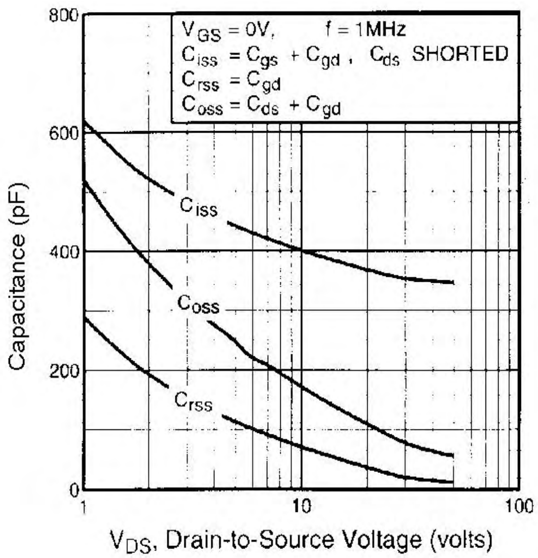


Fig 5. Typical Capacitance Vs. Drain-to-Source Voltage

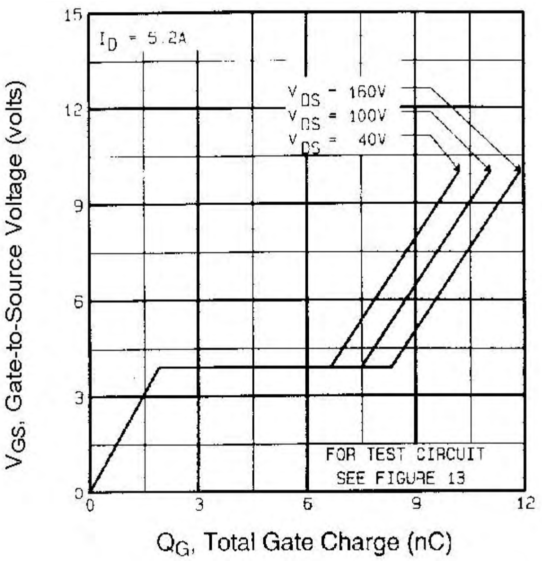


Fig 6. Typical Gate Charge Vs. Gate-to-Source Voltage

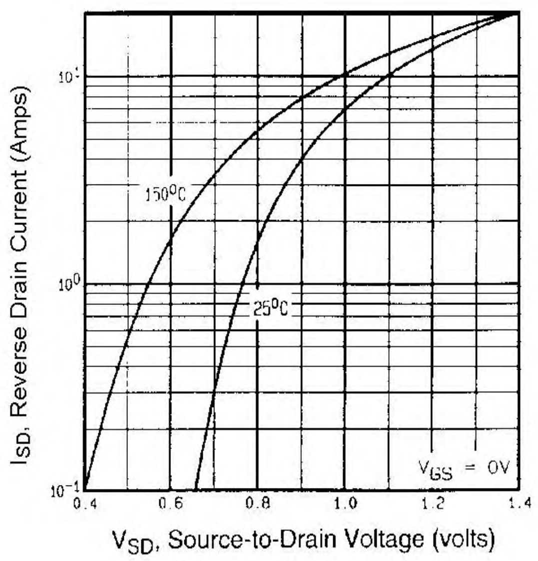


Fig 7. Typical Source-Drain Diode Forward Voltage

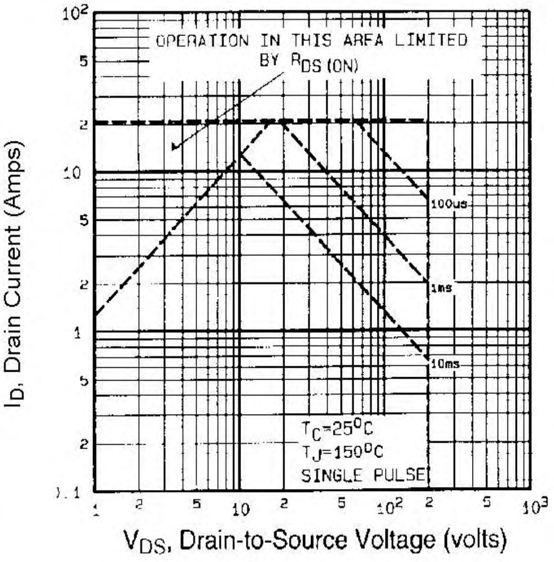


Fig 8. Maximum Safe Operating Area

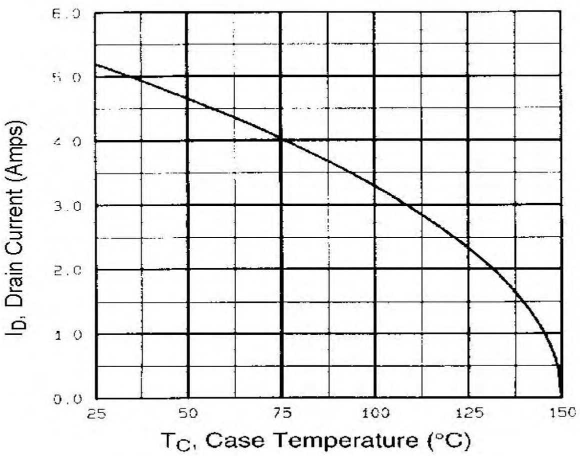


Fig 9. Maximum Drain Current Vs. Case Temperature

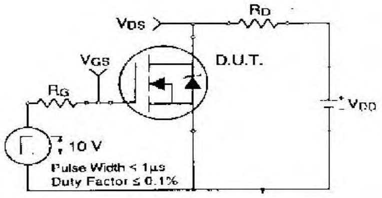


Fig 10a. Switching Time Test Circuit

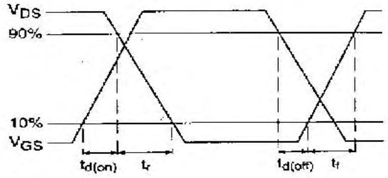


Fig 10b. Switching Time Waveforms

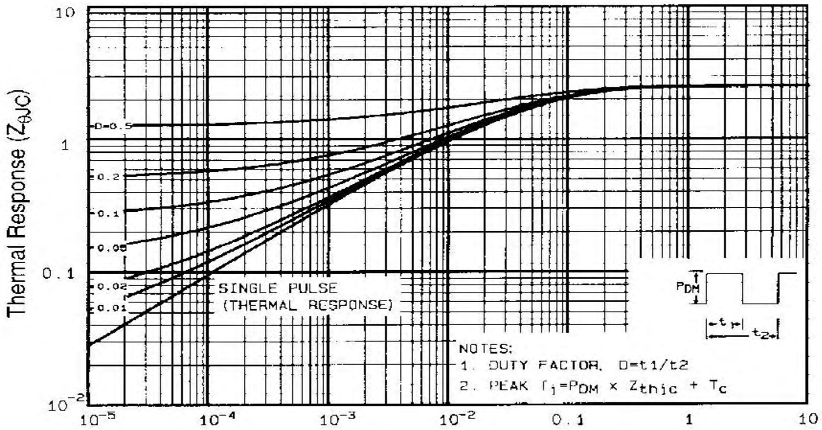


Fig 11. Maximum Effective Transient Thermal Impedance, Junction-to-Case

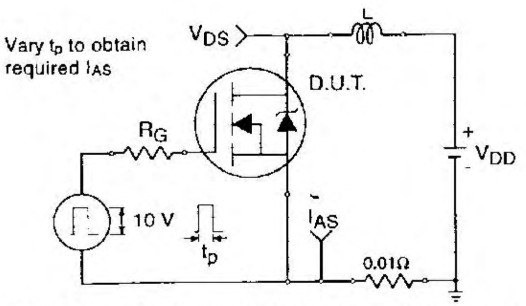


Fig 12a. Unclamped Inductive Test Circuit

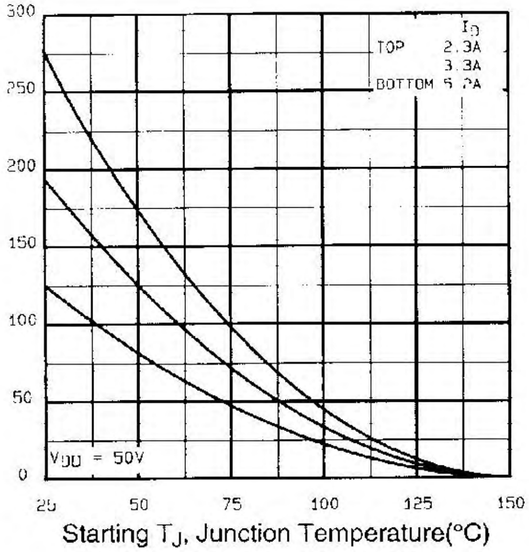


Fig 12c. Maximum Avalanche Energy Vs. Drain Current

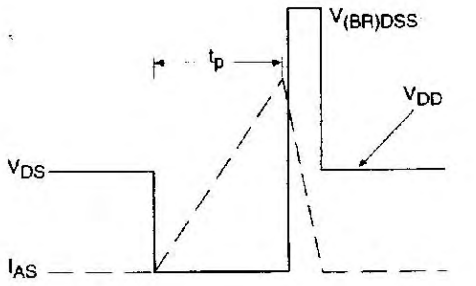


Fig 12b. Unclamped Inductive Waveforms

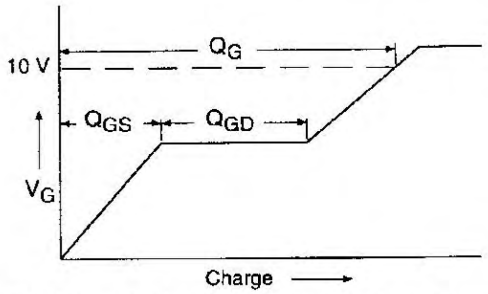


Fig 13a. Basic Gate Charge Waveform

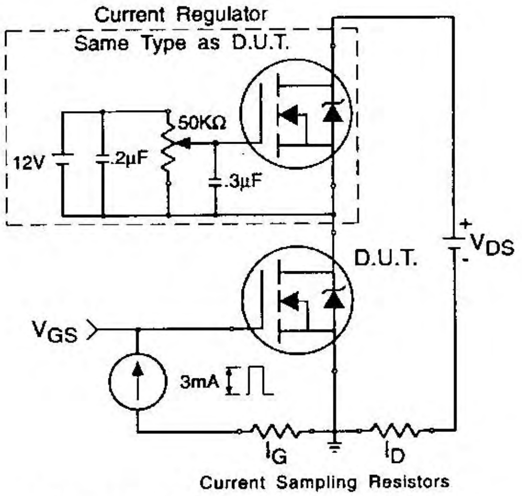
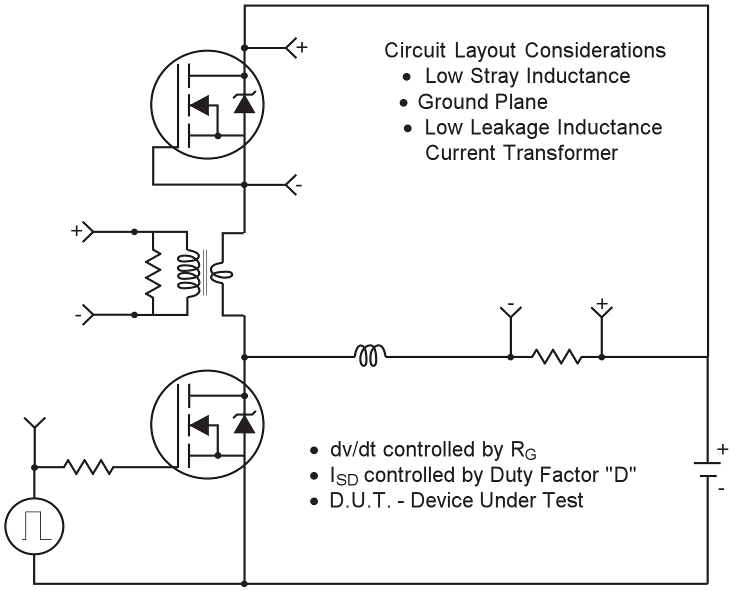


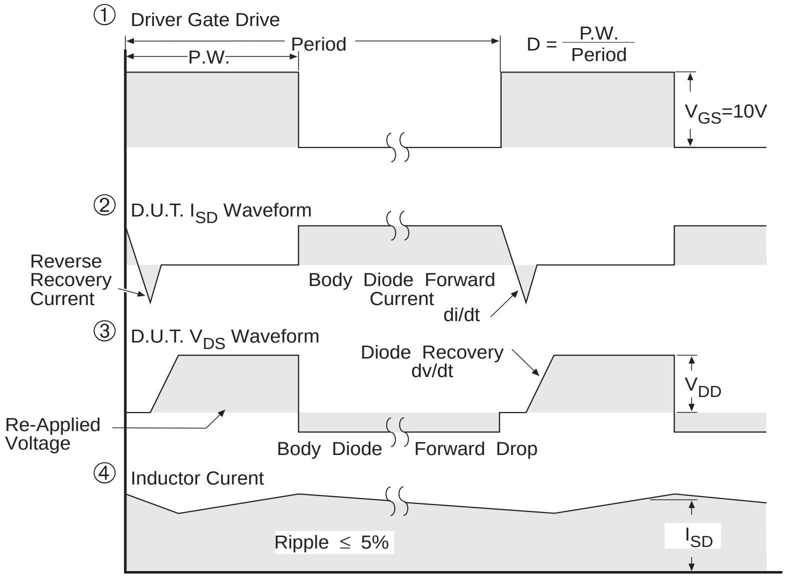
Fig 13b. Gate Charge Test Circuit

Peak Diode Recovery dv/dt Test Circuit



* Reverse Polarity for P-Channel

** Use P-Channel Driver for P-Channel Measurements

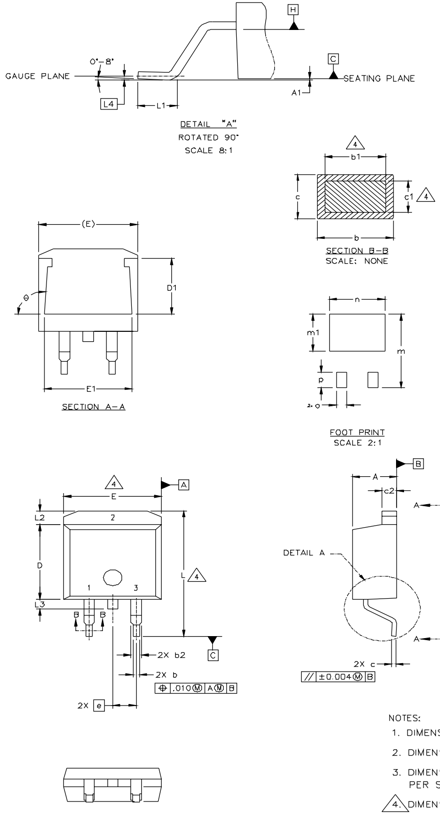


*** V_{GS} = 5.0V for Logic Level and 3V Drive Devices

Fig 14 For N Channel HEXFETS

D^{2}Pak Package Outline

Dimensions are shown in millimeters (inches)



SYMBOL	DIMENSIONS				NOTES
	MILLIMETERS		INCHES		
	MIN.	MAX.	MIN.	MAX.	
A	4.06	4.83	.160	.190	
A1		0.127		.005	
b	0.51	0.99	.020	.039	
b1	0.51	0.89	.020	.035	4
b2	1.14	1.40	.045	.055	
c	0.43	0.63	.017	.025	
c1	0.38	0.74	.015	.029	4
c2	1.14	1.40	.045	.055	
D	8.51	9.65	.335	.380	3
D1	5.33		.210		
E	9.65	10.67	.380	.420	3
E1	6.22		.245		
e	2.54 BSC		.100 BSC		
L	14.61	15.88	.575	.625	
L1	1.78	2.79	.070	.110	
L2		1.65		.065	
L3	1.27	1.78	.050	.070	
L4	0.25 BSC		.010 BSC		
m	17.78		.700		
m1	8.89		.350		
n	11.43		.450		
o	2.08		.082		
p	3.81		.150		
θ	90°	93°	90°	93°	

LEAD ASSIGNMENTS

HEXFET	IGBTs, CoPACK	DIODES
1.- GATE	1.- GATE	1.- ANODE *
2.- DRAIN	2.- COLLECTOR	2.- CATHODE
3.- SOURCE	3.- EMITTER	3.- ANODE

* PART DEPENDENT.

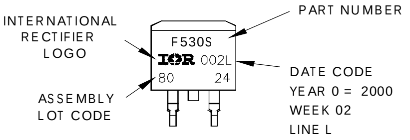
NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M-1994
2. DIMENSIONS ARE SHOWN IN MILLIMETERS [INCHES].
3. DIMENSION D & E DO NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED 0.127 [.005"] PER SIDE. THESE DIMENSIONS ARE MEASURED AT THE OUTMOST EXTREMES OF THE PLASTIC BODY.
4. DIMENSION b1 AND c1 APPLY TO BASE METAL ONLY.
5. CONTROLLING DIMENSION: INCH.

D^{2}Pak Part Marking Information

EXAMPLE: THIS IS AN IRF530S WITH
LOT CODE 8024
ASSEMBLED ON WW 02, 2000
IN THE ASSEMBLY LINE "L"

Note: "P" in assembly line
position indicates "Lead-Free"



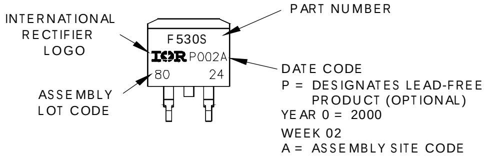
INTERNATIONAL
RECTIFIER
LOGO

PART NUMBER

ASSEMBLY
LOT CODE

DATE CODE
YEAR 0 = 2000
WEEK 02
LINE L

OR



INTERNATIONAL
RECTIFIER
LOGO

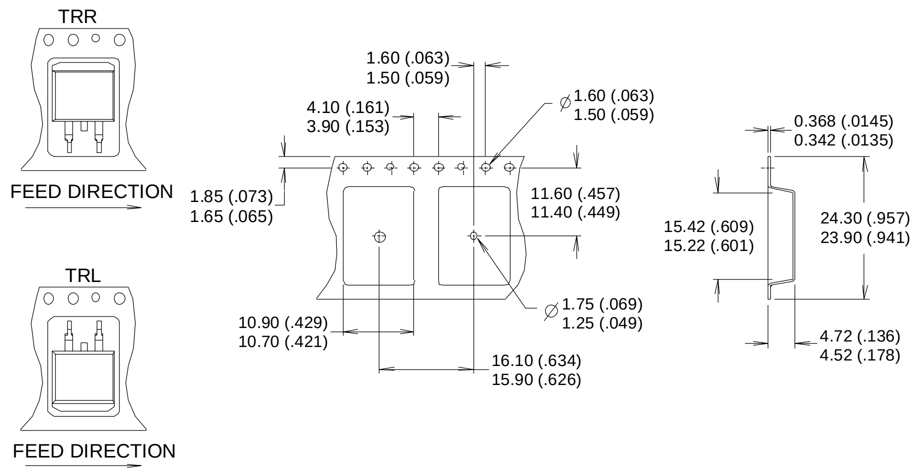
PART NUMBER

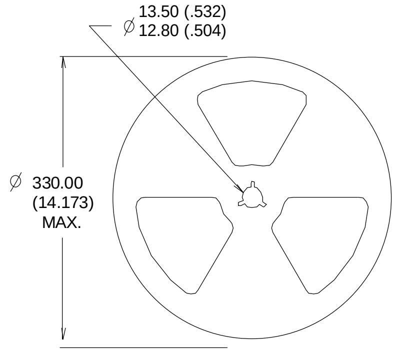
ASSEMBLY
LOT CODE

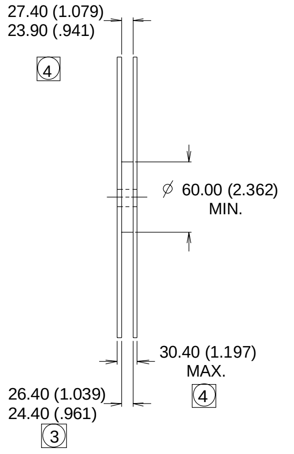
DATE CODE
P = DESIGNATES LEAD-FREE
PRODUCT (OPTIONAL)
YEAR 0 = 2000
WEEK 02
A = ASSEMBLY SITE CODE

D²Pak Tape & Reel Information

Dimensions are shown in millimeters (inches)







NOTES :
1. COMFORMS TO EIA-418.
2. CONTROLLING DIMENSION: MILLIMETER.
3 DIMENSION MEASURED @ HUB.
4 INCLUDES FLANGE DISTORTION @ OUTER EDGE.

International
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