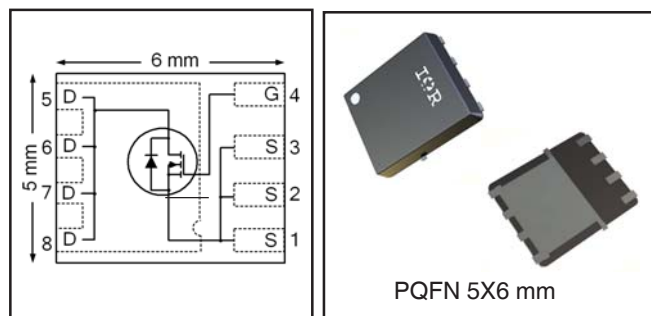


HEXFET® Power MOSFET

V_{DS}	20	V
$V_{GS\ max}$	± 12	V
$R_{DS(on)\ max}$ (@ $V_{GS} = 4.5V$)	3.0	mΩ
(@ $V_{GS} = 2.5V$)	4.0	
$Q_g\ typ$	44	nC
I_D (@ $T_{C(Bottom)} = 25^\circ C$)	80 ^⑦	A



Applications

- Battery Protection Switch

Features and Benefits

Features

Low Thermal Resistance to PCB (< 2.4°C/W)
100% Rg tested
Low Profile (<1.2mm)
Industry-Standard Pinout
Compatible with Existing Surface Mount Techniques
RoHS Compliant Containing no Lead, no Bromide and no Halogen
MSL1, Industrial Qualification

Benefits

Enable better thermal dissipation
Increased Reliability
Increased Power Density
Multi-Vendor Compatibility
Easier Manufacturing
Environmentally Friendlier
Increased Reliability

results in
⇒

Orderable part number	Package Type	Standard Pack		Note
		Form	Quantity	
IRLH6224TRPBF	PQFN 5mm x 6mm	Tape and Reel	4000	
IRLH6224TR2PBF	PQFN 5mm x 6mm	Tape and Reel	400	EOL notice # 259

Absolute Maximum Ratings

	Parameter	Max.	Units
V_{DS}	Drain-to-Source Voltage	20	V
V_{GS}	Gate-to-Source Voltage	± 12	
$I_D @ T_A = 25^\circ C$	Continuous Drain Current, $V_{GS} @ 10V$	28	A
$I_D @ T_A = 70^\circ C$	Continuous Drain Current, $V_{GS} @ 10V$	22	
$I_D @ T_{C(Bottom)} = 25^\circ C$	Continuous Drain Current, $V_{GS} @ 10V$	105 ^{⑥ ⑦}	
$I_D @ T_{C(Bottom)} = 100^\circ C$	Continuous Drain Current, $V_{GS} @ 10V$	67 ^⑥	
$I_D @ T_C = 25^\circ C$	Continuous Drain Current, $V_{GS} @ 10V$ (Package Limited)	80 ^⑦	
I_{DM}	Pulsed Drain Current ^①	400	
$P_D @ T_A = 25^\circ C$	Power Dissipation ^②	3.6	W
$P_D @ T_{C(Bottom)} = 25^\circ C$	Power Dissipation ^②	52	
	Linear Derating Factor ^③	0.029	W/°C
T_J T_{STG}	Operating Junction and Storage Temperature Range	-55 to + 150	°C

Notes ① through ⑥ are on page 9

Static @ $T_J = 25^\circ\text{C}$ (unless otherwise specified)

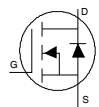
	Parameter	Min.	Typ.	Max.	Units	Conditions
BV_{DSS}	Drain-to-Source Breakdown Voltage	20	—	—	V	$V_{GS} = 0V, I_D = 250\mu A$
$\Delta BV_{DSS}/\Delta T_J$	Breakdown Voltage Temp. Coefficient	—	5.0	—	mV/ $^\circ\text{C}$	Reference to 25°C , $I_D = 1.0\text{mA}$
$R_{DS(on)}$	Static Drain-to-Source On-Resistance	—	2.3	3.0	$m\Omega$	$V_{GS} = 4.5V, I_D = 20A$ ③ $V_{GS} = 2.5V, I_D = 16A$ ③
$V_{GS(th)}$	Gate Threshold Voltage	0.5	0.8	1.1	V	$V_{DS} = V_{GS}, I_D = 50\mu A$
$\Delta V_{GS(th)}$	Gate Threshold Voltage Coefficient	—	-4.2	—	mV/ $^\circ\text{C}$	
I_{DSS}	Drain-to-Source Leakage Current	—	—	1	μA	$V_{DS} = 16V, V_{GS} = 0V$ $V_{DS} = 16V, V_{GS} = 0V, T_J = 125^\circ\text{C}$
I_{GSS}	Gate-to-Source Forward Leakage	—	—	100	nA	$V_{GS} = 12V$
	Gate-to-Source Reverse Leakage	—	—	-100	nA	$V_{GS} = -12V$
g_{fs}	Forward Transconductance	150	—	—	S	$V_{DS} = 10V, I_D = 20A$
Q_g	Total Gate Charge	—	86	—	nC	$V_{GS} = 10V, V_{DS} = 15V, I_D = 20A$
Q_g	Total Gate Charge	—	44	—	nC	$V_{DS} = 10V$ $V_{GS} = 4.5V$ $I_D = 20A$
Q_{gs1}	Pre-Vth Gate-to-Source Charge	—	3.8	—		
Q_{gs2}	Post-Vth Gate-to-Source Charge	—	4.7	—		
Q_{gd}	Gate-to-Drain Charge	—	8.5	—		
Q_{godr}	Gate Charge Overdrive	—	27	—		
Q_{sw}	Switch Charge ($Q_{gs2} + Q_{gd}$)	—	13	—	nC	$V_{DS} = 16V, V_{GS} = 0V$
Q_{oss}	Output Charge	—	30	—		
R_g	Gate Resistance	—	2.0	—	Ω	
$t_{d(on)}$	Turn-On Delay Time	—	9.4	—	ns	$V_{DD} = 15V, V_{GS} = 4.5V$ $I_D = 20A$ $R_G = 1.8\Omega$
t_r	Rise Time	—	23	—		
$t_{d(off)}$	Turn-Off Delay Time	—	67	—		
t_f	Fall Time	—	36	—		
C_{iss}	Input Capacitance	—	3710	—	pF	$V_{GS} = 0V$
C_{oss}	Output Capacitance	—	1050	—		$V_{DS} = 10V$
C_{iss}	Reverse Transfer Capacitance	—	770	—		$f = 1.0\text{MHz}$

Avalanche Characteristics

	Parameter	Typ.	Max.	Units
E_{AS}	Single Pulse Avalanche Energy ②	—	125	mJ
I_{AR}	Avalanche Current ①	—	20	A

Diode Characteristics

	Parameter	Min.	Typ.	Max.	Units	Conditions
I_S	Continuous Source Current (Body Diode)	—	—	67	A	MOSFET symbol showing the integral reverse p-n junction diode.
I_{SM}	Pulsed Source Current (Body Diode) ①	—	—	400		
V_{SD}	Diode Forward Voltage	—	—	1.2	V	$T_J = 25^\circ\text{C}, I_S = 20A, V_{GS} = 0V$ ③
t_{rr}	Reverse Recovery Time	—	38	57	ns	$T_J = 25^\circ\text{C}, I_F = 20A, V_{DD} = 15V$
Q_{rr}	Reverse Recovery Charge	—	82	125	nC	$di/dt = 300A/\mu s$ ③
t_{on}	Forward Turn-On Time	Time is dominated by parasitic Inductance				


Thermal Resistance

	Parameter	Typ.	Max.	Units
$R_{\theta JC}$ (Bottom)	Junction-to-Case ④	—	2.4	$^\circ\text{C/W}$
$R_{\theta JC}$ (Top)	Junction-to-Case ④	—	34	
$R_{\theta JA}$	Junction-to-Ambient ⑤	—	35	
$R_{\theta JA} (<10s)$	Junction-to-Ambient ⑤	—	22	

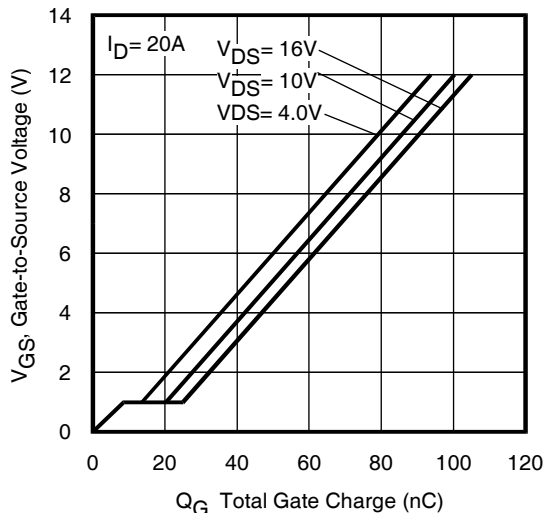
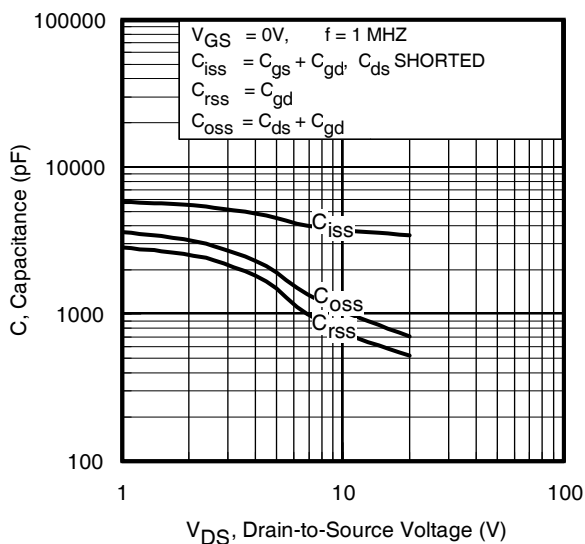
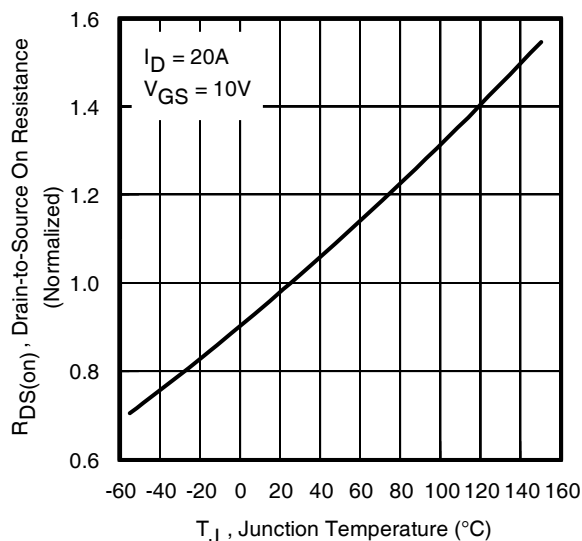
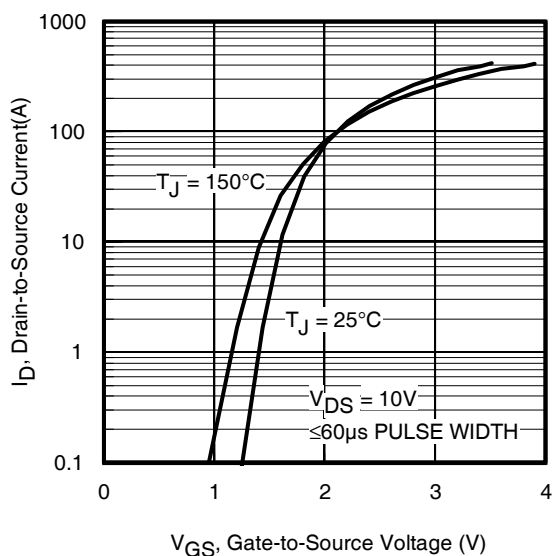
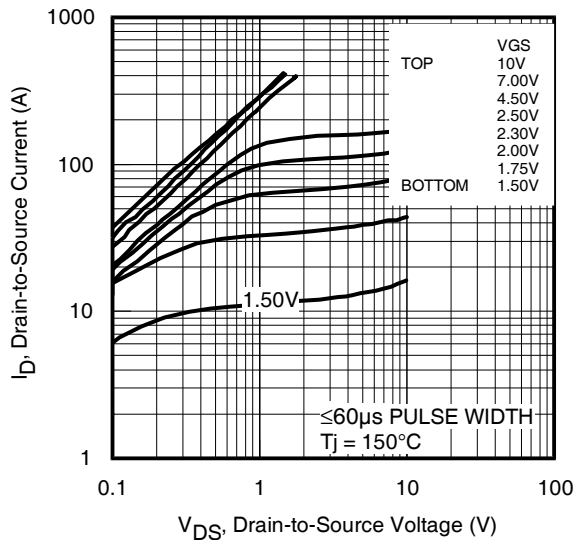
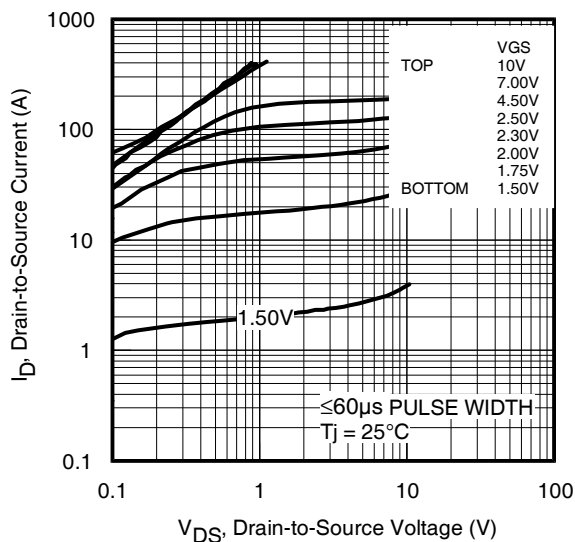
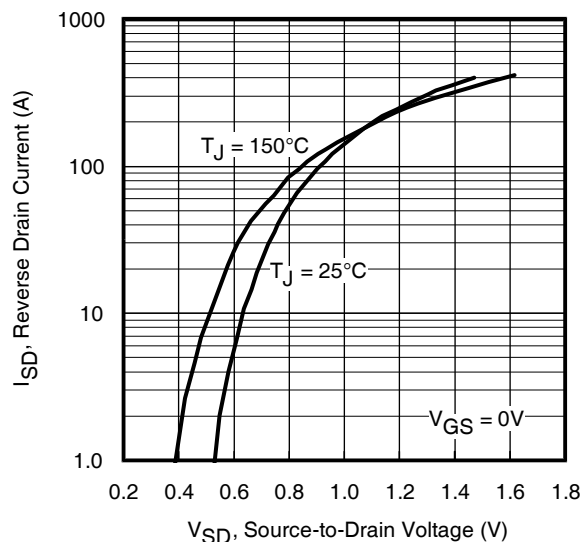
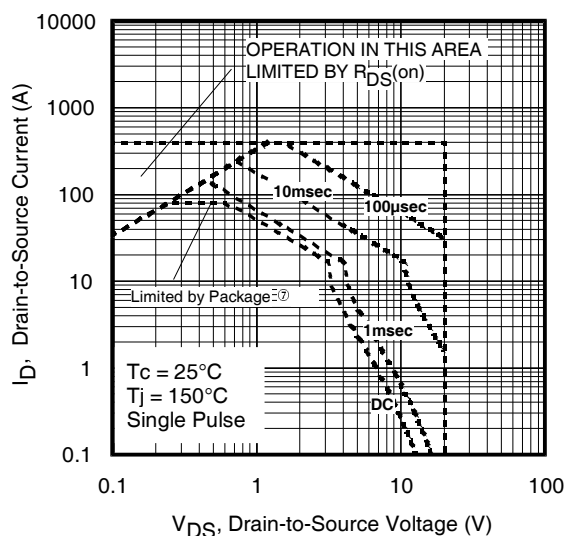
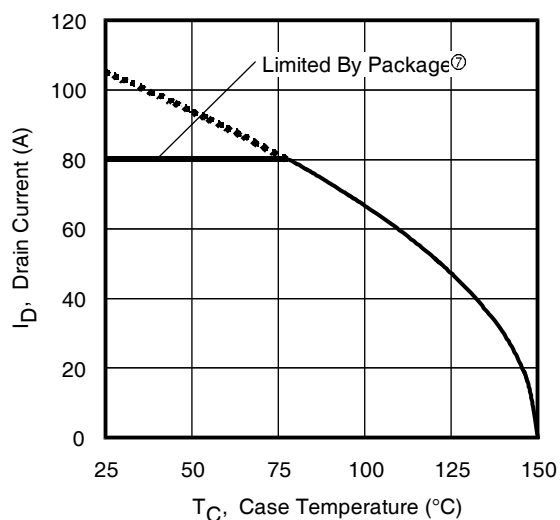
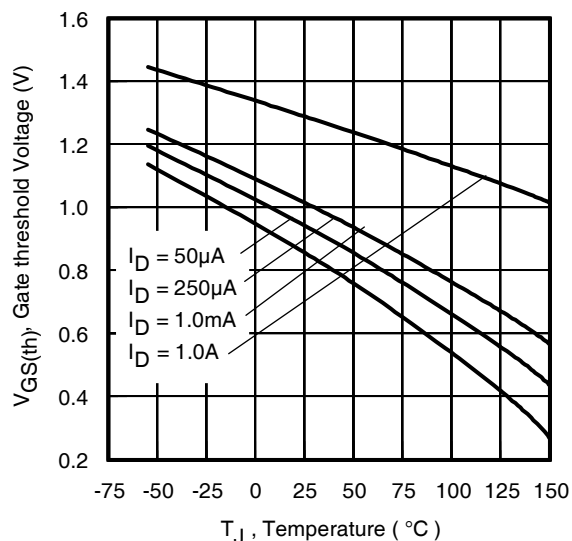
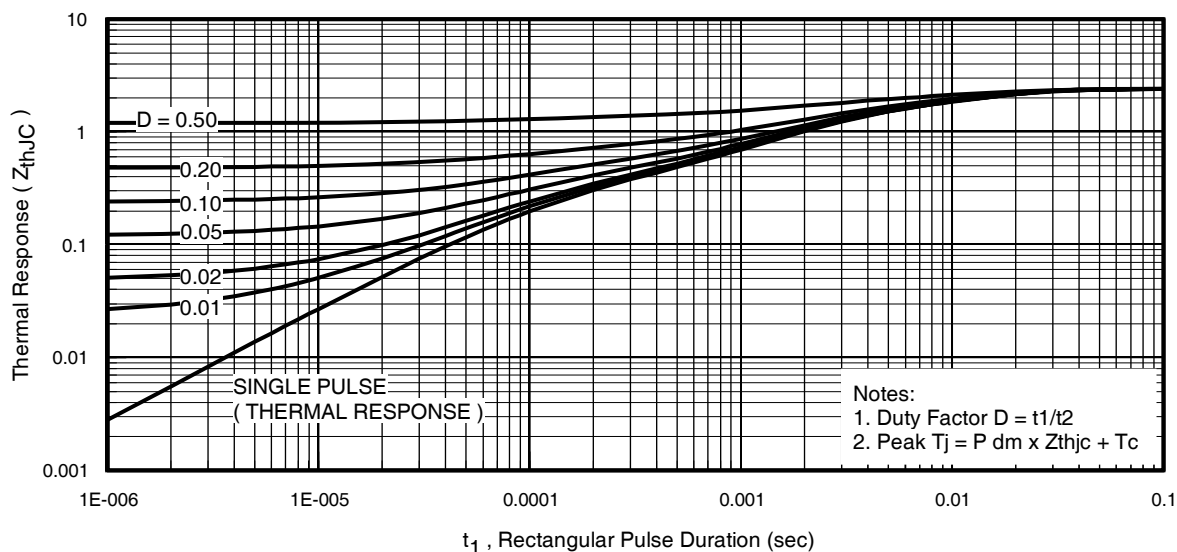
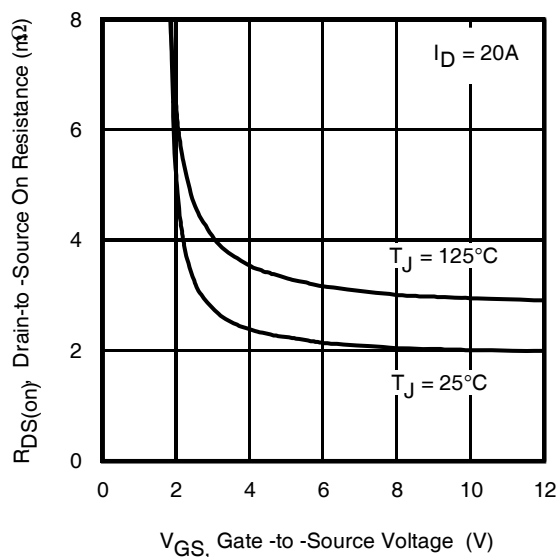
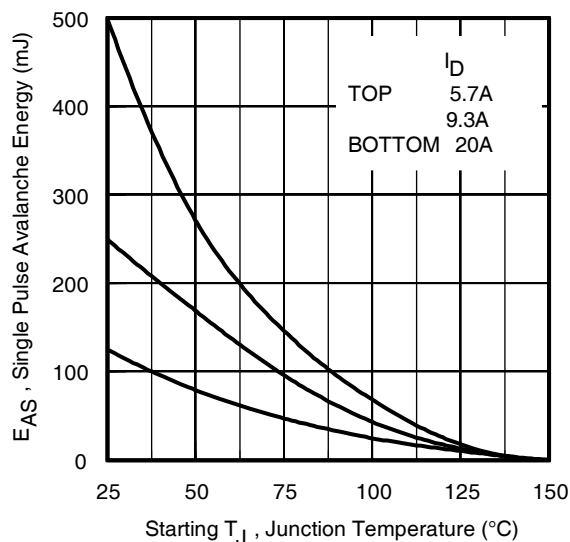
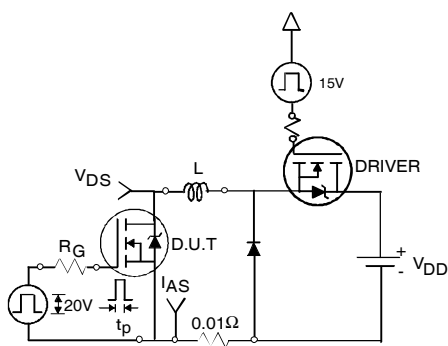
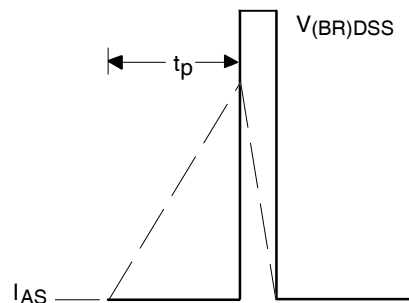
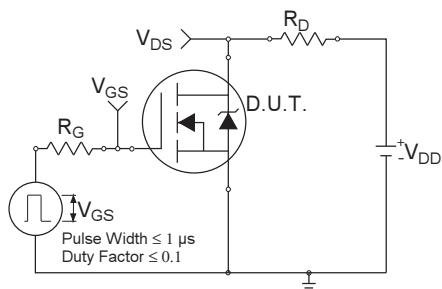
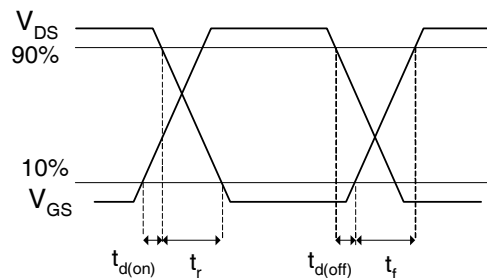


Fig 5. Typical Capacitance vs. Drain-to-Source Voltage

Fig 6. Typical Gate Charge vs. Gate-to-Source Voltage


Fig 7. Typical Source-Drain Diode Forward Voltage

Fig 8. Maximum Safe Operating Area

Fig 9. Maximum Drain Current vs. Case (Bottom) Temperature

Fig 10. Threshold Voltage vs. Temperature

Fig 11. Maximum Effective Transient Thermal Impedance, Junction-to-Case (Bottom)


Fig 12. On-Resistance vs. Gate Voltage

Fig 13. Maximum Avalanche Energy vs. Drain Current

Fig 14a. Unclamped Inductive Test Circuit

Fig 14b. Unclamped Inductive Waveforms

Fig 15a. Switching Time Test Circuit

Fig 15b. Switching Time Waveforms

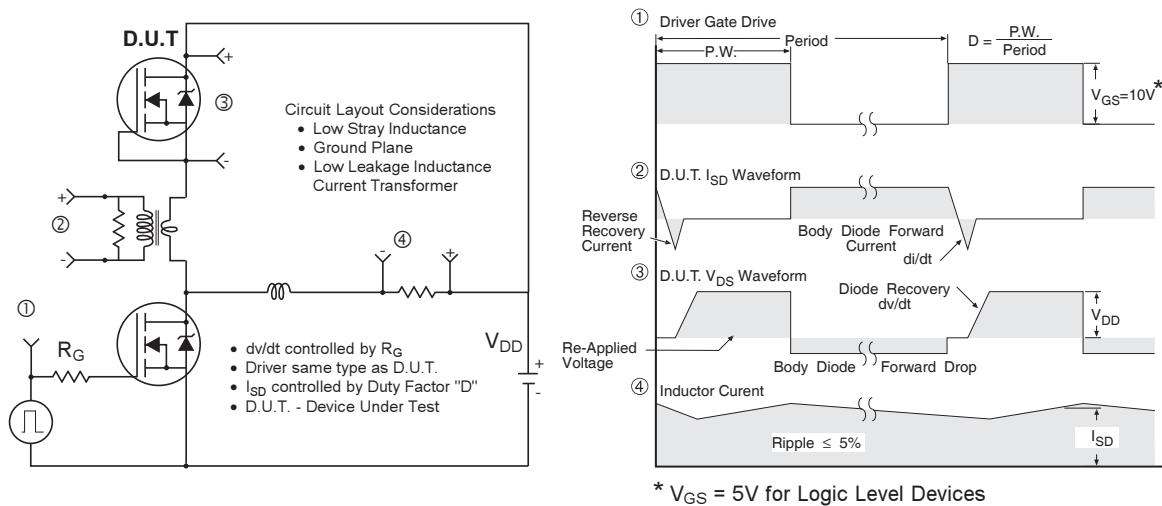


Fig 16. Peak Diode Recovery dv/dt Test Circuit for N-Channel HEXFET® Power MOSFETs

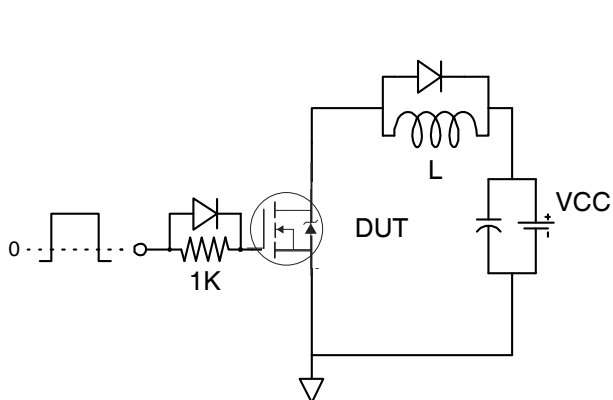


Fig 17. Gate Charge Test Circuit

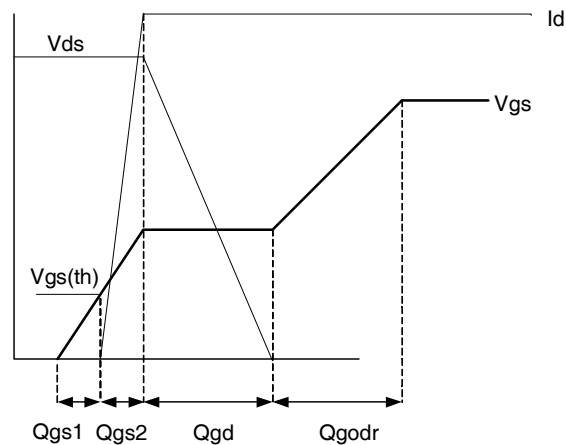
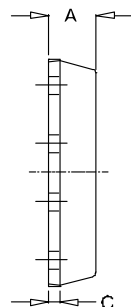
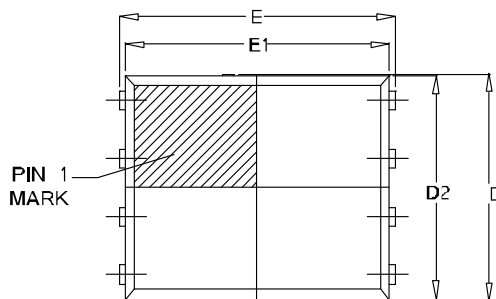


Fig 18. Gate Charge Waveform

PQFN 5x6 Outline "E" Package Details

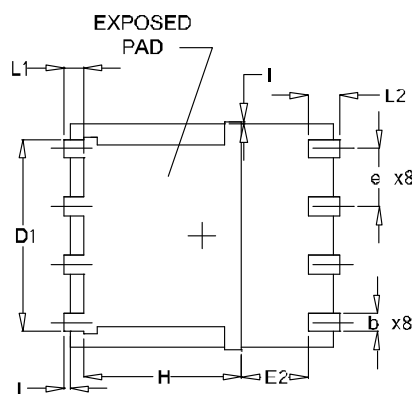


SIDEVIEW



TOP VIEW

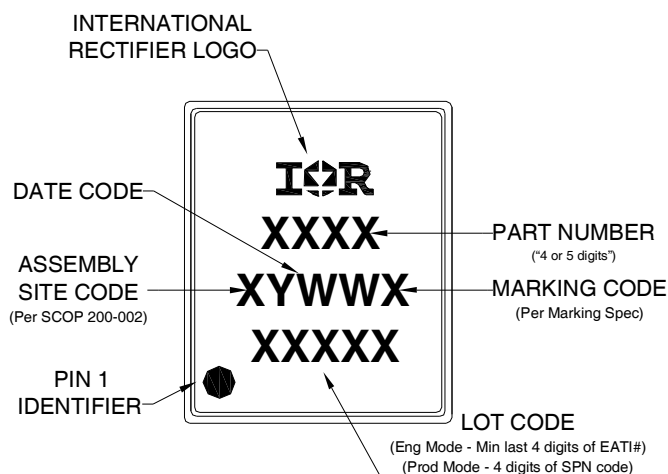
SYMBOL	OUTLINE PQFN 5X6E		
	MIN.	NOM	MAX.
A	0.90	1.03	1.17
b	0.33	0.41	0.48
C	0.20	0.25	0.35
D	4.80	4.98	5.15
D1	3.91	4.11	4.31
D2	4.80	4.90	5.00
E	5.90	6.02	6.15
E1	5.65	5.75	5.85
E2	1.10	—	—
e	1.27 BSC		
L	0.05	0.15	0.25
L1	0.38	0.44	0.50
L2	0.51	0.68	0.86
H	3.32	3.45	3.58
I	—	—	0.18



BOTTOM VIEW

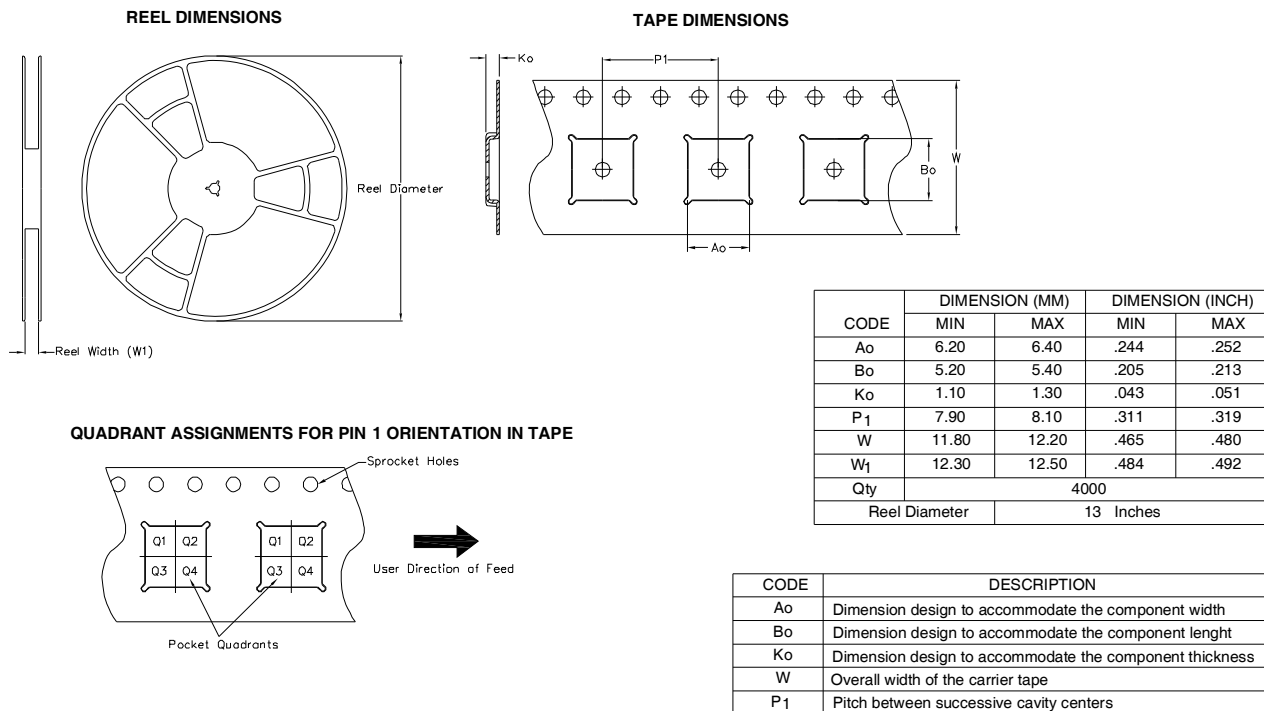
For footprint and stencil design recommendations, please refer to application note AN-1154 at <http://www.irf.com/technical-info/appnotes/an-1154.pdf>

PQFN 5x6 Outline "E" Part Marking



Note: For the most current drawing please refer to IR website at: <http://www.irf.com/package/>

PQFN 5x6 Outline "E" Tape and Reel



Note: For the most current drawing please refer to IR website at: <http://www.irf.com/package/>

Note: For the most current drawing please refer to IR website at: <http://www.irf.com/package/>

Qualification information[†]

Qualification level	Indus trid ^{††} (per JEDEC JES D47F ^{†††} guidelines)	
Moisture Sensitivity Level	PQFN 5mm x 6mm	MSL1 (per JEDEC J-STD-020D ^{†††})
RoHS compliant	Yes	

[†] Qualification standards can be found at International Rectifier's web site

<http://www.irf.com/product-info/reliability>

^{††} Higher qualification ratings may be available should the user have such requirements.
Please contact your International Rectifier sales representative for further information:

<http://www.irf.com/whoto-call/salesrep/>

^{†††} Applicable version of JEDEC standard at the time of product release.

Notes:

- ① Repetitive rating; pulse width limited by max. junction temperature.
- ② Starting $T_J = 25^{\circ}\text{C}$, $L = 0.63\text{mH}$, $R_G = 50\Omega$, $I_{AS} = 20\text{A}$.
- ③ Pulse width $\leq 400\mu\text{s}$; duty cycle $\leq 2\%$.
- ④ R_{θ} is measured at T_J of approximately 90°C .
- ⑤ When mounted on 1 inch square 2 oz copper pad on 1.5x1.5 in. board of FR-4 material.
- ⑥ Calculated continuous current based on maximum allowable junction temperature.
- ⑦ Package is limited to 80A by die-source to lead-frame bonding technology

Revision History

Date	Comment
5/12/2014	- Updated ordering information to reflect the End-Of-life (EOL) of the mini-reel option (EOL notice #259) - Updated Tape and Reel on page 8. - Updated data sheet based on corporate template.

International
 Rectifier

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