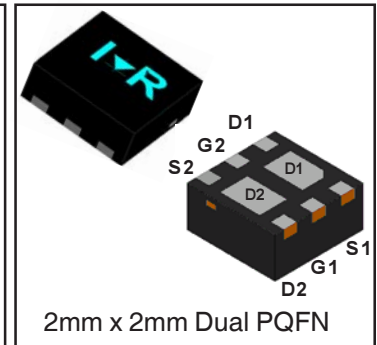
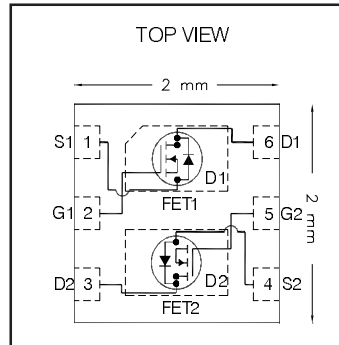


HEXFET® Power MOSFET

V_{DS}	30	V
V_{GS}	±12	V
$R_{DS(on) \max}$ (@ $V_{GS} = 4.5V$)	63	mΩ
$R_{DS(on) \max}$ (@ $V_{GS} = 2.5V$)	82	mΩ
I_D (@ $T_{c(Bottom)} = 25^\circ C$)	3.4 ②	A



Applications

- Charge and discharge switch for battery application
- Load/System Switch

Features and Benefits

Features

Low $R_{DS(on)}$ ($\leq 63m\Omega$)
Low Thermal Resistance to PCB ($\leq 19^\circ C/W$)
Low Profile ($\leq 1.0mm$)
Industry-Standard Pinout
Compatible with Existing Surface Mount Techniques
RoHS Compliant Containing no Lead, no Bromide and no Halogen

results in
⇒

Resulting Benefits

Lower Conduction Losses
Enable better thermal dissipation
Increased Power Density
Multi-Vendor Compatibility
Easier Manufacturing
Environmentally Friendlier

Orderable part number	Package Type	Standard Pack		Note
		Form	Quantity	
IRLHS6376TRPBF	PQFN Dual 2mm x 2mm	Tape and Reel	4000	
IRLHS6376TR2PBF	PQFN Dual 2mm x 2mm	Tape and Reel	400	EOL notice #259

Absolute Maximum Ratings

	Parameter	Max.	Units
V_{DS}	Drain-to-Source Voltage	30	V
V_{GS}	Gate-to-Source Voltage	±12	
I_D @ $T_A = 25^\circ C$	Continuous Drain Current, V_{GS} @ 4.5V	3.6 ②	A
I_D @ $T_A = 70^\circ C$	Continuous Drain Current, V_{GS} @ 4.5V	2.9	
I_D @ $T_{C(Bottom)} = 25^\circ C$	Continuous Drain Current, V_{GS} @ 4.5V	7.6 ②	
I_D @ $T_{C(Bottom)} = 100^\circ C$	Continuous Drain Current, V_{GS} @ 4.5V	4.9 ②	
I_D @ $T_{C(Bottom)} = 25^\circ C$	Continuous Drain Current, V_{GS} @ 4.5V (Package Limited)	3.4 ②	
I_{DM}	Pulsed Drain Current ①	30	
P_D @ $T_A = 25^\circ C$	Power Dissipation ④	1.5	W
P_D @ $T_{C(Bottom)} = 25^\circ C$	Power Dissipation ④	6.6	
	Linear Derating Factor ④	0.012	W/°C
T_J T_{STG}	Operating Junction and Storage Temperature Range	-55 to + 150	°C

Notes ① through ⑥ are on page 2

Static @ $T_J = 25^\circ\text{C}$ (unless otherwise specified)

	Parameter	Min.	Typ.	Max.	Units	Conditions
BV_{DSS}	Drain-to-Source Breakdown Voltage	30	—	—	V	$V_{GS} = 0V, I_D = 250\mu A$
$\Delta BV_{DSS}/\Delta T_J$	Breakdown Voltage Temp. Coefficient	—	0.023	—	V/ $^\circ\text{C}$	Reference to 25°C , $I_D = 1\text{mA}$
$R_{DS(on)}$	Static Drain-to-Source On-Resistance	—	48	63	m Ω	$V_{GS} = 4.5V, I_D = 3.4A$ ③②
		—	61	82		$V_{GS} = 2.5V, I_D = 3.4A$ ③②
$V_{GS(th)}$	Gate Threshold Voltage	0.5	0.8	1.1	V	$V_{DS} = V_{GS}, I_D = 10\mu A$
$\Delta V_{GS(th)}$	Gate Threshold Voltage Coefficient	—	-3.6	—	mV/ $^\circ\text{C}$	
I_{DSS}	Drain-to-Source Leakage Current	—	—	1.0	μA	$V_{DS} = 24V, V_{GS} = 0V$
		—	—	150		$V_{DS} = 24V, V_{GS} = 0V, T_J = 125^\circ\text{C}$
I_{GSS}	Gate-to-Source Forward Leakage	—	—	100	nA	$V_{GS} = 12V$
	Gate-to-Source Reverse Leakage	—	—	-100		$V_{GS} = -12V$
g_{fs}	Forward Transconductance	8.8	—	—	S	$V_{DS} = 10V, I_D = 3.4A$ ②
Q_g	Total Gate Charge ⑥	—	2.8	—	nC	$V_{DS} = 15V$
Q_{gs}	Gate-to-Source Charge ⑥	—	0.13	—		$V_{GS} = 4.5V$
Q_{gd}	Gate-to-Drain Charge ⑥	—	1.1	—		$I_D = 3.4A$ ② (See Fig.17 & 18)
R_G	Gate Resistance	—	4.6	—	Ω	
$t_{d(on)}$	Turn-On Delay Time	—	4.4	—	ns	$V_{DD} = 10V, V_{GS} = 4.5V$
t_r	Rise Time	—	11	—		$I_D = 3.4A$ ②
$t_{d(off)}$	Turn-Off Delay Time	—	11	—		$R_G = 1.8\Omega$
t_f	Fall Time	—	9.4	—		See Fig.15
C_{iss}	Input Capacitance	—	270	—	pF	$V_{GS} = 0V$
C_{oss}	Output Capacitance	—	32	—		$V_{DS} = 25V$
C_{rss}	Reverse Transfer Capacitance	—	20	—		$f = 1.0\text{MHz}$

Diode Characteristics

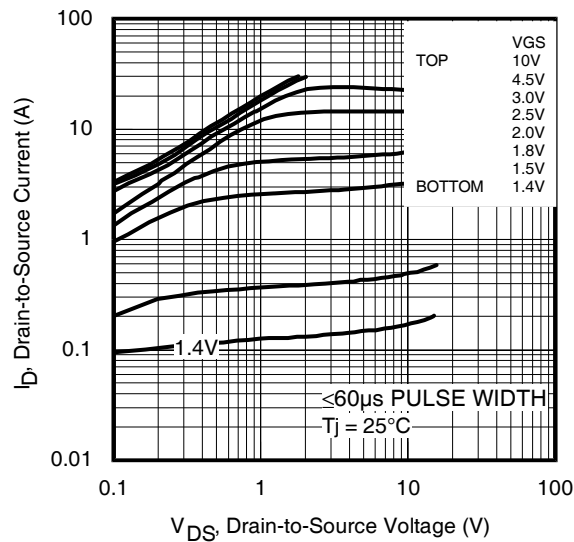
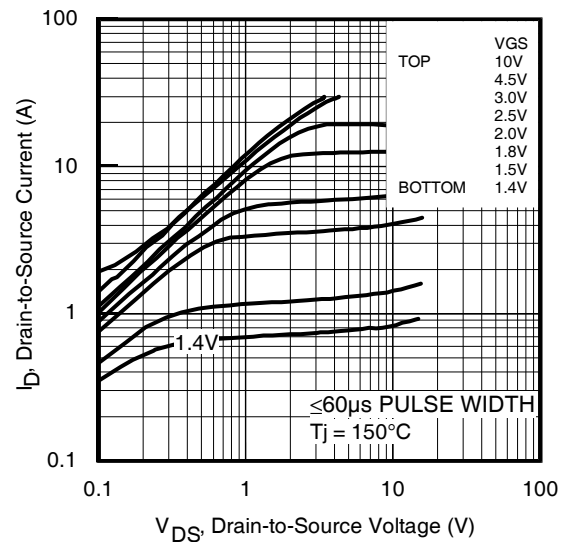
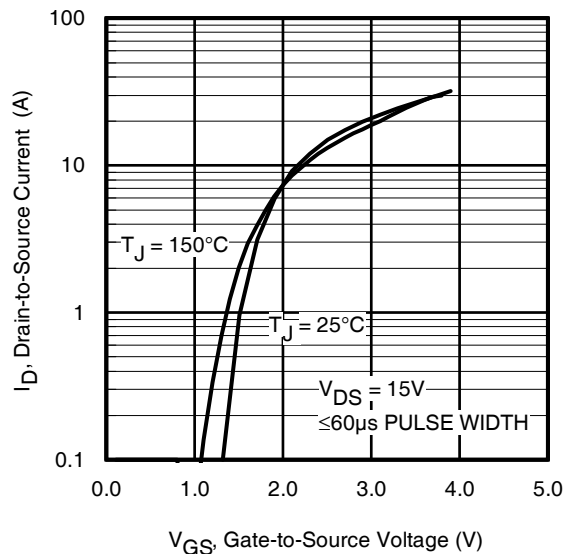
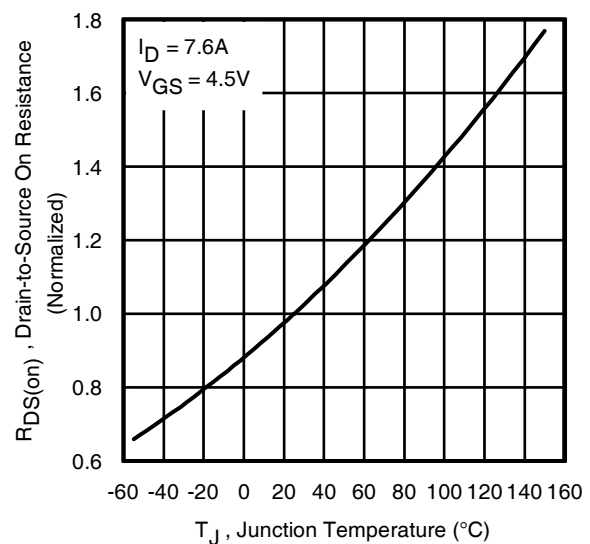
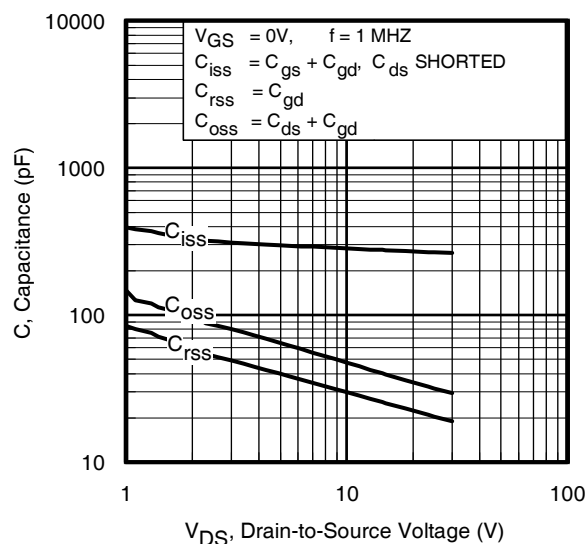
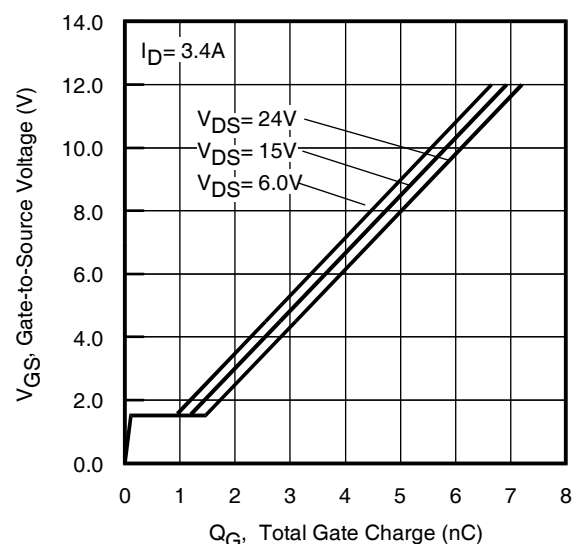
	Parameter	Min.	Typ.	Max.	Units	Conditions
I_S	Continuous Source Current (Body Diode)	—	—	7.6②	A	MOSFET symbol showing the integral reverse p-n junction diode.
I_{SM}	Pulsed Source Current (Body Diode) ①	—	—	30		
V_{SD}	Diode Forward Voltage	—	—	1.2	V	$T_J = 25^\circ\text{C}, I_S = 3.4A$ ②, $V_{GS} = 0V$ ③
t_{rr}	Reverse Recovery Time	—	8.0	12	ns	$T_J = 25^\circ\text{C}, I_F = 3.4A$ ②, $V_{DD} = 15V$
Q_{rr}	Reverse Recovery Charge	—	5.9	8.9	nC	$di/dt = 260A/\mu s$ ③
t_{on}	Forward Turn-On Time	Time is dominated by parasitic Inductance				

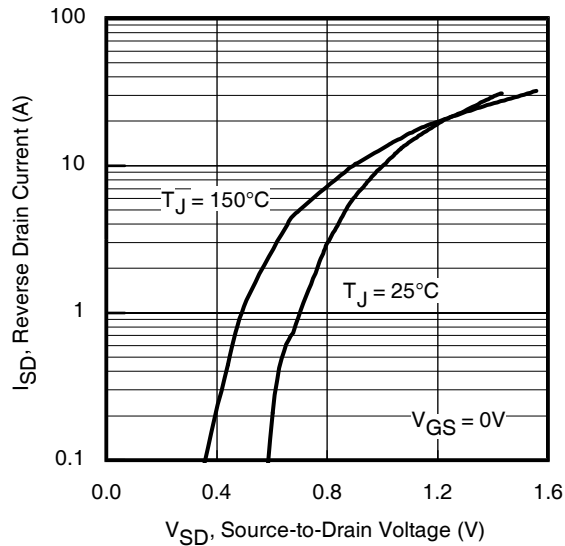
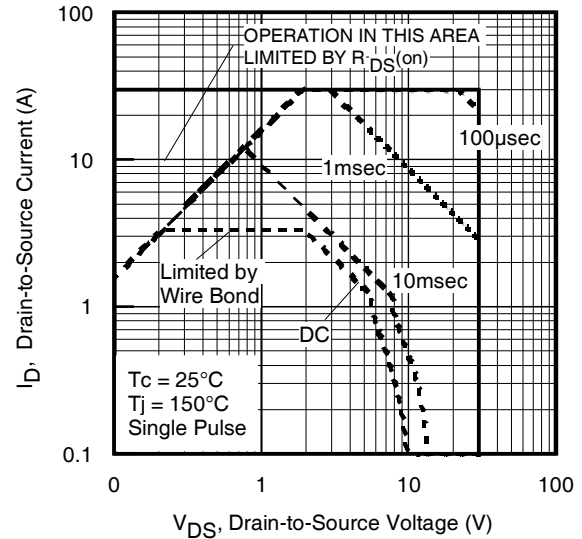
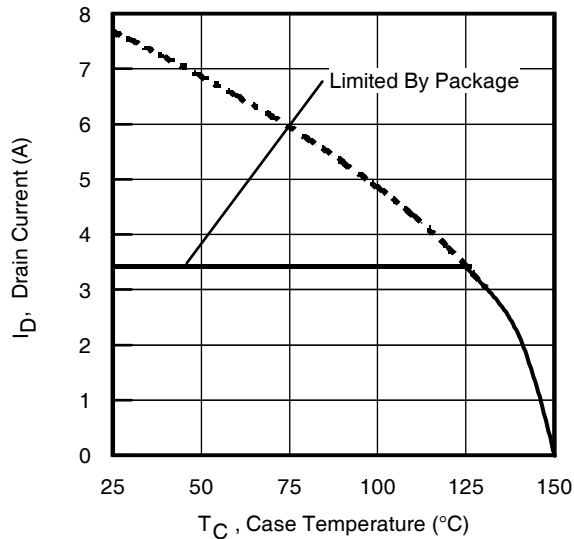
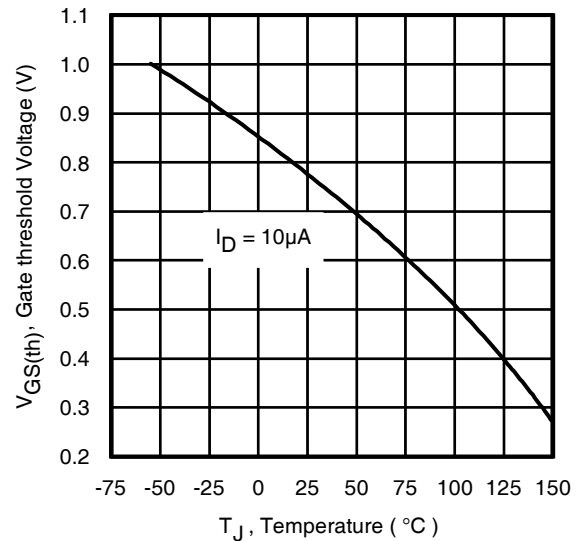
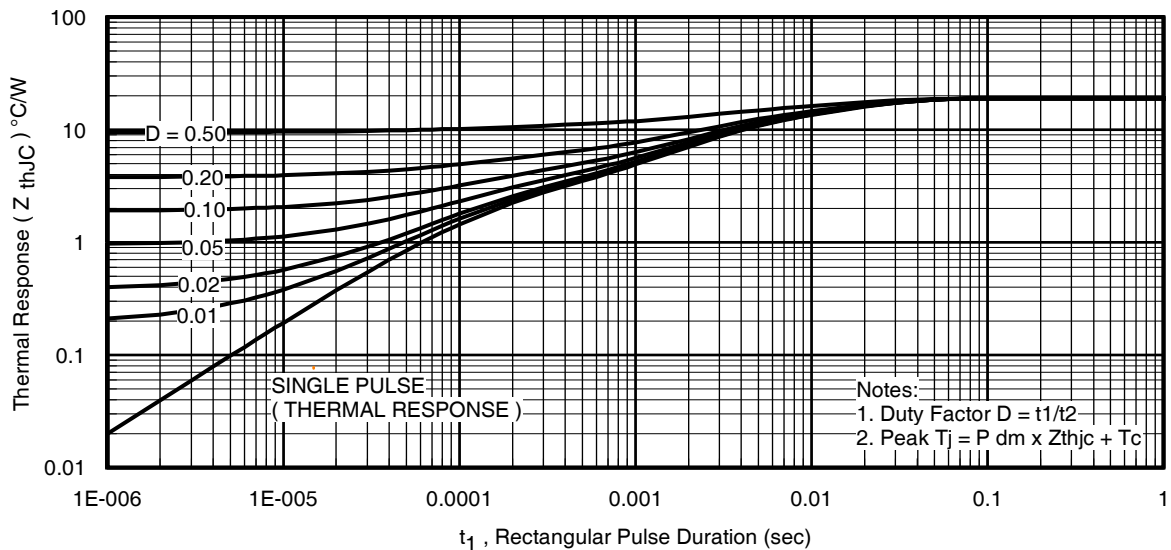
Thermal Resistance

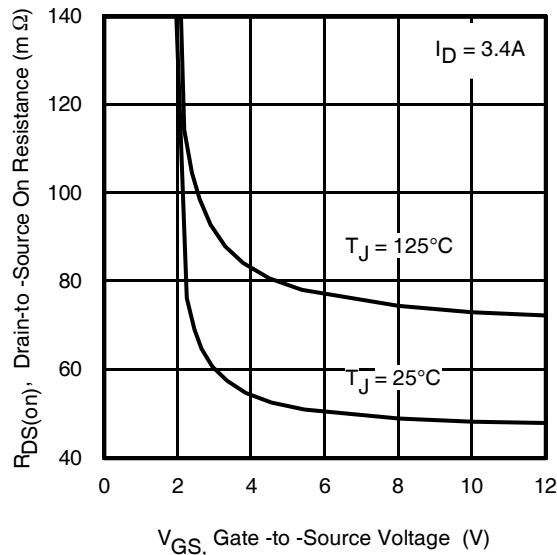
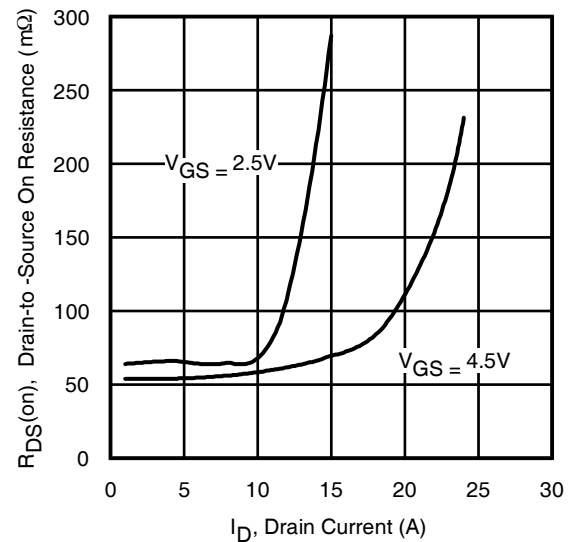
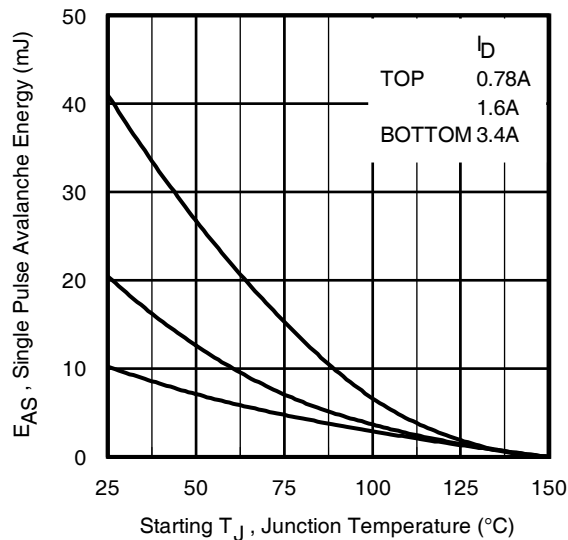
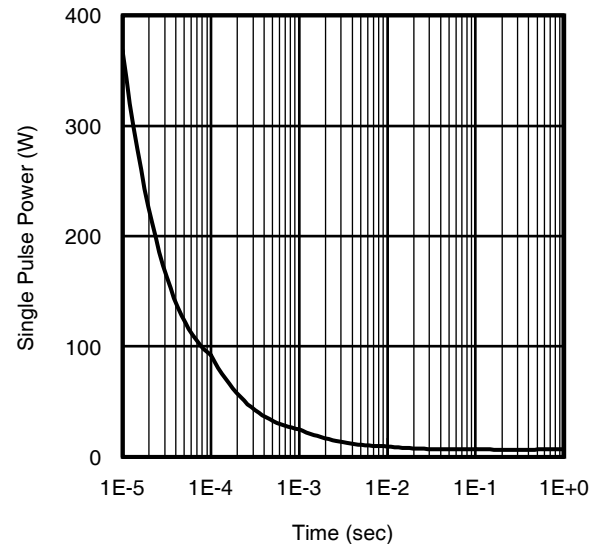
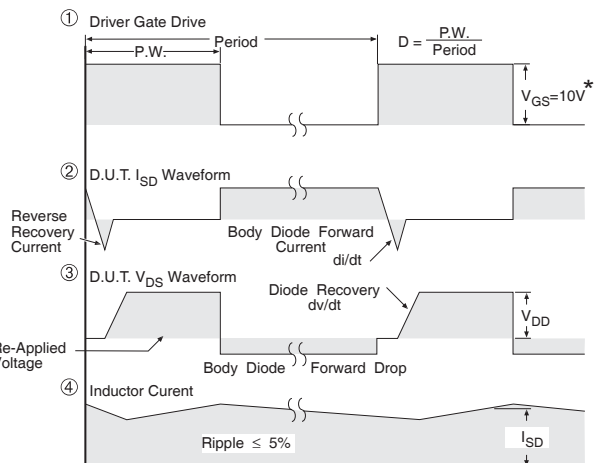
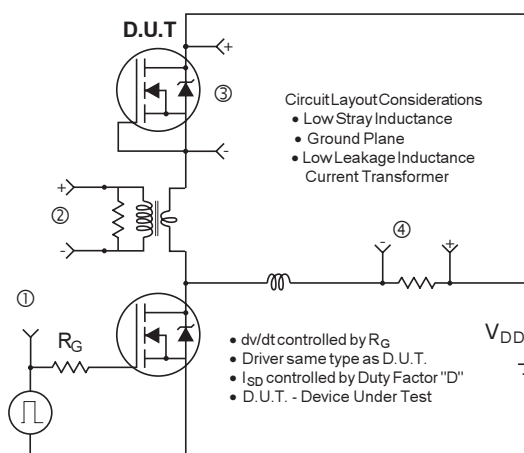
	Parameter	Typ.	Max.	Units
$R_{\theta JC}$ (Bottom)	Junction-to-Case ⑤	—	19	$^\circ\text{C/W}$
$R_{\theta JC}$ (Top)	Junction-to-Case ⑤	—	175	
$R_{\theta JA}$	Junction-to-Ambient ④	—	86	
$R_{\theta JA} (<10s)$	Junction-to-Ambient ④	—	69	

Notes:

- ① Repetitive rating; pulse width limited by max. junction temperature.
- ② Current limited by package.
- ③ Pulse width $\leq 400\mu s$; duty cycle $\leq 2\%$.
- ④ When mounted on 1 inch square copper board.
- ⑤ R_{θ} is measured at T_J of approximately 90°C .
- ⑥ For DESIGN AID ONLY, not subject to production testing.

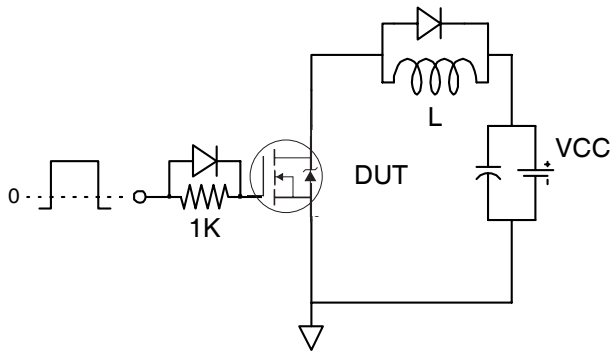
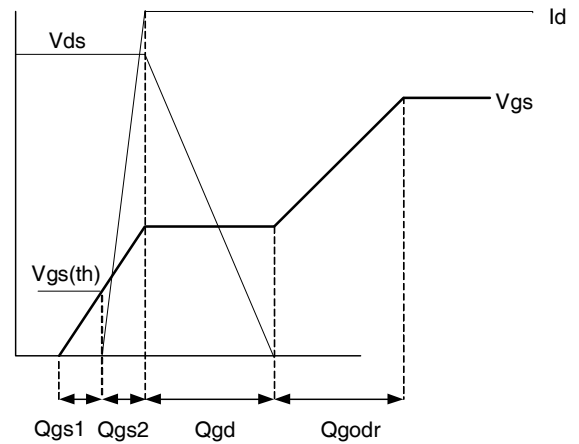
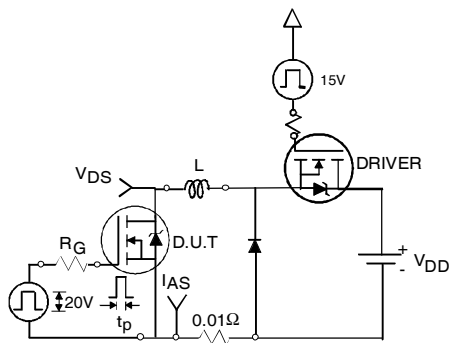
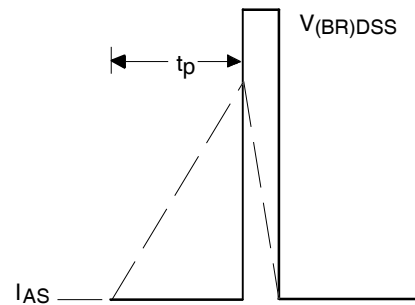
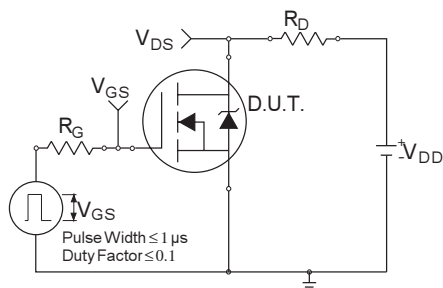
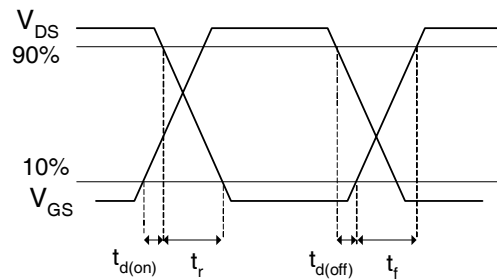

Fig 1. Typical Output Characteristics

Fig 2. Typical Output Characteristics

Fig 3. Typical Transfer Characteristics

Fig 4. Normalized On-Resistance vs. Temperature

Fig 5. Typical Capacitance vs. Drain-to-Source Voltage

Fig 6. Typical Gate Charge vs. Gate-to-Source Voltage


Fig 7. Typical Source-Drain Diode Forward Voltage

Fig 8. Maximum Safe Operating Area

Fig 9. Maximum Drain Current vs. Case (Bottom) Temperature

Fig 10. Threshold Voltage vs. Temperature

Fig 11. Maximum Effective Transient Thermal Impedance, Junction-to-Case (Bottom)

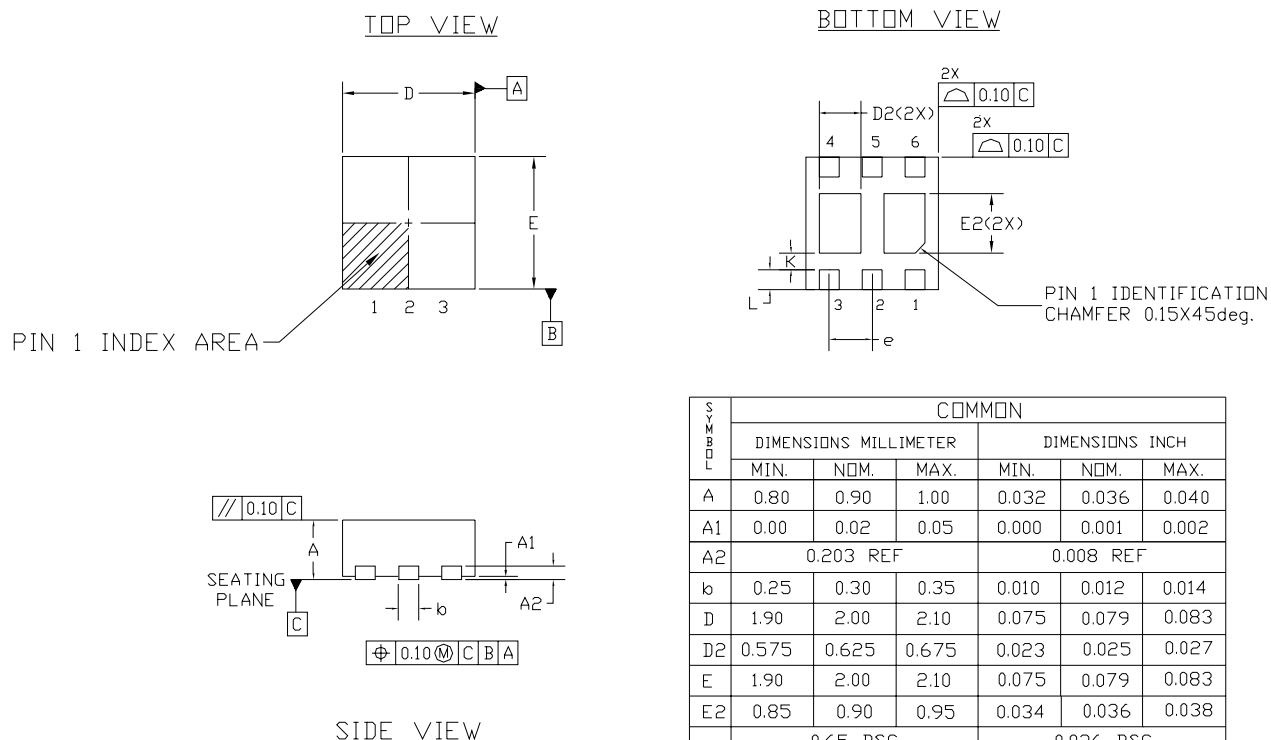

Fig 12. On-Resistance vs. Gate Voltage

Fig 13. Typical On-Resistance vs. Drain Current

Fig 14. Maximum Avalanche Energy vs. Drain Current

Fig 15. Typical Power vs. Time


* $V_{GS} = 5V$ for Logic Level Devices

Fig 16. Peak Diode Recovery dv/dt Test Circuit for N-Channel HEXFET® Power MOSFETs


Fig 17a. Gate Charge Test Circuit

Fig 17b. Gate Charge Waveform

Fig 18a. Unclamped Inductive Test Circuit

Fig 18b. Unclamped Inductive Waveforms

Fig 19a. Switching Time Test Circuit

Fig 19b. Switching Time Waveforms

PQFN Dual 2x2 Outline Package Details



NOTES :

1. DIMENSION AND TOLERANCING CONFORM TO ASME Y14.5M-1994.
2. CONTROLLING DIMENSIONS : MILLIMETER. CONVERTED INCH DIMENSION ARE NOT NECESSARILY EXACT.

For more information on board mounting, including footprint and stencil recommendation, please refer to application note AN-1136:

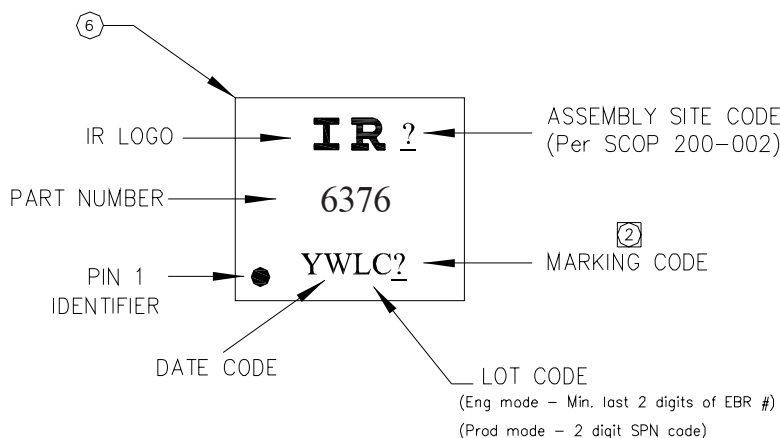
<http://www.irf.com/technical-info/appnotes/an-1136.pdf>

For more information on package inspection techniques, please refer to application note AN-1154:

<http://www.irf.com/technical-info/appnotes/an-1154.pdf>

PQFN Dual 2x2 Outline Part Marking

TOP MARKING (LASER)



Note: For the most current drawing please refer to IR website at: <http://www.irf.com/package/>

PQFN Dual 2x2 Outline Tape and Reel

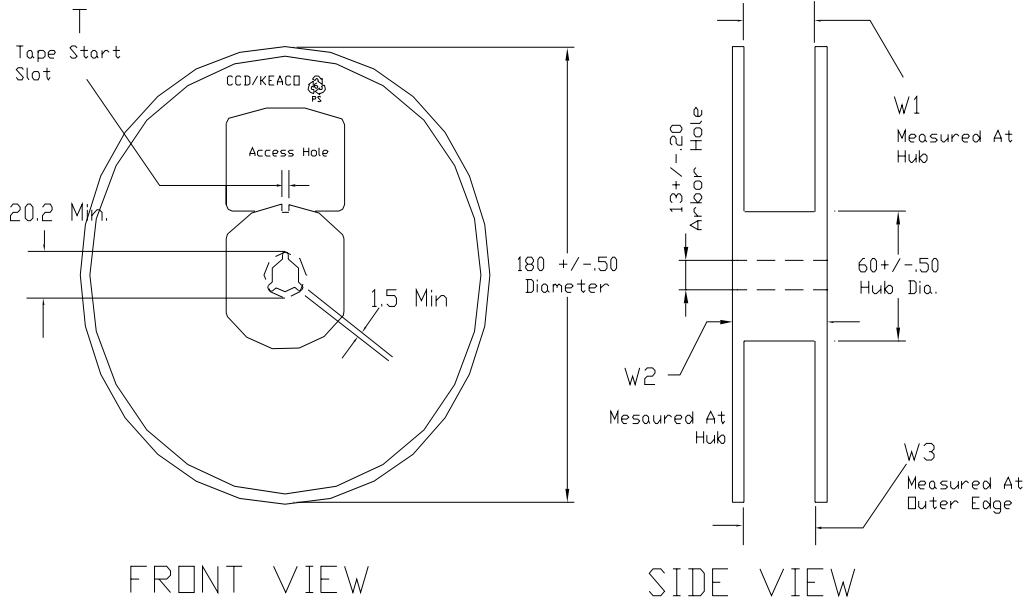
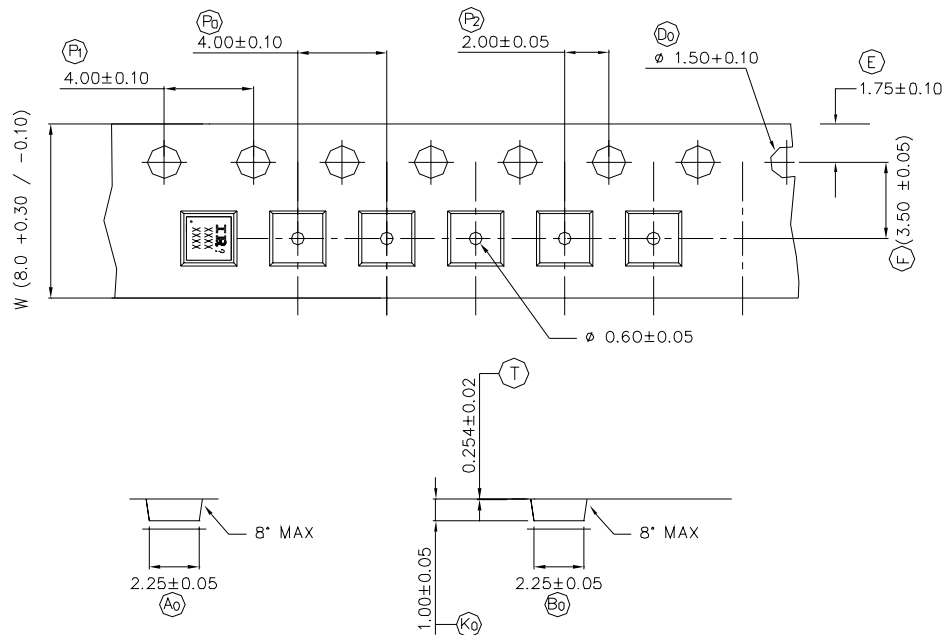


TABLE 1: REEL DETAILS

TAPE WIDTH	T	W1	W2	W3	PART NO
8 MM	3 ± 0.50	8.4 ^{+1.5} _{-0.0}	14.4 Max	7.90 Min 10.9 Max	91586-1
12 MM	5 ± 0.50	12.4 ^{+2.0} _{-0.0}	18.4 Max	11.9 Min 15.4 Max	91586-2

Note: Surface resistivity is $\geq 1 \times 10^5$ but $< 1 \times 10^{12}$ ohm/sq.



NOTE: The Surface Resistivity is $10^4 - 10^8$ OHM/SQ

Qualification information[†]

Qualification level	Industrial (per JEDEC JESD47F ^{††} guidelines)	
Moisture Sensitivity Level	PQFN Dual 2mm x 2mm	MSL1 (per JEDEC J-STD-020D ^{††})
RoHS compliant	Yes	

† Qualification standards can be found at International Rectifier's web site
<http://www.irf.com/product-info/reliability>

†† Applicable version of JEDEC standard at the time of product release.

Revision History

Date	Comment
1/20/2014	- Updated ordering information to reflect the End-Of-Life (EOL) of the mini-reel option (EOL notice #259). - Updated data sheet with the new IR corporate template. - Updated the qual level from Consumer to Industrial, on page 9.

International
 Rectifier

IR WORLD HEADQUARTERS: 101 N. Sepulveda Blvd., El Segundo, California 90245, USA
 To contact International Rectifier, please visit <http://www.irf.com/whoto-call/>