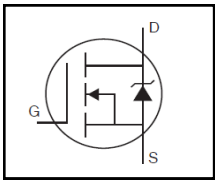
IRLR2705PbF

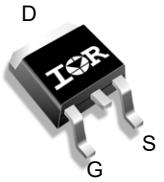
HEXFET® Power MOSFET

Features

- Logic-Level Gate Drive
- Ultra Low On-Resistance
- Advanced Process Technology
- Fast Switching
- Fully Avalanche Rated
- Lead-Free



V_{DSS}	55V
$R_{DS(on)}$	0.040Ω
I_D	28A⑤



D- Pak
IRLR2705PbF

Description

Fifth Generation HEXFETs utilize advanced processing techniques to achieve the lowest possible on-resistance per silicon area. This benefit, combined with the fast switching speed and ruggedized device design that HEXFET Power MOSFETs are well known for, provides the designer with an extremely efficient device for use in a wide variety of applications.

The D-PAK is designed for surface mounting using vapor phase, infrared, or wave soldering techniques. Power dissipation levels up to 1.5 watts are possible in typical surface mount applications.

G	D	S
Gate	Drain	Source

Base part number	Package Type	Standard Pack		Orderable Part Number
		Form	Quantity	
IRLR2705PbF	D-Pak	Tape and Reel	2000	IRLR2705TRPbF

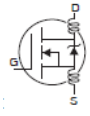
Absolute Maximum Ratings

Symbol	Parameter	Max.	Units
I_D @ T_C = 25°C	Continuous Drain Current, V_{GS} @ 10V	28	A
I_D @ T_C = 100°C	Continuous Drain Current, V_{GS} @ 10V	20	
I_{DM}	Pulsed Drain Current ①	110	
P_D @T_C = 25°C	Maximum Power Dissipation	68	W
	Linear Derating Factor	0.45	W/°C
V_{GS}	Gate-to-Source Voltage	± 16	V
E_{AS}	Single Pulse Avalanche Energy②	110	mJ
I_{AR}	Avalanche Current①	16	A
E_{AR}	Repetitive Avalanche Energy ①	6.8	mJ
dv/dt	Peak Diode Recovery dv/dt ③	5.0	V/ns
T_J T_{STG}	Operating Junction and Storage Temperature Range	-55 to + 175	°C
	Soldering Temperature, for 10 seconds (1.6mm from case)	300	

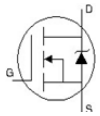
Thermal Resistance

Symbol	Parameter	Typ.	Max.	Units
$R_{\theta JC}$	Junction-to-Case	⸺	2.2	°C/W
$R_{\theta JA}$	Junction-to-Ambient (PCB Mount) ⑥	⸺	50	
$R_{\theta JA}$	Junction-to-Ambient	⸺	110	

Electrical Characteristics @ T_J = 25°C (unless otherwise specified)

	Parameter	Min.	Typ.	Max.	Units	Conditions
$V_{(BR)DSS}$	Drain-to-Source Breakdown Voltage	55	—	—	V	V_{GS} = 0V, I_D = 250µA
$\Delta V_{(BR)DSS}/\Delta T_J$	Breakdown Voltage Temp. Coefficient	—	0.065	—	V/°C	Reference to 25°C, I_D = 1mA
$R_{DS(on)}$	Static Drain-to-Source On-Resistance	—	—	0.040	Ω	V_{GS} = 10V, I_D = 17A ④
		—	—	0.051		V_{GS} = 5.0V, I_D = 17A ④
		—	—	0.065		V_{GS} = 4.0V, I_D = 14A ④
$V_{GS(th)}$	Gate Threshold Voltage	1.0	—	2.0	V	V_{DS} = V_{GS}, I_D = 250µA
gfs	Forward Trans conductance	11	—	—	S	V_{DS} = 25V, I_D = 16A ⑦
I_{DSS}	Drain-to-Source Leakage Current	—	—	25	µA	V_{DS} = 55V, V_{GS} = 0V
		—	—	250		V_{DS} = 44V,V_{GS} = 0V,T_J =150°C
I_{GSS}	Gate-to-Source Forward Leakage	—	—	100	nA	V_{GS} = 16V
	Gate-to-Source Reverse Leakage	—		-100		V_{GS} = -16V
Q_g	Total Gate Charge	—	—	25	nC	I_D = 16A
Q_{gs}	Gate-to-Source Charge	—	—	5.2		V_{DS} = 44V
Q_{gd}	Gate-to-Drain (‘Miller’) Charge	—		14		V_{GS} = 5.0V, See Fig. 6 and 13 ④⑦
$t_{d(on)}$	Turn-On Delay Time	—	8.9	—	ns	V_{DD} = 28V
t_r	Rise Time	—	100	—		I_D = 16A
$t_{d(off)}$	Turn-Off Delay Time	—	21	—		R_G = 6.5Ω,V_{GS} = 5.0V
t_f	Fall Time	—	29	—		R_D = 1.8Ω, See Fig. 10 ④⑦
L_D	Internal Drain Inductance	—	4.5	—	nH	Between lead, 6mm (0.25in.) from package and center of die contact 
L_S	Internal Source Inductance	—	7.5	—		
C_{iss}	Input Capacitance	—	880	—	pF	V_{GS} = 0V
C_{oss}	Output Capacitance	—	220	—		V_{DS} = 25V
C_{rss}	Reverse Transfer Capacitance	—	94	—		f = 1.0MHz, See Fig. 5⑦

Source-Drain Ratings and Characteristics

	Parameter	Min.	Typ.	Max.	Units	Conditions
I_S	Continuous Source Current (Body Diode)	—	—	28	A	MOSFET symbol showing the integral reverse p-n junction diode. 
I_{SM}	Pulsed Source Current (Body Diode) ①	—	—	110		
V_{SD}	Diode Forward Voltage	—	—	1.3	V	T_J = 25°C,I_S = 17A,V_{GS} = 0V ④
t_{rr}	Reverse Recovery Time	—	76	110	ns	T_J = 25°C ,I_F = 16A
Q_{rr}	Reverse Recovery Charge	—	190	290	nC	di/dt = 100A/µs ④⑦
t_{on}	Forward Turn-On Time	Intrinsic turn-on time is negligible (turn-on is dominated by L_S+L_D)				

Notes:

① Repetitive rating; pulse width limited by max. junction temperature. (See fig. 11).

② V_{DD} = 25V, starting T_J = 25°C, L = 610µH, R_G = 25Ω, I_{AS} = 16A. (See fig. 12)

③ $I_{SD} \leq$ 16A, dv/dt ≤ 270A/µs, $V_{DD} \leq V_{(BR)DSS}$, $T_j \leq$ 175°C

④ Pulse width ≤ 300µs; duty cycle ≤ 2%.

⑤ Calculated continuous current based on maximum allowable junction temperature; Package limitation current = 20A.

⑥ When mounted on 1" square PCB (FR-4 or G-10 Material). For recommended footprint and soldering techniques refer to application note #AN-994.

⑦ Uses IRLZ34N data and test conditions.

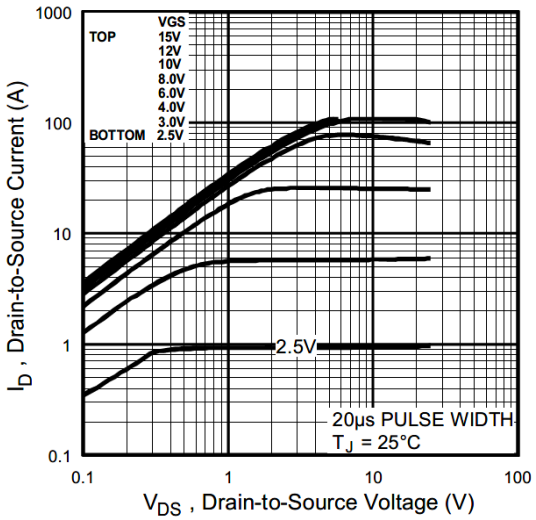


Fig. 1 Typical Output Characteristics

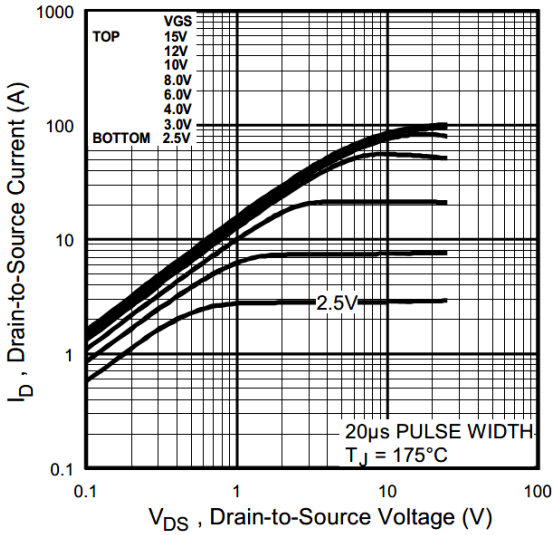


Fig. 2 Typical Output Characteristics

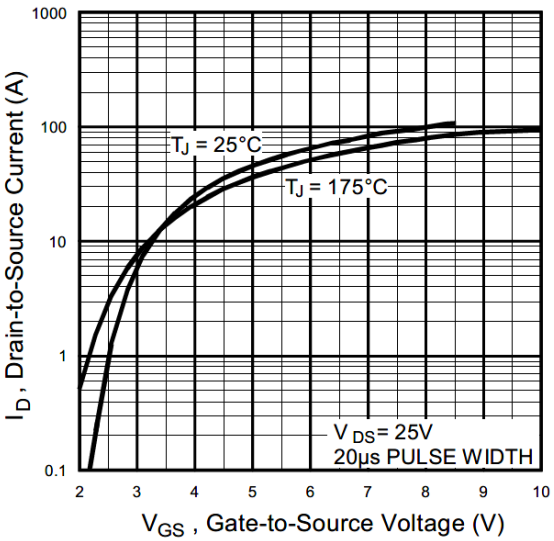


Fig. 3 Typical Transfer Characteristics

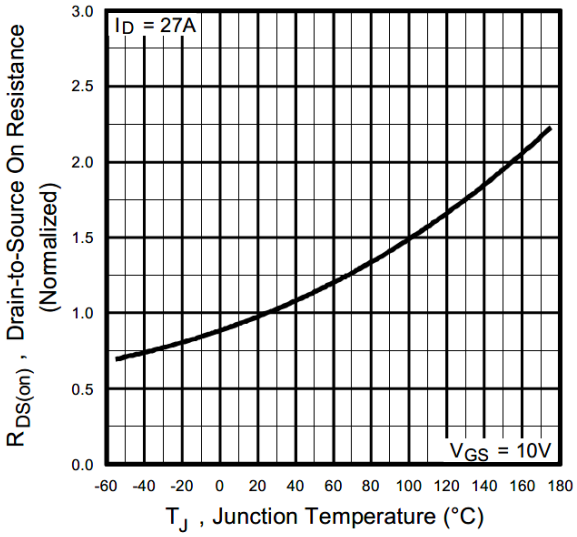


Fig. 4 Normalized On-Resistance vs. Temperature

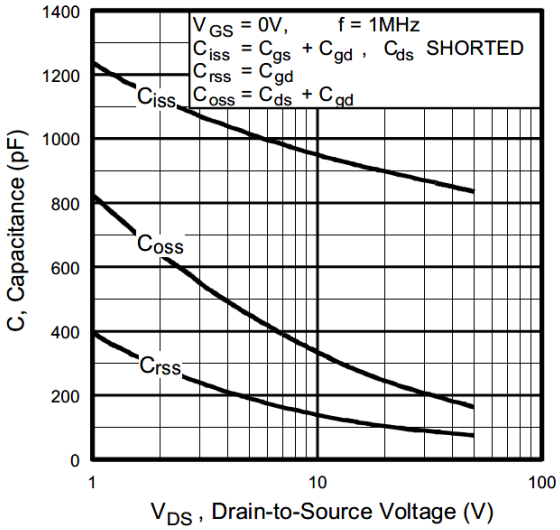


Fig 5. Typical Capacitance vs. Drain-to-Source Voltage

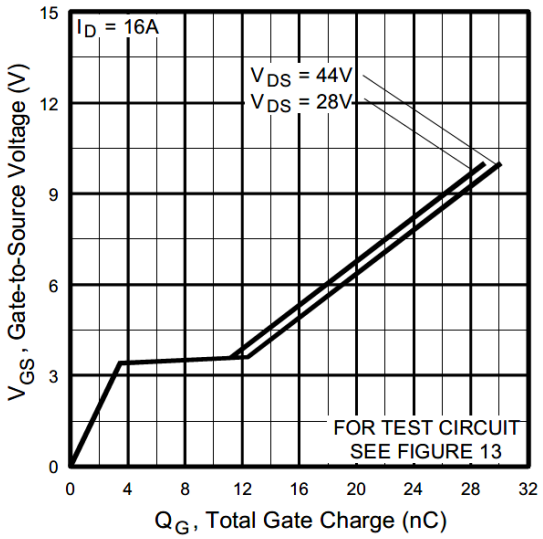


Fig 6. Typical Gate Charge vs. Gate-to-Source Voltage

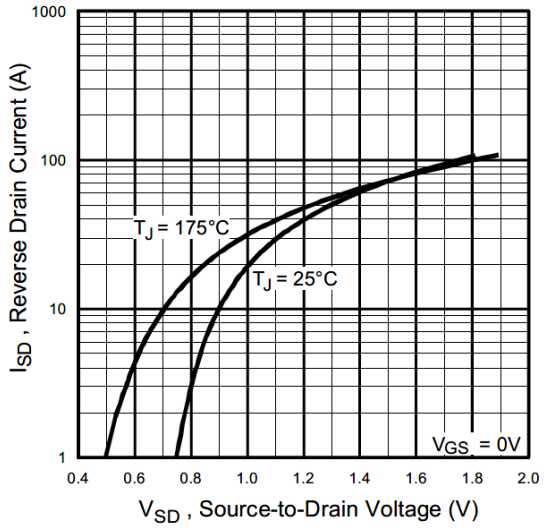


Fig. 7 Typical Source-to-Drain Diode Forward Voltage

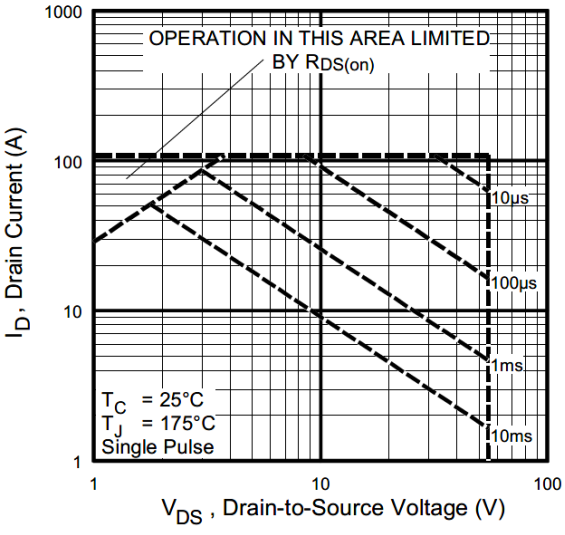


Fig 8. Maximum Safe Operating Area

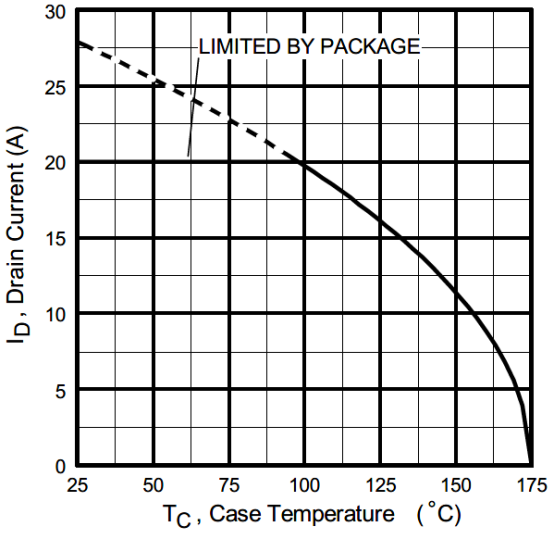


Fig 9. Maximum Drain Current vs. Case Temperature

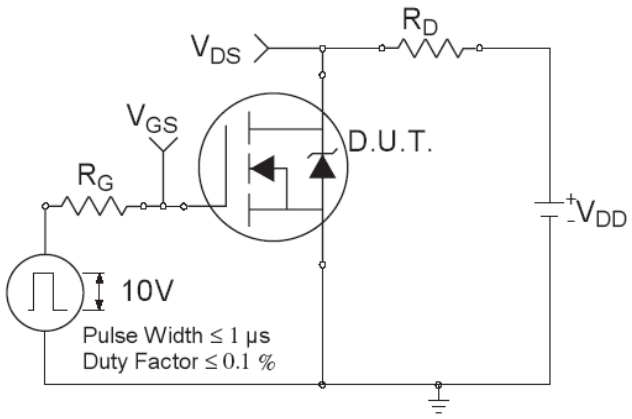


Fig 10a. Switching Time Test Circuit

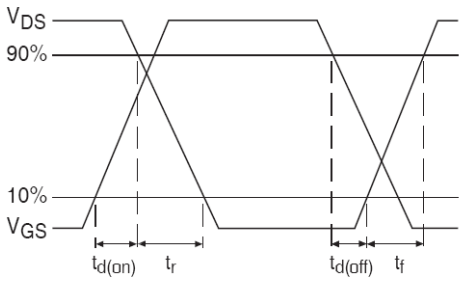


Fig 10b. Switching Time Waveforms

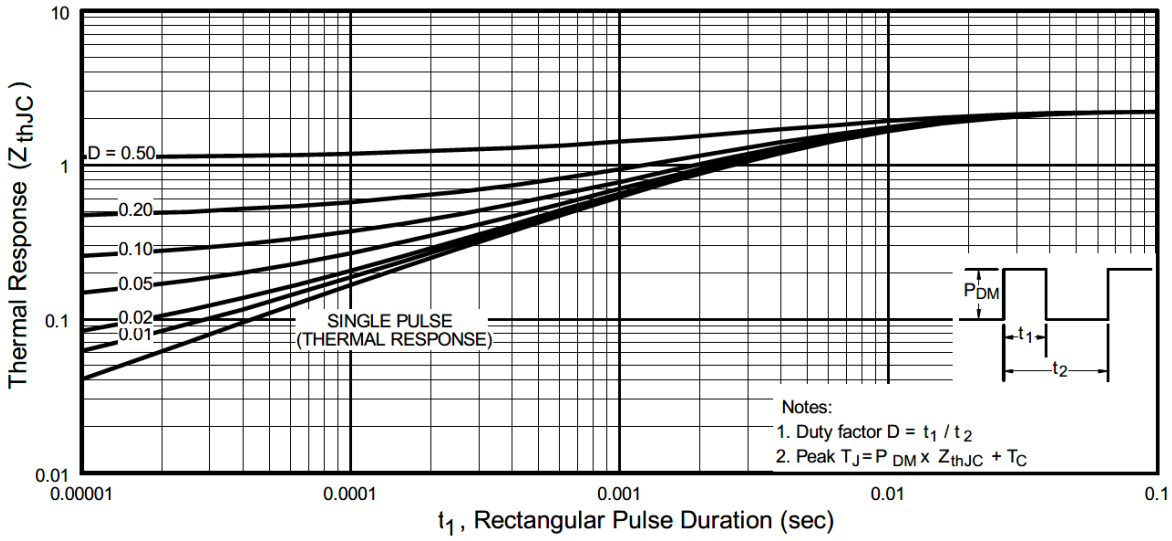


Fig 11. Maximum Effective Transient Thermal Impedance, Junction-to-Case

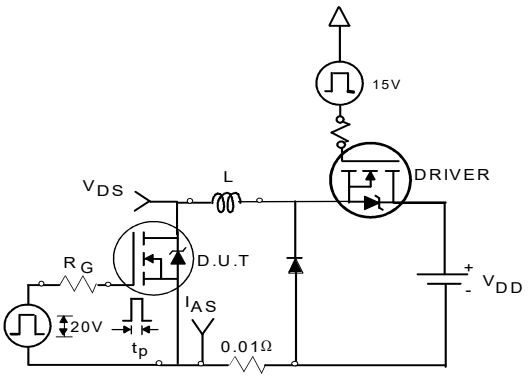


Fig 12a. Unclamped Inductive Test Circuit

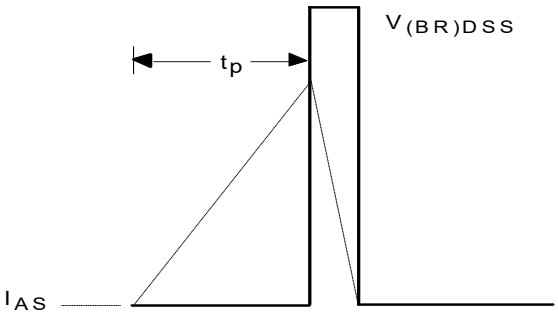


Fig 12b. Unclamped Inductive Waveforms

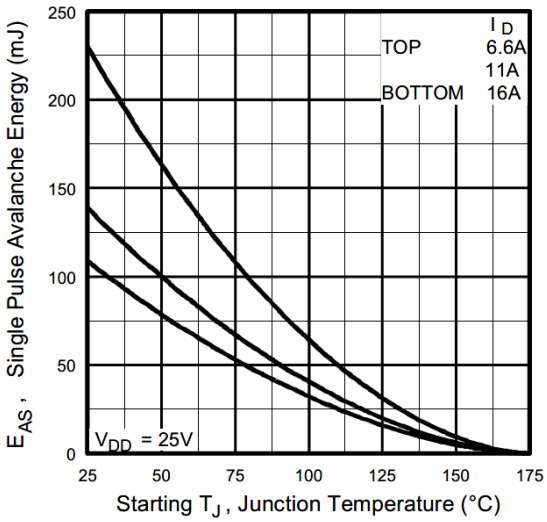


Fig 12c. Maximum Avalanche Energy vs. Drain Current

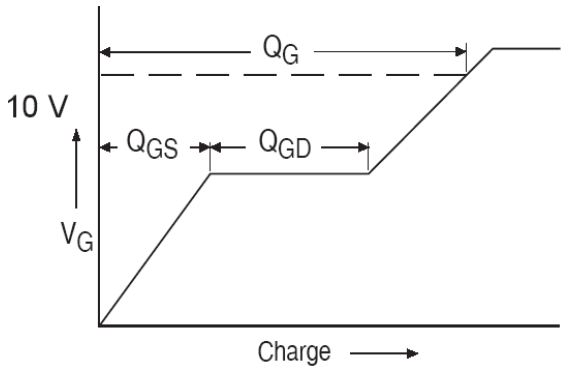


Fig 13a. Gate Charge Waveform

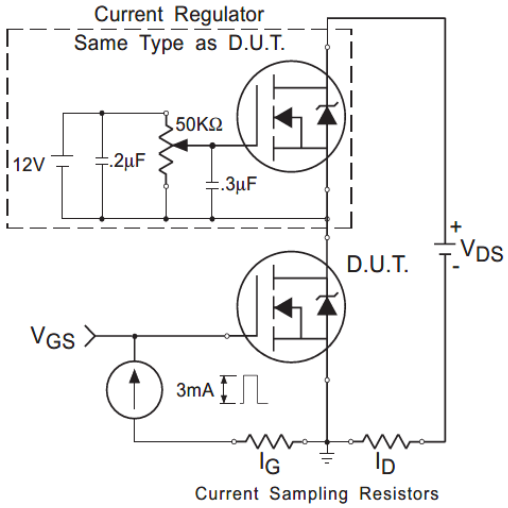


Fig 13b. Gate Charge Test Circuit

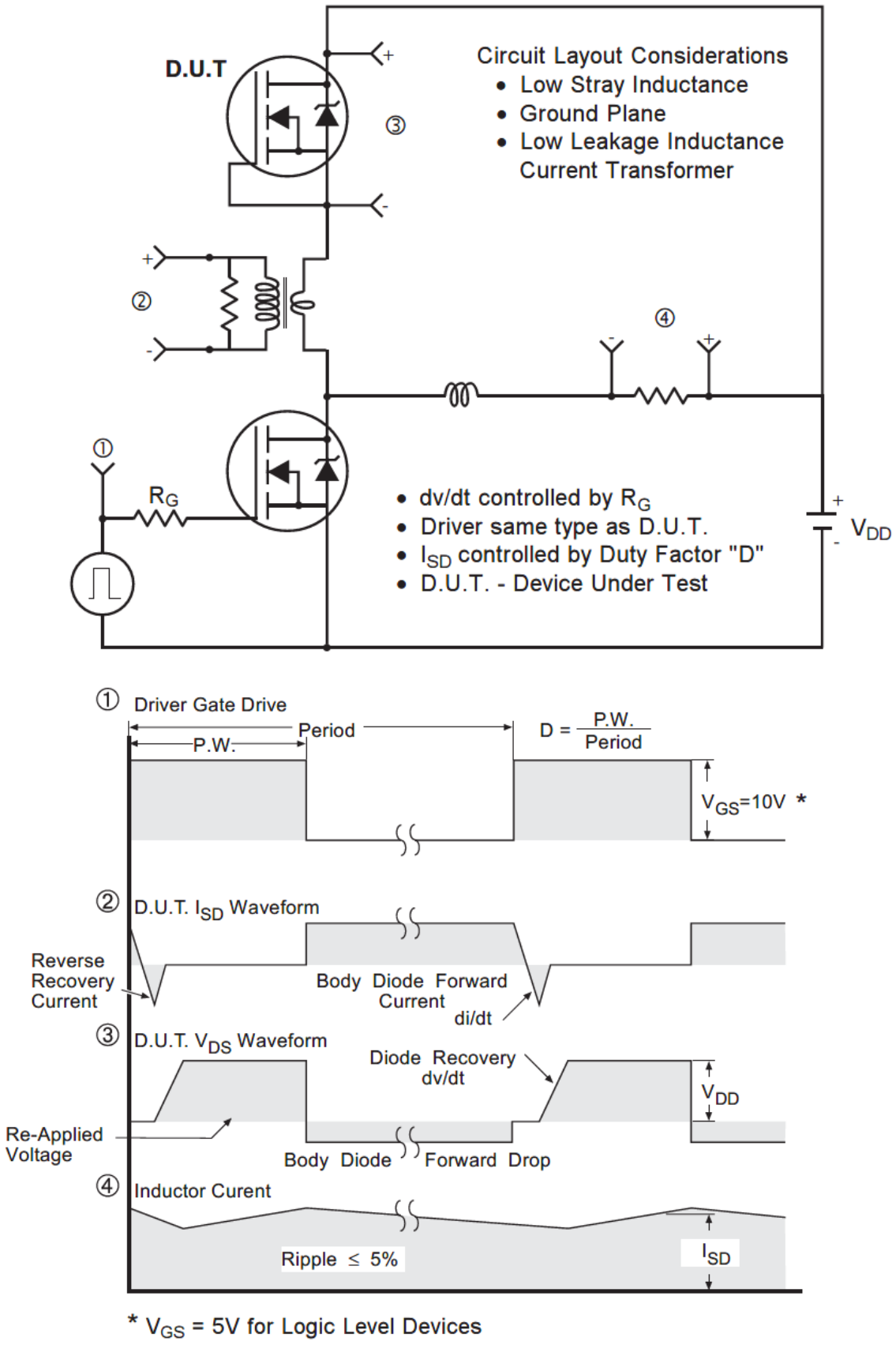
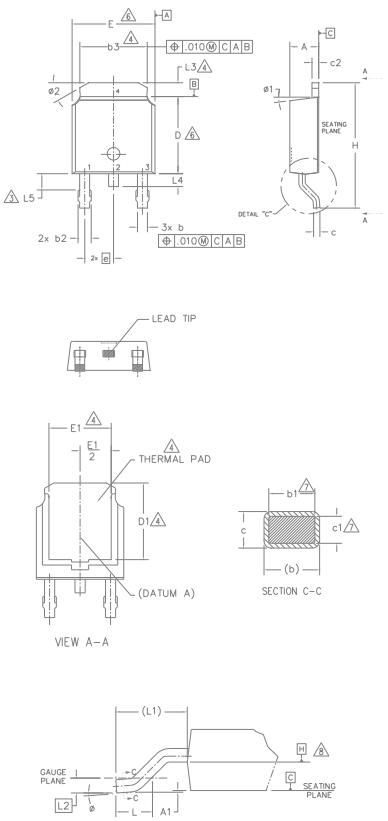


Fig 14. Peak Diode Recovery dv/dt Test Circuit for N-Channel HEXFET® Power MOSFETs

D-Pak (TO-252AA) Package Outline (Dimensions are shown in millimeters (inches))



NOTES:
1.– DIMENSIONING AND TOLERANCING PER ASME Y14.5M–1994
2.– DIMENSION ARE SHOWN IN INCHES [MILLIMETERS].
3.– LEAD DIMENSION UNCONTROLLED IN L5.
4.– DIMENSION D1, E1, L3 & b3 ESTABLISH A MINIMUM MOUNTING SURFACE FOR THERMAL PAD.
5.– SECTION C–C DIMENSIONS APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN .005 AND 0.10 [0.13 AND 0.25] FROM THE LEAD TIP.
6.– DIMENSION D & E DO NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED .006 [0.15] PER SIDE. THESE DIMENSIONS ARE MEASURED AT THE OUTMOST EXTREMES OF THE PLASTIC BODY.
7.– DIMENSION b1 & c1 APPLIED TO BASE METAL ONLY.
8.– DATUM A & B TO BE DETERMINED AT DATUM PLANE H.
9.– OUTLINE CONFORMS TO JEDEC OUTLINE TO–252AA.

SYMBOL	DIMENSIONS				NOTES
	MILLIMETERS		INCHES		
	MIN.	MAX.	MIN.	MAX.	
A	2.18	2.39	.086	.094	
A1	–	0.13	–	.005	
b	0.64	0.89	.025	.035	
b1	0.64	0.79	.025	.031	7
b2	0.76	1.14	.030	.045	
b3	4.95	5.46	.195	.215	4
c	0.46	0.61	.018	.024	
c1	0.41	0.56	.016	.022	7
c2	0.46	0.89	.018	.035	
D	5.97	6.22	.235	.245	6
D1	5.21	–	.205	–	4
E	6.35	6.73	.250	.265	6
E1	4.32	–	.170	–	4
e	2.29 BSC		.090 BSC		
H	9.40	10.41	.370	.410	
L	1.40	1.78	.055	.070	
L1	2.74 BSC		.108 REF.		
L2	0.51 BSC		.020 BSC		
L3	0.89	1.27	.035	.050	4
L4	–	1.02	–	.040	
L5	1.14	1.52	.045	.060	3
ø	0°	10°	0°	10°	
ø1	0°	15°	0°	15°	
ø2	25°	35°	25°	35°	

LEAD ASSIGNMENTS

HEXFET
1.– GATE
2.– DRAIN
3.– SOURCE
4.– DRAIN

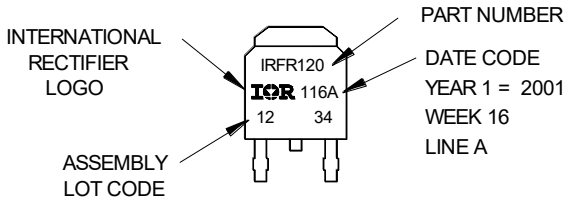
IGBT & CoPAK
1.– GATE
2.– COLLECTOR
3.– EMITTER
4.– COLLECTOR

D-Pak (TO-252AA) Part Marking Information

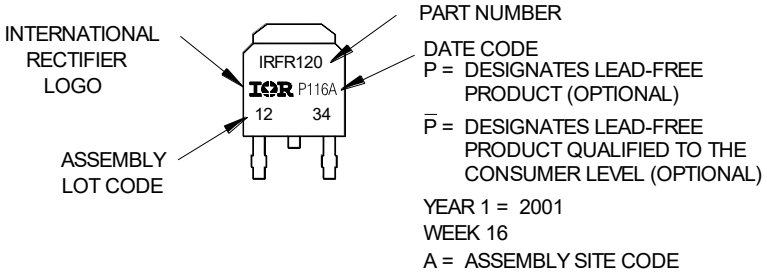
EXAMPLE: THIS IS AN IRFR120
WITH ASSEMBLY
LOT CODE 1234
ASSEMBLED ON WW 16, 2001
IN THE ASSEMBLY LINE "A"

Note: "P" in assembly line position indicates "Lead-Free"

"P̄" in assembly line position indicates "Lead-Free" qualification to the consumer-level

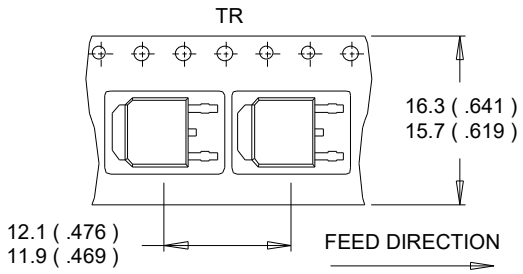


OR

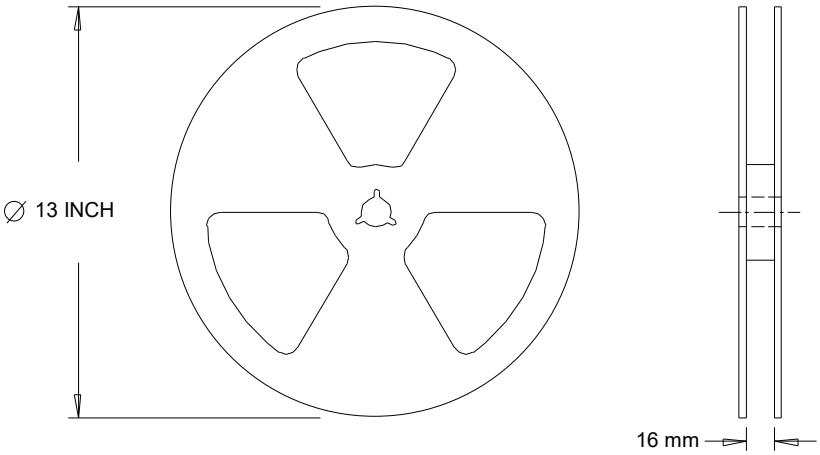


Notes:
1. For the most current drawing please refer to Infineon website at http://www.infineon.com/package/

D-Pak (TO-252AA) Tape & Reel Information Dimensions are shown in millimeters (inches)



NOTES :
1. CONTROLLING DIMENSION : MILLIMETER.
2. ALL DIMENSIONS ARE SHOWN IN MILLIMETERS (INCHES).
3. OUTLINE CONFORMS TO EIA-481 & EIA-541.



NOTES :
1. OUTLINE CONFORMS TO EIA-481.

Note: For the most current drawing please refer to Infineon's web site www.infineon.com

Revision History

Date	Rev.	Comments
01/09/2025	2.1	• Changed datasheet with corporate template. • Removed I-Pack “(IRLU2705PbF)-All pages • Updated typo Rdson unit from “W” to “Ω”-page 2 • Updated disclaimer on last page.

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