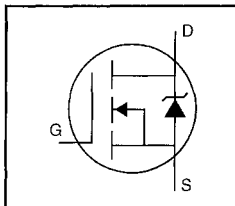


## HEXFET® Power MOSFET

- Surface Mount
- Available in Tape & Reel
- Dynamic  $dv/dt$  Rating
- Logic-Level Gate Drive
- $R_{DS(on)}$  Specified at  $V_{GS}=4V$  &  $5V$
- $175^{\circ}C$  Operating Temperature
- Fast Switching



$$V_{DSS} = 60V$$

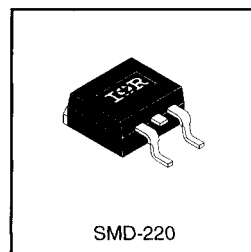
$$R_{DS(on)} = 0.10\Omega$$

$$I_D = 17A$$

### Description

Third Generation HEXFETs from International Rectifier provide the designer with the best combination of fast switching, ruggedized device design, low on-resistance and cost-effectiveness.

The SMD-220 is a surface mount power package capable of accommodating die sizes up to HEX-4. It provides the highest power capability and the lowest possible on-resistance in any existing surface mount package. The SMD-220 is suitable for high current applications because of its low internal connection resistance and can dissipate up to 2.0W in a typical surface mount application.



SMD-220

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### Absolute Maximum Ratings

	Parameter	Max.	Units
$I_D$ @ $T_C = 25^{\circ}C$	Continuous Drain Current, $V_{GS}$ @ 5.0 V	17	A
$I_D$ @ $T_C = 100^{\circ}C$	Continuous Drain Current, $V_{GS}$ @ 5.0 V	12	
$I_{DM}$	Pulsed Drain Current ①	68	W
$P_D$ @ $T_C = 25^{\circ}C$	Power Dissipation	60	
$P_D$ @ $T_A = 25^{\circ}C$	Power Dissipation (PCB Mount)**	3.7	$W/^{\circ}C$
	Linear Derating Factor	0.40	
	Linear Derating Factor (PCB Mount)**	0.025	
$V_{GS}$	Gate-to-Source Voltage	$\pm 10$	V
$E_{AS}$	Single Pulse Avalanche Energy ②	110	mJ
$dv/dt$	Peak Diode Recovery $dv/dt$ ③	4.5	V/ns
$T_J, T_{STG}$	Junction and Storage Temperature Range	-55 to +175	$^{\circ}C$
	Soldering Temperature, for 10 seconds	300 (1.6mm from case)	

### Thermal Resistance

	Parameter	Min.	Typ.	Max.	Units
$R_{\theta JC}$	Junction-to-Case	—	—	2.5	$^{\circ}C/W$
$R_{\theta JA}$	Junction-to-Ambient (PCB mount)**	—	—	40	
$R_{\theta JA}$	Junction-to-Ambient	—	—	62	

\*\* When mounted on 1" square PCB (FR-4 or G-10 Material).

For recommended footprint and soldering techniques refer to application note #AN-994.

**Electrical Characteristics @  $T_J = 25^\circ\text{C}$  (unless otherwise specified)**

	Parameter	Min.	Typ.	Max.	Units	Test Conditions
$V_{(BR)DSS}$	Drain-to-Source Breakdown Voltage	60	—	—	V	$V_{GS}=0V, I_D=250\mu A$
$\Delta V_{(BR)DSS}/\Delta T_J$	Breakdown Voltage Temp. Coefficient	—	0.060	—	$V/^\circ C$	Reference to $25^\circ C, I_D=1mA$
$R_{DS(on)}$	Static Drain-to-Source On-Resistance	—	—	0.10	$\Omega$	$V_{GS}=5.0V, I_D=10A$ ④
		—	—	0.14		$V_{GS}=4.0V, I_D=8.5A$ ④
$V_{GS(th)}$	Gate Threshold Voltage	1.0	—	2.0	V	$V_{DS}=V_{GS}, I_D=250\mu A$
$g_{fs}$	Forward Transconductance	7.3	—	—	S	$V_{DS}=25V, I_D=10A$ ④
$I_{DSS}$	Drain-to-Source Leakage Current	—	—	25	$\mu A$	$V_{DS}=60V, V_{GS}=0V$
		—	—	250		$V_{DS}=48V, V_{GS}=0V, T_J=150^\circ C$
$I_{GSS}$	Gate-to-Source Forward Leakage	—	—	100	nA	$V_{GS}=10V$
	Gate-to-Source Reverse Leakage	—	—	-100		$V_{GS}=-10V$
$Q_g$	Total Gate Charge	—	—	18	nC	$I_D=17A$
$Q_{gs}$	Gate-to-Source Charge	—	—	4.5		$V_{DS}=48V$
$Q_{gd}$	Gate-to-Drain ("Miller") Charge	—	—	12		$V_{GS}=5.0V$ See Fig. 6 and 13 ④
$t_{d(on)}$	Turn-On Delay Time	—	11	—	ns	$V_{DD}=30V$
$t_r$	Rise Time	—	110	—		$I_D=17A$
$t_{d(off)}$	Turn-Off Delay Time	—	23	—		$R_G=9.0\Omega$
$t_f$	Fall Time	—	41	—		$R_D=1.7\Omega$ See Figure 10 ④
$L_D$	Internal Drain Inductance	—	4.5	—	nH	Between lead, 6 mm (0.25in.) from package and center of die contact
$L_S$	Internal Source Inductance	—	7.5	—		
$C_{iss}$	Input Capacitance	—	870	—	pF	$V_{GS}=0V$
$C_{oss}$	Output Capacitance	—	360	—		$V_{DS}=25V$
$C_{rss}$	Reverse Transfer Capacitance	—	53	—		$f=1.0MHz$ See Figure 5


**Source-Drain Ratings and Characteristics**

	Parameter	Min.	Typ.	Max.	Units	Test Conditions
$I_S$	Continuous Source Current (Body Diode)	—	—	17	A	MOSFET symbol showing the integral reverse p-n junction diode.
$I_{SM}$	Pulsed Source Current (Body Diode) ①	—	—	68		
$V_{SD}$	Diode Forward Voltage	—	—	1.5	V	$T_J=25^\circ C, I_S=17A, V_{GS}=0V$ ④
$t_{rr}$	Reverse Recovery Time	—	110	260	ns	$T_J=25^\circ C, I_F=17A$
$Q_{rr}$	Reverse Recovery Charge	—	0.49	1.5	$\mu C$	$di/dt=100A/\mu s$ ④
$t_{on}$	Forward Turn-On Time	Intrinsic turn-on time is negligible (turn-on is dominated by $L_S+L_D$ )				

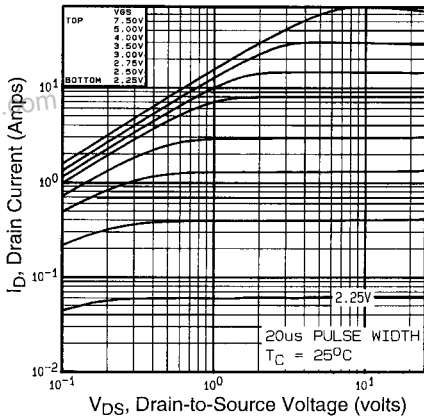
**Notes:**

① Repetitive rating; pulse width limited by max. junction temperature (See Figure 11)

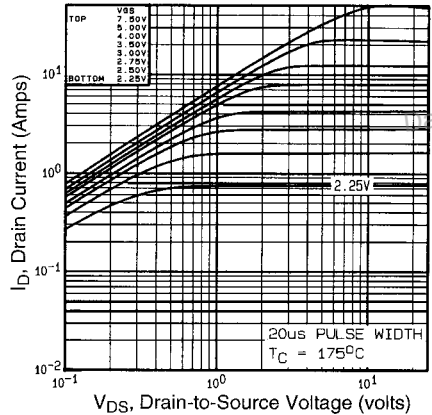
③  $I_{SD} \leq 17A, di/dt \leq 140A/\mu s, V_{DD} \leq V_{(BR)DSS}, T_J \leq 175^\circ C$

②  $V_{DD}=25V, starting T_J=25^\circ C, L=444\mu H, R_G=25\Omega, I_{AS}=17A$  (See Figure 12)

④ Pulse width  $\leq 300 \mu s$ ; duty cycle  $\leq 2\%$

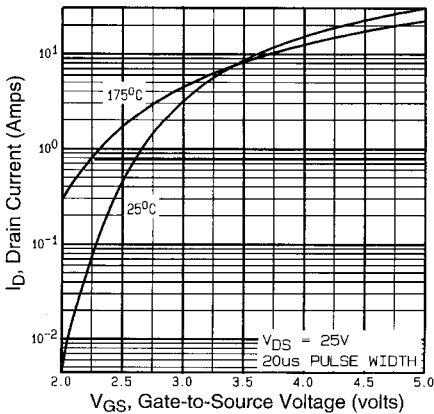


**Fig 1.** Typical Output Characteristics,  
 $T_C=25^\circ\text{C}$

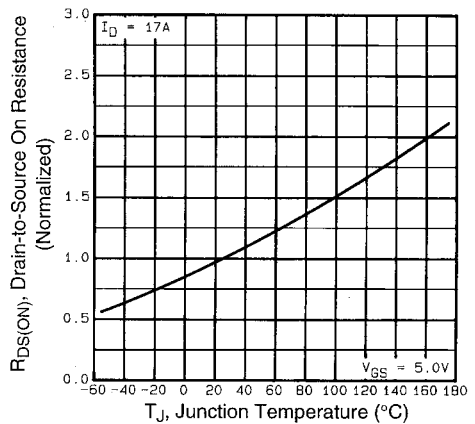


**Fig 2.** Typical Output Characteristics,  
 $T_C=175^\circ\text{C}$

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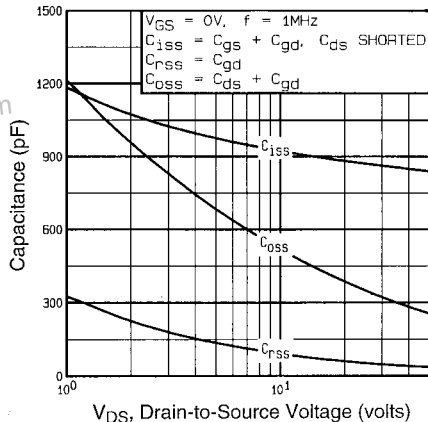


**Fig 3.** Typical Transfer Characteristics

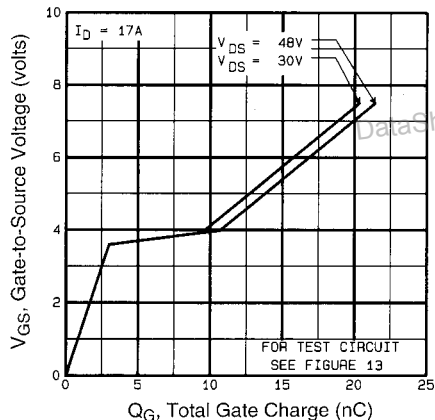


**Fig 4.** Normalized On-Resistance  
Vs. Temperature

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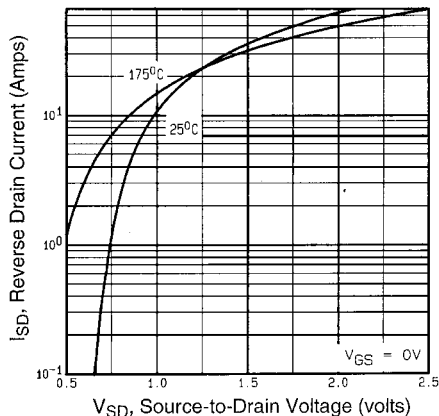


**Fig 5.** Typical Capacitance Vs. Drain-to-Source Voltage

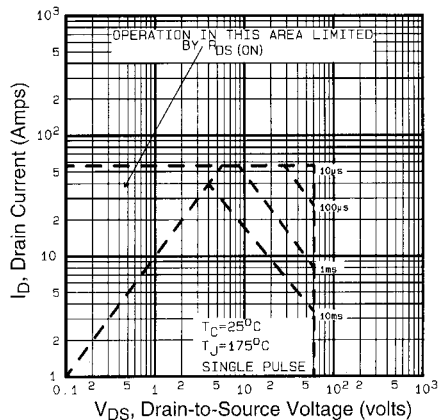


**Fig 6.** Typical Gate Charge Vs. Gate-to-Source Voltage

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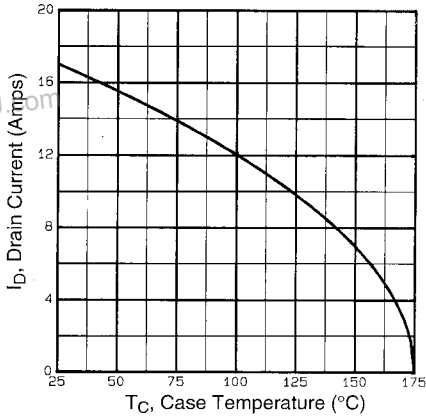


**Fig 7.** Typical Source-Drain Diode Forward Voltage

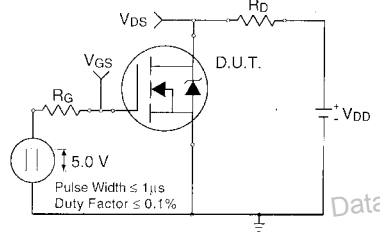


**Fig 8.** Maximum Safe Operating Area

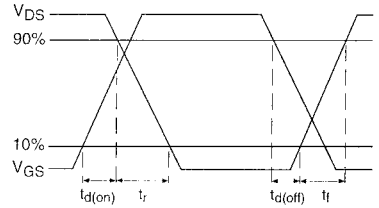
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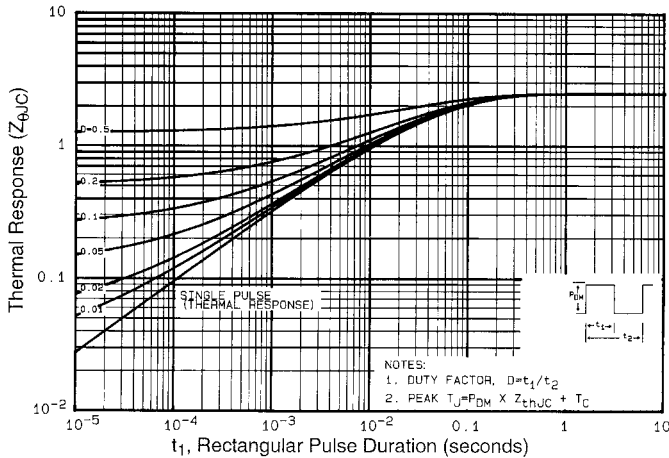
**Fig 9.** Maximum Drain Current Vs. Case Temperature



**Fig 10a.** Switching Time Test Circuit



**Fig 10b.** Switching Time Waveforms



**Fig 11.** Maximum Effective Transient Thermal Impedance, Junction-to-Case

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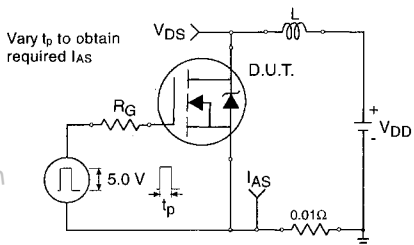


Fig 12a. Unclamped Inductive Test Circuit

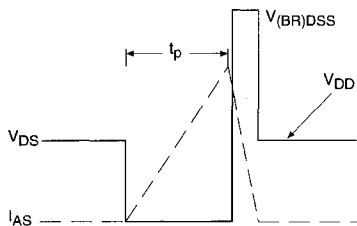


Fig 12b. Unclamped Inductive Waveforms

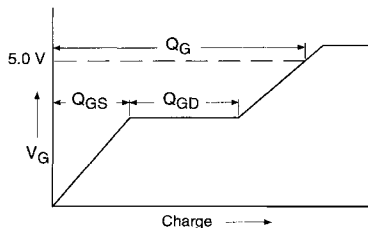


Fig 13a. Basic Gate Charge Waveform

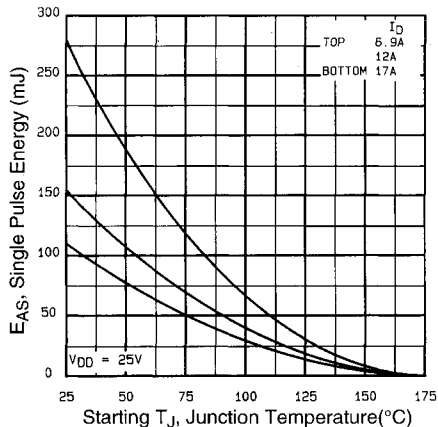


Fig 12c. Maximum Avalanche Energy Vs. Drain Current

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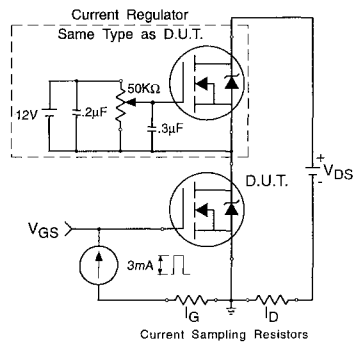


Fig 13b. Gate Charge Test Circuit

**Appendix A:** Figure 14, Peak Diode Recovery  $dv/dt$  Test Circuit – See page 1505

**Appendix B:** Package Outline Mechanical Drawing – See page 1507

**Appendix C:** Part Marking Information – See page 1515

**Appendix D:** Tape & Reel Information – See page 1519

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