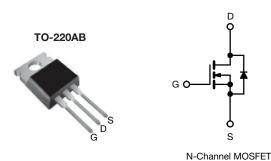


Power MOSFET



PRODUCT SUMMARY				
V _{DS} (V)	60			
$R_{DS(on)}(\Omega)$	V _{GS} = 5.0 V	0.028		
Q _g (Max.) (nC)	66			
Q _{gs} (nC)	12			
Q _{gd} (nC)	43			
Configuration	Single			

FEATURES

- Dynamic dV/dt rating
- · Logic-level gate drive
- R_{DS(on)} specified at V_{GS} = 4 V and 5 V
- 175 °C operating temperature
- · Fast switching
- · Ease of paralleling
- Simple drive requirements
- Material categorization: for definitions of compliance please see <u>www.vishav.com/doc?99912</u>

Note

* This datasheet provides information about parts that are RoHS-compliant and / or parts that are non RoHS-compliant. For example, parts with lead (Pb) terminations are not RoHS-compliant. Please see the information / tables in this datasheet for details

DESCRIPTION

Third generation power MOSFETs from Vishay provide the designer with the best combination of fast switching, ruggedized device design, low on-resistance and cost-effectiveness.

The TO-220AB package is universally preferred for all commercial-industrial applications at power dissipation levels to approximately 50 W. The low thermal resistance and low package cost of the TO-220AB contribute to its wide acceptance throughout the industry.

ORDERING INFORMATION	
Package	TO-220AB
Lead (Pb)-free	IRLZ44PbF
Lead (Pb)-free and halogen-free	IRLZ44PbF-BE3

ABSOLUTE MAXIMUM RATINGS (TC)	= 25 °C, un	less otherwis	se noted)				
PARAMETER			SYMBOL	LIMIT	UNIT		
Drain-source voltage			V _{DS}	60	- V		
Gate-source voltage			V_{GS}	± 10			
Continuous drain current	\/ -+ \(\)	$T_C = 25 ^{\circ}C$ $T_C = 100 ^{\circ}C$		50			
	V _{GS} at 5 V	T _C = 100 °C	ID	36	А		
Pulsed drain current ^a			I _{DM}	200			
Linear derating factor			1.0	W/°C			
Single pulse avalanche energy b			E _{AS}	400	mJ		
Maximum power dissipation	T _C = 25 °C		T _C = 25 °C		P _D	150	W
Peak diode recovery dV/dt ^c			dV/dt	4.5	V/ns		
Operating junction and storage temperature range		T _J , T _{stg}	-55 to +175	175			
Soldering recommendations (peak temperature) ^d	For 10 s			300	°C		
Mounting torque	6-32 or M3 screw			10	lbf ⋅ in		
				1.1	N⋅m		

Notes

- a. Repetitive rating; pulse width limited by maximum junction temperature (see fig. 11)
- b. V_{DD} = 25 V, starting T_J = 25 °C, L = 179 μ H, R_g = 25 Ω , I_{AS} = 51 A (see fig. 12)
- c. $I_{SD} \le 51$ A, $dV/dt \le 250$ A/s, $V_{DD} \le V_{DS}$, $T_{J} \le 175$ °C
- d. 1.6 mm from case
- e. Current limited by the package, (die current = 51 A)



Vishay Siliconix

THERMAL RESISTANCE RATINGS				
PARAMETER	SYMBOL	TYP.	MAX.	UNIT
Maximum junction-to-ambient	R _{thJA}	-	62	
Case-to-sink, flat, greased surface	R _{thCS}	0.50	-	°C/W
Maximum junction-to-case (drain)	R _{thJC}	-	1.0	

SPECIFICATIONS ($T_J = 25 ^{\circ}C$, t	ınless otherw	ise noted)					
PARAMETER	SYMBOL	TEST	MIN.	TYP.	MAX.	UNIT	
Static							
Drain-source breakdown voltage	V_{DS}	$V_{GS} = 0$	60	-	-	V	
V _{DS} temperature coefficient	$\Delta V_{DS}/T_{J}$	Reference	to 25 °C, I _D = 1 mA	-	0.070	-	V/°C
Gate-source threshold voltage	V _{GS(th)}	$V_{DS} = V$	_{GS} , I _D = 250 μA	1.0	-	2.0	V
Gate-source leakage	I _{GSS}	V	V _{GS} = 10 V		-	± 100	nA
Zero gate voltage drain current	$V_{DS} = 60 \text{ V}, V_{GS} = 0 \text{ V}$		$80 \text{ V}, \text{ V}_{GS} = 0 \text{ V}$	-	-	25	μΑ
Zero gate voltage drain current	I _{DSS}	V _{DS} = 48 V, V	V _{DS} = 48 V, V _{GS} = 0 V, T _J = 150 °C		-	250	
Drain-source on-state resistance	D	V _{GS} = 5.0 V	I _D = 31 A ^b	-	-	0.028	Ω
	R _{DS(on)}	$V_{GS} = 4.0 \text{ V}$	I _D = 25 A ^b	-	-	0.039	
Forward transconductance	9 _{fs}	V _{DS} = 2	5 V, I _D = 31 A ^b	23	-	-	S
Dynamic							
Input capacitance	C _{iss}	V	$V_{GS} = 0 V$,			-	
Output capacitance	C _{oss}	V _I	$V_{GS} = 0 \text{ V},$ $V_{DS} = 25 \text{ V},$ f = 1.0 MHz, see fig. 5		1200	-	pF
Reverse transfer capacitance	C _{rss}	f = 1.0			200	-	
Total gate charge	Qg			-	-	66	
Gate-source charge	Q _{gs}	$V_{GS} = 5.0 \text{ V}$	$V_{GS} = 5.0 \text{ V}$ $I_D = 51 \text{ A}, V_{DS} = 48 \text{ V},$ see fig. 6 and 13 b		-	12	nC
Gate-drain charge	Q _{gd}		g. o and ro	-	-	43	1
Turn-on delay time	t _{d(on)}		V _{DD} = 30 V, I _D = 51 A,		17	-	- ns
Rise time	t _r	$V_{DD} = 3$			230	-	
Turn-off delay time	t _{d(off)}	$R_g = 4.6 \Omega$, $R_D = 0.56 \Omega$, see fig. 10 b		-	42	-	
Fall time	t _f				110	-	
Internal drain inductance	L _D	Between lead, 6 mm (0.25") from package and center of die contact		-	4.5	-	nH
Internal source inductance	L _S			_	7.5	-	ווח
Drain-Source Body Diode Characteristi	cs						
Continuous source-drain diode current	I _S	showing the	MOSFET symbol showing the		-	50°	- A
Pulsed diode forward current ^a	I _{SM}	integral reverse p - n junction diode		-	-	200	
Body diode voltage	V _{SD}	T _J = 25 °C, I _S = 51 A, V _{GS} = 0 V ^b		-	-	2.5	V
Body diode reverse recovery time	t _{rr}	T _J = 25 °C, I _F = 51 A, dl/dt = 100 A/μs b		-	130	180	ns
Body diode reverse recovery charge	Q _{rr}			-	0.84	1.3	μC
Forward turn-on time	t _{on}	Intrinsic turn	on time is negligible (turr	-on is do	minated b	y L _S and	L _D)

Notes

- a. Repetitive rating; pulse width limited by maximum junction temperature (see fig. 11)
- b. Pulse width \leq 300 µs; duty cycle \leq 2 %
- c. Current limited by the package, (die current = 51 A)



TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)

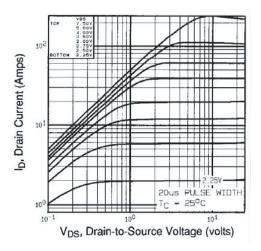


Fig. 1 - Typical Output Characteristics, T_C = 25 °C

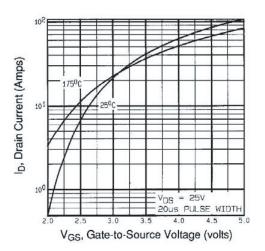


Fig. 3 - Typical Transfer Characteristics

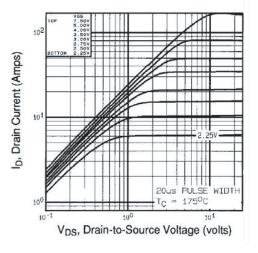


Fig. 2 - Typical Output Characteristics, T_C = 175 °C

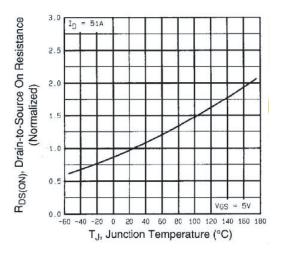


Fig. 4 - Normalized On-Resistance vs. Temperature



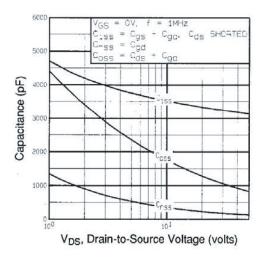


Fig. 5 - Typical Capacitance vs. Drain-to-Source Voltage

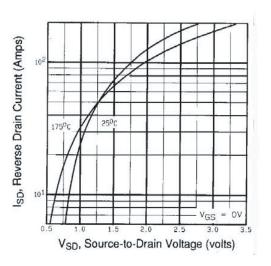


Fig. 7 - Typical Source-Drain Diode Forward Voltage

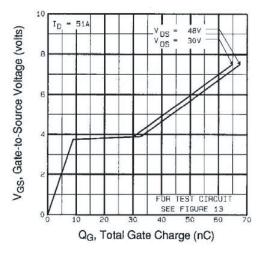


Fig. 6 - Typical Gate Charge vs. Gate-to-Source Voltage

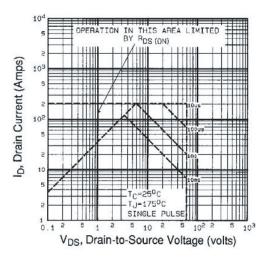


Fig. 8 - Maximum Safe Operating Area



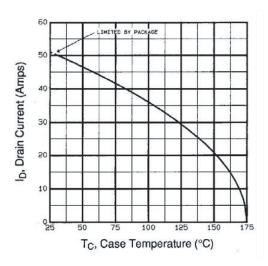


Fig. 9 - Maximum Drain Current vs. Case Temperature

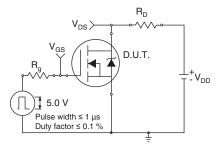


Fig. 10a - Switching Time Test Circuit

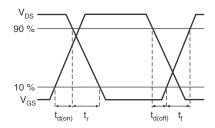


Fig. 10b - Switching Time Waveforms

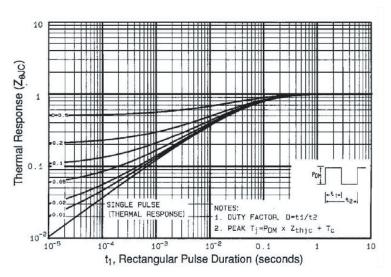
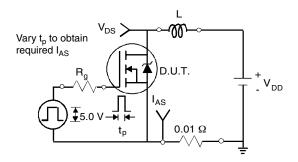


Fig. 10 - Maximum Effective Transient Thermal Impedance, Junction-to-Case







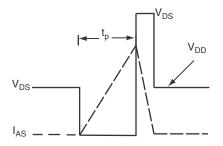


Fig. 12b - Unclamped Inductive Waveforms

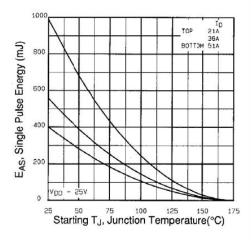


Fig. 12c - Maximum Avalanche Energy vs. Drain Current

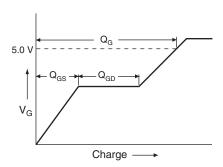


Fig. 13a - Basic Gate Charge Waveform

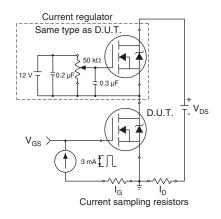
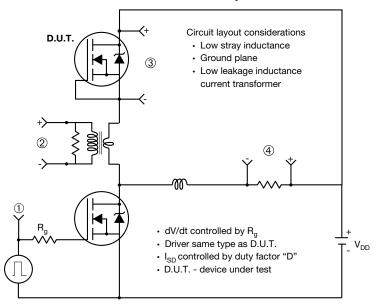


Fig. 13b - Gate Charge Test Circuit



Peak Diode Recovery dV/dt Test Circuit



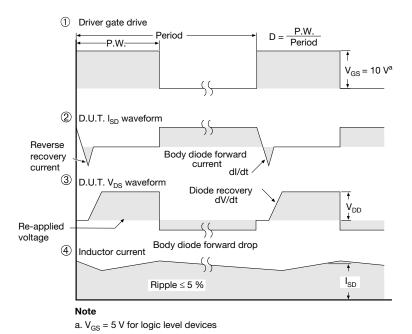


Fig. 11 - For N-Channel

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