International
IOR Rectifier

Data Sheet No. PD60276

Not recommended for new designs. Please use IRS20955.

IRS20954SPBF

Protected Digital Audio Driver

Features

- Floating PWM input enables easy half bridge implementation
- Integrated programmable bi-directional over-current protection with self-reset function
- Programmable compensated preset deadtime for improved THD performances
- High noise immunity
- ±100 V high voltage ratings deliver up to 500 W output power
- 3.3 V / 5 V logic compatible input
- Operates up to 800 kHz
- Ro HS compliant

Product Summary

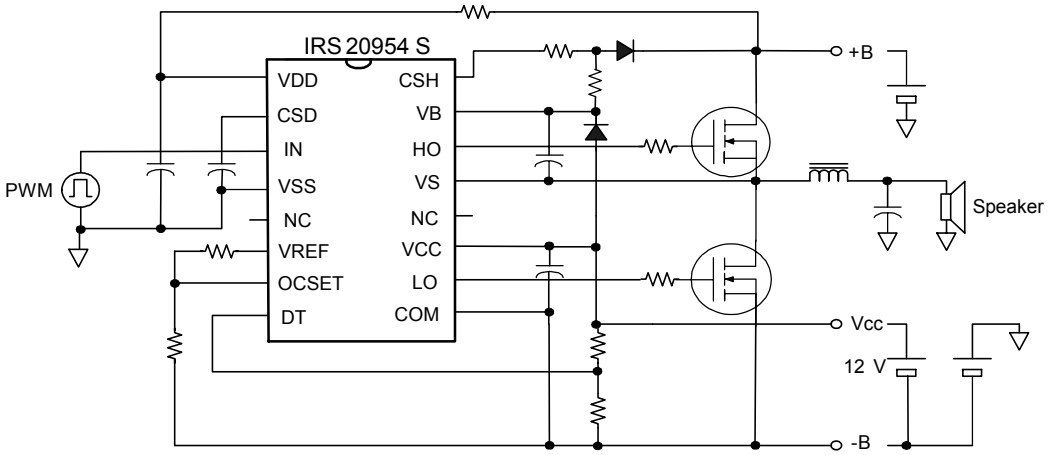
V_{OFFSET} (max)		± 100 V
Gate driver	Io+	1.0 A
	Io -	1.2 A
Selectable Deadtime		15 ns, 25 ns, 35ns, 45 ns
Propagation delay		90 ns
OC protection delay		1 µs (max)

Description

The IRS2 0954 is a high voltage, high spe ed M OSFET drive r with floating PWM input, spe cially desi gned for Cla ss D au dio amplifier ap plications. The bi-di rectional cu rrent sensi ng requires no external shunt resistors. It can ca pture over-current conditions at either p ositive or negative load current direction. A built-in control block p rovides secure prote ction sequence against over-current conditions, including a programmable reset timer. The internal de adtime gen eration blo ck provide s accurate gat e swit ch timing and en ables optim um deadtime settings for b etter audio performances, such as T HD and a udio noise floor.

Package

Typical Connection



(Please refer to Lead Assignments for correct pin configuration. This diagram shows electrical connections only)

Absolute Maximum Ratings

Absolute maximum ratings indicate sustained limits beyond which damage to the device may occur. All voltage parameters are absolute voltages referenced to COM; all currents are defined positive into any lead. The thermal resistance and power dissipation ratings are measured under board mounted and still air conditions.

Symbol	Definition	Min.	Max.	Units
V_B	High-side floating supply voltage	-0.3	220	V
V_S	High-side floating supply voltage (Note 1)	V_B-20	V_B+0.3	
V_{HO}	High-side floating output voltage	Vs-0.3	V_B+0.3	
V_{CSH}	CSH pin input voltage	Vs-0.3	V_B+0.3	
V_{CC}	Low-side fixed supply voltage (Note 1)	-0.3	20	
V_{LO}	Low-side output voltage	-0.3	V_{CC} +0.3	
V_{DD}	Floating input supply voltage	-0.3	210	
V_{SS}	Floating input supply voltage (Note 1)	(see I_{DDZ})	V_{DD}+0.3	
V_{IN}	PWM input voltage	V_{SS} -0.3	V_{DD}+0.3	
V_{CSD}	CSD pin input voltage	V_{SS} -0.3	V_{DD}+0.3	
V_{DT}	DT pin input voltage	-0.3	V_{CC} +0.3	
V_{OCSET}	OCSET pin input voltage	-0.3	V_{CC} +0.3	
V_{REF}	VREF pin voltage	-0.3	V_{CC} +0.3	
I_{DDZ}	Floating input supply zener clamp current (Note 1)	-	10	mA
I_{CCZ}	Low-side supply zener clamp current (Note 1)	-	10	
I_{BSZ}	Floating supply zener clamp current (Note 1)	-	10	
I_{OREF}	Reference output current	-	5	
d V_S /dt	Allowable V_S voltage slew rate	-	50	V/ns
d V_{SS} /dt	Allowable V_{SS} voltage slew rate (Note 2)	-	50	
d V_{SS} /dt	Allowable V_{SS} voltage slew rate upon power-up (Note 3)	-	50	V/ms
P_D	Maximum power dissipation	-	1.0	W
$R_{th,JA}$	Thermal resistance, junction to ambient	-	115	°C/W
T_J	Junction temperature	-	150	°C
T_S	Storage temperature	-55	150	
T_L	Lead temperature (soldering, 10 seconds)	-	300	

Note1: V_{DD} - V_{SS}, V_{CC} -COM and V_B - V_S contain internal shunt zener diodes. Please note that the voltage ratings of these can be limited by the clamping current.
Note2: For the rising and falling edges of step signal of 10 V; V_{ss}=15 V to 200 V.
Note3: V_{ss} ramps up from 0 V to 200 V.

Recommended Operating Conditions

For proper operation, the device should be used within the recommended conditions below. The V_s and COM offset ratings are tested with supplies biased at I_{DD}=5 mA, V_{CC}=12 V, and V_B-V_S=12 V.

Symbol	Definition Min.		Max.	Units
V_B	High-side floating supply absolute voltage	V_S+10 V	$_S$+18	V
V_S	High-side floating supply offset voltage	Note 1	100	
I_{DDZ}	Floating input supply Zener clamp current	1	5	mA
V_{SS}	Floating input supply absolute voltage	0	200	V
V_{HO}	High-side floating output voltage	V_S	V_B	
V_{CC}	Low-side fixed supply voltage	10	18	
V_{LO}	Low-side output voltage	0	V_{CC}	
V_{IN}	PWM input voltage	V_{SS}	V_{DD}	
V_{CSD}	CSD pin input voltage	V_{SS}	V_{DD}	
V_{DT}	DT pin input voltage	0	V_{CC}	
I_{OREF}	Reference output current to COM (Note 2)	0.3	0.8	mA
V_{OCSET} OCSET	pin input voltage	0.5	5	V
T_A Ambie	nt temperature	-40	125	°C
I_{PW}	Input pulse width	10 (note 3)	-	ns

Note 1: Logic operational for V_S equal to –5 V to +200 V. Logic state held for V_S equal to –5 V to –V_{BS}.
Note 2: Nominal voltage for V_{REF} is 5 V. I_{OREF} of 0.3 mA to 0.8 mA dictates total external resistor value on V_{REF} to be 6.3 kΩ to 16.7 kΩ.
Note 3: Output logic status may not respond correctly if input pulse width is smaller than the minimum pulse width

Electrical Characteristics

V_{CC}, V_{BS}= 12 V, I_{DD}=5 mA, V_{SS}=20 V, V_S=0 V, C_L=1 nF, and T_A=25 °C unless otherwise specified.

Symbol	Definition	Min.	Typ.	Max.	Units	Test Conditions
Low-side Supply						
UV_{CC+}	V_{CC} supply UVLO positive threshold	8.4	8.9	9.4	V	
UV_{CC-}	V_{CC} supply UVLO negative threshold	8.2	8.7	9.2		
I_{QCC}	Low-side quiescent current	-	-	3	mA	V_{DT} = V_{CC}
V_{CLAMPL}	Low-side Zener diode clamp voltage	19.8	20.8	21.8	V	I_{CC}=2 mA
High-side Floating Supply						
UV_{BS+}	High-side well UVLO positive threshold	8.0	8.5	9.0	V	
UV_{BS-}	High-side well UVLO negative threshold	7.8	8.3	8.8		
I_{QBS}	High-side quiescent current	-	-	1	mA	
I_{LKH}	High- to low-side leakage current	-	-	50	µA	V_B=V_S =200 V
V_{CLAMPH}	High-side Zener diode clamp voltage	19.8	20.8	21.8	V	I_{BS}=2 mA
Floating Input Supply						
UV_{DD+}	V_{DD}, V_{SS} floating supply UVLO positive threshold	8.2	8.7	9.2	V V	$_{SS}$ =0 V
UV_{DD-}	V_{DD}, V_{SS} floating supply UVLO negative threshold	7.7	8.2	8.7		
I_{QDD}	Floating input quiescent current	-	-	1	mA	V_{DD}=9.5 V +V_{SS}
V_{CLAMPM}	Floating input Zener diode clamp voltage	9.9	10.4	10.9	V	I_{DD}=2 mA
I_{LKM}	Floating input side to low-side leakage current	-	-	50	µA	V_{DD}=V_{SS} =200 V

Electrical Characteristics (cont.)

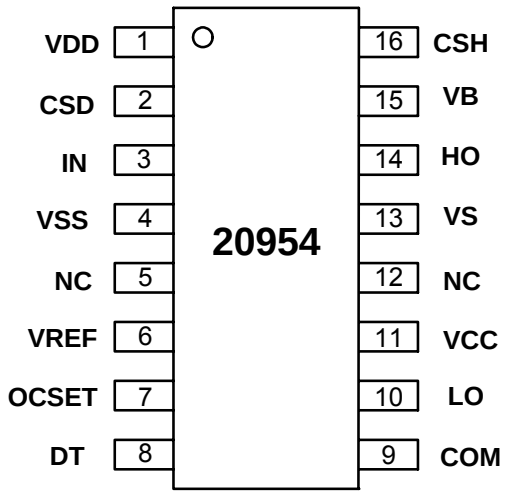
Symbol	Definition	Min.	Typ.	Max.	Units	Test Conditions
Floating PWM Input						
V_{IH}	Logic high input threshold voltage	2.3	-	-	V	
V_{IL}	Logic low input threshold voltage	-	-	1.5		
I_{IN+}	Logic "1" input bias current	-	-	40	µA	V_{IN} =3.3 V
I_{IN-}	Logic "0" input bias current	-	-	5		V_{IN} = V_{SS}
Protection						
V_{REF}	Reference output voltage 4.6		5.1	5.6	V	I_{OREF} =0.5 mA
$V_{th,OCL}$	Low-side OC threshold in V_S 1.0		1.2	1.4		OCSET=1.2 V, Fig. 13
$V_{th,OCH}$	High-side OC threshold in V_{CSH}	1.0+ Vs	1.2+ Vs	1.4+ Vs		Vs=200 V, Fig. 14
$V_{th,1}$	CSD pin shutdown release threshold	0.62 x V_{DD}	0.70 x V_{DD}	0.78 x V_{DD}		V_{SS} =0 V
$V_{th,2}$	CSD pin self reset threshold	0.26 x V_{DD}	0.30 x V_{DD}	0.34 x V_{DD}		
I_{CSD+}	CSD pin discharge current	50	100	150	µA V	$_{SD}$ = V_{SS} +5 V
I_{CSD-}	CSD pin charge current	50	100	150		
t_{SD}	Shutdown propagation delay from V_{CSD} > V_{SS} + $V_{th,OCH}$ to shutdown	- -		1	µs	Fig. 2
t_{OCH}	Propagation delay time from V_{CSH} > $V_{th,OCH}$ to shutdown	- -		1		Fig. 3
t_{OCL}	Propagation delay time from Vs> $V_{th,OCL}$ to shutdown	- -		1		Fig. 4
Gate Driver (Fig.5)						
Io+	Output high short circuit current (source)	0.8 1.0		-	A	V_o=0 V, PW≤10 µs
Io-	Output low short circuit current (sink)	1.0	1.2	-		V_o=12 V, PW≤10 µs
V_{OL}	Low level output voltage LO – COM, HO - VS	- -		0.1	V	
V_{OH}	High level output voltage VCC – LO, VB - HO	- -		1.4		I_o=0 A
t_r	Turn-on rise time	-	15	-	ns	
t_f	Turn-off fall time	- 10 -				
ton_1	High- and low-side turn-on propagation delay, floating inputs	- 105		-		V_{DT} = V_{CC}, V_S = 100 V, V_{SS} = COM
toff_1	High and low-side turn-off propagation delay, floating inputs	-	90	-		
ton_2	High- and low-side turn-on propagation delay, non-floating inputs	- 105		-		
toff_2	High- and low-side turn-off propagation delay, non-floating inputs	- 90 -				
DT1	Deadtime: LO turn-off to HO turn-on (DT_{LO-HO}) & HO turn-off to LO turn-on (DT_{HO-LO})	8 15		22		V_{DT}>V_{DT1}, V_{SS} = COM
DT2	Deadtime: LO turn-off to HO turn-on (DT_{LO-HO}) & HO turn-off to LO turn-on (DT_{HO-LO})	15 25 35				V_{DT1}>V_{DT}> V_{DT2}, V_{SS} = COM
DT3	Deadtime: LO turn-off to HO turn-on (DT_{LO-HO}) & HO turn-off to LO turn-on (DT_{HO-LO})	20 35 50				V_{DT2}>V_{DT}> V_{DT3}, V_{SS} = COM
DT4	Deadtime: LO turn-off to HO turn-on (DT_{LO-HO}) & HO turn-off to LO turn-on (DT_{HO-LO})V_{DT}= V_{DT4}	25 45 60				V_{DT3}>V_{DT}, V_{SS} = COM

Electrical Characteristics (cont.)

Symbol	Definition	Min.	Typ.	Max.	Units	Test Conditions
V_{DT1}	DT mode select threshold 2	0.51·(V_{cc})	0.57·(V_{cc})	0.63·(V_{cc})	V	
V_{DT2}	DT mode select threshold 3	0.32·(V_{cc})	0.36·(V_{cc})	0.40·(V_{cc})		
V_{DT3}	DT mode select threshold 4	0.21·(V_{cc})	0.23·(V_{cc})	0.25·(Vv		

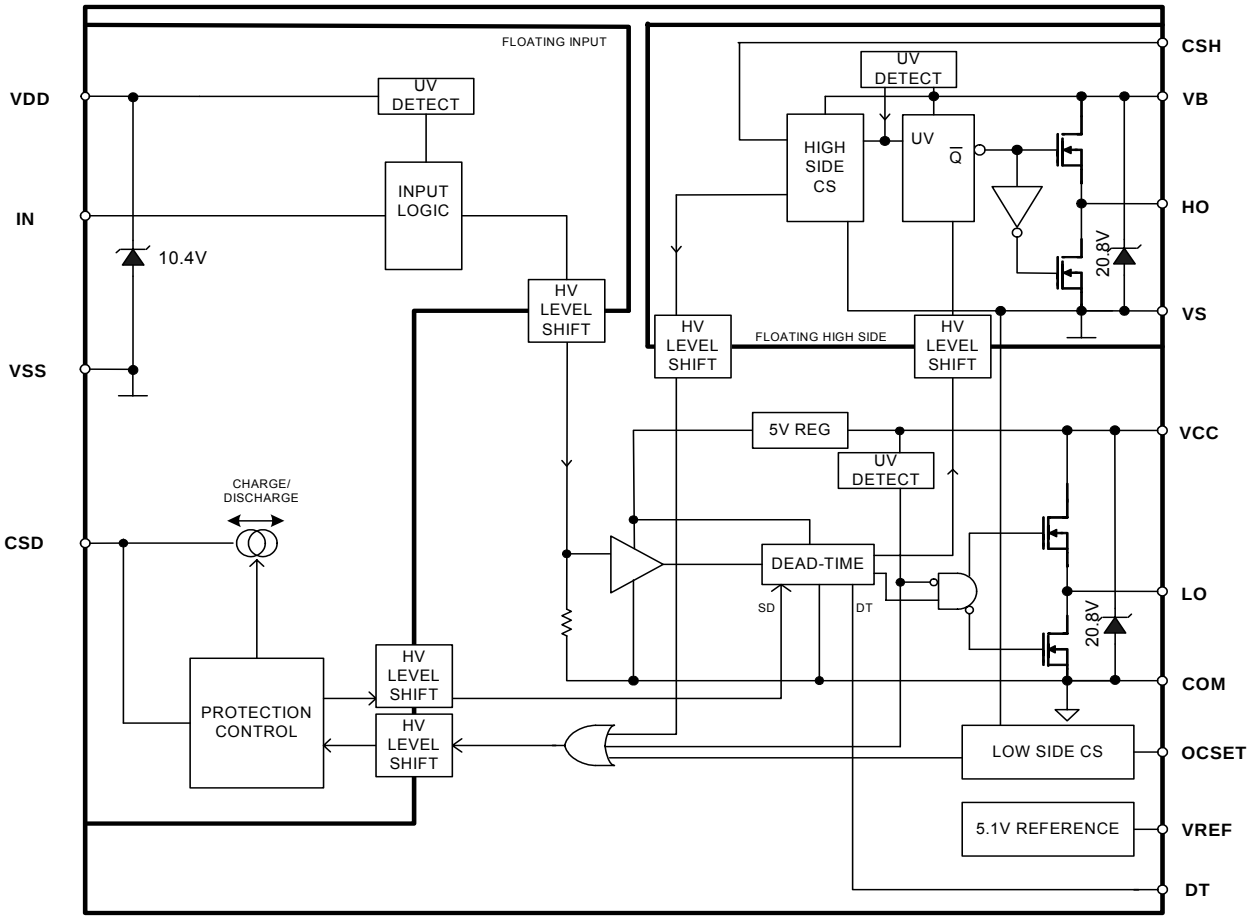
Lead Definitions

Pin #	Symbol	Description
1	VDD	Floating input positive supply
2	CSD	Shutdown timing capacitor, referenced to VSS
3	IN	PWM non-inverting input, in phase with HO
4	VSS	Floating input supply return
5	NC	
6	VREF	5 V reference output for setting OCSET
7	OCSET	Low-side over-current threshold setting, referenced to COM
8	DT	Input for programmable deadtime, referenced to COM
9	COM	Low-side supply return
10	LO	Low-side output
11	VCC	Low-side logic supply
12	NC	
13	VS	High-side floating supply return
14	HO	High-side output
15	VB	High-side floating supply
16	CSH	High-side over-current sensing input, referenced to VS



IRS20954 16 Lead SOIC (narrow body)

Block Diagram



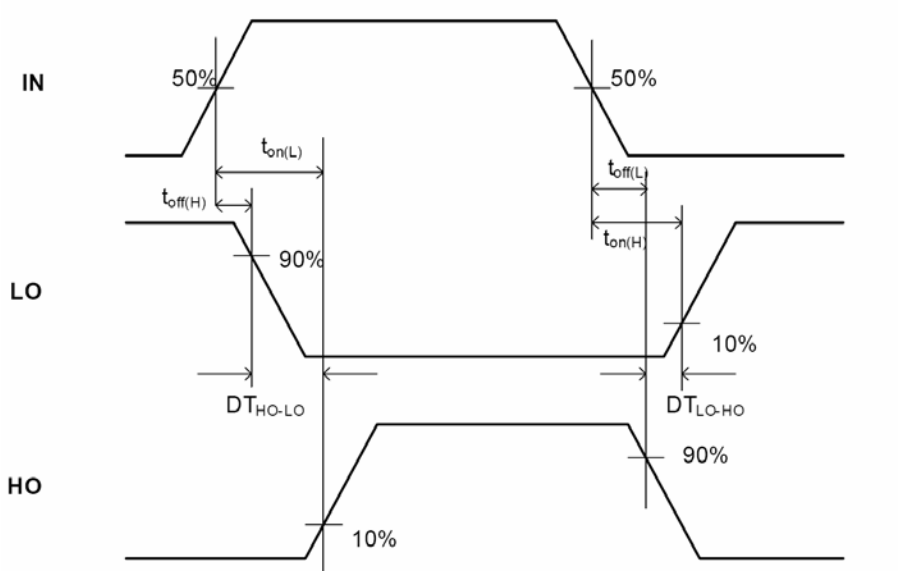


Figure 1: Switching Time Waveform Definitions

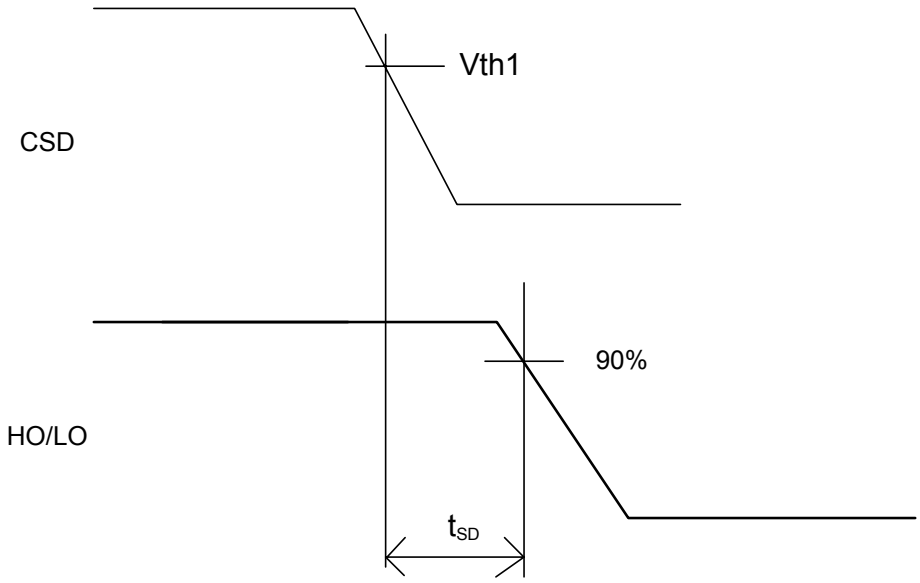


Figure 2: CSD to Shutdown Waveform Definitions

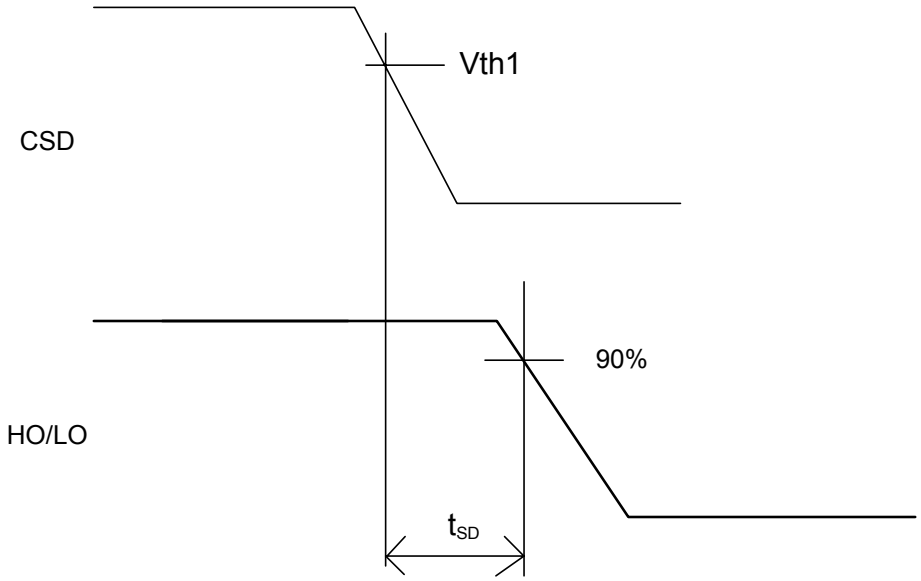


Figure 3: CSH to Shutdown Waveform Definitions

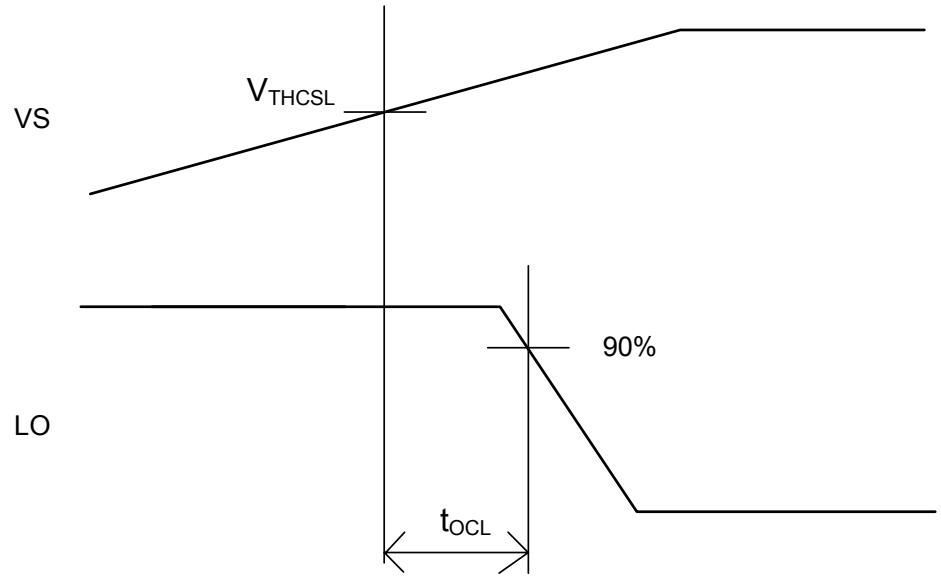


Figure 4: V_s > $V_{TH,SCL}$ to Shutdown Waveform Definitions

Functional Description

Floating PWM Input

The IRS20954 has a floating input interface which enables easy half bridge implementation. Three pins, V_{DD}, CSD and IN, are referenced to V_{SS}. As a result, the PWM input signal can be directly fed into IN referencing ground, which is typically middle point of DC bus in a half bridge configuration.
The IRS20954 also has a non-floating input with V_{SS} tied to COM.

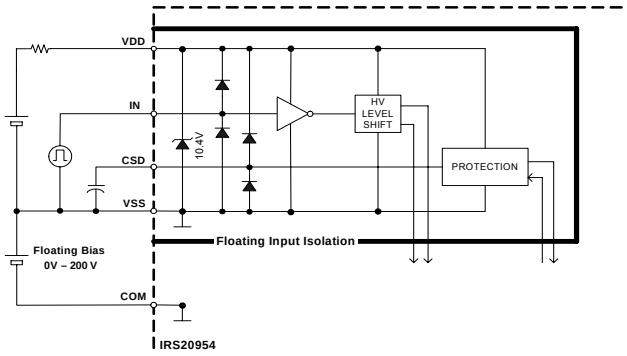


Figure 5: Floating PWM Input Structure

Over-Current Protection (OCP)

The IRS20954 features over-current protection to protect the power MOSFET from over load conditions. The IRS20954 enters shutdown mode when it detects over-current condition either from low-side or high-side current sensing. The timing control block measures resume timing interval with an external timing capacitor Ct. All the critical timing of the over-current protection is specified and guaranteed for secure protection.

The sequence on the over-current detection is:

1. As soon as either high or low-side current sensing block detects over-current condition, the OC Latch (OCL) flips and shutdowns the outputs LO and HO.
2. The CSD pin starts discharging the external capacitor C_t.
3. When V_{SCD} crosses the lower threshold V_{th2}, the output signal from the COMP2 resets the OCL.
4. The CSD pin starts charging the external capacitor C_t.
5. When V_{SCD} crosses the upper threshold V_{th1}, the COMP1 flips and enables shutdown signal released.
6. If one of current sensing block detects over-current condition, the sequence is repeated until the cause of over-current goes away.

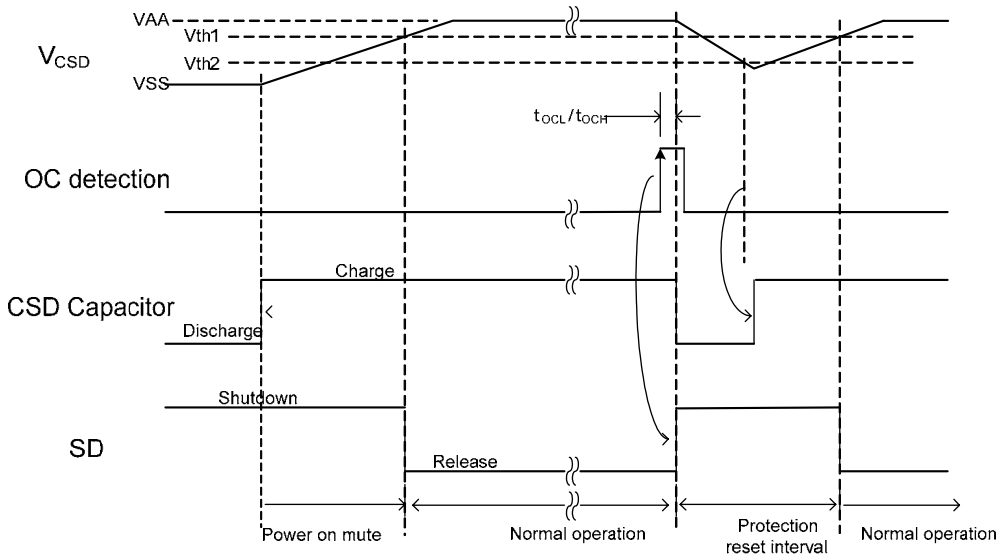


Figure 6: Over-Current Protection Timing Chart

Protection Control

The internal pr otection co ntrol block man ages oper ational mode between shutdo wn and normal, with a help from CSD pin. Shutdown mode forces LO and HO to output 0 V to the COM and V_S respectively to turn the power MOSFET off.

The external capacitor pin, CSD, provides five functions.

1. Power up delay timer for self reset configuration
2. Self-reset configuration
3. Shutdo wn input
4. Latche d protection configuration
5. Shutdown status output (host I/F)

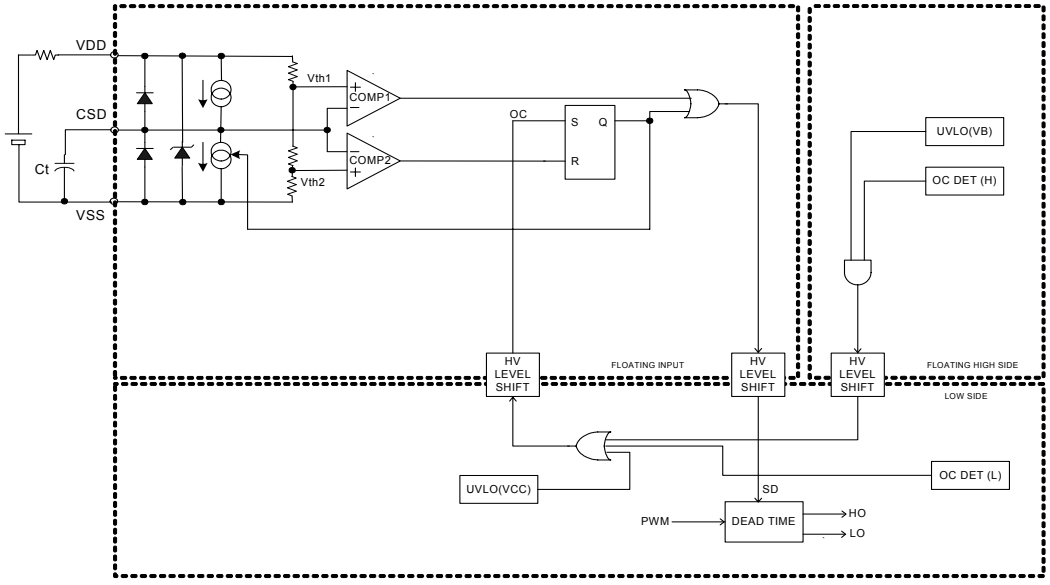


Figure 7: Shutdown Functional Block Diagram

Self Reset Protection

By simply putting a capacitor between the CSD and V_{SS}, the OCP in the IRS20954 acts as a self.

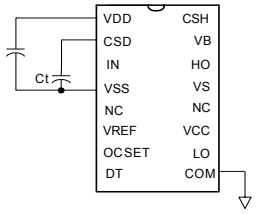


Figure 8: Self-Reset Protection Configuration

Designing Ct

Timing capacitor Ct programs the protection resume interval timing t_{PR} given as:

$$t_{PR} = 1.1 \cdot \frac{C_t \cdot V_{DD}}{I_{CSD}} \quad [s]$$

or

$$C_t = \frac{t_{PR} \cdot I_{CSD}}{1.1 \cdot V_{DD}} \quad [F]$$

For example, t_{PR} is 1.2 s with a 10 µF capacitor for V_{DD}=10.8 V. The start-up time t_{SU}, from power-up to shutdown release, is given as:

$$t_{SU} = 0.7 \cdot \frac{C_t \cdot V_{DD}}{I_{CSD}} \quad [s]$$

or

$$C_t = \frac{t_{SU} \cdot I_{CSD}}{0.7 \cdot V_{DD}} \quad [F]$$

where I_{CSD} is charge/discharge current in CSD pin, 100 µA.
V_{DD} is supply voltage respect to V_{SS}.

Protection-resume timing t_{PR} should be long enough to avoid overheating and failure of the MOSFET from the repetitive sequences of shutdown and resume when the load is in continuous short circuit. In most of applications, the minimum recommended protection-resume timing t_{PR} is 0.1 s.

Shutdown Input

By externally discharging Ct down to below V_{th2}, for example with a transistor shown in Fig. 9, the IRS20954 enters shutdown mode. The operation resumes when the voltage of CSD pin comes back and cross the upper threshold of CSD, V_{th1}, by its charging process.

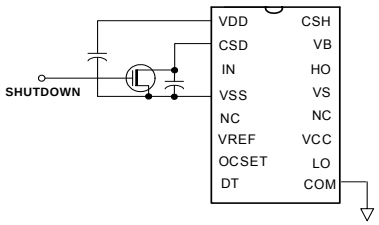


Figure 9: Shutdown Input

Latched Protection

Connecting CSD to V_{DD} through a 10 kΩ or less resistor configures the IRS20954 as a latched over-current protection. The over-current protection stays in shutdown mode after over-current condition detected. To reset the latch status, an external reset switch brings CSD pin voltage down below the lower threshold, V_{th2}. Minimum reset pulse width required is 200 ns.

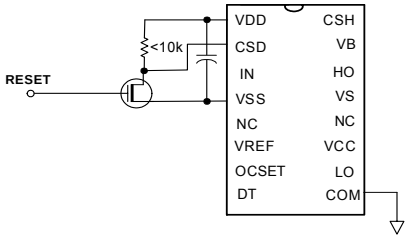


Figure 10: Latched Protection Configuration

Interfacing with System Controller

The IRS20954 communicates with external system controller by adding simple interfacing circuit shown in Fig. 11. A generic PNP-BJT U1, such as 2N3906, is to send out SD signal when OCP event happens by capturing sinking current in CSD pin. Another generic NPN-BJT U2, such as 2N3094, is to reset the internal protection logic by pulling the CSD voltage below V_{th2}. Note that the CSD pin is configured as a latched type OCP in this configuration.

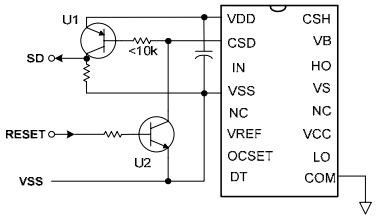


Figure 11: Interfacing System Controller

Programming OCP Trip Level

In a Class D audio amplifier, the direction of the load current alternates according to the audio input signal. An over-current condition can therefore happen during either a positive current cycle or a negative current cycle. The IRS20954 uses $R_{DS(ON)}$ in the output MOSFET as current sensing resistors. Due to the high voltage IC structural constraints, high and low-side have different implementations of current sensing. Once measured current gets exceeded pre-determined threshold, OC output signal is fed to the protection block to shutdown the MOSFET to protect the devices.

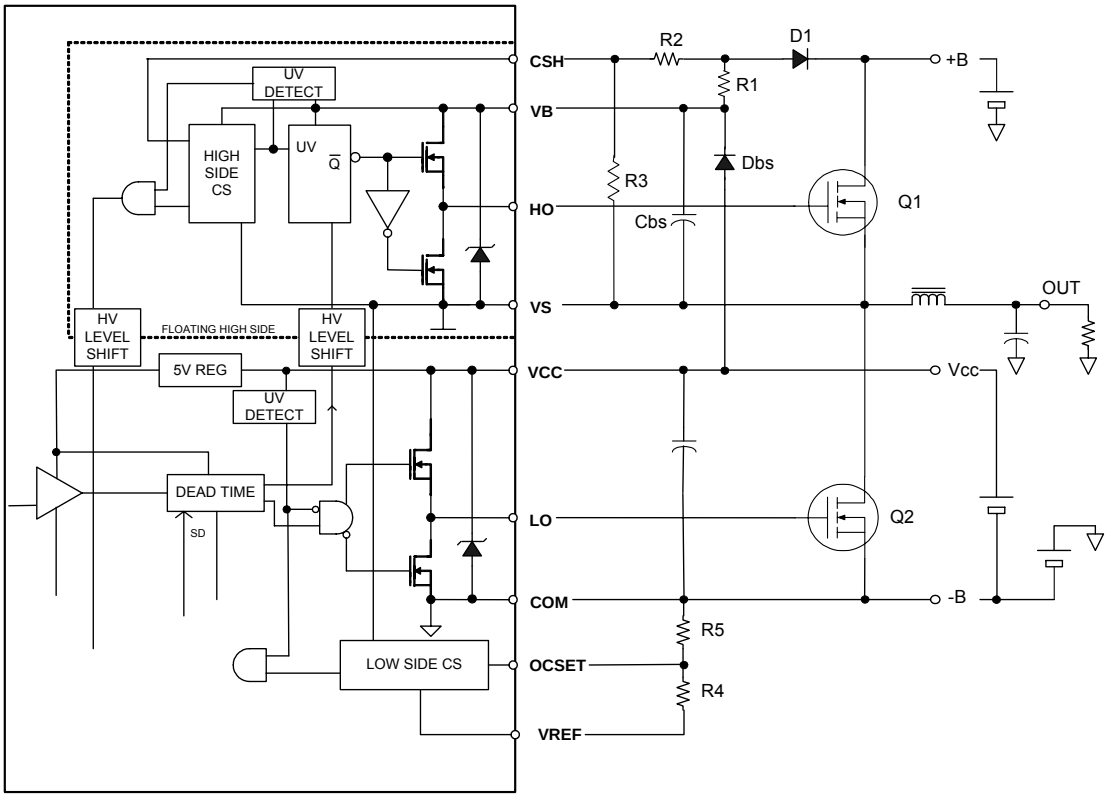


Figure 12: Bi-Directional Over-Current Protection

Low-side Over-Current Sensing

For the negative load current, low-side over-current sensing monitors over load condition and shutdown the switching operation if the load current exceeds the preset trip level.

The low-side current sensing is based on measurement of V_{DS} during the low-side MOFET on state. In order to avoid incorrect current value due to overshoot , V_S sensing ignores the first 200 ns signal after LO turned on.
OCSET pin is to progr am the threshold for l ow-side over-current sensing. The threshold voltage at V_S pin tur ning on the OC protection is the same as the vo ltage applied to the OCSET pin to COM. It is recommended to use V_{REF} to supply a reference voltage to a resistive divider, R4 and R5, generating a voltage to OCSET for better immunity against V_{CC} fluctuations.

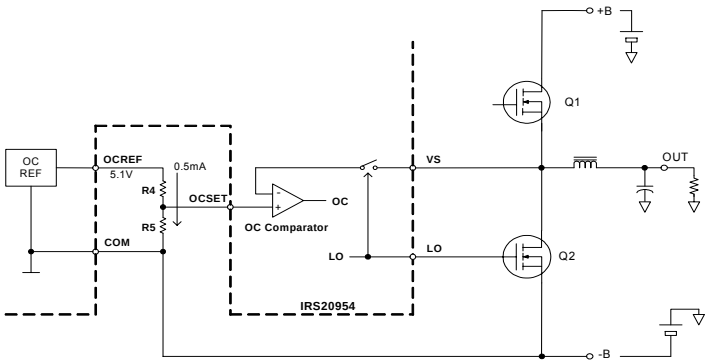


Figure 13: Low-Side Over-Current Sensing

Since the sensed voltage of V_S is compared with the voltages fed to the OCSET pin, the required voltage of OCSET with respect to COM for a trip level I_{TRIP+} is:

$V_{OCSET} = V_{DS(LOW\text{-}SIDE)} = I_{TRIP+} \times R_{DS(ON)}$

In order to neglect the input bias current of OCSET pin, it is recommended to use 10 k Ω total for R4 and R5 to drain 0.5 mA through the resistors.

High-side Over-Current Sensing

For the positive load current, high-side over-current sensing monitors over load condition by measuring V_{DS} with CSH and Vs pins and shutdown the operation. The CSH pin is to detect the drain-to-source voltage refers to the V_S pin which is the source of the high-side MOSFET. In order to neglect overshoot ringing at the switching edges, CSH sensing circuitry starts monitoring after the first 300 ns the HO is on by blanking the signal from CSH pin.

In contrast to the low-side current sensing, the threshold of CSH pin to engage OC protection is internally fixed at 1.2 V. An external resistive divider R2 and R3 can be used to program a higher threshold.

An external reverse blocking diode, D1, is to block high voltage feeding into the CSH pin while high-side is off. By subtracting a forward voltage drop of 0.6 V at D1, the minimum threshold which can be set in the high-side is 0.6 V across the drain to source.

With the configuration in Fig. 14, the voltage in CSH is:

$$V_{CSH} = \frac{R3}{R2 + R3} \cdot \left(V_{DS(HIGHSIDE)} + V_{F(D1)}\right)$$

Where:
$V_{DS(HIGH\text{-}SIDE)}$ is drain to source voltage of the high-side MOSFET in its ON state
$VF_{(D1)}$ is the forward drop voltage of D1

Since $V_{DS(HIGH\text{-}SIDE)}$ is determined by the product of drain current I_D and $R_{DS(ON)}$ in the high-side MOSFET. V_{CSH} can be written as:

$$V_{CSH} = \frac{R3}{R2 + R3} \cdot \left(R_{DS(ON)} \cdot I_D + V_{F(D1)}\right)$$

$$\frac{R2}{R3} = \frac{V_{DS} + V_F}{Vth_{OCH}} - 1$$

The reverse blocking diode D1 is forward biased by a 10 kΩ resistor R1 when the high-side MOSFET is on.

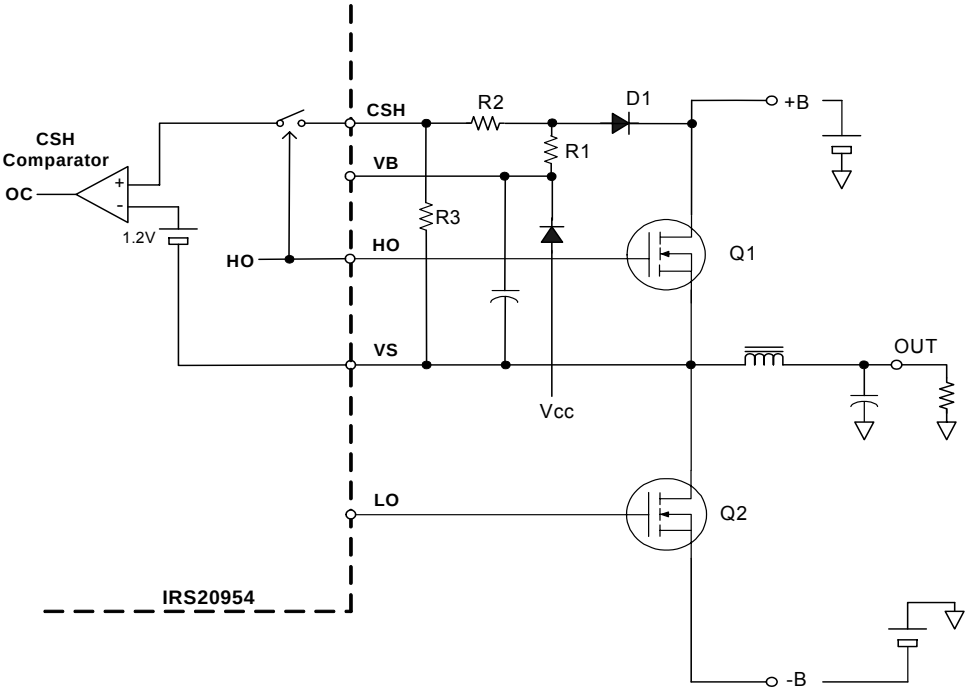


Figure 14: Programming High-side Over-Current Threshold

OCP Design Example

High-side Over-current Setting

Fig. 14 demonstrates the typical peripheral circuit of high-side current sensing. For example, the over-current protection level is set to trip at 30 A with a MOSFET with $R_{DS(ON)}$ of 100 mΩ, the component values of R2 and R3 are calculated as:

Choose R2+R3=10 kΩ, thus $R_3 = 10k\Omega - R_2$.

$$R_3 = 10\ k\Omega \frac{Vth_{OCH}}{V_{DS} + V_F}$$

Vth_{OCL} = 1.2 V
V_F = 0.6 V
$V_{DS@ID=30A}$ = 100 mΩ x 30 A = 3 V

V_{DS} is the voltage drop at I_D=30 A across $R_{DS(ON)}$ of the high-side MOSFET. V_F is a forward voltage of reverse blocking diode, D1. The values of R2 and R3 from the E-12 series are:
R2 = 6.8 kΩ
R3 = 3.3 kΩ

Choosing the Right Reverse Blocking Diode

The reverse blocking diode D1 is determined by voltage rating and speed. To block bus voltage, reverse voltage has to be higher than (+B)-(-B). Also the reverse recovery time needs to be as fast as the bootstrap charging diode. The Philips BAV21W, 200 V, 50 ns high speed switching diode, is more than sufficient.

Low-side Over-current Setting

Designing with the same MOSFET as in high-side with $R_{DS(ON)}$ of 100 mΩ, the OCSET voltage, V_{OCSET}, to set 30 A trip level is given by:

$V_{OCSET} = I_{TRIP+} \times R_{DS(ON)} = 30\ A \times 100\ m\Omega = 3.0\ V$

Choose R4+R5=10 kΩ for proper loading of VREF pin, thus

$$R_5 = \frac{V_{OCSET}}{V_{REF}} \cdot 10\ k\Omega$$
$$= \frac{3.0V}{5.1V} \cdot 10\ k\Omega$$
$$= 5.8\ k\Omega$$

W here V_{REF} is the output voltage of VREF pin, 5.1 V typical.

Choose R5 = 5.6 kΩ and R4 = 3.9 kΩ from E-12 series.

In general, $R_{DS(ON)}$ has a positive temperature coefficient that needs to be considered when the threshold level is being set. Although this characteristic is preferable from a device protection point of view, these variation needs to be considered as well as variations of external or internal component values.

Deadtime Generator

The deadtime generator block provides a blanking time between the high-side on and low-side on to avoid a simultaneous on state causing shoot-through. The IRS20954 has an internal deadtime generation block to reduce the number of external components in the output stage of a Class D audio amplifier. Selectable deadtime programmed through the DT/SD pin voltage is an easy and reliable function, which requires only two external resistors. This selectable deadtime way of setting prevents outside noise from modulating the switching timing, which is critical to the audio performances.

How to Determine Optimal Deadtime

The effective deadtime in an actual application differs from the deadtime specified in this datasheet due to finite switching fall time, t_f. The deadtime value in this datasheet is defined as the time period from the starting point of turn-off on one side of the switching stage to the starting point of turn-on on the other side as shown in Fig. 15. The fall time of MOSFET gate voltage must be subtracted from the deadtime value in the datasheet to determine the effective dead time of a Class D audio amplifier.

(Effective deadtime) = (Deadtime in datasheet) – (fall time, t_f)

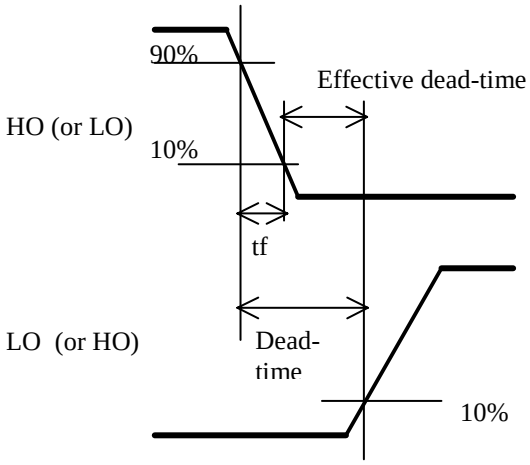


Figure 15: Effective Deadtime

A longer dead time period is required for a MOSFET with a larger gate charge value because of the longer t_f. A shorter effective deadtime setting is always beneficial to achieve better linearity in the Class D switching stage. However, the likelihood of shoot-through current increases with narrower deadtime settings in mass production. Negative values of effective deadtime may cause excessive heat dissipation in the MOSFETs, potentially leading to serious damage. To calculate the optimal deadtime in a given application, the fall time tf for both output voltages, HO and LO, in the actual circuit needs to be measured. In addition, the effective deadtime can also vary with temperature and device parameter variations. Therefore, a minimum effective deadtime of 10 ns is recommended to avoid shoot-through current over the range of operating temperatures and supply voltages.

Programming Deadtime

DT pin provides a function setting deadtime. The IRS20954 determines its deadtime based on the voltage applied to the DT pin. An internal comparator translates which pre-determined deadtime is being used by comparing internal reference voltages. Threshold voltages for each mode are set internally by a resistive voltage divider off V_{CC}, negating the need of using a precise absolute voltage to set the mode. The relationship between the operation mode and the voltage at DT pin is illustrated in the Fig. 16 below.

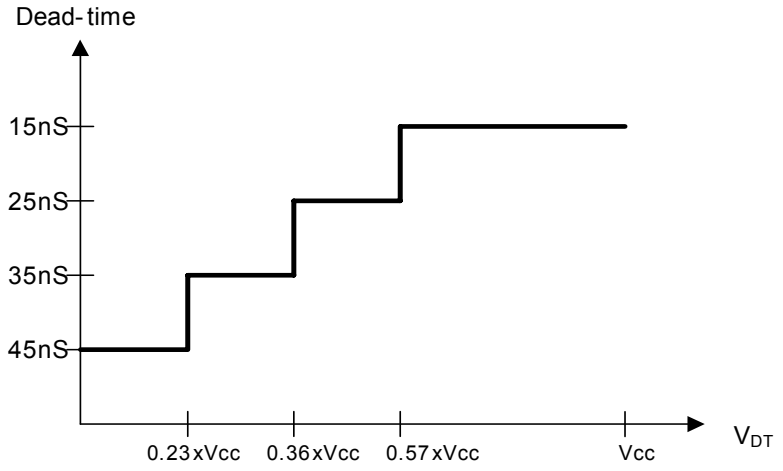


Figure 16: Deadtime Settings vs. V_{DT} Voltage

Table 1 shows suggested values of resistance for setting the deadtime. Resistors with up to 5% tolerance can be used if these listed values are followed.

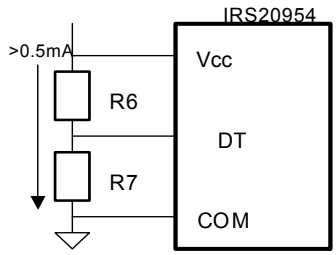


Figure 17: External Resistor

Deadtime mode	R6 R7		DT/SD voltage
DT1	<10 kΩ	Open	(V_{cc})
DT2	5.6 kΩ	4.7 kΩ	0.46(V_{cc})
DT3	8.2 kΩ	3.3 kΩ	0.29(V_{cc})
DT4	Open	<10 kΩ kΩ	COM

Table 1: Suggested Resistor Values for Deadtime Settings

Power Supply Considerations

Supplying V_{DD}

V_{DD} is designed to be supplied with the internal zener diode clamp. V_{DD} supply current I_{DD} can be estimated by:

I_{DD} = 1.5 mA x 300 x 10^{-9} x switching frequency + 0.5 mA + 0.5 mA
(Dynamic power consumption) (Static) (zener bias)

The resistance of R_{dd} to feed this I_{DD} therefore is:

$$Rdd \le \frac{V_{+B} - 10.8V}{I_{DD}} \quad [\Omega]$$

In case of 400 kHz average PWM switching frequency, the required I_{DD} is 1.18 mA. A condition using 50 V power supply voltage yields R_{dd}=33 kΩ.

Make sure I_{DD} is below the maximum zener diode bias current, $I_{DDZ,}$ at static state conditions such as a condition with no PWM input.

$$I_{DDZ} \ge \frac{V_{+B} - 10.8V}{Rdd} - 0.5\ mA$$

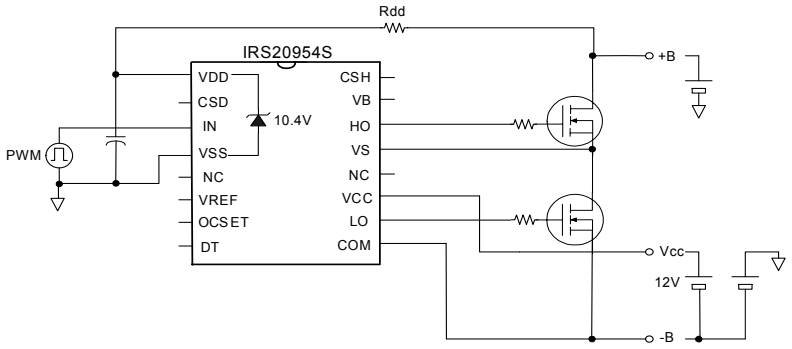


Figure 18: Supplying V_{DD}

Charging V_{BS} Prior to start

The high-side bootstrap power supply can be charged up through a resistor from the positive supply bus to V_B pin by utilizing an internal 20.8 V zener diode clamp between V_B and V_S. Advantage of this scheme is to eliminate the minimum duration required for the initial low-side ON.

To determine the requirement for Rcharge, following condition has to be met;

$$I_{CHARGE} > I_{QBS}$$

Where I_{CHARGE} is a required charging current through Rcharge
I_{QBS} is high-side quiescent current

Note that Rcharge can drain floating supply charge during on state of high-side, which limits maximum PWM modulation index capability of the system. Rcharge should be large enough not to discharge the floating power supply during the high-side ON.

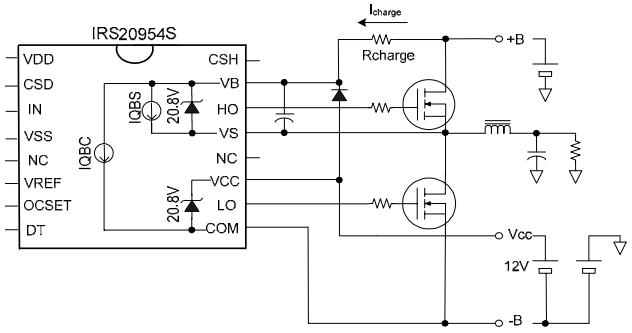


Figure 19: Bootstrap Supply Pre-Charging

Start-up Sequence (UVLO)

The protection control block monitors the status of the power supply of V_{DD} and V_{CC} whether the voltages are above the Under Voltage Lockout threshold. The LO and HO of the IRS20954 are disabled by shutdown until the UVLO of V_{CC} and V_{DD} are released and CSD timer capacitor Ct is charged up. After the UVLO of V_{CC} is released, CSD pin resets power-on timer. At the

time the voltage at CSD pin reached the release threshold, V_{th1}, shutdown logic enables LO and HO. The OC detection blocks for the low-side and high-side are disabled until UVLO of V_{CC} and V_{BS} are released.

Power-down Sequence

As soon as V_{DD} or V_{CC} reaches the UV LO negative going threshold, protection logic makes LO and HO 0 V to turn off the MOSFET.

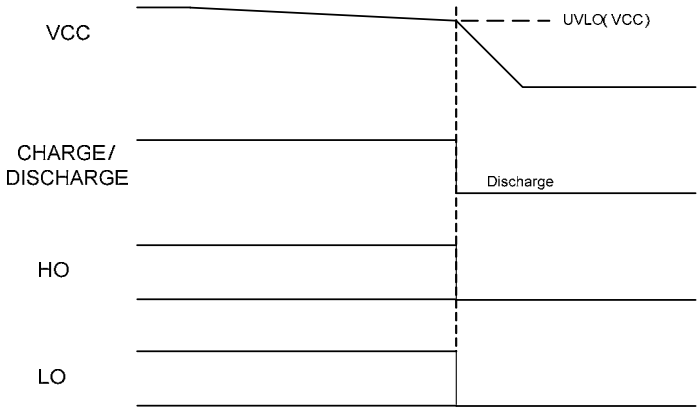


Figure 20: IRS20954 Power-Down Timing Chart

Power Supply Decoupling

As the IRS20954 contains analog circuitry, careful attention to the power supply decoupling should be taken to achieve proper operation. Ceramic capacitors of 0.1 µF or more close to the power supply pins are recommended.

Please also refer to the application note AN-978 for general considerations of high voltage gate driver IC.

V_{SS} Negative Bias Clamping

There is a case that V_{SS} can go below the COM potential such as a case missing negative supply in dual supply configuration. This causes excessive negative V_{SS} voltage to damage the IRS20954. It is recommended to have a diode to clamp potential negative bias to V_{SS}, if there is a possibility. A standard recovery 1 A diode such as 1N4002 is sufficient in most cases for this purpose.

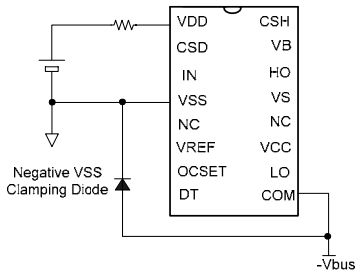


Figure 21: Negative V_{SS} Clamping

Junction Temperature Estimation

The power dissipation in the IRS20954 consists of following dominant items;

- P_{MID}: dissipation in floating input logic and protection
- P_{LOW}: dissipation in low-side
- P_{HIGH}: dissipation in high-side

1. P_{MID}: Dissipation in Floating Input Section

The dissipation in floating input section is given by;

$$P_{MID} = P_{ZDD} + P_{LDD}$$

$$\approx \frac{V_{+BUS} - V_{DD}}{R_{DD}} \cdot V_{DD}$$

Where
P_{ZDD} is dissipation from internal zener diode clamping V_{DD} voltage.
P_{LDD} is dissipation from internal logic circuitry.
V_{+BUS} is positive bus voltage feeding V_{DD} from.
R_{DD} is a resistor feeding V_{DD} from V_{+BUS}.

For obtaining a value of R_{DD}, refer to Supplying V_{DD} section above.

2. P_{LOW}: Dissipation in Low-side

The dissipation in low-side includes loss from logic circuitry and loss from driving LO, and is given by;

$$P_{LOW} = P_{LDD} + P_{LO}$$

$$= \left(I_{QCC} \cdot V_{CC}\right) + \left(Vcc \cdot Q_g \cdot f_{SW} \cdot \frac{R_O}{R_O + R_g + R_{g(\text{int})}} \right)$$

Where
P_{LDD} is dissipation from internal logic circuitry.
P_{LO} is dissipation from gate drive stage to LO.
R_O is equivalent output impedance of LO, typically 10 Ω for the IRS20954.
$R_{g(int)}$ is internal gate resistance of MOSFET.
R_g is external gate resistance.
Qg is total gate charge of low-side MOSFET.

3. P_{HIGH}: Dissipation in High-side

The dissipation in high-side includes loss from logic circuitry and loss from driving LO and is given by;

$$P_{HIGH} = P_{LDD} + P_{HO}$$

$$= \left(I_{QBS} \cdot V_{BS}\right) + \left(V_{BS} \cdot Q_g \cdot f_{SW} \cdot \frac{R_O}{R_O + R_g + R_{g(\text{int})}}\right)$$

Where
P_{LDD} is dissipation from internal logic circuitry.
P_{HO} is dissipation from gate drive stage to LO.
R_O is equivalent output impedance of HO, typically 10 Ω for the IRS20954.
$R_{g(int)}$ is internal gate resistance of high-side MOSFET.
R_g is external gate resistance.
Qg is total gate charge of high-side MOSFET.

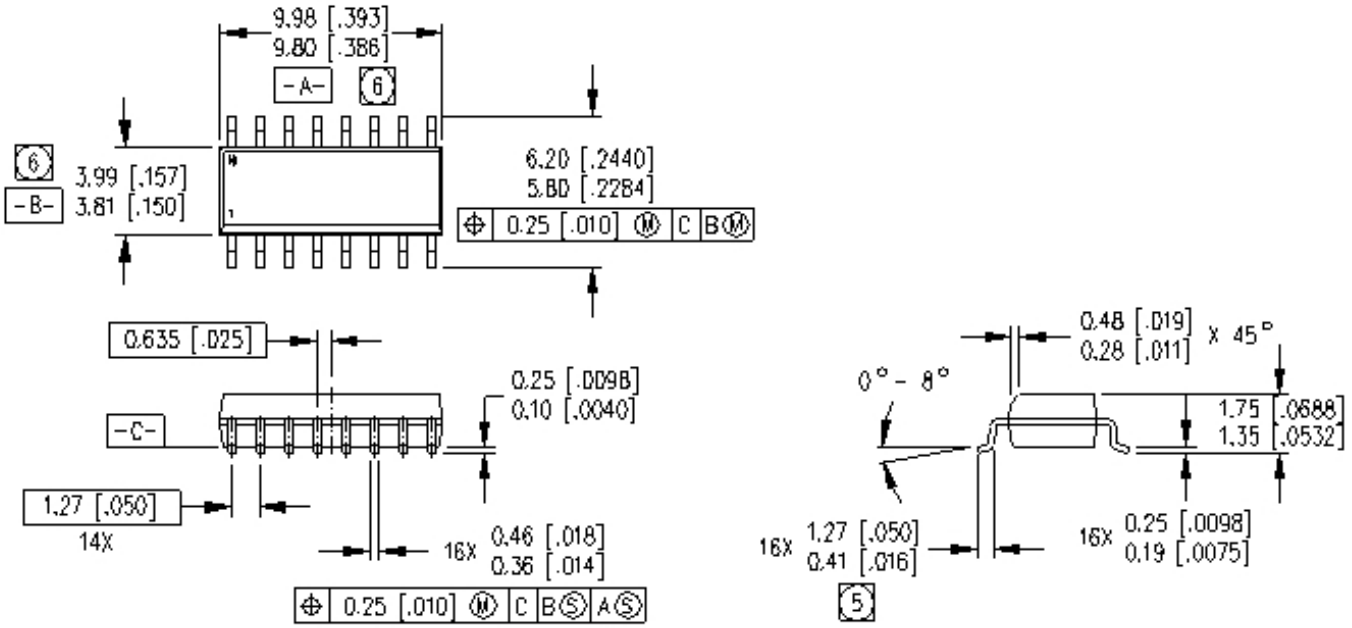
Then, total dissipation Pd is given by;

$$P_d = P_{MID} + P_{LOW} + P_{HIGH}$$

Estimated Tj from the thermal resistance between ambient and junction temperature, Rth_{JA};

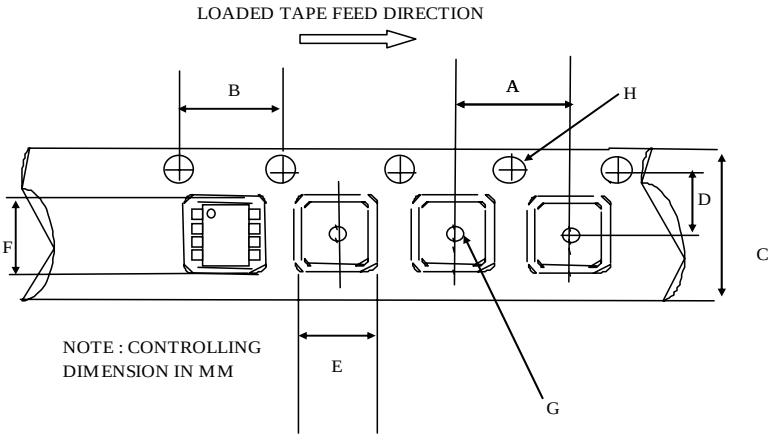
$$T_j = Rth_{JA} \cdot P_d + T_A < 150\ ^\circ C$$

Case Outline



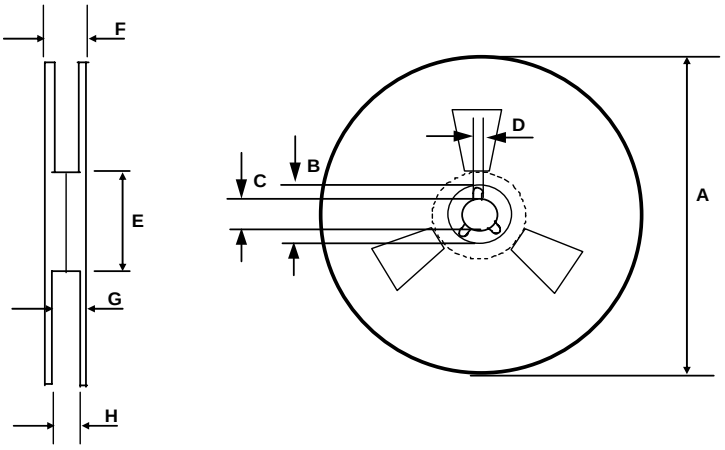
NOTES:
1. DIMENSIONING & TOLERANCING PER ANSI Y14.5W-1982
2. CONTROLLING DIMENSION. MILLIMETER
3. DIMENSIONS ARE SHOWN IN MILLIMETER [INCHES]
4. OUTLINE CONFORMS TO JEDEC OUTLINE MS-012AC
5. DIMENSION IS THE LENGTH OF LEAD FOR SOLDERING TO A SUBSTRATE
6. DIMENSION DOES NOT INCLUDE MOLD PROTUSIONS. MOLD PROTUSIONS SHALL NOT EXCEED 0.15 [.006]

16-Lead SOIC (narrow body)



CARRIER TAPE DIMENSION FOR 16SOICN

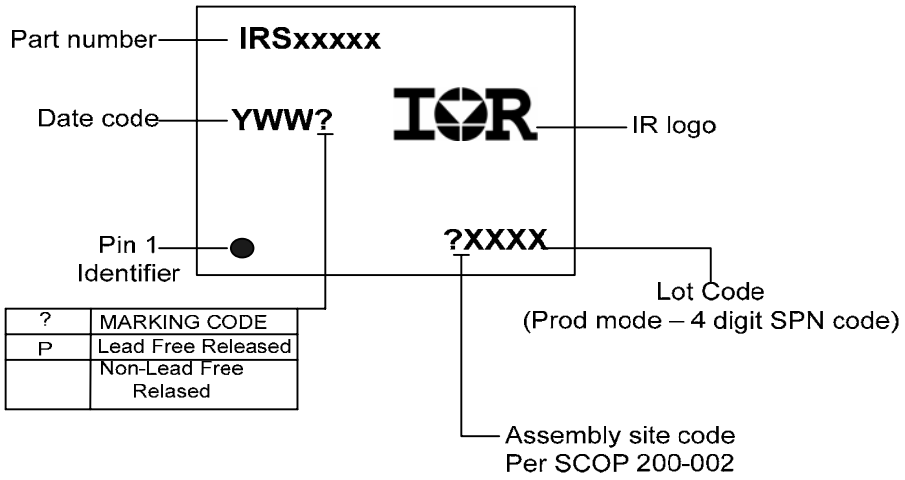
Code	Metric		Imperial	
	Min	Max	Min	Max
A	7.90	8.10	0.311	0.318
B 3.9	0	4.10	0.153	0.161
C	15.70	16.30	0.618	0.641
D	7.40	7.60	0.291	0.299
E	6.40	6.60	0.252	0.260
F	10.20	10.40	0.402	0.409
G	1.50	n/a	0.059	n/a
H	1.50	1.60	0.059	0.062



REEL DIMENSIONS FOR 16SOICN

Code	Metric		Imperial	
	Min	Max	Min	Max
A	329.60	330.25	12.976	13.001
B	20.95	21.45	0.824	0.844
C	12.80	13.20	0.503	0.519
D	1.95	2.45	0.767	0.096
E	98.00	102.00	3.858	4.015
F	n/a	22.40	n/a	0.881
G	18.50	21.10	0.728	0.830
H	16.40	18.40	0.645	0.724

LEAD-FREE PART MARKING INFORMATION



?	MARKING CODE
P	Lead Free Released
	Non-Lead Free Relased

ORDER INFORMATION

16-Lead SOIC IRS20954SPbF

16-Lead SOIC Tape & Reel IRS20954STRPbF