International
IOR Rectifier

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IRS2500S

TRANSITION MODE PFC CONTROL IC

Features

- PFC Control IC
- Boost or Flyback Converter Modes
- Critical-conduction / Transition mode operation
- Over-current protection
- Static and Dynamic DC bus overvoltage protection
- Micropower startup (<50μA)
- Low quiescent current (2.5mA)
- Latch immunity and ESD protection
- Wide range PFC for universal AC line input
- Low THD
- Open load Over voltage protection
- Noise immunity

Typical Applications

- Switched Mode Power Supplies
- Electronic Ballasts
- LED Drivers

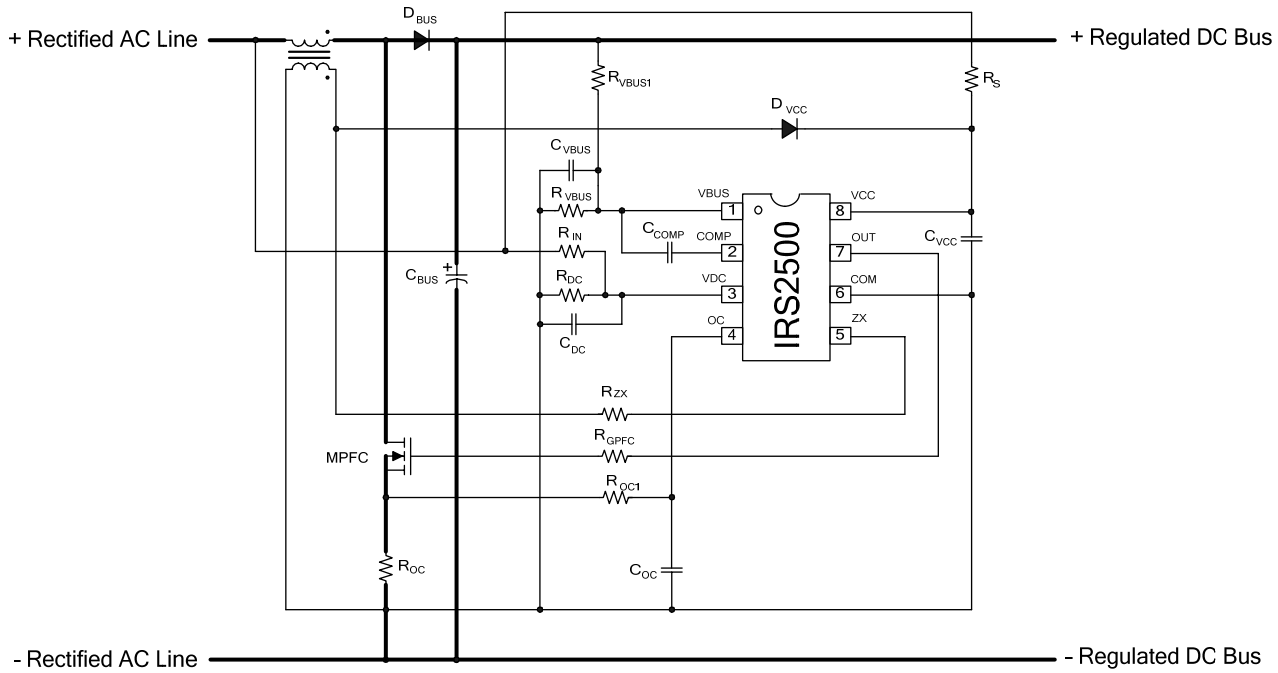
Product Summary

Topology	Boost / Flyback
I_{o+} & I_{o-} (typical)	500 / 500 mA
t_r & t_f (typical)	60 / 30 nS

Packages

8-Lead SOIC

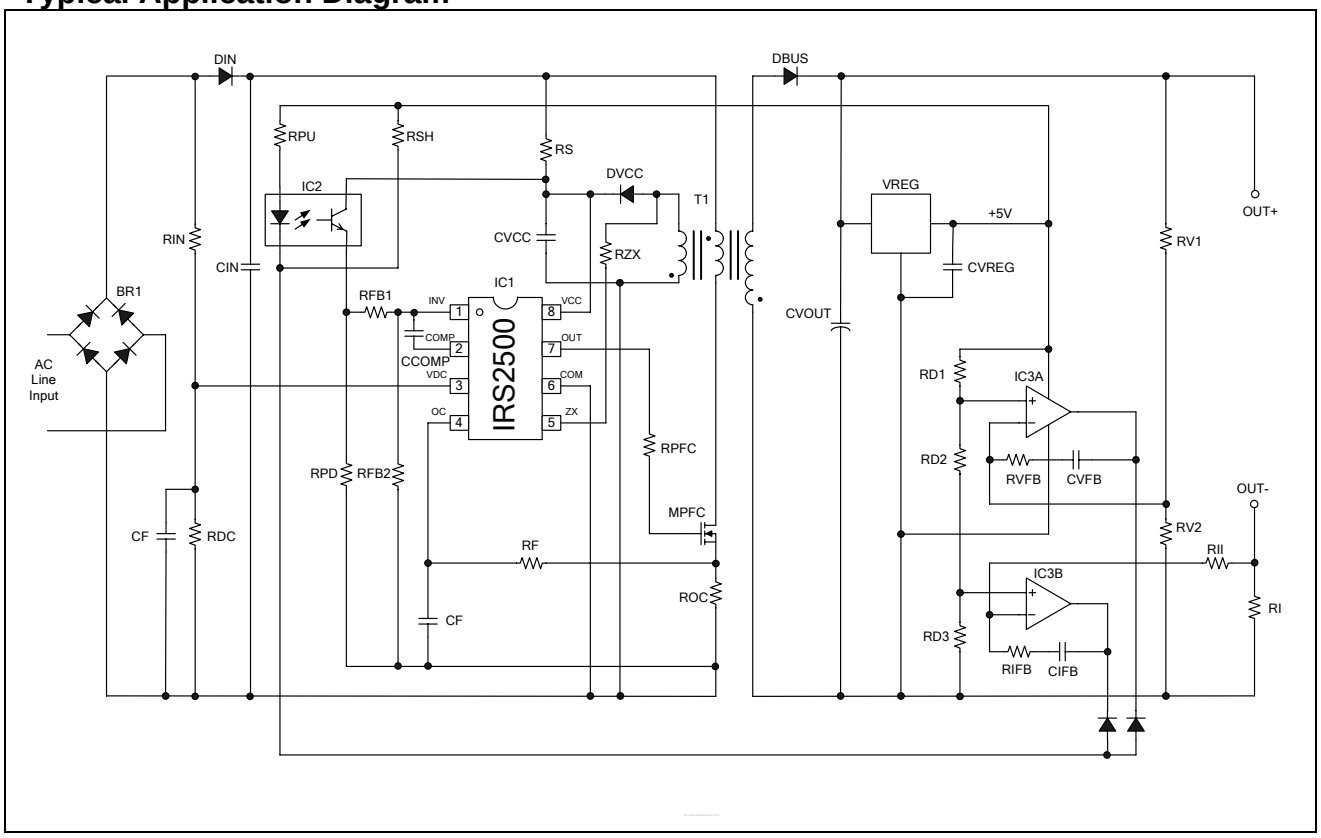
Typical Connection Diagram



Description

The IRS2500 is a fully integrated, fully protected PFC SMPS control IC designed to drive Boost or Flyback switching regulators providing high power factor. Typical applications are PFC pre-regulators for SMPS and electronic ballasts for fluorescent or HID lighting as well as single stage Flyback converters widely used in low power LED drivers. The IRS2500 is pin compatible with most industry standard critical conduction or transition mode PFC control IC with additional improvements to increase performance. The PFC circuitry provides high PF, low THD and stable DC bus regulation over a wide line/load range. The IRS2500 protection features include cycle by cycle over-current protection and output over voltage protection.

Typical Application Diagram



Qualification Information†

Qualification Level		Industrial††
		Comments: This family of ICs has passed JEDEC's Industrial qualification. IR's Consumer qualification level is granted by extension of the higher Industrial level.
Moisture Sensitivity Level		MSL2††† 260°C (per IPC/JEDEC J-STD-020)
ESD	Machine Model	Class B (per JEDEC standard JESD22-A115)
	Human Body Model	Class 2 (per EIA/JEDEC standard EIA/JESD22-A114)
IC Latch-Up Test		Class I, Level A (per JESD78)
RoHS Compliant		Yes

† Qualification standards can be found at International Rectifier's web site http://www.irf.com/

†† Higher qualification ratings may be available should the user have such requirements. Please contact your International Rectifier sales representative for further information.

††† Higher MSL ratings may be available for the specific package types listed here. Please contact your International Rectifier sales representative for further information.

Absolute Maximum Ratings

Absolute maximum ratings indicate sustained limits beyond which damage to the device may occur. All voltage parameters are absolute voltages referenced to COM, all currents are defined positive into any lead. The thermal resistance and power dissipation ratings are measured under board mounted and still air conditions.

Symbol	Definition	Min.	Max.	Units
V_{CC}	Supply Voltage†	-0.3	VCLAMP	
V_{OUT}	Gate Driver Output Voltage	-0.3	VCC + 0.3	V
I_{OMAX}	Maximum allowable output current (OUT) due to external power transistor miller effect	-500	500	mA
I_{CC}	VCC current	0	25	mA
V_{COMP}	COMP Pin Voltage	-0.3	VCC + 0.3	V
V_{OC}	OC Pin Voltage			
V_{VBUS}	VBUS Pin Voltage	-0.3	7.0	
V_{DC}	VDC Pin Voltage			
V_{ZX}	ZX Pin Voltage			
I_{COMP}	COMP Pin Current	-5	5	mA
I_{ZX}	ZX Pin Current			
I_{OC}	OC Pin Current			
P_D	Package Power Dissipation @ TA ≤ +25ºC	---	0.625	W
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient	---	128	ºC/W
T_J	Junction Temperature	-55	150	ºC
T_S	Storage Temperature	-55	150	
T_L	Lead Temperature (soldering, 10 seconds)	---	300	

Recommended Operating Conditions

For proper operation the device should be used within recommended conditions.

Symbol	Definition	Min.	Max.	Units
V_{CC}	Supply Voltage†	VCCUV+	VCLAMP	V
I_{CC}	VCC Supply Current	0	10	mA
I_{OC}	OC Pin Current	-1	1	
I_{ZX}	ZX Pin Current			
T_J	Junction Temperature	-25	125	ºC

†: This IC contains a zener clamp structure between the chip VCC and COM which has a nominal breakdown voltage of 20V. This supply pin should not be driven by a DC, low impedance power source greater than the VCLAMP specified in the Electrical Characteristics section.

Electrical Characteristics

V_{CC} = 14 V +/- 0.25 V, C_{OUT}=1000 pF, C_{VCC}=0.1 µF, T_A=25 °C unless otherwise specified.

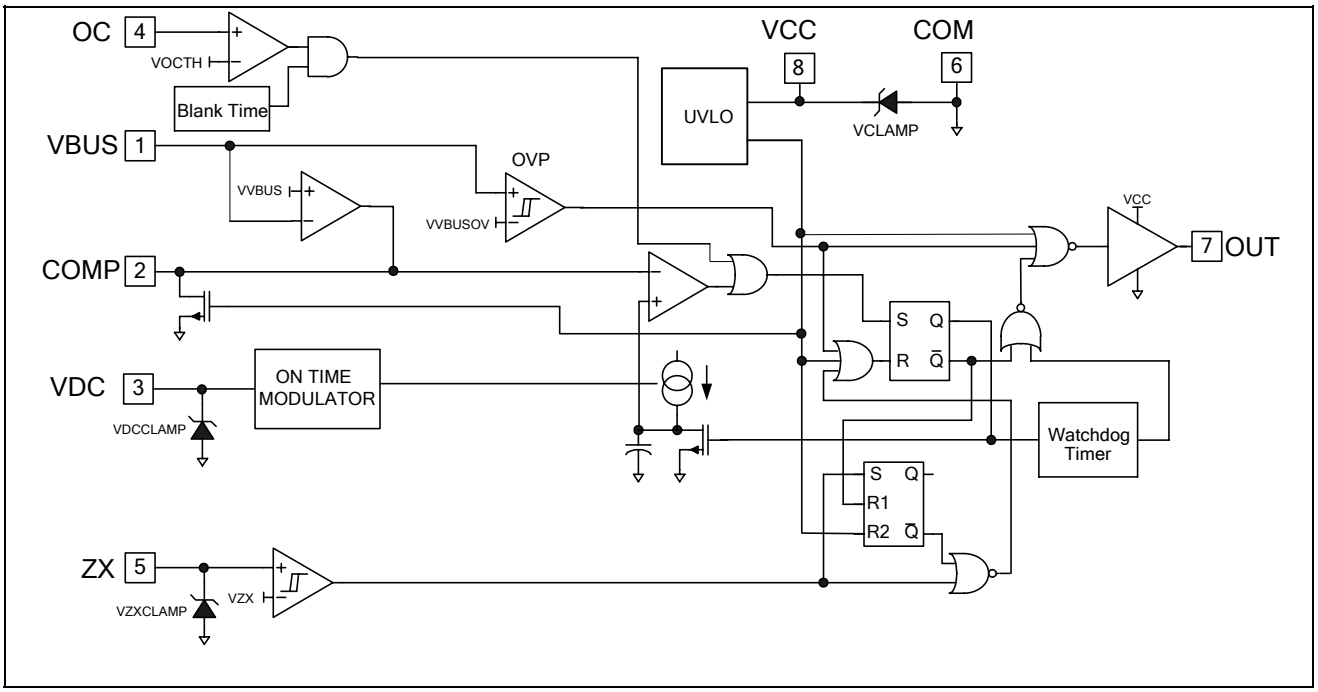
Symbol	Definition	Min	Typ	Max	Units	Test Conditions
Supply Characteristics						
VCCUV+	VCC Supply Undervoltage Positive Going Threshold	11.5	12.5	13.5		
VCCUV-	VCC Supply Undervoltage Negative Going Threshold	9.5	10.5	11.5		
VUVHYS	VCC Supply Undervoltage Lockout Hysteresis	1.5	2.0	3.0		
IQCCUV	UVLO Mode VCC Quiescent Current	---	30	---	uA	VCC = 8V
ICC	VCC Supply Current	---	2.3	5.0	mA	VBUS=2.5V PFC off time = 5us
VCLAMP	VCC Zener Clamp Voltage	---	20.0	---	V	ICC = 10mA
Error Amplifier Characteristics						
ICOMP SOURCE	COMP Pin Error Amplifier Output Current Sourcing	---	10	---	mA	VVBUS = 2.4V VCOMP=4.0V
ICOMP SINK	COMP Pin Error Amplifier Output Current Sinking	---	-23	---		VVBUS = 2.6V VCOMP=4.0V
VCOMPOH	Error Amplifier Output Voltage Swing (high state)	---	6.0	---	V	VBUS=2.0V ICOMP=-0.5mA
VCOMPOL	Error Amplifier Output Voltage Swing (low state)	---	0.25	---		VBUS=3.0V ICOMP=+0.5mA
VCOMPFLT	Error Amplifier Output Voltage in Fault Mode	---	0	---		VBUS=3.0V
IVBUS	Input bias current	---	---	-1	uA	VBUS=0 to 3V
Gv	Voltage gain	60	80	---	dB	Open loop
GB	Bandwidth	---	1	---	MHz	
Control Characteristics						
VVBUS	VBUS Internal Reference Voltage	2.46	2.5	2.54	V	VCOMP = 4.0V
VZX+	ZX Pin Threshold Voltage (Arm)	---	1.6	---		
VZX-	ZX Pin Threshold Voltage (Trigger)	---	0.7	---		
VZXclamp	ZX pin Clamp Voltage (high state)	---	5.2	---		IZX = 1mA
VDCclamp	VDC pin Clamp Voltage	---	5.2	---		IDC = 1mA
tBLANK	OC pin current-sensing blank time	---	320	---	ns	VBUS=2.5V VCOMP=4.0V
tWD	PFC Watch-dog Pulse Interval	---	400	---	us	ZX = 0,VCOMP = 4.0V
tONMIN	PFC Minimum ON time	---	0.3	---	us	ZX = 0,VCOMP = 0.25V
tONMAX	PFC Maximum ON Time	10	50	---	us	ZX = 0,VCOMP = 6.0V, VDC = 2V

Electrical Characteristics (cont'd)

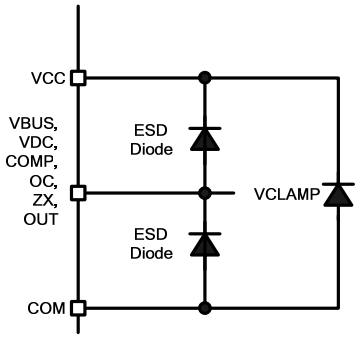
VCC = 14V +/- 0.25V, COUT = 1000pF,
VCOMP = VOC = VBUS = VZX = 0V, T_A=25C unless otherwise specified.

Protection Circuitry Characteristics						
VOCTH	OC Pin Over-current Sense Threshold	0.93	1.1	1.22	V	
VVBUSOV	VBUS Over-voltage Comparator Threshold		2.7			Guaranteed by design
VVBUSOV HYS	VBUS Over-voltage Comparator Hysteresis	50	100	150	mV	Guaranteed by design
ICOMPOV+	Dynamic Over-voltage detection threshold		30		uA	
ICOMPOV-	Dynamic Over-voltage detection reset		8			
Gate Driver Output Characteristics						
VOL	Low-Level Output Voltage	---	0	100	mV	IO = 0
VOH	High-Level Output Voltage	---	0	11	V	IO = 0
t_r	Turn-On Rise Time	---	60	110	ns	
t_f	Turn-Off Fall Time	---	30	70		
I0+	Source Current	---	500	---	mA	
I0-	Sink Current	---	500	---		

Functional Block Diagram



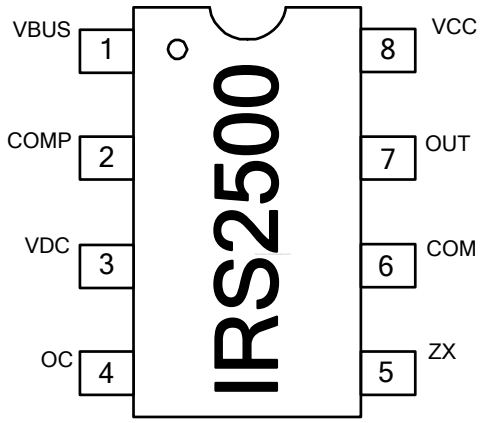
Input/Output Pin Equivalent Circuit Diagrams



Lead Definitions

Symbol	Description
VBUS	DC Bus Sensing Input
COMP	PFC Error Amplifier Compensation
VDC	Full Wave Voltage Input
OC	PFC Current Sensing Input
ZX	PFC Zero-Crossing Detection
COM	IC Power & Signal Ground
OUT	Gate Drive Output
VCC	Logic & Low-Side Gate Driver Supply

Lead Assignments



Application Information and Additional Details

Power factor correction is required in many electrical appliances in order to minimize reactive current losses in AC power transmission lines. The degree to which an electronic circuit matches an ideal purely resistive load is measured by the phase shift (displacement) between the input voltage and input current and the amount of current waveform distortion. In other words how well the shape of the input current waveform matches the shape of the sinusoidal input voltage.

The power factor (PF) is defined as the ratio between real power and apparent power with the maximum value of 1.0 representing a totally resistive load where the current waveform shape matches the voltage waveform shape exactly. The distortion of the input current waveform is quantified by the *total harmonic distortion* (THD), which is the sum of all harmonic content of the waveform expressed as a percentage.

An ideal power factor of 1.0 corresponds to zero phase shift and a THD of 0% representing a purely sinusoidal input current waveform in phase with the line voltage. The lower the power factor the more current is needed to supply the same power to the load, which results is higher conduction losses in transmission lines. For this reason it is desirable to have a high PF and a low THD. To achieve this, the IRS2500 implements an active power factor correction (PFC) circuit.

The control method implemented in the IRS2500 may be used in a Boost converter (Figure 8) or a low power single stage Flyback converter for small power supplies or LED drivers. The IRS2500 operates in critical-conduction mode (CrCM), also known as transition mode. This means that during each switching cycle of the PFC MOSFET, the circuit waits until the inductor current discharges to zero before turning the PFC MOSFET on again. The PFC MOSFET is turned on and off at a much higher frequency (>10KHz) than the line input frequency (50 to 60Hz).

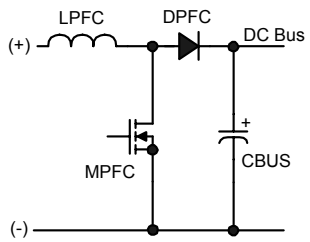


Figure 8: Boost converter circuit.

When the switch MPFC is turned on, the inductor LPFC is connected between the rectified line input (+) and (-) causing the current in LPFC to increase linearly. When MPFC is turned off, LPFC is connected between the rectified line input (+) and the DC bus capacitor CBUS through diode DPFC. The stored energy in LPFC is transferred to the output, supplying a current into CBUS. MPFC is turned on and off at a high frequency and the voltage on CBUS charges up to a specified voltage. The voltage feedback loop of the IRS2500 regulates the output to the desired voltage by continuously monitoring the DC output and adjusting the on-time of MPFC accordingly. If the output voltage is too high, the on-time is decreased and if it is too low, the on-time is increased. This negative feedback control loop operates with a slow loop speed and a low loop gain such that the average inductor current smoothly follows the low-frequency line input voltage to obtain high power factor and low THD.

The loop speed is intentionally slow with respect to the AC line frequency so that there is no appreciable change in the on time during a single line half cycle. This allows the current to follow shape of the sinusoidal voltage.

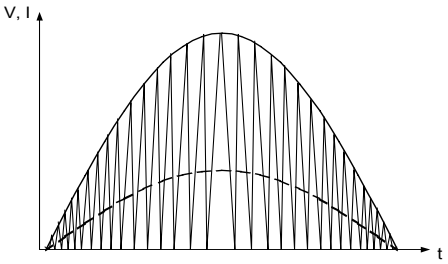


Figure 9: Sinusoidal line input voltage (solid line), triangular PFC Inductor current and smoothed sinusoidal line input current (dashed line) over one half-cycle of the AC line input voltage**.**

Corrections to the output voltage therefore require several line cycles. With a fixed on-time, and an off-time determined by the inductor current discharging to zero, the result is a system where the switching frequency is free-running and constantly changing from a high frequency near the zero crossing of the AC input line voltage, to a lower frequency at the peaks (Figure 9).

When the line input voltage is low (near the zero crossing), the inductor current will increase only a small amount and the discharge time will be short resulting in a high switching frequency. When the input line voltage is high (near the peak), the inductor current will charge up to a much higher

level and the discharge time will be longer giving a lower switching frequency.

The PFC control circuit of the IRS2500 (Figure 10) includes six control pins: VBUS, COMP, ZX, OUT, VDC and OC. The VBUS pin measures the DC bus voltage through an external resistor voltage divider. The COMP pin voltage determines the on-time of MPFC and sets the feedback loop response speed with an external RC integrator. The ZX pin detects when the inductor current discharges to zero each switching cycle using a secondary winding from the PFC inductor. The OUT pin is the low-side gate driver output for the external MOSFET, MPFC. The VDC pin senses the line input cycle providing phase information to control the on time modulation described in the next section. The OC pin senses the current flowing through MPFC and performs cycle-by-cycle over-current protection.

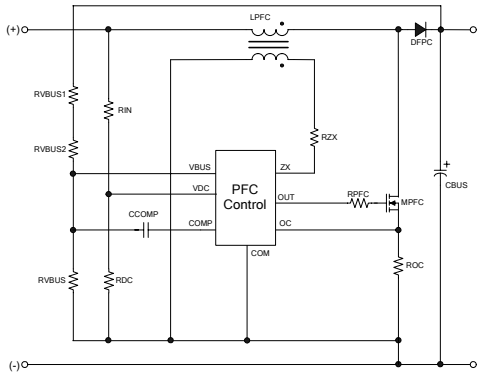


Figure 10: IRS2500 simplified PFC control circuit.

The VBUS pin is compared with a fixed internal 2.5V reference voltage for regulating the DC output voltage (Figure 11). The feedback loop error amplifier increases or decreases the COMP pin voltage. The resulting voltage on the COMP pin sets the threshold for the charging of the internal timing capacitor (C1, Figure 11) and therefore determines the on-time of MPFC.

The error amplifier operates at a slow loop speed preventing rapid changes in PWM duty cycle during a single input line cycle. This prevents distortion achieving high power factor and low THD.

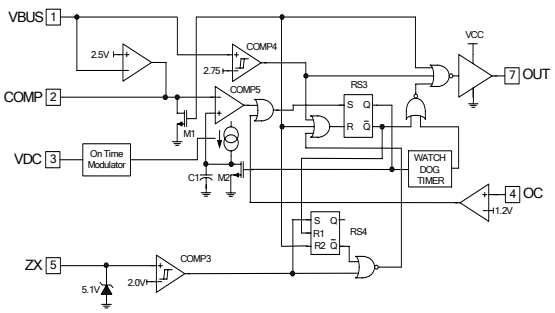


Figure 11: IRS2500 detailed PFC control circuit.

The off-time of MPFC is determined by the time it takes the LPFC current to discharge to zero. The zero current level is detected by a secondary winding on LPFC that is connected to the ZX pin through an external current limiting resistor RZX. A positive-going edge exceeding the internal threshold VZX+ signals the beginning of the off-time. A negative-going edge on the ZX pin falling below VZX- will occur when the LPFC current discharges to zero, which signals the end of the off-time and MPFC is turned on again (Figure 12). The ZX pin is internally biased to ensure that the voltage detected from the inductor drops fully to zero before triggering the next PWM cycle. A wide hysteresis prevents false triggering by ringing oscillations.

The cycle repeats itself indefinitely until the IRS2500 is disabled through an over-voltage condition on the DC bus or if the negative transition of ZX pin voltage does not occur. Should the negative edge on the ZX pin not occur, MPFC will remain off until the watch-dog timer forces a turn-on of MPFC for an on-time duration programmed by the voltage on the COMP pin. The watch-dog pulses occur every 300-400us (tWD) indefinitely until a correct positive and negative-going signal is detected at the ZX pin and normal operation is resumed. Should the OC pin voltage exceed the VOCTH over-current threshold during the on-time the gate drive output will turn off. The circuit will then wait for a negative-going transition on the ZX pin or a forced turn-on from the watch-dog timer to turn the output on again.

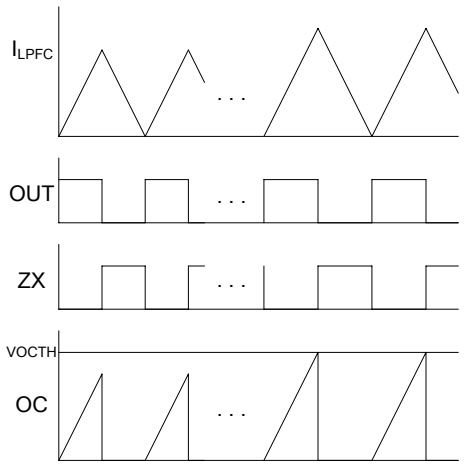


Figure 12: Inductor current, OUT pin, ZX pin and OC pin timing diagram.

On-time Modulation Circuit

A fixed on-time of MPFC over an entire cycle of the line input voltage produces a peak inductor current which naturally follows the sinusoidal shape of the line input voltage. The smoothed, averaged line input current is in phase with the line input voltage for high power factor but a high total harmonic distortion (THD), as well as individual higher harmonics, of the current are still possible. This is mostly due to cross-over distortion of the line current near the zero-crossings of the line input voltage. To achieve low harmonics that are acceptable for compliance with international standards and general market requirements, an additional on-time modulation circuit has been added to the PFC control. This circuit dynamically increases the on-time of MPFC as the line input voltage nears the zero-crossings (Figure 13). This causes the peak LPFC current, and therefore the smoothed line input current, to increase near the zero-crossings of the line input voltage. This reduces the amount of cross-over distortion in the line input current which reduces the THD and higher harmonics. The on time modulation function is controlled via the VDC input. The full wave rectified voltage from the bridge rectifier is divided down by RIN and RDC to provide an input with a peak voltage of approximately 1V at 90VAC input and 3V at 277VAC. CDC is added to remove noise from the signal, the value is typically 10nF. The on time modulation function is not required in some applications. In such cases the VDC input should be tied to VCC through a 10K resistor.

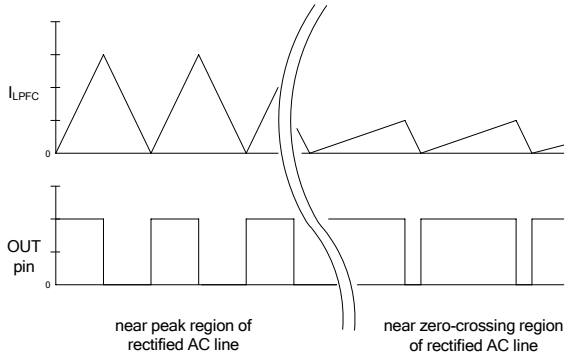


Figure 13: On-time modulation circuit timing diagram.

Output Over-voltage Protection

The IRS2500 incorporates both static and dynamic overvoltage protection. Static over voltage protection monitors the feedback voltage at the VBUS pin and disables the gate drive output if this voltage exceeds the target voltage by 8%. This is activated by an internal comparator set to detect a threshold of 2.7V, which is 8% above the regulation threshold of 2.5V.
However, under startup condition or when a load is removed from the output the error amplifier output voltage at the COMP pin swings low. Since the compensation capacitor CCOMP is connected from this output back to the VBUS input a current will flow during the COMP voltage transition. This pulls down the VBUS voltage, which allows the output voltage to exceed the desired regulation level during the transition and results in an overshoot before the voltage at the VBUS input exceeds the regulation threshold.
In order to compensate for this effect, the IRS2500 includes dynamic detection of the error amplifier output current. During a swing in the negative direction the error amplifier output current peaks at a much high level than the level during steady state operation. This higher current is internally detected and triggers the overvoltage protection circuitry disabling the PWM output until the error amplifier output has settled to a new level. This prevents the output voltage from overshooting the desired level by a significant amount under the transient conditions described. For this reason the loop should be designed such that voltage ripple at COMP is minimized during steady state operation.

PCB Layout Guidelines

For correct operation of the IRS2500, the PCB should be designed to avoid noise coupling to the control inputs and ground loops. By following the recommendations listed here potential issues will be avoided:

1. The circuit signal and power grounds should be joined together at one point only. The signal ground should be a star point located close to the COM pin of the IRS2500.

2. The point at which the signal ground is connected to the power ground is recommended to be at the current sense resistor (ROC) ground.

3. A 0.1µF noise decoupling capacitor should be located between the VCC and COM pins of the IRS2500 located as close to the IC as possible.

4. All traces to the VBUS input should be as short as possible. This means that resistors and capacitors that are connected to this input should be located as close to the IRS2500 as possible. The voltage feedback divider resistor connected to COM should be connected to a signal ground close to the COM pin.

5. Traces carrying high voltage switching signals such as those connected to the MOSFET drain or gate drive signals should not be located close to traces connected directly to the VBUS input.

6. The divider network resistor (RDC) and filter capacitor (CDC) connected to the VDC input of the IRS2500 should be located as closely to the IC as possible with the grounded end connected to the circuit signal ground.

7. The compensation capacitor CCOMP should be located close to the IRS2500 with short traces leading to the VBUS and COMP pins.

8. The over current detection filter resistor (ROC) and capacitor (COC) should be located as close to the IRS2500 as possible with COC connected to the circuit signal ground.

9. The zero crossing detection resistor should be located close to the IRS2500 if possible to prevent possible noise appearing at this input.

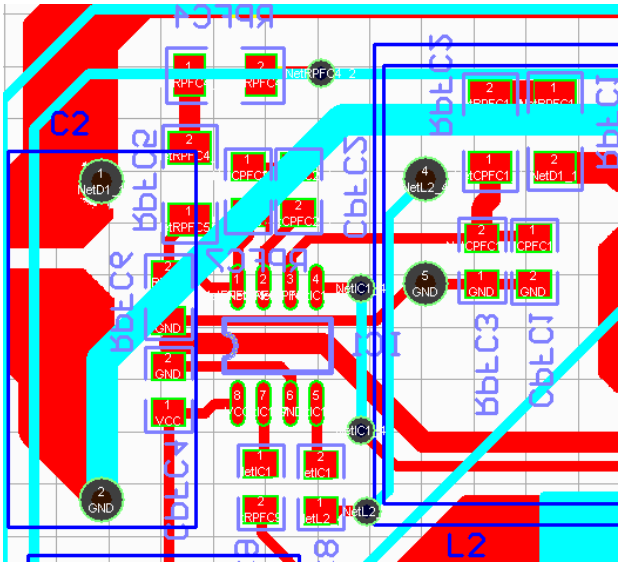


Figure 14: Layout Example

Figure 14 shows a layout where the IRS2500 is located on the bottom side of the PCB. The bottom side traces are shown in red and the top side traces in pale blue. The circuit power ground can be seen at the C2 GND node with the signal ground star point is located at the junction between RPFC6 and CPFC4 to the left of the IRS2500 (IC1). (Note that the component designators in this example are different from those used in the datasheet schematics)
The traces from IC1 pin 6, RPFC3 and CPFC1 (the VDC divider low side) all run directly to the star point without crossing any other grounds. The signal ground is connected to the power ground at the current sense resistor. A large trace can be seen running from the star point off the left to where the MOSFET is situated (not shown). This is the single point where the signal and power grounds are connected. The VCC supply decoupling capacitor shown in this example is CPFC4, which is located very close to the IRS2500 and grounded directly to the signal ground star point.
Traces leading to pin 1 (VBUS) are all short and components connected to pin 1 (RPFC5, RPFC6 and RPFC7) are all located close to IC1. There are no traces connected to high voltage switching nodes located anywhere close to pin 1.
The board layout shown in figure 14 complies with all of the guidelines stated enabling optimum operation of the IRS2500.

PFC Design Equations (for Boost Converter)

Step1: Calculate PFC inductor value:

$$L_{PFC} = \frac{(VBUS - \sqrt{2} \cdot VAC_{MIN}) \cdot VAC_{MIN}^2 \cdot \eta}{2 \cdot f_{MIN} \cdot P_{OUT} \cdot VBUS} \quad \text{[Henries]} \quad (1)$$

where,

$VBUS$ = DC bus voltage
VAC_{MIN} = Minimum rms AC input voltage
η = PFC efficiency (typically 0.95)
f_{MIN} = Minimum PFC switching frequency at minimum AC input voltage
P_{OUT} = Ballast output power

Step 2: Calculate peak PFC inductor current:

$$i_{PK} = \frac{2 \cdot \sqrt{2} \cdot P_{OUT}}{VAC_{MIN} \cdot \eta} \quad \text{[Amps Peak]} \quad (2)$$

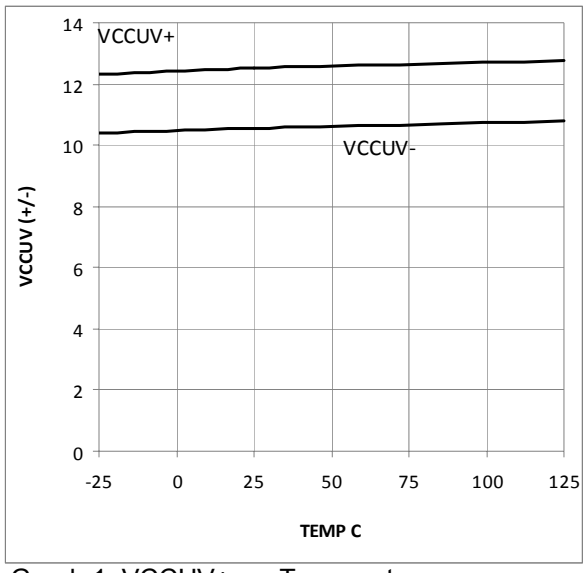
Note: The PFC inductor must not saturate at i_{PK} over the specified ballast operating temperature range. Proper core sizing and air-gapping should be considered in the inductor design.

Step 3: Calculate PFC over-current resistor ROC value:

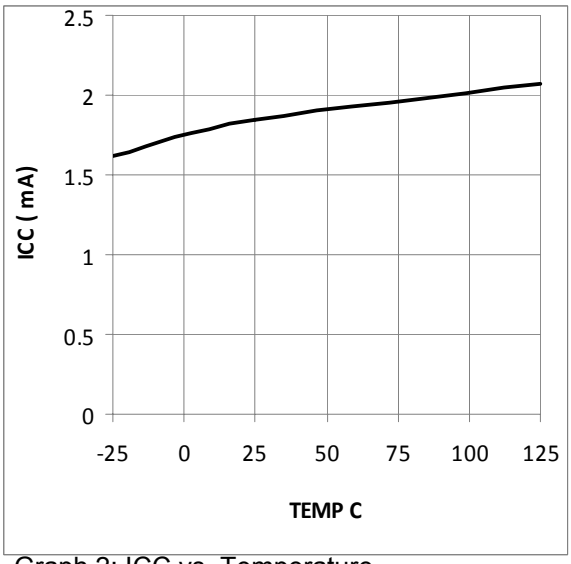
$$R_{OC} = \frac{VOCTH}{i_{PK}} \quad \text{where VOCTH = 1.1V} \quad \text{[Ohms]} \quad (3)$$

Step 4: Calculate start-up resistor RVCC value:

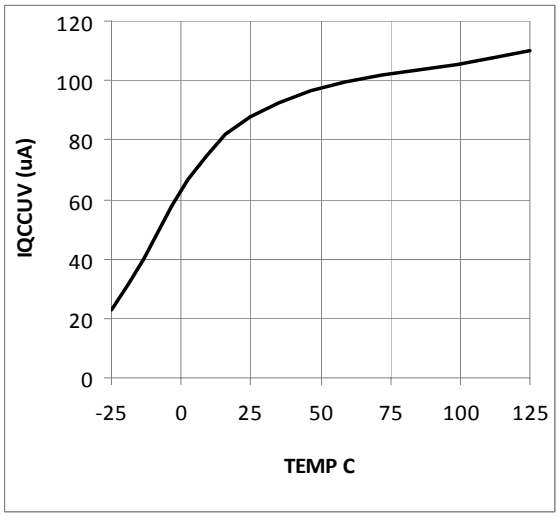
$$R_{VCC} = \frac{VAC_{MIN\ PK} + 10}{IQCCUV} \quad \text{[Ohms]} \quad (4)$$



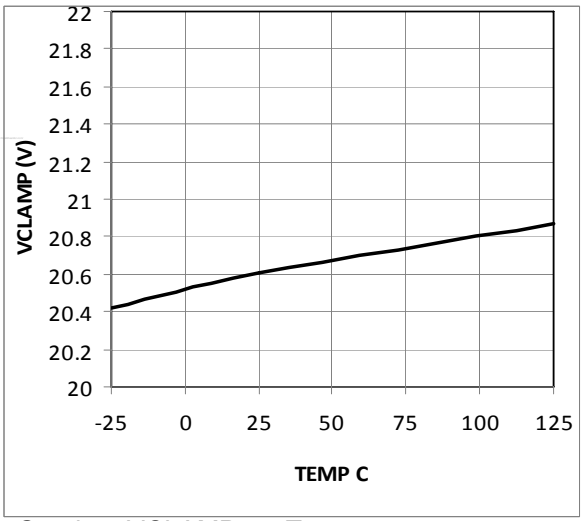
Graph 1: VCCUV+ vs. Temperature



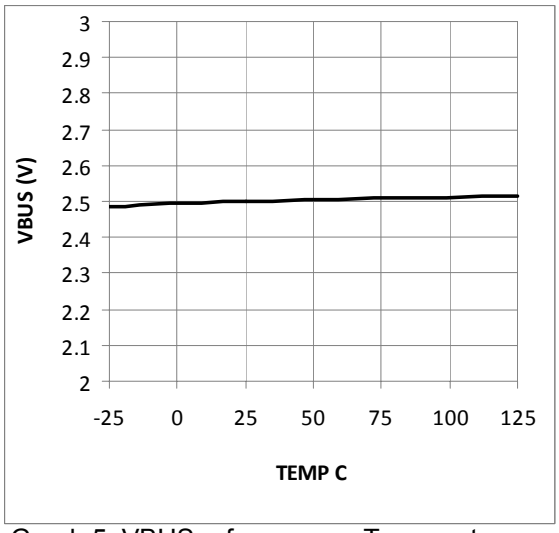
Graph 2: ICC vs. Temperature



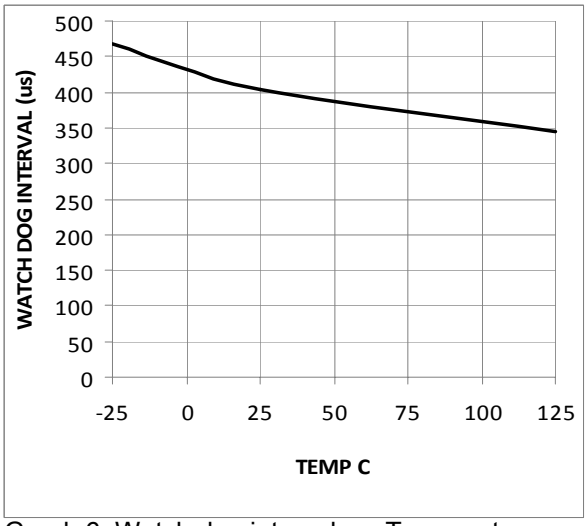
Graph 3: IQCCUV vs. Temperature



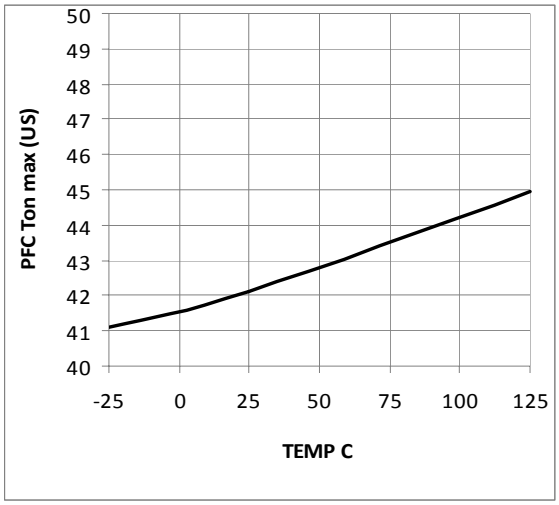
Graph 4: VCLAMP vs. Temperature



Graph 5: VBUS reference vs. Temperature

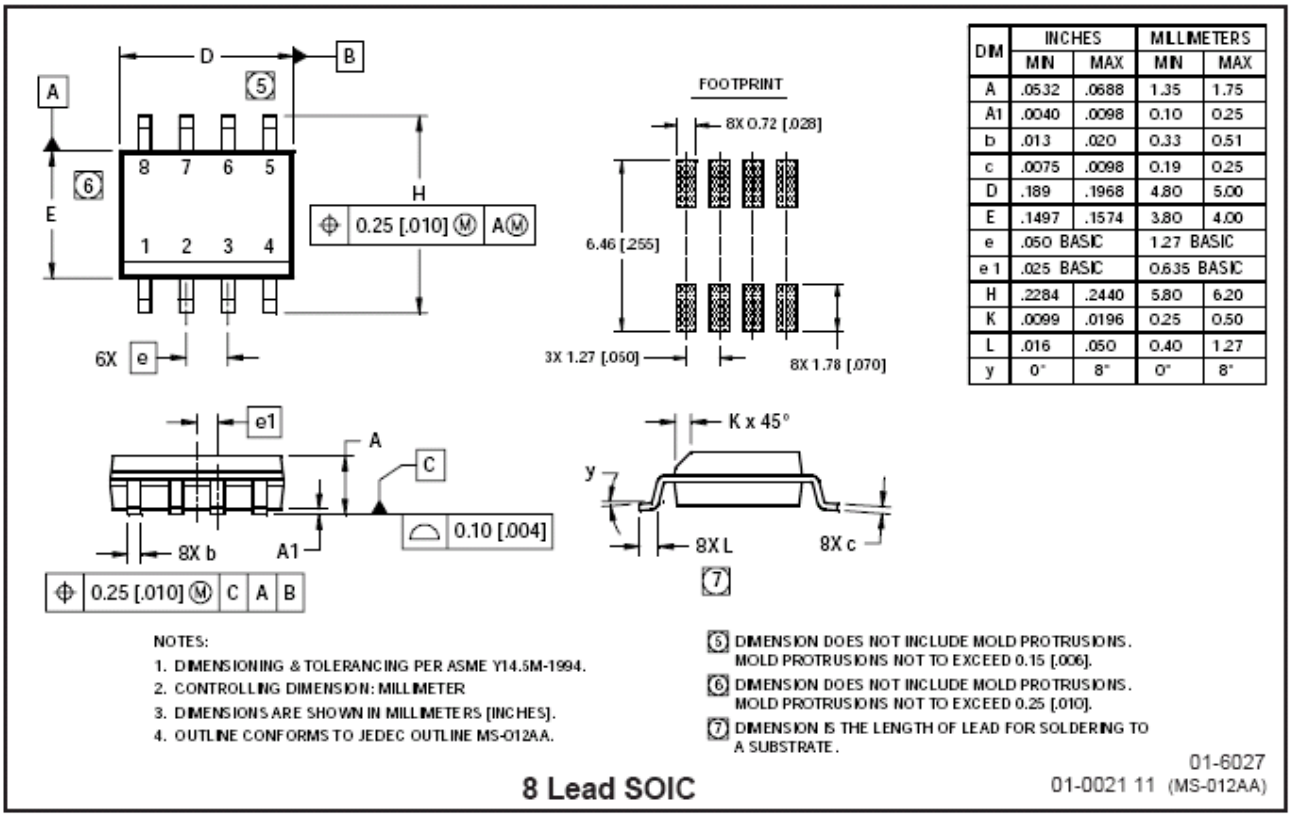


Graph 6: Watch dog interval vs. Temperature



Graph 7: PFC Ton max (us)

Package Details



DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	.0532	.0688	1.35	1.75
A1	.0040	.0098	0.10	0.25
b	.013	.020	0.33	0.51
c	.0075	.0098	0.19	0.25
D	.189	.1968	4.80	5.00
E	.1497	.1574	3.80	4.00
e	.050 BASIC		1.27 BASIC	
e1	.025 BASIC		0.635 BASIC	
H	.2284	.2440	5.80	6.20
K	.0099	.0196	0.25	0.50
L	.016	.050	0.40	1.27
y	0°	8°	0°	8°

NOTES:
1. DIMENSIONING & TOLERANCING PER ASME Y14.5M-1994.
2. CONTROLLING DIMENSION: MILLIMETER
3. DIMENSIONS ARE SHOWN IN MILLIMETERS [INCHES].
4. OUTLINE CONFORMS TO JEDEC OUTLINE MS-012AA.

5 DIMENSION DOES NOT INCLUDE MOLD PROTRUSIONS. MOLD PROTRUSIONS NOT TO EXCEED 0.15 [.006].

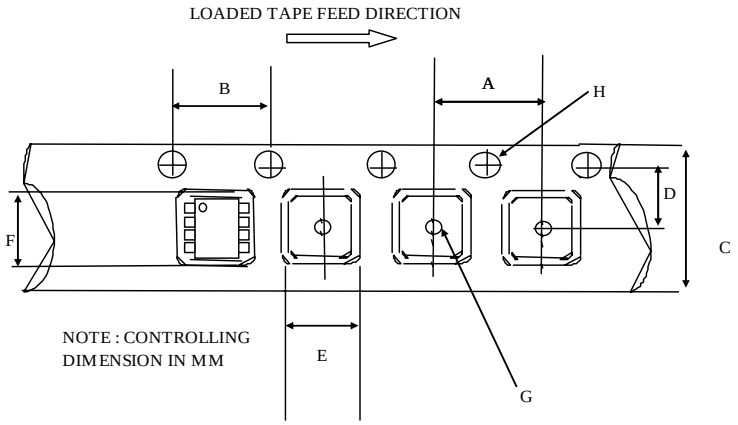
6 DIMENSION DOES NOT INCLUDE MOLD PROTRUSIONS. MOLD PROTRUSIONS NOT TO EXCEED 0.25 [.010].

7 DIMENSION IS THE LENGTH OF LEAD FOR SOLDERING TO A SUBSTRATE.

01-6027
01-0021 11 (MS-012AA)

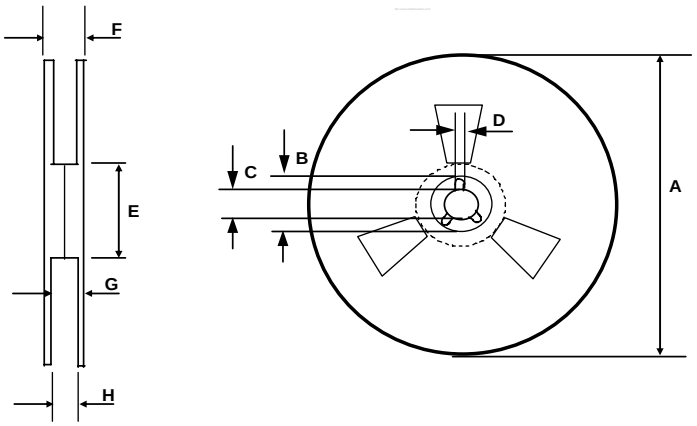
8 Lead SOIC

Tape and Reel Details



CARRIER TAPE DIMENSION FOR 8SOICN

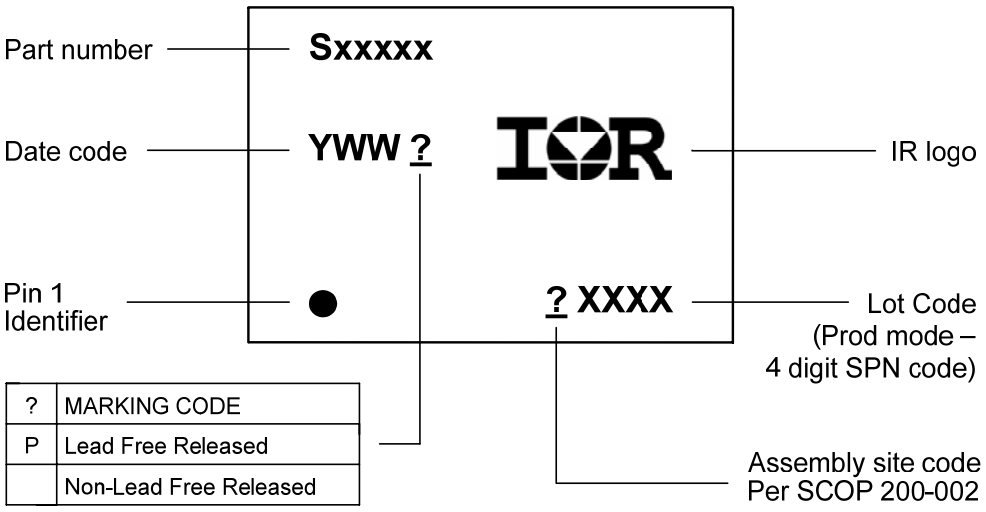
Code	Metric		Imperial	
	Min	Max	Min	Max
A	7.90	8.10	0.311	0.318
B	3.90	4.10	0.153	0.161
C	11.70	12.30	0.46	0.484
D	5.45	5.55	0.214	0.218
E	6.30	6.50	0.248	0.255
F	5.10	5.30	0.200	0.208
G	1.50	n/a	0.059	n/a
H	1.50	1.60	0.059	0.062



REEL DIMENSIONS FOR 8SOICN

Code	Metric		Imperial	
	Min	Max	Min	Max
A	329.60	330.25	12.976	13.001
B	20.95	21.45	0.824	0.844
C	12.80	13.20	0.503	0.519
D	1.95	2.45	0.767	0.096
E	98.00	102.00	3.858	4.015
F	n/a	18.40	n/a	0.724
G	14.50	17.10	0.570	0.673
H	12.40	14.40	0.488	0.566

Part Marking Information



?	MARKING CODE
P	Lead Free Released
	Non-Lead Free Released

Ordering Information

Base Part Number	Package Type	Standard Pack		Complete Part Number
		Form	Quantity	
IRS2500	SOIC8	Tube/Bulk	95	IRS2500SPBF
		Tape and Reel	2500	IRS2500STRPBF

For technical support, please contact IR's Technical Assistance Center
http://www.irf.com/technical-info/

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