GENERAL DESCRIPTION

The IS1636N is an integrated monolithic chip for Bluetooth mono headset application. It is a single-chip, Bluetooth v2.0 + EDR baseband with an integrated transceiver.

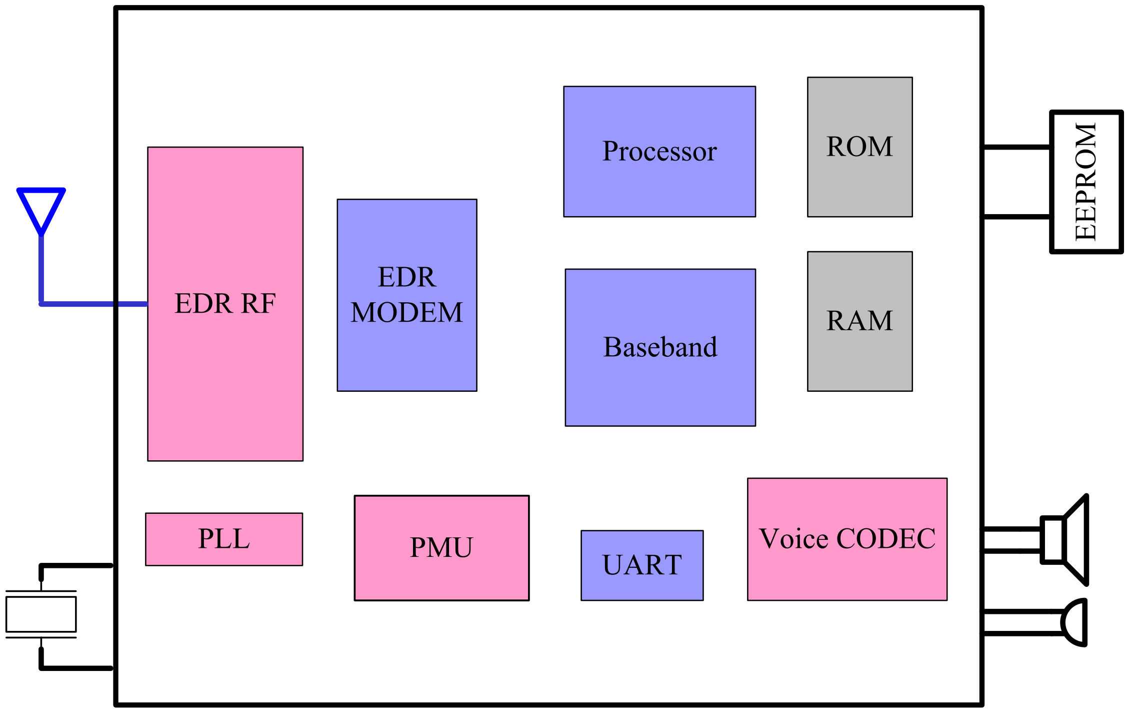
The IS1636N integrates most external components for a mono headset including voice codec, Li-Ion battery charger, and one low drop regulator. The reductions of external components can be used for a tiny headset easily.

A new voice manage structure achieve lower noise level and higher signal level. This implementation improves the audio quality to fit human's vocal experience and keep audio quality even under terrible environment.

FEATURES

- Bluetooth v2.0 + EDR which is backward-compatible with BT1.1 and 1.2.
- Programmable output power control meets specific requirements
- A lowest eBOM in the current market at such power consumption
- Integrated Power Manager Unit (PMU) that can charge a Li-ion battery, LED driver and switching regulator
- Better audio quality
- Capable charging voltage from a zero battery, and sustain direct DC input for adaptor from 4.8V ~ 6.5 V
- Support standard HCI commands for test requirements
  Standard QFN 48 package that size is only 7x7 mm2

Figure 1: Functional Block Diagram



Contents

1 Features

System Specification

- Bluetooth Specification v.2.0 with EDR in 2.4 GHz ISM band
- Both BDR and EDR eSCO supported.
- Main input clock of 16MHz frequency
- Full Bluetooth RF Interface & Lower Link Controller functions
- Support 64 kb/s PCM format (A-Law or µ-Law), or CVSD (Continuous Variable Slope Delta Modulation) for SCO channel operation.

RF Hardware

- Combined TX/RX RF terminal simplifies external matching and reduces external antenna switches.
- +2dBm output power with level control.
- For Class2/3, transmitter support without the requirement for external power amplifier or TR switch at the same time..
- Fully integrated synthesizer has been created. There requires no external VCO, varactor diode, resonator and loop filter.
- Crystal oscillation with build-in digital trimming for temperature/process variations.
- Fully support for power saving mode includes Park, Hold and Sniff

Power Manager Unit

- Battery protection features including over voltage and under voltage protect.
- A Li-ion poly-battery charging features with adjustable charging current
- Internal Low Drop Regulator (LDO) that can eliminate the external coil inductor
- Voltage Detection circuit is used for battery monitoring in portable applications

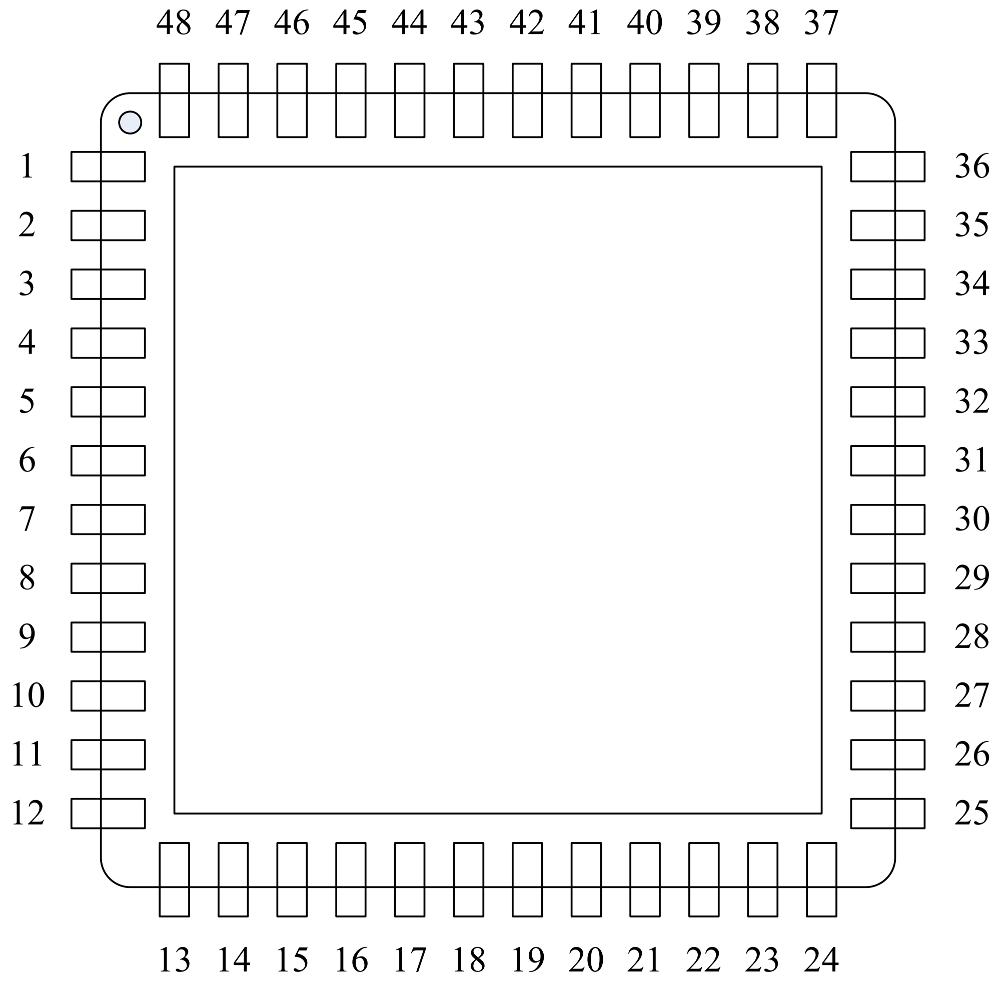
Flexible HCI interface

- An embedded UART (Universal Asynchronous Receiver Transmitter) is included in this chip that support HCI-UART I/O interface
- Standard Bluetooth HCI test commands sets

Package

- QFN 48 standard package

2 Pin Assignments and Signal Descriptions



Pin No.	I/O	Pin Name	Pin Descriptions
1	O	LOUT+	Differential audio output (+). 1.6Vp-p maximum differential output used in conjunction with LINE_OUT-. DC offset relative to ground typically 0.85V. Output impedance of 20~30 ohms, with 1K ohm minimum load.
2	O	LOUT-	Differential audio output (-). 1.6Vp-p maximum differential output used in conjunction with LINE_OUT+. DC offset relative to ground typically 0.85V. Output impedance of 20~30 ohms, with 1K ohm minimum load.
3	—	AGND	Analog ground for audio CODEC. Connect to common ground.
4	—	VDD_CORE	Digital core logic power. Connect to 1.8V supply.
5	—	GND	Digital Ground. Connect to common ground.
6	—	VDD_IO	Digital I/O Power. Connect to 1.8V supply.
7	I	RST_N	External reset signal input
8	I	MFB	Multi-Function Button for 4 keys setting. It’s active when receive a LOW level signal.
9	—	LED1	LED1 sinking point.
10	—	LED0	LED0 sinking point.
11	I	PowerKey	Power enables input and the Multi-Function Button as the default setting.
12	—	BK18_O	Buck 1.8V output.
13	—	BK_GND	Buck ground.
14	—	BK_LX	Internal switch output for Buck converter.
15	—	BK_IN	Buck 1.8V input. Connect to SYS_PW directly.
16	—	SYS_PW	Internal system power output
17	—	VDD_SAR	SAR 1.8V input power
18	AI	BAT_IN	A Li-ion battery positive input point
19	AI	ADP_IN	A DC adaptor positive input point
20	—	VDD_CORE	Digital core logic power. Connect to 1.8V supply.
21	I	HCI_RXD	HCI UART Serial Port Receive Data.
22	O	HCI_TXD	HCI UART Serial Port Transmit Data.
23	—	NC	NC
24	—	GND	Digital Ground. Connect to common ground.
25	I	TEST	Test mode by configure it LOW.

Pin No.	I/O	Pin Name	Pin Descriptions
26	I	VOL-	General purpose I/O, Volume Down key as the default setting. It's active when receive a LOW level signal.
27	I	VOL+	General purpose I/O, Volume Up key as the default setting. It's active when receive a LOW level signal.
28	—	NC	NC
29	O	SCL	EEPROM interface Clock signal
30	I/O	SDA	EEPROM interface for Data signal
31	—	NC	NC
32	—	VDD_IO	Digital I/O Power. Connect to 1.8V supply.
33	—	XO_P	16MHz Crystal input positive
34	—	XO_N	16MHz Crystal input negative
35	—	EP_GND	RF ground
36	—	VCC_RF	1.8V input power for RF VCO and Transceiver
37	I/O	RF_TP6	RF test pin
38	I/O	RF_TP3	RF test pin
39	I/O	RF_TP5	RF test pin
40		RX_CLS1	Class 1 signal input
41	—	EP	RF ground
42		RTX	Combined RF T/R path
43	—	EP	RF ground
44	—	AGND	CODEC ground
45	I	LIN-	Differential audio input signal (−). 160mVp-p maximum differential input range.
46	I	LIN +	Differential audio input signal (+). 160mVp-p maximum differential input range.
47	AO	MIC_BIAS	Microphone's bias voltage output when SCO is established
48	—	AVDD	Audio CODEC power. Connect to a clean 1.8V supply.
49	—	EPGND	System thermal ground at backside.(1)

Notes:
(1) The backside for thermal ground on PCB must as large as possible.

3 Radio Transceiver

The IS1636N is design optimized for use in Bluetooth 2.4 GHz system. It provide low-power, low-cost with high receive sensitivity and high transmit power that extend the effective communicate range.

3.1 TRANSMITTER

The internal PA has a maximum output power of +2dBm with level control 8dB from amplitude control. This is applied into Class2/3 radios without external RF PA. If you want a larger output power for Class1 application, the external PA must be used.

The transmitter features IQ direct conversion to minimize the frequency drift. And it can excess 30dB power range with temperature compensation machine.

3.2 RECEIVER

The LNA can be operated into two type modes. One type is TR-combined mode for single port application. The other type is TR-separated mode for dual port application that used an external PA/LNA application.

The ADC is utilized to sample input analogue wave to convert into digital for de-modulator analysis. Before the ADC, a channel filter has been integrated into receiver channel that can reduce the external component count and increase the anti-interference capacity.

There is an RSSI signal to the processor that it can control the power to make a good tradeoff for effective distance and current consumption.

3.3 SYNTHESIZER

The internal loop filter is used to reduce external RC components. This can reduce cost and variations for components. This internal LC tank for VCO is utilized to reduce variation for components. The cost is down at the same time.

A fully integrated synthesizer has been created. There requires no external VCO, varactor diode, resonator and loop filter

4 MODEM

There are three different modulations for Bluetooth v2.0 + EDR. In figure 2, we summarized these modulations and data rate.

Figure 2 – Modulation type for Bluetooth v2.0 + EDR

Data Rate	Modulation	Bits/Symbol
BDR: 1 Mbps	GFSK	1
EDR: 2 Mbps	π/4 DQPSK	2
EDR: 3 Mbps	8DPSK	3

4.1 Basic Data Rate MODEM (BDR)

On the Bluetooth v1.2 specification and below, 1 Mbps was the standard data rate based on Gaussian Frequency Shift Keying (GFSK) modulation scheme. This basic rate modem meets BDR requirements of Bluetooth v2.0+EDR specification

4.2 Enhanced Data Rate MODEM (EDR)

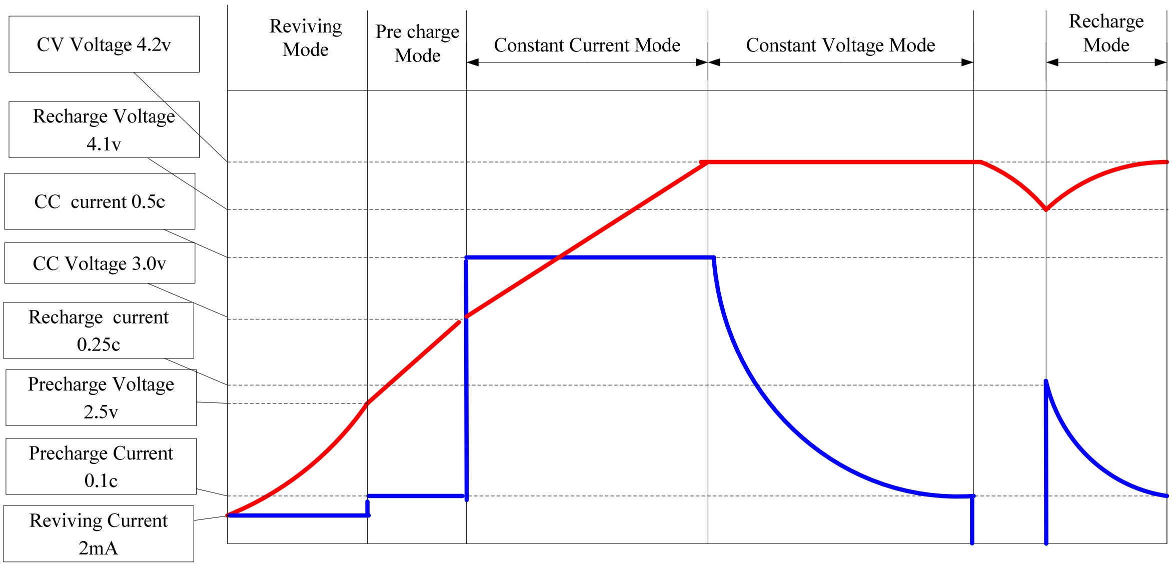
On the Bluetooth v2.0+EDR specification, Enhanced Data Rate (EDR) has been introduced to provide 2 and 3 Mbps data rates as well as 1 Mbps. This enhanced data rate modem meets EDR requirements of Bluetooth v2.0+EDR specification. For the viewpoint of baseband, both BDR and EDR utilize the same 1MHz symbol rate and 1.6 KHz slot rate. For BDR, 1 symbol represents 1 bit. However each symbol in the payload part of EDR packets represents 2 or 3 bits. This is achieved by using two different modulations, π/4 DQPSK and 8DPSK

5 Power Manage Unit

The PMU inside the chip have two main features, charging a Li-ion battery and some regulators for voltage translation. A power switch is used to switch over the power source between battery and adaptor automatically. The charging current is configured in the EEPROM. Whenever the adaptor is plug-in, charging circuit is active. Reviving, Pre-charging, Constant Current and Constant Voltage modes are implemented and re-charging function is also included.

The 10-bit Successive-Approximation-Register analog to digital converter (SAR ADC) provides one dedicated channel for battery voltage level detection. The warning level is programmable and stored in the EEPROM. The built-in voltage converter is used to convert the battery or adaptor power for RF or digital IO power supply. It also integrates hardware architecture to control power on/off procedure.

Figure 3 –Charging curve

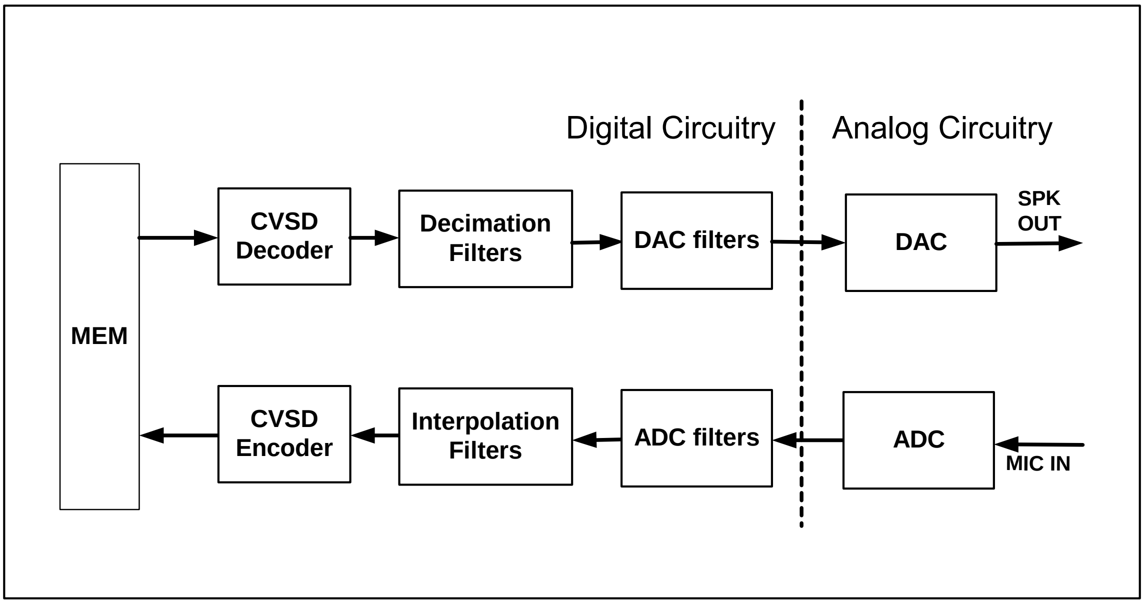


6 Voice CODEC

The mono audio codec is described by the following figure. There are several stages for input and output that all can be programmed for varying gain response characteristics. At the microphone input side, you may use single-end input or differential input. One critical point in maintaining a high quality signal is to provide a stable bias voltage source for the condenser microphone's FET. DC blocking capacitors may be used at both positive and negative sides of input. Internally, this analog signal is converted to 15-bit 8 kHz linear PCM data.

The voice data taken from common memory is converted to an analogue value by a DAC. A multistage amplifier drives the audio signal and provides a differential signal between Line_out+ and Line_out-. The output amplifier is capable of driving a speaker directly if its impedance is greater or equal to 16Ω.

Figure 4 : The signal path for audio processing



7 Test Mode and UART Interface

Hardwired control logic is presented in front of the UART devices for HCI protocol handling and packet buffering. This control logic is part of the HCI controller defined in Bluetooth specification 1.2. This logic is partially responsible for the HCI protocol handling to/from the host and it also maps the registers of the UART devices indirectly to the 8051 such that the system can receive or send a HCI packet to/from the respective host interface. The UART physical interface with adjustable baud rates from 2400 bps to 115200 bps.

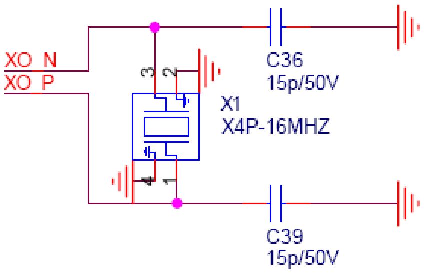
These HCI commands through UART interface fully supports Bluetooth test mode as defined in Bluetooth specification 2.0. By some hardware change, the device supports testing features to complete RF qualification. And some specify commands to achieve audio test and analog circuit calibration. These features include:

- Fixed carrier frequency transmission
- Received fixed frequency carrier
- Fixed frequency transmission with PRBS-9 pattern
- Transmitter test
    - Hopping on or off
    - Multiple packet types supported or not
    - Multiple data pattern supported or not
- Receiver test
    - Multiple packet types supported or not
    - Multiple data pattern supported or not
- Audio loop back test
- Calibration for voltage detector

8 Clock Generation

IS1636N is composed of an integrated crystal oscillation function. With an external crystal and two specified load capacitors, a high quality system reference timer source is obtained. A typical schematic diagram is shown as bellow.

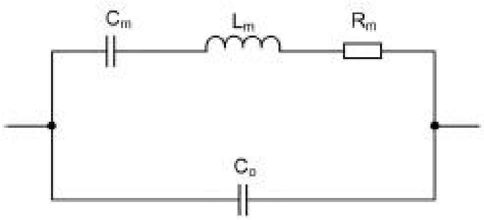
Figure 5 : The clock source for IS1636N



8.1 LOAD CAPACITOR

In general, the resonant frequency of a crystal is determined by its motional inductor L_m and motional capacitor C_m as shown in Figure 6 in nature. However, accompanying with oscillator circuitry, its oscillating frequency somehow can be fine trimmed by equivalent load capacitance.

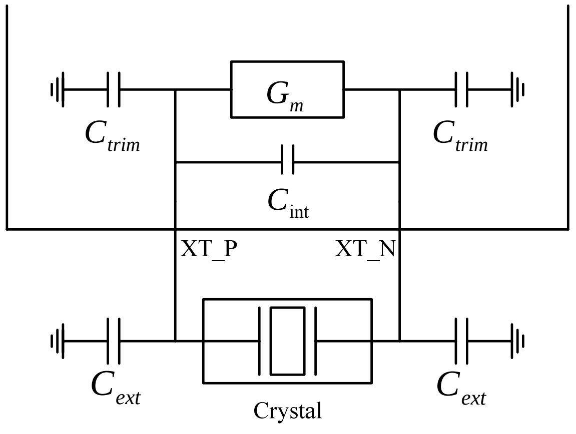
Figure 6 : Electrical equivalent circuit for a crystal



A conceptual diagram of a crystal oscillator is shown in Figure 7. With the given Lm, the resonant oscillating frequency is determined by

$$f = \frac{1}{2\pi\sqrt{L_m C_L}}$$

Figure 7 : The conceptual diagram for a crystal oscillator



And C_L is ***overall load capacitanc***e seen by crystal terminals.

$$C_L = C_{\text{int}} + \frac{C_{trim}}{2} + \frac{C_{ext} \times C_{ext}}{C_{ext} + C_{ext}}$$

Where C_{ext} is on-board ***external load capacitor***, C_{trim} is on-chip ***internal trim capacitor***, and Cint is ***on-chip fix capacitor***.

8.2 FREQUENCY TRIM

IS1636N enables frequency adjustments to be made. This feature is typically used to remove the initial tolerance frequency errors associated with the crystal and its equivalent load capacitance in mass production. Frequency trim is achieved by adjusting the crystal load capacitance through on-chip trim capacitors C_{trim} integrated in chip.

The value of trimming capacitance is around 200fF per LSB at 5 bits word, therefore

$$C_{trim} = 200\text{fF} * (1\sim31)$$

The overall adjustable clock frequency is around 40 KHz.

9 Electrical Characteristics

Table 1: Absolute Maximum Voltages

Symbol	Parameter	Min	Typical	Max	Unit
VDD_CORE VDD_SAR AVDD	Digital core supply voltage SAR ADC supply voltage CODEC supply voltage		1.8	1.98	V
VDD_IO VCC_RF	I/O supply voltage RF supply voltage	1.7		1.9	V
VIN_LDO18	LDO supply voltage	2.1		5	V
ADP_IN	Input voltage for adaptor	4.5		6.5	V
BAT_IN	Input voltage for battery			4.2	V
$T_{OPERATION}$	Operating temperature range	TBD		TBD	°C
T_{STORE}	Storage temperature	-40		+125	°C

Notes:
(2)

Table 2: Recommended operate condition for power supply

Symbol	Parameter	Min	Typical	Max	Unit
VDD_CORE VDD_SAR AVDD	Digital core supply voltage SAR ADC supply voltage CODEC supply voltage		1.8	1.98	V
VDD_IO VCC_RF	I/O supply voltage RF supply voltage		1.8		V
VIN_LDO18	LDO supply voltage	3.1		4.2	V
ADP_IN	Input voltage for adaptor		5		V
BAT_IN	Input voltage for battery	3.1		4.2	V

Notes:
(3)

Table 3: LDO Electrical Specifications

Symbol	Parameter	Min	Typical	Max	Unit
V_{IN}	Input voltage	3.1		4.2	V
V_{OUT}	Output voltage		1.8		V
I_{MAX}	Maximum load current		100		mA
C_{LOAD}	Load capacitance		1		µF
V_{RIPPLE}	Output ripple		20		mV_{RMS}

Table 4: Digital I/O pins

Symbol	Parameter	Min	Typical	Max	Unit
V_{IH}	High-level input voltage	1.5			V
V_{IL}	Low-level input voltage	-0.3		0.8	V
V_{OH}	High-level output voltage I_{OH} = 4mA	1.56			V
V_{OL}	Low-level output voltage I_{OL} = 4mA			0.4	V

Table 5: Current consumption

V_{BAT_IN} = 3.8V Temperature = 20 ºC and output power = 0 dBm		
Conditions	**Typical**	**Unit**
HV3 connection with 500 ms interval sniff mode	11.87	mA
HV3 connection with no sniff mode	12.95	mA
2EV3 connection	10.44	mA
ACL connection with 1.28s interval sniff mode	250	µA
Leakage current when system shutdown	1.5	µA

Notes:
(4)

Table 6: Audio section

Audio Codec,16Bit Resolution	**Min**	**Typ**	**Max**	**Unit**
Microphone Amplifier				
Input scale		160		mVp-p
Gain resolution				
Stage 1(two levels)	0		14	dB
Stage 2 : 0~26dB, 16 steps		1.73		dB/Step
Microphone input impedance		20		KΩ
Common Mode Voltage		0.85		V
Bandwidth	3.2		3.84	KHz
Analogue to Digital Converter				
Input Sample Rate		2		MSample/s
Output Sample Rate		8		KSamples/s
Digital to Analogue Converter				
Gain Resolution : -20dB~0dB, 8 Steps		-2.85		dB/Step
Min gain		-20		dB
Max gain		0		dB
Loudspeaker Driver				
Output Voltage Full Scale Swing (differential)		1.6		V Pk-Pk
Output Impedance	16			Ω
Common Mode Voltage		0.85		V
Bandwidth		3.3		KHz
Audio loop test				
Send Distortion and Noise (SD + N)		TBD		
Sending Idle Channel Noise		TBD		
Receive Distortion and Noise (SD + N)		TBD		
Receiving Idle Channel Noise		TBD		

Table 7: Charger section

	Min	Typ	Max	Unit
Total power dissipation		TBD		mW
Supply voltage	4.5	5	6.5	V
Operation Current		5		mA
VDD Sleep Current		10		uA
Output Voltage		4.2		V
Current Regulation Threshold		100		mV
Charge Terminated Current Detect Threshold		100		mV
Precharge Threshold		3		V
Precharge Current Regulation		100		mV
Recharge Threshold		4.1		V
Charging Current	1		100	mA

Table 8: Transmitter section for BDR

VCC_RF = 1.8V Temperature = 25ºC				
Parameter	**Min**	**Typ**	**Max**	**Unit**
Frequency range	2402		2480	MHz
Output power	-2	0	4	dBm
Channel spacing		1		MHz
Power control range	2		8	dB
2^{nd} Harmonic Content				dBm
3^{rd} Harmonic Content				dBm
20db bandwidth for modulated carrier		920		kHz
Adjacent channel transmit power F = F_0 ± 2Mhz				dBm
Adjacent channel transmit power F = F_0 ± 3Mhz				dBm
Adjacent channel transmit power F = F_0 ≥ 3Mhz				dBm
$\Delta f1_{avg}$ Maximum Modulation	140	155	170	kHz
$\Delta f2_{avg}$ Minimum Modulation		140		kHz
$\Delta f1_{avg}$ / $\Delta f2_{avg}$		0.95		
In-Band spurious emission				
± 500 KHz			-20	dBc
Out-Band spurious emission				
746 MHz to 764 MHz				dBm/Hz
851 MHz to 894 MHz				dBm/Hz
925 MHz to 960 MHz				dBm/Hz
1805 MHz to 1880 MHz				dBm/Hz
1930 MHz to 1990 MHz				dBm/Hz
2110 MHz to 2170 MHz				dBm/Hz
LO performance				
Lock time				μs
Initial carrier frequency tolerance				kHz
Frequency Drift				
DH1 packet				kHz
DH3 packet				kHz
DH5 packet				
Drift Rate				kHz/50us

Table 9: Transmitter section for EDR

VCC_RF = 1.8V Temperature = 25ºC		Typ	Unit
Maximum RF transmit power		2.0	dBm
Output power variation		1.5	dB
Relative transmit power		-1.5	dB
π/4 DQPSK max carrier frequency stability w_0			kHz
π/4 DQPSK max carrier frequency stability w_i			kHz
π/4 DQPSK max carrier frequency stability $\mid w_0 + w_i \mid$			kHz
8DPSK max carrier frequency stability w_0			kHz
8DPSK max carrier frequency stability w_i			kHz
8DPSK max carrier frequency stability $\mid w_0 + w_i \mid$			kHz
π/4 DQPSK Modulation Accuracy	RMS DEVM		%
	99% DEVM		%
	Peak DEVM		%
8 DPSK Modulation Accuracy	RMS DEVM		%
	99% DEVM		%
	Peak DEVM		%
In-band spurious emissions	$F > F_0 + 3MHz$		dBm
	$F < F_0 - 3MHz$		dBm
	$F = F_0 - 3MHz$		dBm
	$F = F_0 - 2MHz$		dBm
	$F = F_0 - 1MHz$		dB
	$F = F_0 + 1MHz$		dB
	$F = F_0 + 2MHz$		dBm
	$F = F_0 + 3MHz$		dBm
EDR Differential Phase Encoding			%

Table 10: Receiver section for BDR

VCC_RF = 1.8V Temperature = 25ºC					
Parameter		**Min**	**Typ**	**Max**	**Unit**
Frequency range		2402		2480	MHz
Rx sensitivity at 0.1% BER	2402 MHz		-89		dBm
	2441 MHz		-89		dBm
	2480 MHz		-89		dBm
Input IP3			1		dBm
Maximum received signal at 0.1% BER					dBm
Interference Performance					
C/I co-channel (5)					dB
C/I +1 MHz adjacent channel					dB
C/I -1 MHz adjacent channel					dB
C/I +2 MHz adjacent channel					dB
C/I -2 MHz adjacent channel					dB
C/I +3 MHz adjacent channel					dB
C/I -3 MHz adjacent channel					dB
C/I over 3 MHz adjacent channel					dB
C/I Image channel					dB
C/I 1 MHz adjacent to image channel					dB
Inter modulation Performance					
Maximum level of inter-modulation interference (6)					dBm
Spurious Emission performance					
30 MHz to 1 GHz					dBm/Hz
1 GHz to 6 GHz					dBm/Hz

Notes:

(5) Measured at channel frequency 2441 MHz

(6) Measured at f1 – f2 = 5MHz. Measurement is performed in accordance with Bluetooth RF test RCV/CA/05/c, i.e., wanted signal at -64dBm

F1 = -39dBm sine wave and f2 = -39dBm Bluetooth-modulated signal, f0 = 2f1-f2, and |f2-f2| = n* 1MHz, where n is 3, 4, or 5. For the typical case, n = 5

Table 11: Receiver section for EDR at π/4 DQPSK modulated signal

VCC_RF = 1.8V Temperature = 25ºC					
Parameter		**Min**	**Typ**	**Max**	**Unit**
Frequency range		2402		2480	MHz
Rx sensitivity at 0.1% BER	2402 MHz		-89		dBm
	2441 MHz		-89		dBm
	2480 MHz		-89		dBm
Input IP3			1		dBm
Maximum received signal at 0.1% BER					dBm
Interference Performance					
C/I co-channel (5)					dB
C/I +1 MHz adjacent channel					dB
C/I -1 MHz adjacent channel					dB
C/I +2 MHz adjacent channel					dB
C/I -2 MHz adjacent channel					dB
C/I +3 MHz adjacent channel					dB
C/I -3 MHz adjacent channel					dB
C/I over 3 MHz adjacent channel					dB
C/I Image channel					dB
C/I 1 MHz adjacent to image channel					dB
Inter modulation Performance					
Maximum level of inter-modulation interference (6)					dBm
Spurious Emission performance					
30 MHz to 1 GHz					dBm/Hz
1 GHz to 6 GHz					dBm/Hz

Notes:

(7) Measured at channel frequency 2441 MHz

(8) Measured at f1 – f2 = 5MHz. Measurement is performed in accordance with Bluetooth RF test RCV/CA/05/c, i.e., wanted signal at -64dBm

F1 = -39dBm sine wave and f2 = -39dBm Bluetooth-modulated signal, f0 = 2f1-f2, and |f2-f2| = n* 1MHz, where n is 3, 4, or 5. For the typical case, n = 5

Table 12: Receiver section for EDR at 8DPSK modulated signal

VCC_RF = 1.8V Temperature = 25ºC					
Parameter		**Min**	**Typ**	**Max**	**Unit**
Frequency range		2402		2480	MHz
Rx sensitivity at 0.1% BER	2402 MHz		-82		dBm
	2441 MHz		-82		dBm
	2480 MHz		-82		dBm
Input IP3			1		dBm
Maximum received signal at 0.1% BER					dBm
Interference Performance					
C/I co-channel (5)					dB
C/I +1 MHz adjacent channel					dB
C/I -1 MHz adjacent channel					dB
C/I +2 MHz adjacent channel					dB
C/I -2 MHz adjacent channel					dB
C/I +3 MHz adjacent channel					dB
C/I -3 MHz adjacent channel					dB
C/I over 3 MHz adjacent channel					dB
C/I Image channel					dB
C/I 1 MHz adjacent to image channel					dB
Inter modulation Performance					
Maximum level of inter-modulation interference (6)					dBm
Spurious Emission performance					
30 MHz to 1 GHz					dBm/Hz
1 GHz to 6 GHz					dBm/Hz

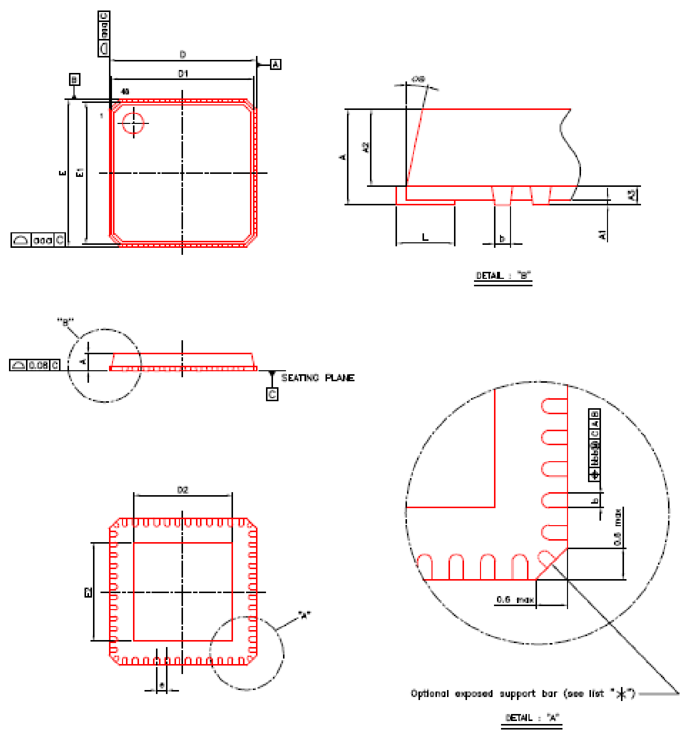
Notes:

(9) Measured at channel frequency 2441 MHz

(10) Measured at f1 – f2 = 5MHz. Measurement is performed in accordance with Bluetooth RF test RCV/CA/05/c, i.e., wanted signal at -64dBm

F1 = -39dBm sine wave and f2 = -39dBm Bluetooth-modulated signal, f0 = 2f1-f2, and |f2-f2| = n* 1MHz, where n is 3, 4, or 5. For the typical case, n = 5

10 Package Information



Symbol	Dimension in mm			Dimension in inch		
	MIN	NOM	MAX	MIN	NOM	MAX
A	0.80	0.85	1.00	0.031	0.033	0.039
A1	0.00	0.02	0.05	0.000	0.001	0.002
A2	---	0.65	1.00	---	0.026	0.039
A3	---	0.20	---	---	0.008	---
b	0.18	0.23	0.30	0.007	0.009	0.012
D	7.00 BSC			0.276 BSC		
D1	6.75 BSC			0.266 BSC		
E	7.00 BSC			0.276 BSC		
E1	6.75 BSC			0.266 BSC		
e	0.50 BSC			0.020 BSC		
L	0.30	0.40	0.50	0.012	0.016	0.020
θ	0°	---	12°	0°	---	12°
aaa	---	---	0.25	---	---	0.010
bbb	---	---	0.10	---	---	0.004
Chamfer	---	---	0.60	---	---	0.024

NOTE:

1. CONTROLLING DIMENSION : MILLIMETER
2. REFERENCE DOCUMENT: PROPSED JEDEC MO-220.

Exposed Pad Size & Support bar table

L/F	D2 (mm)			E2 (mm)			*
	MIN	NOM	MAX	MIN	NOM	MAX	
①	4.90	5.05	5.20	4.90	5.05	5.20	YES / NO
②	4.95	5.10	5.25	4.95	5.10	5.25	YES

OVER MOLD

TITLE : 48LD QFN (7X7 mm) PACKAGE OUTLINE			
L/F MATERIAL : A194 FH(PPF)			
APPR.	Holman Chen	DWG NO.	CE048-SW2
ENG.	C.Y.Horng	REV NO.	B
QM.	S.T.LIAO	PRODUCT CODE	CE0481A
CHK.	Y.Y.Lai	DATE	08/08/'02
DWG.	R.K.Wang	SHT No.	1/1
SILICONWARE PRECISION INDUSTRIES CO., LTD.			

COPY CONTROLLED

REV NO	DESCRIPTION	DATE
B	Add Exposed Pad Size & Support bar table	08/08/'02

REV.B

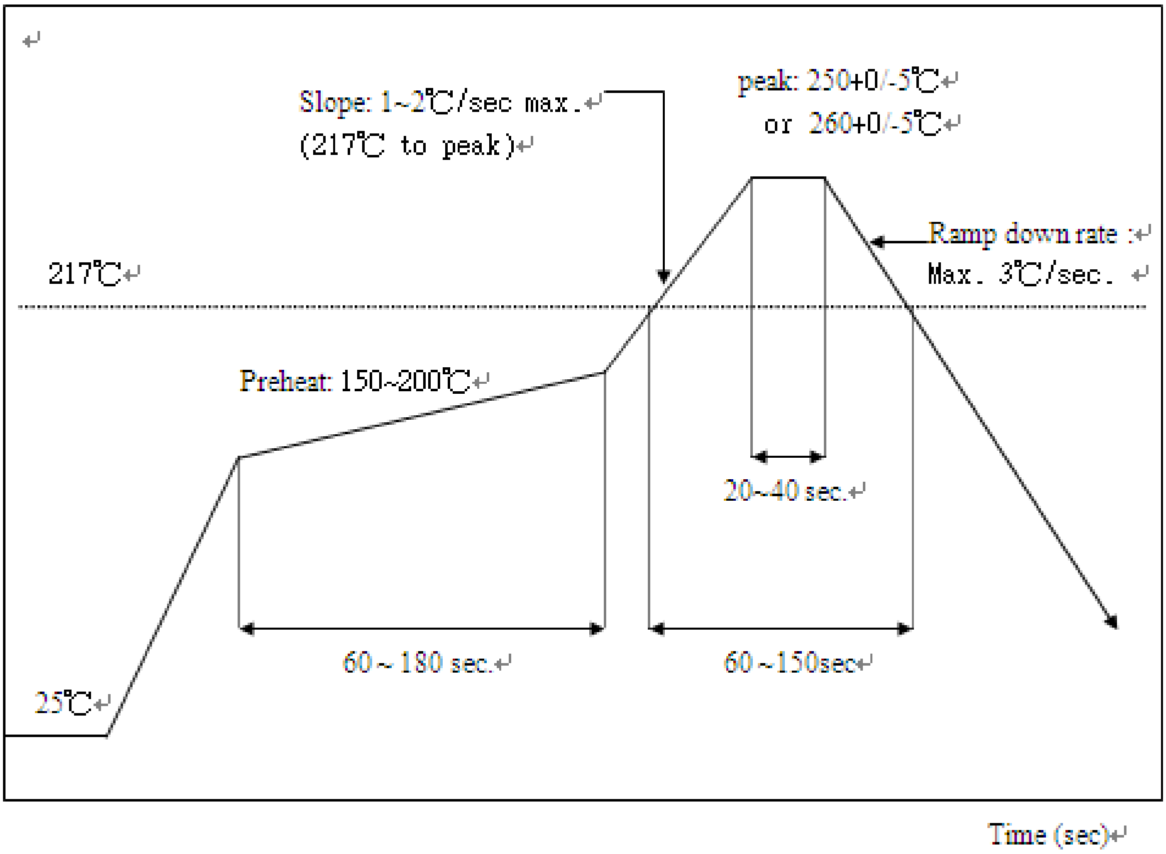
01-5700-10

Appendix A. Reflow Profile

1.) Follow: IPC/JEDEC J-STD-020 C

2.) Condition:

Average ramp-up rate (217℃ to peak): 1~2℃/sec max.
Preheat：150~200C、60~180 seconds
Temperature maintained above 217℃：60~150 seconds
Time within 5℃ of actual peak temperature: 20 ~ 40 sec.
Peak temperature：250+0/-5℃ or 260+0/-5℃
Ramp-down rate : 3℃/sec. max.
Time 25℃ to peak temperature : 8 minutes max.
Cycle interval：5 minus



Appendix B. BQB certification

https://www.bluetooth.org/tpg/Certificate.cfm?QID=1382(

Bluetooth SIG Qualification Design (QDL) Certificate

QDL Certificate: This certificate represents the Specifications declared by the Member as having passed the Bluetooth Qualification/Certification Process as specified within the Bluetooth Specifications and as required within the PRD 2.0.

Design Name: **Bluetooth 2.1+EDR Baseband controller**

Certified Bluetooth

This Product Design has passed the Bluetooth Qualification Process!

Specification Version: 2.1/2.1+EDR

QDID: B013820

Declared Specifications: Baseband Conformance, Radio, Link Manager, Summary ICS, Product Type

Member Company:	Requirements:	Project Dates:
Integrated System Solution Corp.	1. Testing	Assessment Date: March/21/2008
3F, No.2-1, Industry East Rd., 1, Science-Based Industrial Park	2. Documentation	
	3. Assessment	Listing Date: March/21/2008
	4. Declaration	
	5. Listing	
Hsinchu, Taiwan 300	6. Marking	
	7. Compliance to Auditing and Enforcement	
BQE: Jan-Willem Vonk		

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CONTACT INFORMATION

ISSC Corporate Headquarters (Taiwan):
3F, No.2-1, Industry East Rd. I,
Science-Based Industrial Park,
Hsinchu, Taiwan, R.O.C. 300

TEL: 886-3-577-8385
FAX: 886-3-577-8501

ISSC Sales Office (China, Shenzhen**)**
NO.1,11F,Southern International Plaza#B, No.3013,
Yitian Road, Futian District, Shenzhen P.R.C.

TEL: 86-755-8378-2810
FAX: 86-755-8378-2770

ISSC Sales Office (China, Shanghai**):**
2F., Building 59, No. 461, Hongcao Rd., Xu Hui
District, Shanghai 200233, P.R.C.

TEL: 86-21-6485-6299 # 6701
FAX: 86-21-5427-6519

ISSC Sales Office (Taiwan):
4F, No.116, Joutz St., Neihu District
Taipei Taiwan, R.O.C. 114

TEL: 886-2-2659-7699
FAX: 886-2-2659-7967