Noise Reduction Mono Headset IC with A2DP streaming

1. General Description

ISSC IS1685S is a compact, high integration, ultra-low cost, CMOS single-chip RF + baseband IC for Bluetooth v3.0(EDR) (Enhanced Data Rate) 2.4GHz applications. This chip is fully compliant with Bluetooth specification and completely backward-compatible with Bluetooth 1.1, 1.2, 2.0 or 2.1 systems.

It incorporates Bluetooth 1M/2M/3Mbps RF, single-cycle 8051, TX/RX modem, memory controller, task/hopping controller, UART interface, and ISSC Bluetooth software stack to achieve the required Bluetooth v3.0(EDR) functions.

The IS1685S is designed to support high quality voice application, an audio engine and a high performance mono CODEC are integrated for this purpose.

The audio engine provides the A-law/μ-law/CVSD encoding/decoding and also the enhanced noise reduction and echo supression to offer the best voice quality in the both sending and receiving sides.

In addition, to minimize the external components required for portable devices, a power manager unit including the Li-ion battery charger, a switching regulator and LDOs are integrated to reduce BOM cost for various Bluetooth applications.

The device incorporates built-in self-test (BIST) and auto-calibration functions to simplify production test.

2. Features

System Specification

- Compliant with Bluetooth Specification v.3.0 (EDR) in 2.4 GHz ISM band

Baseband Hardware

- 16MHz main clock input
- Built-in internal ROM for program memory
- Built-in 32 KB RAM for data storage and baseband data transfer buffering
- Bluetooth 2.1 Secure Simple Pairing
- Support both Pico-net and Scatter-net applications
- Hard-wired logic for modulation, demodulation, access code correlation, whitening, forward error correction (FEC), header error check (HEC), shorten hamming code, CRC generation/checking, frame check sequence (FCS), encryption bit stream generation, and transmit pulse shaping
- Adaptive Frequency Hopping (AFH) avoids occupied RF channels
- Fast Connection supported

RF Hardware

- Fully Bluetooth 3.0 (EDR) system in 2.4 GHz ISM band.
- Combined TX/RX RF terminal simplifies external matching and reduces external antenna switches.
- Max. +4dBm output power with 20 dB level control from register control.
- Build-in T/R switch for Class 2/3 application

- Build-in channel filter.
- To avoid temperature variation, temperature sensor with temperature calibration is utilized into bias current and gain control.
- Fully integrated synthesizer has been created. There requires no external VCO, varactor diode, resonator and loop filter.
- Crystal oscillation with build-in digital trimming for temperature/process variations.

Audio processor

- Support 64 kb/s A-Law or μ-Law PCM format, or CVSD (Continuous Variable Slope Delta Modulation) for SCO channel operation.
- Noise suppression
- Echo suppression
- SBC decoding
- Packet/Bit error concealment

Audio Codec

- 16 bit mono codec
- 94dB SNR DAC playback
- Integrate headphone amplifier for 16Ω speakers

Peripherals

- Built-in Lithium-ion battery charger
- Integrate 3V, 1.8V LDO and Switching mode regulator
- Built-in 10-bit Aux-ADC for battery monitor and voltage sense.
- LED driver

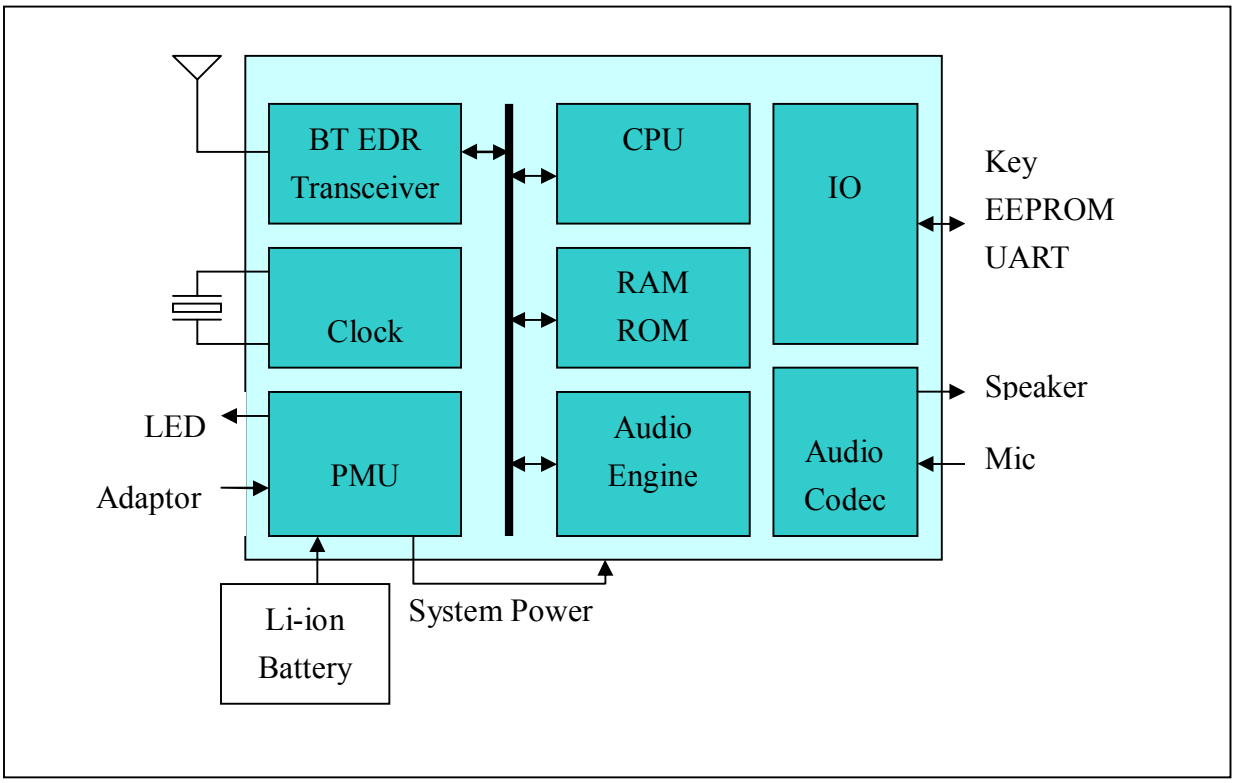
Flexible HCI interface

- High speed HCI-UART (Universal Asynchronous Receiver Transmitter) interface

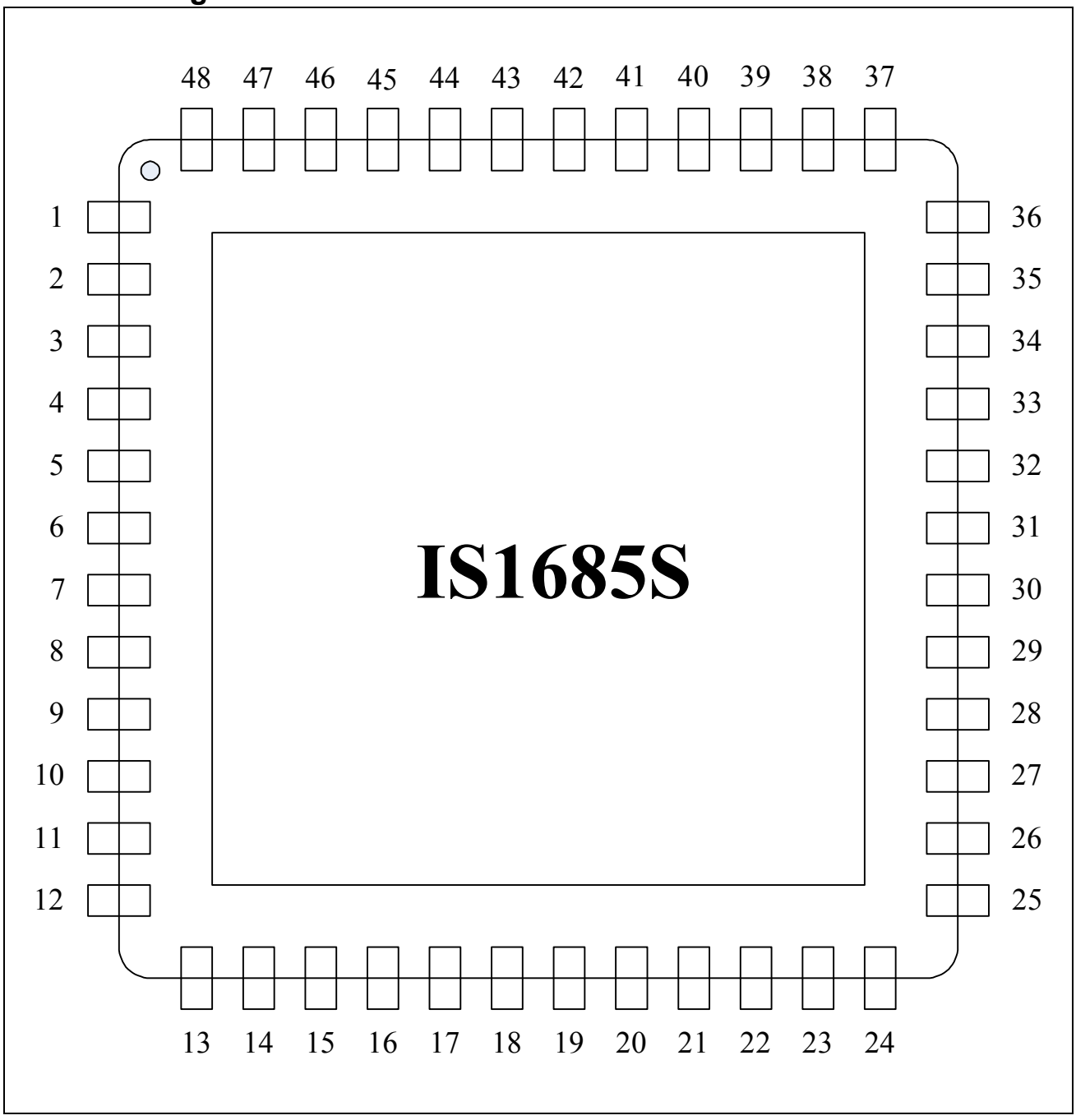
Package

- 7x7mm^2 48QFN standard package

3. Functional Diagram



4. Pin Assignment



5 Pin Descriptions

Pin No.	I/O	Pin Name	Pin Descriptions
1	AO	AOHPM	Headphone common mode output/sense input
2	AO	AOHPL	L-channel analog headphone output
3	P	VDDA	Positive power supply/reference voltage for CODEC
4	AO	VCOM	Internal biasing voltage for CODEC
5	AI	MICP1	Mic 1 mono differential analog positive input
6	AI	MICN1	Mic 1 mono differential analog negative input
7	P	MIC_BIAS	Electric microphone biasing voltage
8	P	VDD_IO	I/O power supply input
9	I/O	P2_3	GPIO, default pull-high input Volume up key (default) Volume up(long Press) for A2DP Enabled
10	I/O	P1_5	GPIO, default pull-high input Volume down (default) Volume down(long Press) for A2DP Enabled
11	AI	RST_N	KEY PIN for FT Test System Reset Pin
12	I/O	P1_2	GPIO, default pull-high input KEY PIN for FT Test EEPROM clock SCL Clock signal for OLED
13	I/O	P1_3	GPIO, default pull-high input KEY PIN for FT Test EEPROM data SDA Data signal for OLED
14	P	1V8	Core 1.8V power input
15	P	3V1_O	3.1V LDO output
16	P	CODEC_VO	3.1V LDO output for CODEC power
17	P	3V1_VIN	3.1V LDO input
18	P	ADAP_IN	Power adaptor input
19	P	BAT_IN	Battery input
20	P	SAR_AVDD	SAR 1.8V input

Pin No.	I/O	Pin Name	Pin Descriptions
21	P	SYS_PWR	System Power Output
22	P	BK_VDD	Buck VDD Power Input
23	P	BK_LX	Buck feedback input
24	P	BK_OUT	Buck output
25	P	MFB	Multi-Function Push Button key Combined Play/Pause key when A2DP enabled.
26	AI	LED1	LED Driver 1
27	AI	LED2	LED Driver 2
28	I/O	P2_4	GPIO, default pull-high input KEY PIN for FT Test System Configuration, H: Boot Mode
29	I/O	P2_2	GPIO, default pull-low input. Keep alive for external LDO power enable application.
30	I/O	P0_5	GPIO, default pull-high input Play/Pause key when A2DP enabled
31	O	HCI_TXD	KEY PIN for FT Test HCI TX data
32	I	HCI_RXD	KEY PIN for FT Test HCI RX data
33	I/O	P1_6	GPIO P1_6, default pull-high input Audio AMP Enable
34	P	VDD_IO	I/O power supply input
35	I	XO_P	16MHz Crystal input positive
36	I	XO_N	16MHz Crystal input negative
37	RP	VCC_RF	RF power input for both synthesizer and TX/RX block
38	I	RX_CLASS1	Class1 RF RX path
39	I/O	RTX	Class2 RTX path; Class1/Class2 TX path
40	I/O	P0_1	GPIO, default pull-high input Class1 TX Control signal of external TR switch when class 1 RF

Pin No.	I/O	Pin Name	Pin Descriptions
41	I/O	P0_3	GPIO, default pull-high input KEY PIN for FT Test Class1 RX Control signal of external TR switch when class 1 RF
42	I/O	P3_0	GPIO, default pull-high input Reverved charger LED driver
43	I/O	P2_0	GPIO, default pull-high input KEY PIN for FT Test System Configuration, H: Application L: Baseband(IBDK Mode)
44	I/O	P0_0	GPIO, default pull-low input. KEY PIN for FT Test Slide Switch Detector
45	I/O	P0_4	GPIO, default pull-high input Audio AMP Enable (When P1_6 is used for other application)
46	P	VDD_IO	I/O power supply input
47	I	EAN	Embedded ROM/External Flash enable H: Embedded; L: External Flash
48	P	VDDAO	Positive power supply dedicated to CODEC output amplifiers.
49	P	GND	Exposed pad as ground

NOTE:

I/O Application Note:

1) KEY PIN for internal Test
HCI_RXD, HCI_TXD, RST_N, P2_0, P2_4, P1_3, P1_2, P0_3, P0_5, P0_0

2) VOL+:P2_3, VOL-: P1_5 if AVRCP disabled.

3) VOL+:P2_3(long press), VOL-: P1_5(long press), FWD: P2_3(short press), REV: P1_5(short press) if AVRCP enabled

4) AUDIO AMP ENABLE: P1_6

5) Play/Pause: P0_5((When AVRCP is enabled and independent Play key is required))

6) P1_2:EEPROM Clock/Clock Signal for OLED
P1_3:EEPROM Data/Data Signal for OLED

7) SLIDE SWITCH DETECT: P0_0
8) CLASS 1 RF TX: P0_1, CLASS 1 RF RX: P0_3
9) External LDO power enable keep alive: P2_2
10) System Configuration: P2_0, P2_4

6 Functional Description

6.1 Overall Architecture

The ISSC IS1685S integrates an enhanced EDR Bluetooth RF & BB core, HCI controller, audio engine and an ENHANCED 8051 processor with an internal mask ROM for program memory and SRAM for data memory. An innovative interconnection structure called the Common-Memory Architecture (CMA) is designed to provide a fast and flexible data movement scheme between the embedded processor, Bluetooth core, and peripheral hardware.

For audio application and power management, IS1685S has build-in an audio processor, mono codec and power management unit to reduce the external components.

6.2 Radio Frequency (RF)

6.2.1 Transmitter

The internal PA has a maximum output power of +4dBm with level control 20dB from amplitude control. This is applied into Class 2/3 radios without external RF PA. For Class1 application, the build-in level control can be used with external PA for power control requirement.

The transmitter features IQ direct conversion to minimize the frequency drift. And it can excess 30dB power range with temperature compensation machine.

6.2.2 Receiver

The LNA can be operated into two type modes. One type is TR-combined mode for single port application. The other type is TR-separated mode for external PA/LNA application.

An ADC is used to sample input analogue wave for digital demodulation. Before the ADC, a channel filter has been integrated into receiver channel to increase the anti-interference capacity and also reduce the external component count.

For avoiding temperature variation issues, a temperature sensor with temperature calibration is utilized into bias current and gain control of LNA, Mixers, and RF AMP.

6.2.3 Synthesizer

The internal loop filter is used to reduce external RC components. This can reduce cost and variations for components. This internal LC tank for VCO is utilized to reduce variation for components. The cost is down at the same time.

A fully integrated synthesizer has been created. There requires no external VCO, varactor diode, resonator and loop filter.

6.3 MODEM

There are three different modulations for Bluetooth v3.0 + EDR. Table 6.3 summarizes these modulations and data rate.

Figure 6.3 Modulation type for Bluetooth v3.0 + EDR

Data Rate	Modulation	Bits/Symbol
BDR: 1 Mbps	GFSK	1
EDR: 2 Mbps	π/4 DQPSK	2
EDR: 3 Mbps	8DPSK	3

6.3.1 Basic Data Rate MODEM (BDR)

On the Bluetooth v1.2 specification and below, 1 Mbps was the standard data rate based on Gaussian Frequency Shift Keying (GFSK) modulation scheme. This basic rate modem meets BDR requirements of Bluetooth v3.0(EDR) specification.

Figure 6.3.1 Data format for BDR

Access Code	Header	Payload

6.3.2 Enhanced Data Rate MODEM (EDR)

On the Bluetooth v3.0(EDR) specification, Enhanced Data Rate (EDR) has been introduced to provide 2 and 3 Mbps data rates as well as 1 Mbps. This enhanced data rate modem meets EDR requirements of Bluetooth v3.0(EDR) specification. For the viewpoint of baseband, both BDR and EDR utilize the same 1MHz symbol rate and 1.6 KHz slot rate. For BDR, 1 symbol represents 1 bit. However each symbol in the payload part of EDR packets represents 2 or 3 bits. This is achieved by using two different modulations, π/4 DQPSK and 8DPSK.

Figure 6.3.2.A Data format for EDR

Access Code	Header	Guard	Sync	Payload	Trailer

For π/4 DQPSK modulation, each symbol carries 2 bits of information. For its constellation diagram, although there are 8 possible phase states, the encoding scheme guarantees the trajectory of the modulation between symbols is restricted to 4 states. For a given starting

point, every phase change between symbols is restricted to +45°, +135°, -45°, and -135°.

Figure 6.3.2.B Phase shift & bit pattern for 2 MHz data rate

Phase Shift	Bit Pattern
+45° (+π/4)	00
+135° (+3π/4)	01
-135°(-3π/4)	11
-45°(-π/4)	10

For 8DPSK modulation, each symbol carries 3 bits of information. For its constellation diagram, it is similar toπ/4 DQPSK but the trajectory of the modulation between symbols has 8 possible phase states. For a given starting point, every phase change between symbols is restricted to 0°, +45°, +90°, +135°, +180°, -135°, -90°, and -45°.

Figure 6.3.2.C Phase shift & bit pattern for 3 MHz data rate

Phase Shift	Bit Pattern
0° (+0)	000
+45° (+π/4)	001
+90° (+π/2)	011
+135° (+3π/4)	010
+180° (+π)	110
-135° (-3π/4)	111
-90° (-π/2)	101

-45° (-π/4)	100

6.4 Baseband

The following modules implemented in hardware constitute the Bluetooth Baseband Core.

The frequency hopping sequence generator produces the correct hop frequency control sequence based on the Bluetooth clock, Bluetooth device address, and the current operating mode.

The access code generates the access code based on the Lower Address Part (LAP) of the Bluetooth device address. The access code is comprised of the preamble, sync word and trailer bits. The detection of the access code uses correlation to detect a valid access code.

Bluetooth uses two types of FEC: 1/3 repetition code and (15, 10) shorten Hamming code respectively. The former basically repeats each transmitted bit three times while the latter has 15 bits of codeword which contains 5 parity bits. The code has capability of correction of all single-bit errors in each codeword.

The purpose of HEC is to protect the header bits. Dedicated header error code generator calculates the HEC bits in the header of a transmitted packet. While on the receiver side, HEC detects corrupted headers.

A 16-bit CRC is adopted to protect payload data transmitted using certain types of Bluetooth packets.

Information confidentiality can be protected by encryption of the packet payload. Dedicated encryption/decryption hardware is designed into the baseband core.

6.5 MCU

The embedded processor for IS1685S is a single-cycle 8051 CPU. The embedded processor will be referred to as simply the processor, 8051, or MCU throughout the remainder of this document. There are a few minor differences between a standard 8051 and this CPU. These include:

1. Alteration of memory timings to match internal and external memory configurations.
2. Modification of idle mode to disable internal CPU clocking. Only externally-clocked interrupt sources can allow the CPU to recover from idle mode.

A single-port synchronous interface is provided to memory. From this single port, the bandwidth is divided among the 7 interfaces spread amongst 5 physical busses described below:

- Embedded processor bus
- Baseband TX bus
- Baseband RX bus
- HCI TX bus
- HCI RX bus
- Audio bus
- DMA bus

In addition, attached to the embedded processor bus are a register bank, a dedicated single-port memory (data segment 1), and flash memory (program segment). The processor coordinates all link control procedures and data movement using a set of pointer registers. For example, when an HCI packet (from the host via USB or UART) is received into the HCI buffer, the processor is interrupted. The processor can then read a

status register to determine the HCI packet type and determine whether to set up the Baseband pointer registers for this memory region for RF-retransmission, or to otherwise directly perform packet processing with the CPU.

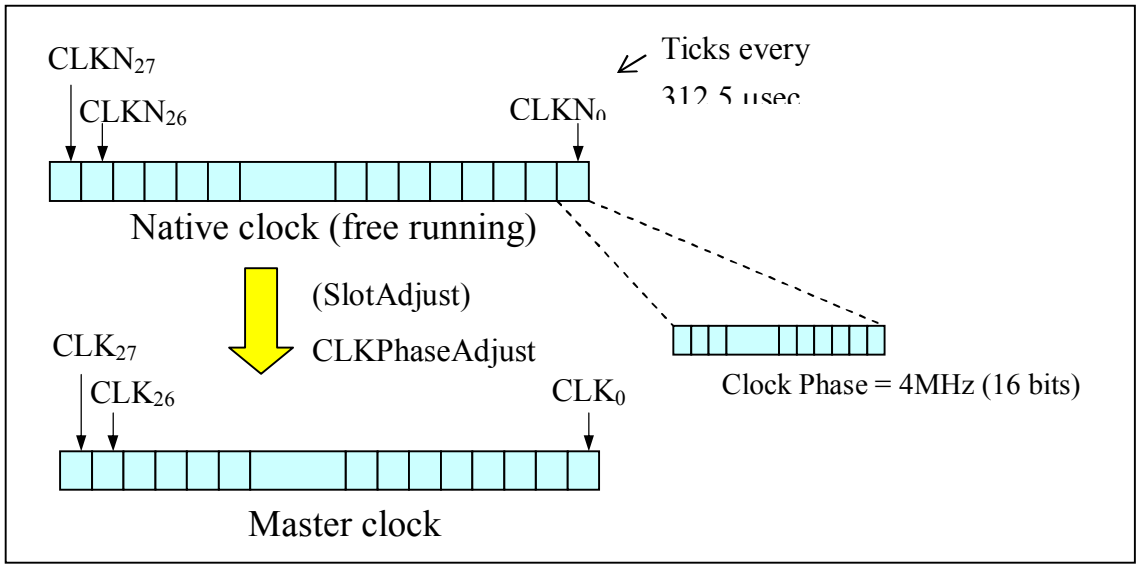
6.6 Bluetooth Clock and Timers

A Bluetooth standard 28-bit counter running at 3.2 kHz implements the native clock defined by Bluetooth specification. This clock provides the transmission and receiving timing of a half time slot (312.5 μs). Another finer counter implemented in 16 bits is also provided as the phase of a half time slot. This phase information is very helpful when a Bluetooth slave wants to adapt to its master's clock. The counter is pre-scalable for the purpose of power saving operations. The diagram below describes a standard Bluetooth native clock and master clock. The clock signal is also used as a slot boundary signal to trigger a baseband packet transmission or receipt.

There are several timers provided by the system, two timers for TX/RX and the others for general purpose.

The powerful pre-scheduling functions for the transceiver are realized different sets of programmable timers. Each set of timers is associated with the task of transmission or receiving. When the timer is configured by firmware, it will automatically execute the TX or RX task at a specific time. Sub-tasks and timing for a TX task remain to be defined.

Figure 6.6 Bluetooth clock



6.7 HCI Control Logic for USB/UART

Hardwired control logic is presented in front of the UART devices for HCI protocol handling and packet buffering. This control logic is part of the HCI controller defined in Bluetooth specification 1.2. This logic is partially responsible for the HCI protocol handling to/from the host and it also maps the registers of the UART devices indirectly to the 8051 such that the system can receive or send a HCI packet to/from the respective host interface. Major functions of this logic include:

- HCI packet formatter and de-formatter (identifying the packet type)
- Frame boundary determination, segmentation and reassembly of HCI packets.
- HCI packet transmission, receiving, and buffering (using common memory HCI buffer).
- Independent receive / transmit channels
- Universal device interface

6.7.1 HCI UART Interface

An embedded HCI UART (Universal Asynchronous Receiver Transmitter) with programmable data rate up to 3Mbps is included in this design. The HCI UART supports the following functions:

- Full-Duplex operation
- Programmable BAUD rate (using 16-bit input clock divider to obtain Baud Rate x16 or x24 or x13 clock base)
- 7 or 8 Data bits
- 1 or 2 Stop bits
- Even / Odd / Mark / Space / None Parity configurations
- Break Generation / Detection
- Maskable individual interrupts to CPU and combined Error interrupt to HCI
- Selectable Direct CPU interface or interface to HCI module

6.8 General Purpose I/O

The IS1685S provides 14 general purpose I/O ports. These general I/Os can be defined as input or output port individually by setting specific register bit. While setting as an input port, a build-in 50KΩ pull high or pull low resistor can be enabled for different application purpose.

6.9 Audio Processor

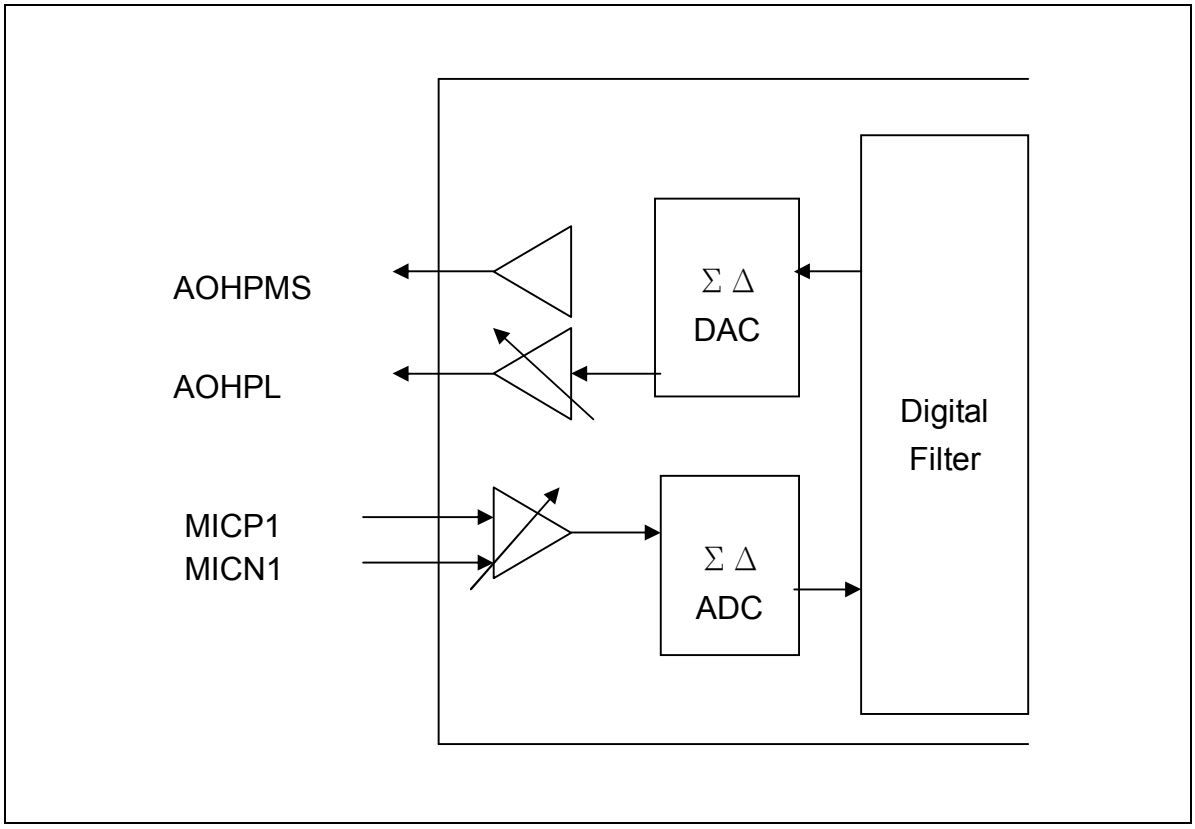
The IS1685S builds in an enhanced audio engine to offer high quality of audio for voice application. The standard A-law/μ-law/CVSD voice functions are implemented in the audio engine. The enhanced audio functions, like AEC, noise reduction, can be achieved with

enhanced algorithm.

6.10 Audio Codec

The build in codec contains a analog to digital convert (ADC), a digital to analog converter (DAC) and additional analog circuits like headphone driver and microphone amplifier.

Figure 6.10 Audio Codec



6.10.1 ADC

The ADC interface supports variety sampling rate from 8k Hz to 48k Hz. The microphone input has 42 dB programmable analog gain and 48db digital gain. A regulated MIC_Bias is available.

6.10.2 DAC

The DAC output is available for both line level and through the headphone amplifier to drive a low impedance headphone. The headphone output volume is adjustable by the combination of the digital/analog gain control.

6.11 Auxiliary ADC

The 10-bit auxiliary analog to digital converter (SAR ADC) provides one dedicated channel for battery power detection and one other channel for external peripheral sensing. This ADC has 10 bits resolution that provides an accurate monitoring for battery voltage. The operating current is very low and almost consumes no power when disabled.

6.12 Power Management (PMU)

The power management unit of IS1685S includes several power control blocks, linear regulators, switch-mode regulator, Aux-ADC, LED driver and Lithium-ion/Polymer battery charger.

6.12.1 3V1_LDO

The IS1685S has build-in the programmable output voltage LDOs (1.8~3.2V) for codec and digital IO power supply. The programmable LDO is used to regulate the high input voltage from battery or adapter. This LDO needs 1uF bypass capacitor.

6.12.2 Buck regulator

The built-in programmable output voltage buck (1.8~2.4V) can converts battery voltage for RF and baseband core power supply. This converter has high conversion efficiency and

fast transient response.

6.12.3 Aux-ADC

The 10-bit Successive-Approximation analog to digital converter (SAR ADC) monitors the battery power and adapter power for charging and power management control.

6.12.4 Li-ion Battery Charger

IS1685S includes a built-in battery charger optimized for use with lithium polymer batteries. The charger features a current sensor for charging control, user programmable current regulation and high accuracy voltage regulation. It charges the battery in four phases:

- reviving mode : 2mA charging current to charge BAT to 2.5V
- pre-charge mode : 0.1C charging current to charge BAT to 3.0V
- constant current mode : 0.xC (default 0.7C) charging current to charge BAT to 4.2V (programmable)
- constant voltage mode : charging is terminated while the charging current drops below 0.YC (default 0.13C)

Charging current in the constant current mode can be configured to provide a wide range of charging current up to 180mA (1mA per step). Charger will re-start charging if the battery voltage falls below an internal threshold.

System operation is allowed when the battery is charging.

6.13 Miscellaneous (Watchdog Timer, and Clock Divider)

System related functions such as watchdog timer, Endian control, and interrupt vectors are

also provided. The purpose of the watchdog timer is to provide a reset to CPU in case when the CPU fails to service the watchdog timer in a pre-defined (programmable) period.

7 Electrical Characteristics

Absolute Maximum Ratings

Rating		Min	Max	Max
Operation Temperature		-40ºC	+85ºC	ºC
Core supply voltage	VDD_CORE, VCC_RF, AVDD_SAR, AVDD_PLL	1.7V	1.98V	V
Codec supply voltage	VDD_AUDIO		3.3	V
I/O voltage	VDD_IO		3.3	V
Supply voltage	BK_VDD		4.3	V
	3V1_VIN		5	V
	BAT_IN		4.3	V
	ADAP_IN		5.5	V
	LED[1:0]		5	V
	Power switch		5.5	V

Recommended Operate Condition

Symbol	Parameter	Min	Typical	Max	Unit
V_{DD18}	Digital core supply voltage SAR ADC supply voltage CODEC supply voltage	1.62	1.8	1.98	V
V_{DDIO}	I/O supply voltage RF supply voltage	2.5	2.7	3.3	V
$T_{OPERATION}$	Operating temperature range	-20	+25	+70	ºC
T_{stg}	Storage temperature	-40		+125	ºC
V_{LDO}	LDO supply voltage	1.8		3.3	V
V_{BAT_IN}	Input voltage for SAR ADC	0.9		3.3	V

Digital I/O pins (I/O pins at V_{DDIO})

Symbol	Parameter	Conditions	Min	Typical	Max	Unit
V_{IH}	High-level input voltage		2		3.3	V
V_{IL}	Low-level input voltage		-0.3		0.8	V
V_{OH}	High-level output voltage	I_{OH} = 4mA	2.4		-	V
V_{OL}	Low-level output voltage	I_{OL} = 4mA	-	-	0.4	V

Radio Characteristics:

Transmitter section for BDR

VCC_RF = 2.7V Temperature = 25ºC		Min	Typ	Max	Bluetooth specification	Unit
Maximum RF transmit power			3	4.0	-6 to 4	dBm
RF power variation over temperature range with compensation enabled			±2			dB
RF power control range			20		≥16	dB
RF power range control resolution			0.3			dB
20dB bandwidth for modulated carrier			900		≤1000	KHz
ACP	F = F_0±2MHz		-33		≤-20	dBm
	F = F_0±3MHz		-45		≤-40	dBm
Note: F_0=2441MHz	F = F_0±>3MHz		-54		≤-40	dBm
Δf_{1avg} maximum modulation		150		165	140<Δf_{1avg}<175	KHz
Δf_{2max} maximum modulation		120		140	≥115	KHz
$\Delta f_{2avg}/\Delta f_{1avg}$		0.92	0.94		≥0.80	
ICFT (abs)		0	5	10	75	KHz
Drift rate (abs)		2		7	≤20	KHz/50us
Drift (single slot packet, abs)			12		≤25	KHz
2nd harmonic content @ Tx= 4dBm			-53		≤-47	dBm
3rd harmonic content @ Tx= 4dBm			-55		≤-47	dBm

Receiver section for BDR

Temperature = 25ºC	Frequency (GHz)	Min	Typ	Max	Bluetooth specification	Unit
Sensitivity at 0.1% BER for all basic rate packet types	2.402		-90		≤-70	dBm
	2.441		-90			
	2.480		-90			
Maximum received signal at 0.1% BER			-10		≥-20	dBm
C/I co-channel			4		≤11	dB
Adjacent channel selectivity C/I Note: F_0=2441MHz	F = F_0+1MHz		-7		≤0	dB
	F = F_0-1MHz		-7		≤0	dB
	F = F_0+2MHz		-36		≤-30	dB
	F = F_0-2MHz		-22		≤-9	dB
	F = F_0-3MHz		-24		≤-20	dB
	F = F_0+5MHz		-50		≤-40	dB
	F = F_{image}		-22		≤-9	dB

Transmitter Section for EDR

Temperature = 25ºC		Min	Typ	Max	Bluetooth specification	Unit
Relative transmit power			-1.4		-4 to 1	dB
π/4 DQPSK max carrier frequency stability	$\|\omega_o\|$ freq. error		2.5	5	≤10 for all blocks	KHz
	$\|\omega_i\|$ initial freq. error		2.5	5	≤75 for all blocks	KHz
	$\|\omega_o+\omega_i\|$ block freq. error		5	10	≤75 for all blocks	KHz
8DPSK max carrier frequency stability	$\|\omega_o\|$ freq. error		2.5	5	≤10 for all blocks	KHz
	$\|\omega_i\|$ initial freq. error		2.5	5	≤75 for all blocks	KHz
	$\|\omega_o+\omega_i\|$ block freq. error		5	10	≤75 for all blocks	KHz
π/4 DQPSK modulation accuracy @ Tx= 2dBm	RMS DEVM		7		≤20	%
	99% DEVM		100		≤30	%
	Peak DEVM			25	≤35	%
8DQPSK modulation accuracy @ Tx= 2dBm	RMS DEVM		7		≤13	%
	99% DEVM		100		≤20	%
	Peak DEVM			20	≤25	%
In-band spurious emissions Note: F_0=2441MHz	F > F_0+3MHz		<-52		≤-40	dBm
	F < F_0-3MHz		<-53		≤-40	dBm

	F = F_0-3MHz		-46		≤-40	dBm
	F = F_0-2MHz		-34		≤-20	dBm
	F = F_0-1MHz		-34		≤-26	dBm
	F = F_0+1MHz		-37		≤-26	dBm
	F = F_0+2MHz		-34		≤-20	dBm
	F = F_0+3MHz		-46		≤-40	dBm
EDR differential phase encoding			100		≥99	%

Receiver Section for EDR

Temperature = 25ºC		Frequency (GHz)	Modulation	Min	Typ	Max	Bluetooth specification	Unit
Sensitivity at 0.01% BER		2.402	π/4 DQPSK		-90		≤-70	dBm
		2.441	π/4 DQPSK		-90			
		2.480	π/4 DQPSK		-90			
		2.402	8DPSK		-83		≤-70	dBm
		2.441	8DPSK		-83			
		2.480	8DPSK		-83			
Maximum received signal at 0.1% BER			π/4 DQPSK		-10		≥-20	dBm
			8DPSK		-10		≥-20	
C/I co-channel at 0.1% BER			π/4 DQPSK		5		≤13	dB
			8DPSK		14		≤21	dB
Adjacent channel selectivity C/I Note: F_0=2441MHz	$F = F_0$+1MHz		π/4 DQPSK		-13		≤0	dB
			8DPSK		-7		≤5	dB
	$F = F_0$-1MHz		π/4 DQPSK		-13		≤0	dB
			8DPSK		-7		≤5	dB
	$F = F_0$+2MHz		π/4 DQPSK		-38		≤-30	dB
			8DPSK		-34		≤-25	dB
	$F = F_0$-2MHz		π/4 DQPSK		-23		≤-7	dB
			8DPSK		-21		≤0	dB
	$F = F_0$-3MHz		π/4 DQPSK		-26		≤-20	dB
			8DPSK		-19		≤-13	dB

	F = F_0+5MHz	π/4 DQPSK		-53		≤-40	dB
		8DPSK		-46		≤-33	dB
	F = F_{image}	π/4 DQPSK		-23		≤-7	dB
		8DPSK		-21		≤0	dB

Audio Codec: ADC

Test Condition: T= 25°C, Vdd=3.3V, 1KHz sine wave input, Bandwidth = 20~20KHz					
Parameter	**Condition**	**Min.**	**Typ.**	**Max.**	**Unit**
Input Level	Line/microphone input, Full scale			2.8	Vpp
Resolution			16		bits
Input Sampling Rate		8		48	kHz
SNR	A-weighted 1KHz@full scale, Line input, microphone input		85		dB
	A-weighted 1KHz@full scale, Microphone boost enable		75		
THD			-70		dB
Digital Gain				48	dB
Analog Gain				42.5	dB
Gain Step			1.5		dB
Input resistance	$R_{L,}$ Microphone input		12		kOhm
Output capacitance	Cp			25	pF

Audio Codec: DAC

Test Condition: T= 25°C, Vdd=3V, 1KHz sine wave input, Bandwidth= 20~20KHz					
Parameter	**Condition**	**Min.**	**Typ.**	**Max.**	**Unit**
Output Level	Full scale		2.35		Vpp
Resolution			16		bits
Output Sampling Rate		8		48	KHz
SNR	A-weighted 1KHz@full scale		94		dB
Max Output Power	R_L=16Ohm		40		mW
	R_L=32Ohm		20		mW
THD	16Ohm load		-65		dB
Digital Gain		-42		0	dB
Analog Gain		-22.5		0	dB
Gain Step			1.5		dB
Output resistance	R_L	16			Ohm
Output capacitance	Cp			100	pF

Battery Charger

Charging Mode (BAT_IN rising to 4.2V)		Min	Typ	Max	Unit
Operation Temperature		-20		70	℃
Input Voltage (Vin) Note: It needs more time to get battery fully charged when Vin=4.5V		4.5		6	V
Battery trickle charge current (BAT_IN < trickle charge voltage threshold)			2		mA
Maximum battery fast charge current Note: C → Battery capacity	Headroom > 0.7V		180		mA
	Headroom = 0.3V		110		mA
Minimum battery fast charge current Note: C → Battery capacity	Headroom > 0.7V		1		mA
	Headroom = 0.3V		1		mA
Trickle charge voltage threshold			3		V
Battery charge termination current, % of fast charge current			10		%
Standby Mode (BAT_IN falling from 4.2V)					
Battery recharge hysteresis (Note1)			100		mV
Battery recharge current (Note2) Note: C → Battery capacity			0.25C		mA

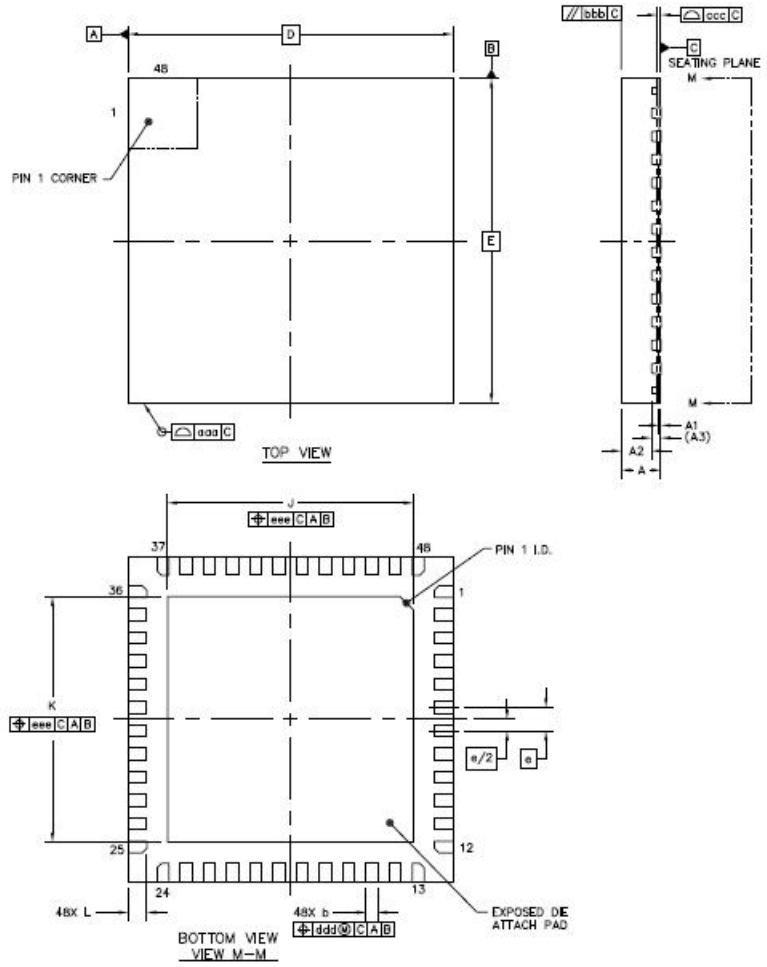
Note1：When charging complete and the adapter is still in, the battery voltage will slowly drop down.
When the voltage drop is larger than 100mV from the full voltage, the re-charging cycle will start.

Note2：If the battery voltage during plug in is larger than 4V, the charging current will be limited to 0.25C
to avoid the battery voltage overshoot.

Clock

Parameters	Test Condition	MIN	TYP	MAX	Unit
Crystal Frequency			16		MHz
Frequency Tolerence			±20		ppm
Operating Temperature		-20		70	^{O}C
Trimming Capacitance			6.4		pF
Trimming Step Size			0.2		pF

8 Package Information



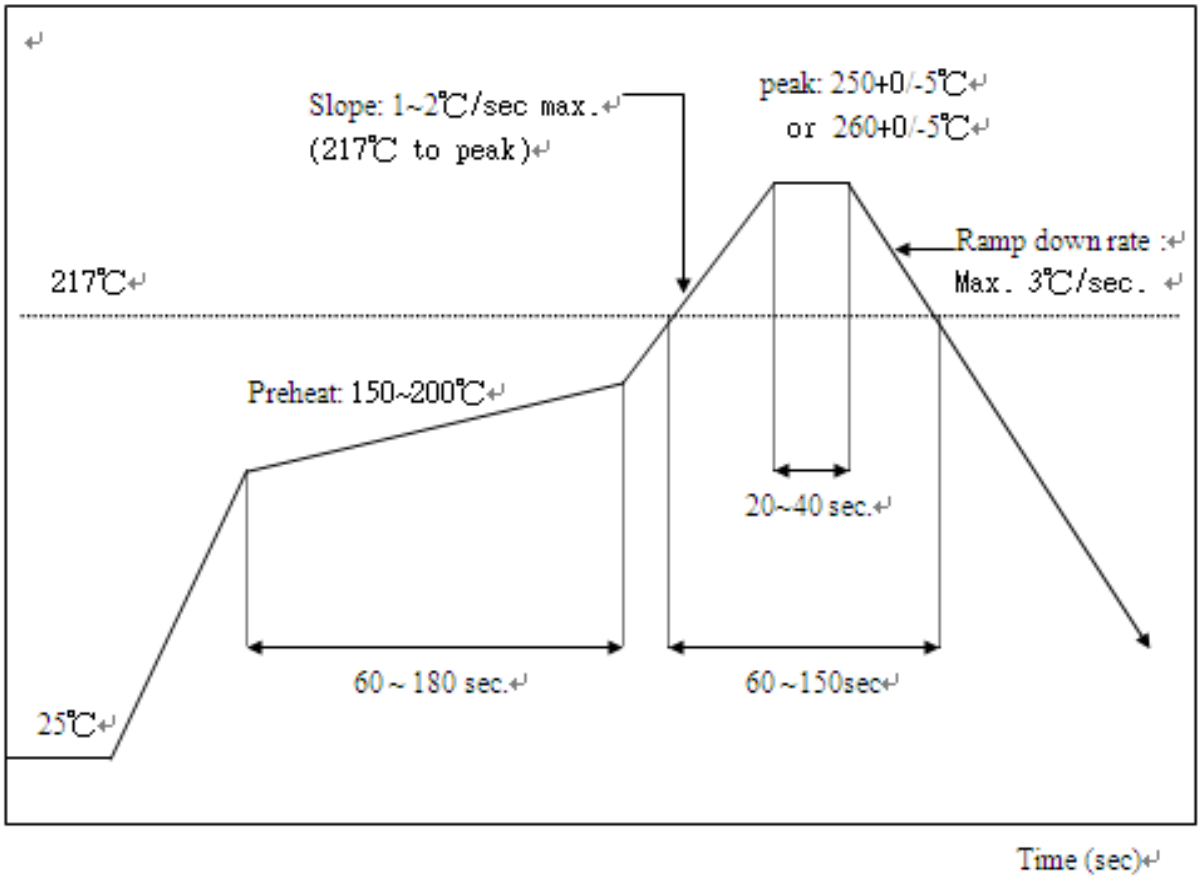
		SYMBOL	MIN	NOM	MAX
TOTAL THICKNESS		A	0.8	0.85	0.9
STAND OFF		A1	0	0.035	0.05
MOLD THICKNESS		A2	---	0.65	0.67
L/F THICKNESS		A3		0.203 REF	
LEAD WIDTH		b	0.2	0.25	0.3
BODY SIZE	X	D		7 BSC	
	Y	E		7 BSC	
LEAD PITCH		e		0.5 BSC	
EP SIZE	X	J	5.2	5.3	5.4
	Y	K	5.2	5.3	5.4
LEAD LENGTH		L	0.35	0.4	0.45
PACKAGE EDGE TOLERANCE		aaa		0.1	
MOLD FLATNESS		bbb		0.1	
COPLANARITY		ccc		0.08	
LEAD OFFSET		ddd		0.1	
EXPOSED PAD OFFSET		eee		0.1	

Appendix A. Reflow Profile

1.) Follow: IPC/JEDEC J-STD-020 C

2.) Condition:

Average ramp-up rate (217℃ to peak): 1~2℃/sec max.
Preheat：150~200C、60~180 seconds
Temperature maintained above 217℃ : 60~150 seconds
Time within 5℃ of actual peak temperature: 20 ~ 40 sec.
Peak temperature：250+0/-5℃ or 260+0/-5℃
Ramp-down rate : 3℃/sec. max.
Time 25℃ to peak temperature : 8 minutes max.
Cycle interval：5 minus



Appendix B. BQB certification

TPG Project	ISSC Bluetooth 3.0(EDR) Single Chip (Component (Tested))
Qualified Design ID (QD ID)	B016749 | Export PICS
PRD 1.0 ID (QP ID)	
Design Name	ISSC Bluetooth 3.0(EDR) Single Chip
Wi-Fi® Certification ID	
Subsetted Designs	**Date Created** / **Type** / **PICS**: Jun 28, 2010 / Main / PICS
Member Company	ISSC Technologies Corp.
Specification Name	3.0
Core Spec Addenda	N/A
Design Model Number	IS1XYZ, where X, Y and Z means 1~9
Hardware Version Number	ISBT_BB_v30
Software Version Number	ISBT_BB_v30
Qualification Assessment Date	July/21/2010
Listing Date	July/21/2010
Design Description	ISSC Bluetooth 3.0(EDR) Single Chip
Product Type	Component (Tested)
Technical Data Sheet (RIN)	** Open Reference Integration Notes (RIN) **
Listed By	Charlie Lee
BQE	Jan-Willem Vonk
Profile / Protocol	**Role / Version (If Any)**
Baseband	
Radio	
Link Manager	