IS1870/71

Bluetooth® Low Energy (BLE) SoC

Features

- Bluetooth smart 4.2 Bluetooth Low-Energy (BLE) compliant
- 256K bytes embedded Flash memory
- UART/SPI/I^2C interface supported
- Integrated crystal oscillator, operates with 32 MHz external crystal
- Temperature sensor supported
- Flexible 31 GPIO pins for IS1870 and 16 GPIO pins for IS1871 configuration
- 4-channel PWM support (IS1870), 1-channel PWM support (IS1871)
- 12 bits ADC support for battery and voltage detection. 16-channel (IS1870)/6-channel (IS1871)
- AES-CMAC hardware engine
- Beacon support
- Low-power consumption
- Peak current: Tx 13 mA, Rx 13 mA at VBAT=3.0V, buck power
- Compact size: 4x4 mm 32QFN (IS1871) and 6x6mm 48QFN (IS1870) packages

Radio Frequency (RF)/Analog Features

- ISM band 2.402 GHz to 2.480 GHz operation
- Channels: 0-39
- Rx sensitivity: -90 dBm in BLE mode
- Tx power: +2 dBm (max)
- Received Signal Strength Indicator (RSSI) monitor

Operating Conditions

- Operating voltage: 1.9V to 3.6V
- Operating temperature: -20°C to 70°C

Applications

- Internet of Things (IoT)
- Wearable/Fitness/Healthcare
- Weight Scale
- Proximity/Find Me services
- Payment/Security
- Digital Beacons
- Consumer Appliances/Home Automation
- Industrial

Packages

Type	IS1870	IS1871
Pin Count	48	32
I/O Pins (up to)	31	16
Contact/Lead Pitch	0.4	0.4
Dimensions	6x6x0.9	4x4x0.9
Package	QFN48	QFN32

Note: All dimensions are in millimeters (mm) unless specified otherwise.

NOTES:

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1.0 DEVICE OVERVIEW

Microchip Technology IS1870/71 embedded 2.4 GHz Bluetooth version 4.2 (BLE) SoC incorporates, 2.4 GHz transceiver, Power Management Unit (PMU), Bluetooth LE stack and RF power amplifier. The user can embed the Bluetooth functionality to IoT applications.

The IS1870/71 is cost effective and designed to provide developers a simple Bluetooth solution with the following features:

- Ease of integration by UART transparent service
- Reduced development time for Bluetooth LE stacks
- Integrated solution, thus reducing the cost
- Inter-operability with Apple® iOS and Android™ OS
- Maximum value in the range of applications

The IS1870/71 provides support for the Beacon technology and improves user experiences in IoT applications, such as auto connection/control and cloud connectivity.

The IS1870/71 can maintain a low-power wireless connection. The low-power consumption and flexible power management maximizes the IS1870/71 lifetime in battery operated devices. A wide operating temperature range allows use in indoor and outdoor environments (industrial temperature range).

The small-form factor package size of the IS1870/71 is designed for wearable applications. The solution providers can minimize the module size to meet the market requirement. The IS187x SoC is designed for the application-enabled accessories and IoT applications.

Operating in the 2.4 GHz ISM band radio, the IS1870/71 is certified for the Bluetooth core specification version 4.2 including support for the enhanced throughput, and the Federal Information Processing Standard (FIPS) compliant encryption support for secure data connections.

The IS1870/71 integrates transceiver and baseband functions to decrease the external components. Therefore, users can complete their design easily and efficiently. A free Bluetooth stack firmware is provided for building embedded BLE solutions that use the IS1870/71 SoC.

For portable and wearable applications, the IS1870/71 SoC's optimized power design helps to minimize current consumption for extended battery life and it minimizes the package size to as small as possible.

Figure 1-1 and Figure 1-2 illustrate a typical example of the IS1870 and IS1871-based system. Table 1-1 provides key features of the IS1870/71 module.

FIGURE 1-1: IS1870-BASED SYSTEM BLOCK DIAGRAM

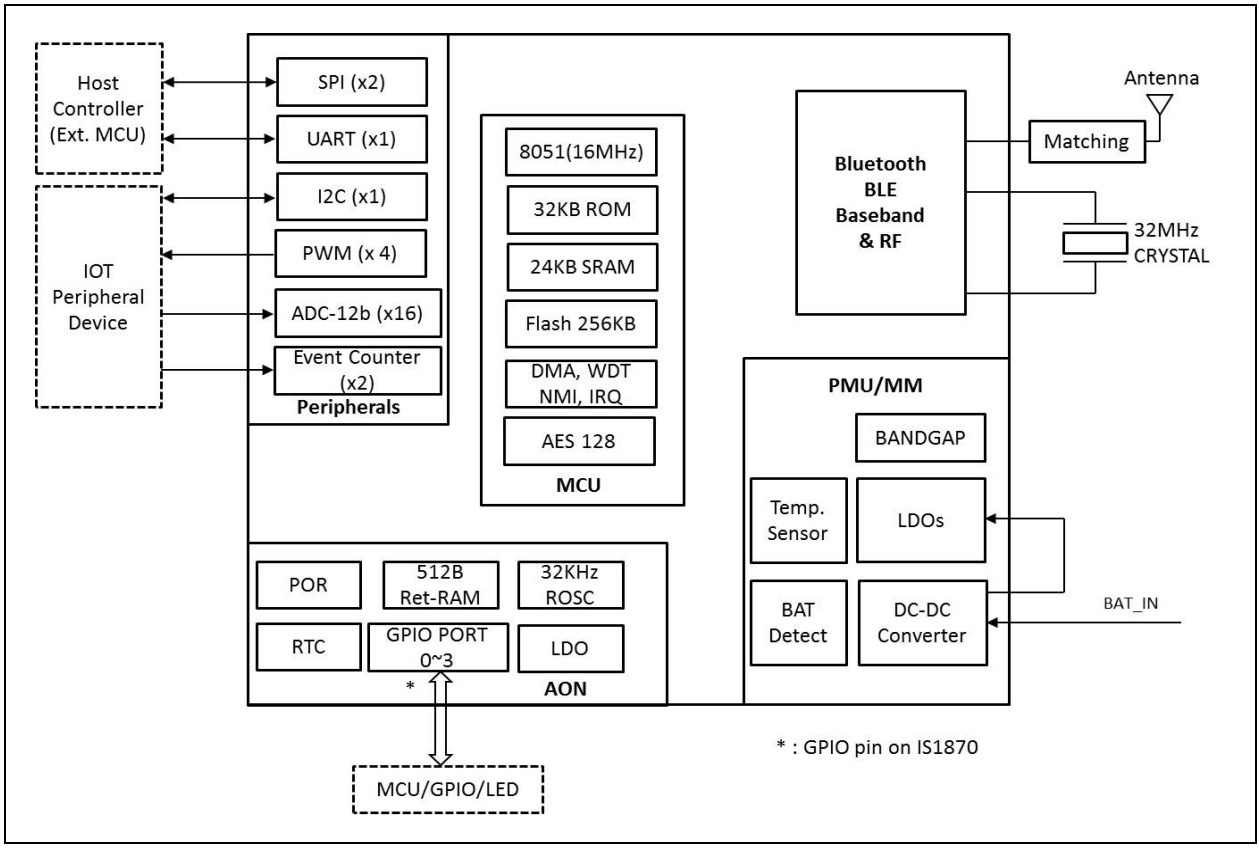


FIGURE 1-2: IS1871-BASED SYSTEM BLOCK DIAGRAM

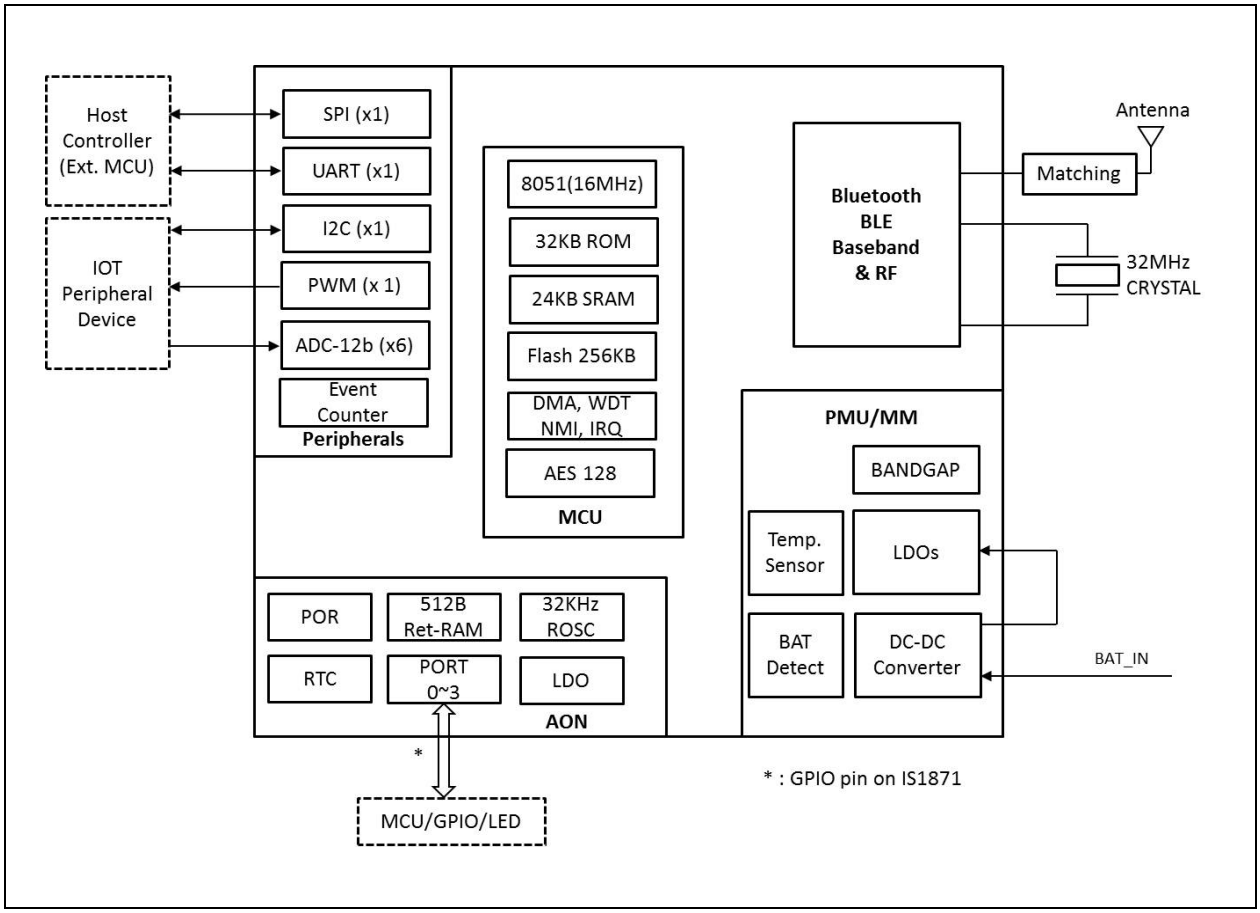


TABLE 1-1: KEY FEATURES

Feature/Modules	IS1870	IS1871
UART	1	1
GPIO	31	15
12-bit ADC Channels	16	6
PWM	4	1
SPI	2	1
I^2C	1	1
Total Pins	48	32
Size (mm)	6x6x0.9	4x4x0.9
Event Counter	2	0
AES-CMAC H/W Engine	Yes	Yes

Pin Description

Figure 1-3 and Figure 1-4 illustrate the IS1870 and IS1871 pin assignment details, and Table 1-2 lists the functions of the various pins.

FIGURE 1-3: IS1870 PIN ASSIGNMENT

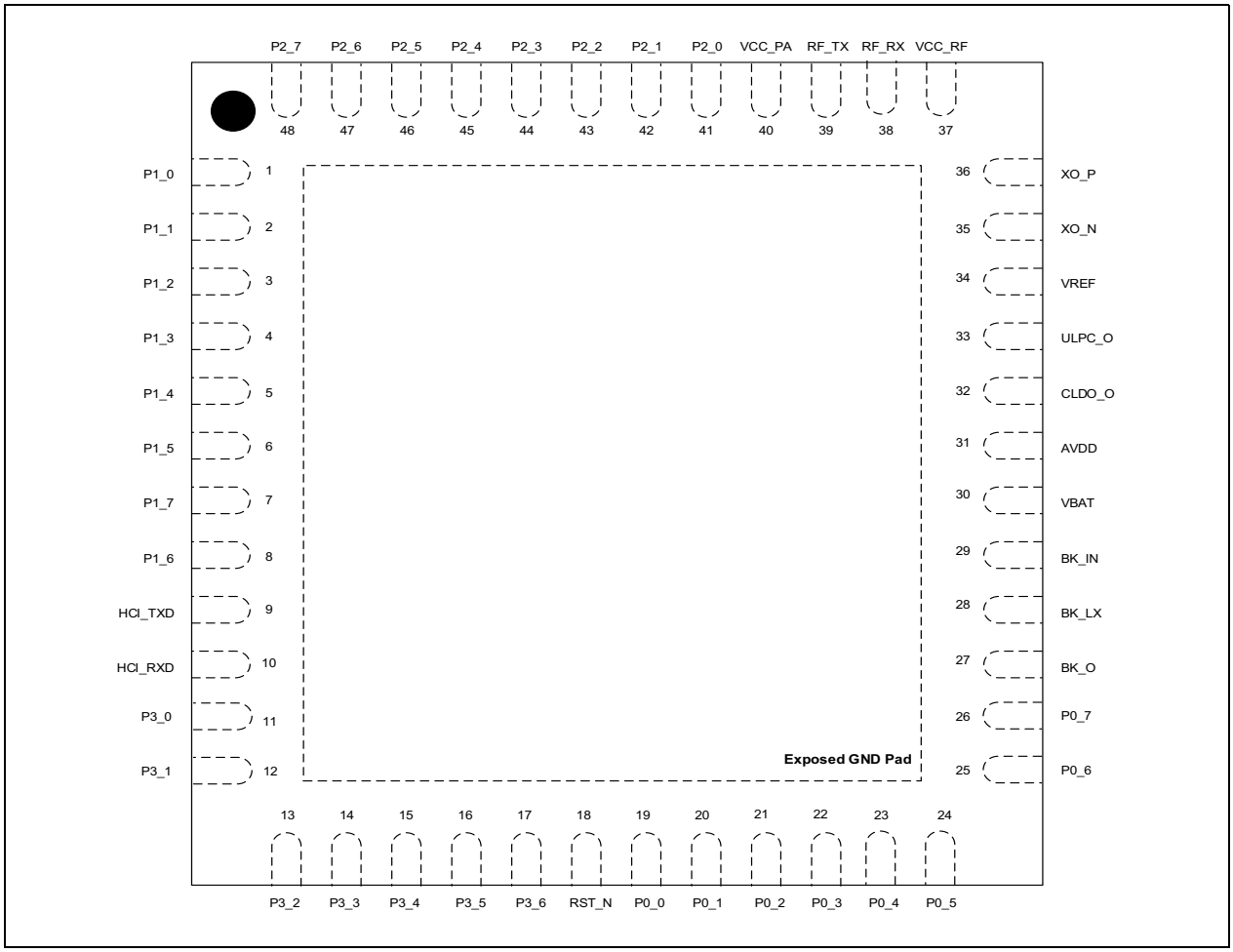


FIGURE 1-4: IS1871 PIN ASSIGNMENT

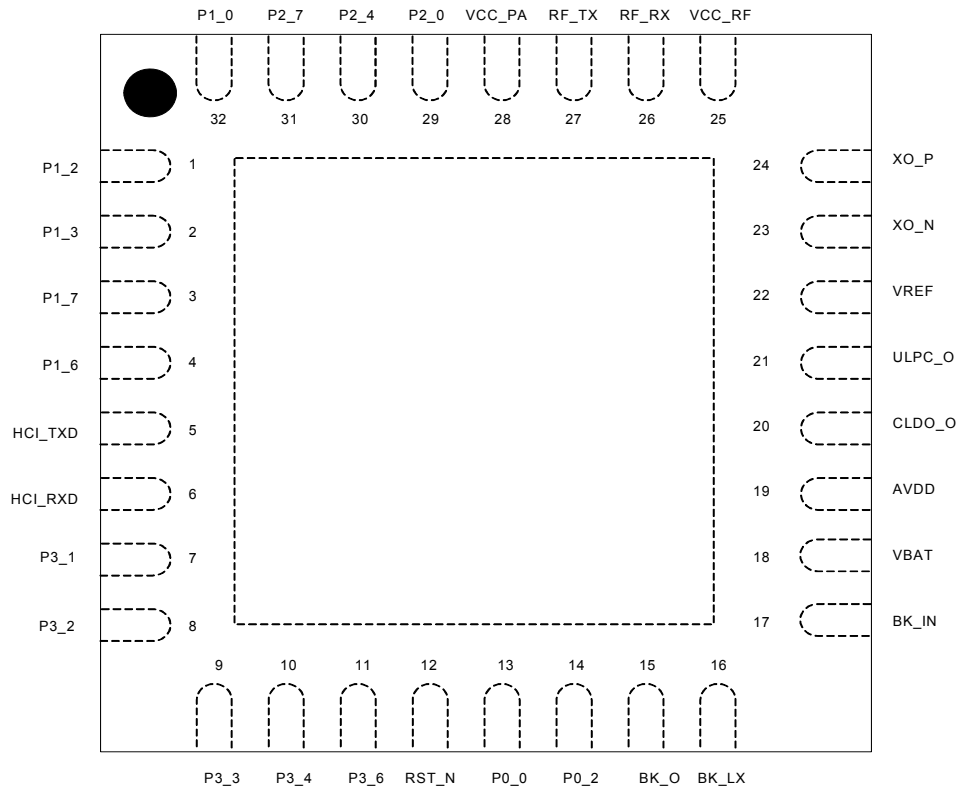


TABLE 1-2: PIN DESCRIPTION

IS1870 Pin No.	IS1871 Pin No.	Pin Name	Type	Description
1	32	P1_0	DIO AI	GPIO: P1_0 ADC input: AD8
2	—	P1_1	DIO AI DI	GPIO: P11 ADC input: AD9 SPI bus: MISO2: 2nd SPI bus (Master Mode)
3	1	P1_2	DIO AI I/O	GPIO: P1_2 ADC input: AD10 I^2C SCL
4	2	P1_3	DIO AI DIO	GPIO: P1_3 ADC input: AD11 I^2C SDA
5	—	P1_4	DIO AI DI	GPIO: P1_4 ADC input: AD12 Event Counter
6	—	P1_5	DIO AI DI	GPIO: P1_5 ADC input: AD13 Event Counter
7	3	P1_7	DIO AO	GPIO: P1_7 External 32.768 KHz Crystal Output: XO32K
8	4	P1_6	DIO AI	GPIO: P1_6 External 32.768 KHz Crystal input: XI32K
9	5	IOA HCI_TXD	DIO DO	GPIO HCI UART TXD
10	6	IOB HCI_RXD	DIO DI	GPIO HCI UART RXD
11	—	P3_0	DIO	GPIO: P3_0
12	7	P3_1	DIO DO	GPIO: P3_1 SPI bus: NCS, SPI Flash: CSN
13	8	P3_2	DIO DI	GPIO: P3_2 SPI bus: MISO, SPI Flash: SDO
14	9	P3_3	DIO DO	GPIO: P3_3 SPI bus: MOSI, SPI Flash: SDI
15	10	P3_4	DIO DO	GPIO: P3_4 SPI bus: SCLK, SPI Flash: SCK
16	—	P3_5	DIO AI	GPIO: P3_5 LED1
17	11	P3_6	DIO DO DO	GPIO: P3_6 UART flow-control RTS PWM0
18	12	RST_N	DI	External Reset
19	13	P0_0	DIO AI DI	GPIO: P0_0 ADC input: AD0 UART flow-control CTS
20	—	P0_1	DIO AI	GPIO: P0_1 ADC input: AD1

Legend: A = Analog D = Digital I = Input O = Output P = Power

IS1870 Pin No.	IS1871 Pin No.	Pin Name	Type	Description
21	14	P0_2	DIO AI AI	GPIO: P0_2 ADC input: AD2 LED0
22	—	P0_3	DIO AI	GPIO:P0_3 ADC input: AD3
23	—	P0_4	DIO AI	GPIO:P0_4 ADC input: AD4
24	—	P0_5	DIO AI	GPIO:P0_5 ADC input: AD5
25	—	P0_6	DIO AI	GPIO:P0_6 ADC input: AD6
26	—	P0_7	DIO AI	GPIO:P0_7 ADC input: AD7
27	15	BK_O	P	1.5V (for internal use, do not connect to external devices)
28	16	BK_LX	P	Buck output (1.55V). For internal use, do not connect to external devices
29	17	BK_IN	P	Buck input. Voltage Range: 1.9V~3.6V
30	18	VBAT	P	Battery input. Voltage Range: 1.9V~3.6V. For internal use, do not connect to external devices
31	19	AVDD	P	input of LDOs: CLDO, PALDO, and RFLDO
32	20	CLDO_O	P	1.2V CLDO Output: Core-logic and memories supply, connect to 1uF (X5R/X7R) capacitor
33	21	ULPC_O	P	1.2V Programmable ULPC Output: Always On-logic and retention memory supply (for internal use, do not connect to external devices)
34	22	VREF	P	PMU band-gap reference voltage output for LDOs and buck (for internal use, do not connect to external devices)
35	23	XO_N	A	32 MHz crystal input negative
36	24	XO_P	A	32 MHz crystal input positive
37	25	VCC_RF	P	Power input for VCO and RF (1.28V). Connect to 1uF (X5R/X7R) capacitor
38	26	RX	AI	RF receive path
39	27	TX	AO	RF transmit path
40	28	VCC_PA	P	Power supply for Power Amplifier (1.55V). Connect to 0.22uF X5R/X7R
41	29	P2_0	DIO	Mode Configuration H: Application mode L: Test mode
42	—	P2_1	DIO DO	GPIO: P2_1 PWM0
43	—	P2_2	DIO DO	GPIO: P2_2 PWM1
44	—	P2_3	DIO DO	GPIO: P2_3 PWM2
45	30	P2_4	DIO	GPIO: P2_4

Legend: A = Analog D = Digital I = Input O = Output P = Power

IS1870 Pin No.	IS1871 Pin No.	Pin Name	Type	Description
46	—	P2_5	DIO AI DO	GPIO: P2_5 ADC input: AD15 PWM3
47	—	P2_6	DIO	P26
48	31	P2_7	DIO AI DO	GPIO: P27 ADC input: AD14 SPI bus: NCS2, 2nd SPI bus (Master mode)

Legend: A = Analog D = Digital I = Input O = Output P = Power

NOTES:

2.0 SYSTEM BLOCK DETAILS

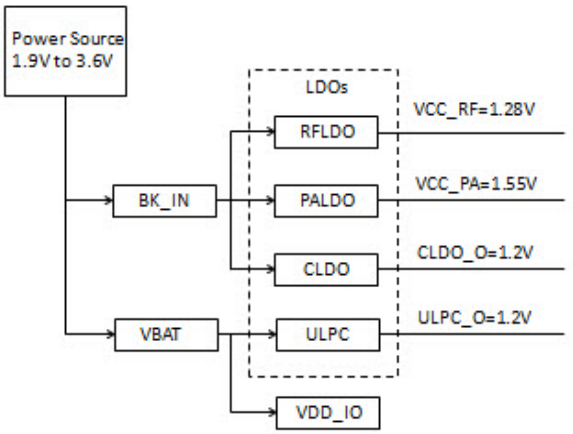
2.1 System Block Descriptions

Each system block of the IS1870/71 is described in this section.

2.1.1 PMU

The IS1870/71 includes a DC-DC converter and four LDOs. These LDOs can be configured for various operating modes and applications to suppress the peak current and maximize battery life, see Figure 2-1.

FIGURE 2-1: IS1870/71 POWER TREE



2.1.2 AON

AON is the hardware-based state machine that controls the power-up and power sequence. It includes a RTC timer and an I/O detector, which can wake-up the system from Standby mode or Power-Saving mode using time-out or I/O transition.

2.1.3 RF

The IS1870/71 has an on-chip RF circuit, a controller, and a modulator (Tx)/demodulator (Rx). The Tx is used to control the synthesizer's phase and output power, and modulate the data based on the BLE specifications. The Rx is used to decode the Bluetooth signal and optimize the performance, such as IQ-imbalance, suppress DC, and flick noise. It is also used to compensate the frequency drift and offset, filter out interference to maximize receiver sensitivity.

2.1.4 PERIPHERALS

The IS1870/71 interface is built-in to connect external MCU and sensors.

2.1.5 MCU

The IS1870/71 has an 8051 core ROM, RAM, embedded Flash to schedule the BLE tasks, process BLE protocol stacks, and profiles.

2.2 System Block Specification

The following are system block specifications:

2.2.1 RF

- Bluetooth BT4.2 LE compliant SoC
- Frequency: 2.402 GHz to 2.480 GHz
- Programmable transmit output power up to +2 dBm maximum
- -25 dBm minimum Tx power to search near-by devices.
- -90 dBm typical receiver power sensitivity
- Digital RSSI indicator (-50 dBm~-90 dBm)
- -20°C to 70°C BLE RF certified

2.2.2 PMU

- Operating battery input voltage range: 1.9V~3.6V
- 1.28V RFLDO: RF IP power supply
- 1.55V PALDO: RF Tx power amplify supply
- 1.2V CLDO: Core-logic and memories supply
- 1.55V DC-DC switching buck converter
- 1.2V programmable ULPC to supply AON-logic and retention memory
- AON-logic to control power-up, power-down and wake up procedures
- Internal 32 kHz(+/-250 ppm) ultra low-power oscillator
- Power-on Reset

2.2.3 MCU

- 1T 8051 with scalable clock
- ROM: 32 KB
- Main SRAM: 24 KB
- Patch-RAM: 8KB
- Retention SRAM: 512B for RF coefficients and system information backup
- Embedded Flash: 256 KB for Device Firmware Upgrade (DFU) and run-time data storage

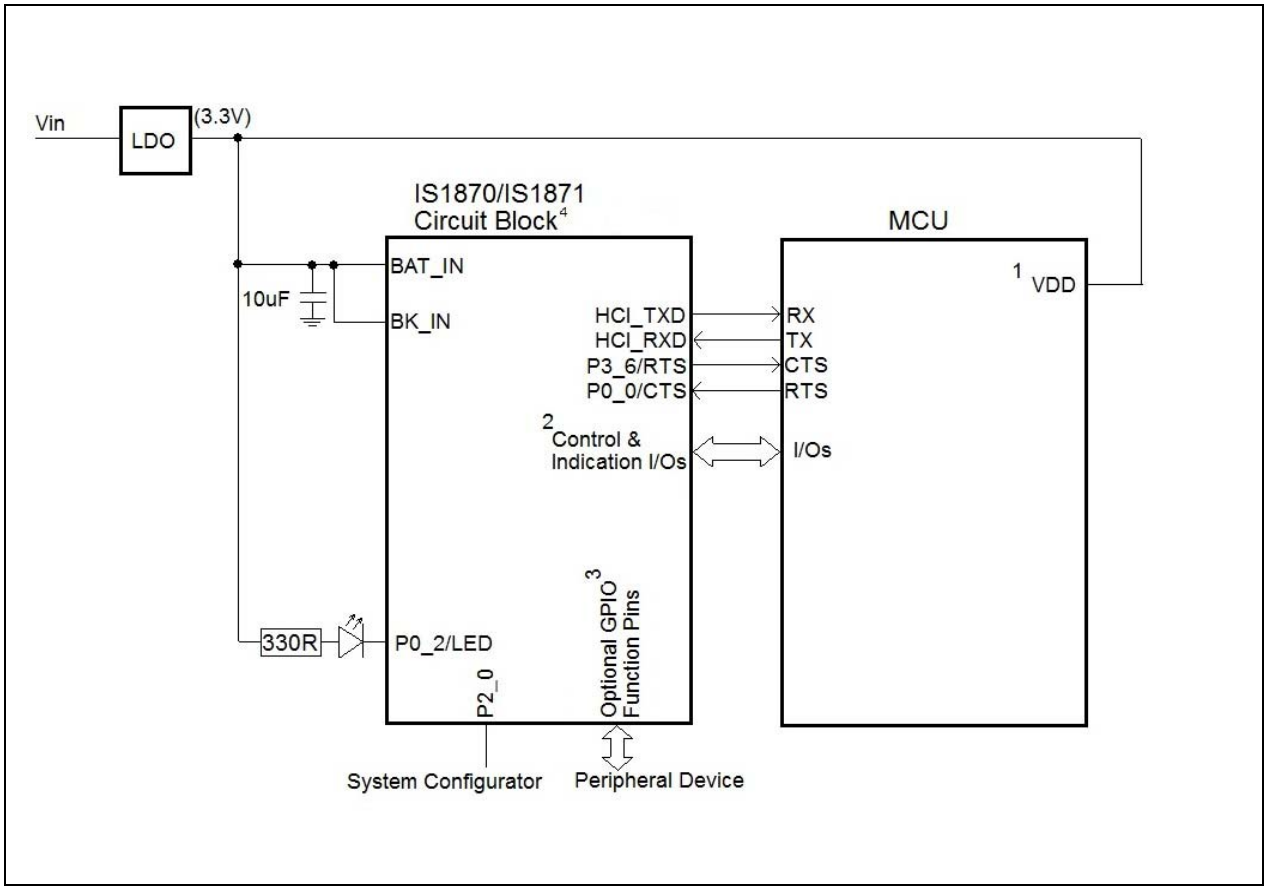
2.2.4 PERIPHERALS

- Flexible GPIO pin configuration
- ADC:
  - 0V~3.6V, 12-bit SDM-ADC with 16-channel (IS1870)/6-Channel (IS1871) hybrid-I/O (Multi-Function). It can be configured as ADC or GPIO input
- Internal 1.9V~3.6V battery voltage monitor
- Precision Temperature Sensor (PTS) (-20°C ~70°C, +/-3°C accuracy)
- 4 MHz clock-rate full duplex 4-wire master/slave SPI with 256 bytes buffer DMA
- HCI over UART up to 921600 bps with flow-control
- 2 wire serial interface (compatible to I^2C)
- General-purpose I/O pins with input internal pull-up /Hi-Z selectable
- 24-bit low-power Real Time Counter (RTC) for background timer in standby mode
- Watchdog timer
- Event Counter option (P1_4,P1_5) provides capture/counter function to external events for frequency calculation. Provides 1K/32K/1M/16M clock rate option to count the frequency range from 60 Hz to 1 MHz. Continuous/One shot count mode can be selected.
- Specific GPIO pins (P1_6, P1_7) support external 32.768 KHz crystal option for RTC.
- PWM:
  - 16 bits PWM design
  - 4 Individual frequency and individual duty cycle channel outputs multiplexed with GPIO pin (P2_1, P2_2, P2_3, P2_5)
  - Three clock source (32K, 1M, 16M) selection to program frequency range from 0.488 Hz to 8 MHz
  - Double buffers output compare registers and top register to avoid glitch
  - Two pair output configurable as inverse channel.

2.3 Host MCU Interface Over UART

Figure 2-2 illustrates a block diagram of the IS1870/71 SoC with MCU BLE application circuit. In the diagram the power supply (3.3V), UART interface, and GPIO control and indication are listed.

FIGURE 2-2: IS1870/71 APPLICATION BLOCK DIAGRAM WITH MCU



Note 1: Ensure VDD_I/O and MCU VDD voltages are compatible.

2: Control and indication ports are configurable in UI tool.

3: Optional GPIO function includes ADC, PWM, I^2C and SPI functions.

4: The GPIO applications of the IS1871 depend on the existed pin out. Some of the GPIO pins are not supported in the IS1871.

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3.0 ELECTRICAL CHARACTERISTICS

This section provides an overview of the IS1870/71 electrical characteristics. Additional information will be provided in future revisions of this document.

Absolute maximum ratings for the IS1870/71 devices are listed below. Exposure to the maximum rating conditions for extended periods may affect device reliability. Functional operation of the device at these or any other conditions, above the parameters indicated in the operation listings of this specification, is not implied.

Absolute Maximum Ratings

(See Note 1)

Ambient temperature under bias ..... -20°C to +70°C
Storage temperature ..... -40°C to +125°C
Voltage on V_{DD} with respect to V_{SS} ..... -0.3V to +3.6V
Voltage on any pin with respect to V_{SS} ..... -0.3V to (V_{DD} + 0.3V)
Maximum output current sunk by any I/O pin ..... 12 mA
Maximum output current sourced by any I/O pin ..... 12 mA

Note 1: Stresses above those listed under **"Absolute Maximum Ratings"** may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions, above those indicated in the operation listings of this specification, is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

TABLE 3-1: ABSOLUTE MAXIMUM RATING

Symbol	Condition	Min.	Max.	UNIT
Supply voltage (V_{DD})	—	-0.3	3.6	V
Voltage on any digital pin	—	-0.3	V_{DD} + 0.3 ≤ 3.9	V
Storage temperature range	—	-40	125	°C
ESD	All pins, excluding RF TX pin, according to machine model, JEDEC EIA/JESD22-A115-C	—	±200	V
	All Pins, according to machine model, JEDEC EIA/JESD22-A115-C	—	±150	V
	According to human-body model, EDEC EIA/JESD22-A114-F	—	±2	kV
	According to charged-device model, JESD22-C101-C	—	±150	V

TABLE 3-2: RECOMMENDED OPERATING CONDITIONS

Symbol	Min.	Typ.	Max.
Ambient operating temperature range	–20°C	+25°C	+70°C
PMU			
V_{DD}(V_{BAT}, BK_IN), AV_{DD}	1.9V	3.0V	3.6V
VCC_RF	1.22V	1.28V	1.34V
VCC_PA	1.5V	1.55V	1.98V
CLDO_O, VREF	1.1V	1.2V	1.32V
ULPC_O	1.1V	1.2V	1.32V
RST_N	1.9V	3.0V	3.6V
Other I/O	1.9V	—	3.6V
GPIO			
VIH (Input High Voltage)	0.7 V_{DD}	—	V_{DD}
VIL (Input Low Voltage)	VSS	—	0.3 V_{DD}
VOH (Output High Voltage) (High drive, 12 mA)	0.8 V_{DD}	—	V_{DD}
VOL (Output Low Voltage) (High drive, 12 mA)	VSS	—	0.2 V_{DD}
Pull-up Resistance	34K	48K	74K
Pull-down Resistance	29K	47K	86K
Supply Current			
Tx mode peak current at V_{DD}=3V, Tx=0 dBm, Buck mode	—	—	13 mA
Rx mode peak current at V_{DD}=3V, Buck mode	—	—	13 mA
Link static current		60 uA	
Standby current	1.9 uA	—	2.9 uA
Power-Saving	1 uA	—	1.7 uA
Analog-to-Digital Converter (ADC)			
Full scale (BAT_IN)	0V	3.0V	3.6V
Full scale (AD0~AD15)	0V	—	3.6V
Conversion time (ENOB 8-bit)	—	131 uS	—
Conversion time (ENOB 10-bit)	—	387 uS	—
Operating current	—	—	500 uA
DNL	-1.12 LSB	—	+1.12 LSB
INL	-4.38 LSB	—	+4.38 LSB
Precise Temperature Sensor (PTS)			
Detect range	-20°C	—	70°C
Digital Output	1387	—	2448
Resolution	—	12 bits/°C	—
Accuracy	-3°C	—	+3°C
Conversion time (ENOB 10-bit)	—	12.35 mS	—
Operating current	—	—	200 uA

3.1 Current Consumption Details

3.1.1 Tx/Rx MODE PEAK CURRENT CONSUMPTION DETAILS

Figure 3-1 and Figure 3-2 illustrate the Tx/Rx mode peak current consumption in connected mode. In both the modes, the peak current of the VBAT input is about 13 mA.

FIGURE 3-1: Tx CURRENT CONSUMPTION IN CONNECTED MODE

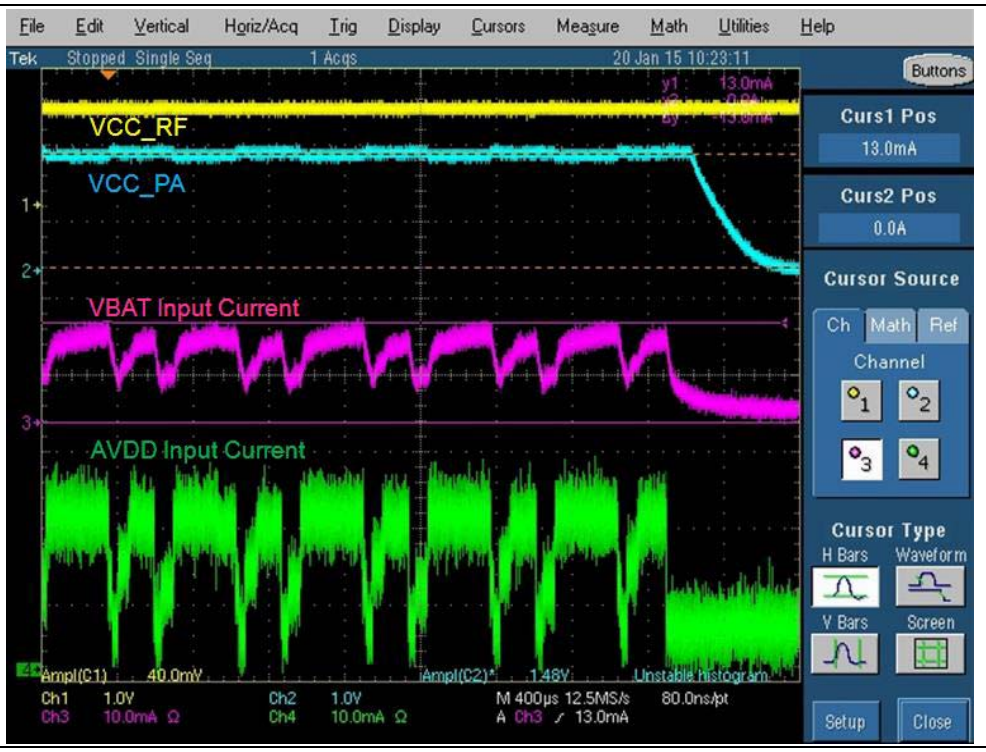
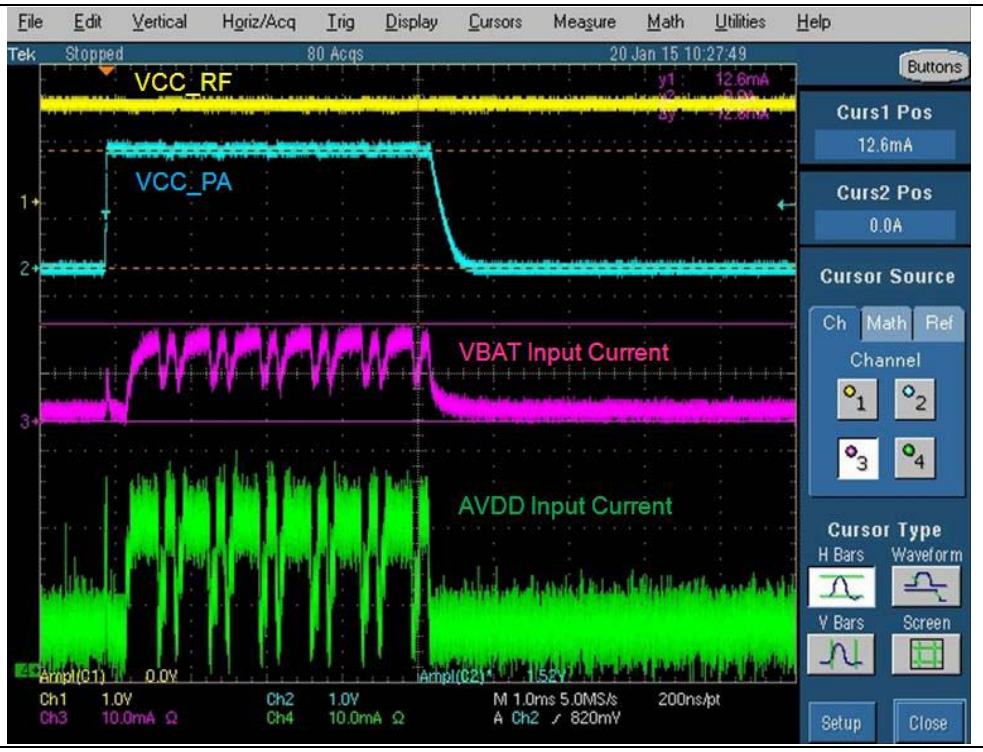


FIGURE 3-2: Rx CURRENT CONSUMPTION IN CONNECTED MODE



For additional information related to the current consumption measurements, test condition, and test environment setup, refer to the "*BM70 BLEDK3 Application Note*". This Application Note covers the testing of the Tx/Rx data transfer in connected mode and four basic modes of BLE devices.

Table 3-3. provides status definition of the BLEDK3 application.

TABLE 3-3: STATUS DEFINITION OF BLEDK3 APPLICATION

Status	Description
Shutdown Mode	BLEDK3 is shutdown.
Standby Mode	BLEDK3 sends advertising packets and wait for connection. BLEDK3 is discoverable and connectible.
BLE Connected Mode	BLE link is established and CCCD of ISSC_Transparent_Tx characteristic is disabled (see **Note 1**).
Transparent Service Enabled Mode	BLE link is established and CCCD of ISSC_Transparent_Tx characteristic is enabled (see **Note 1**).

Note 1: CCCD stands for Client Characteristic Configuration in GATT service characteristics.

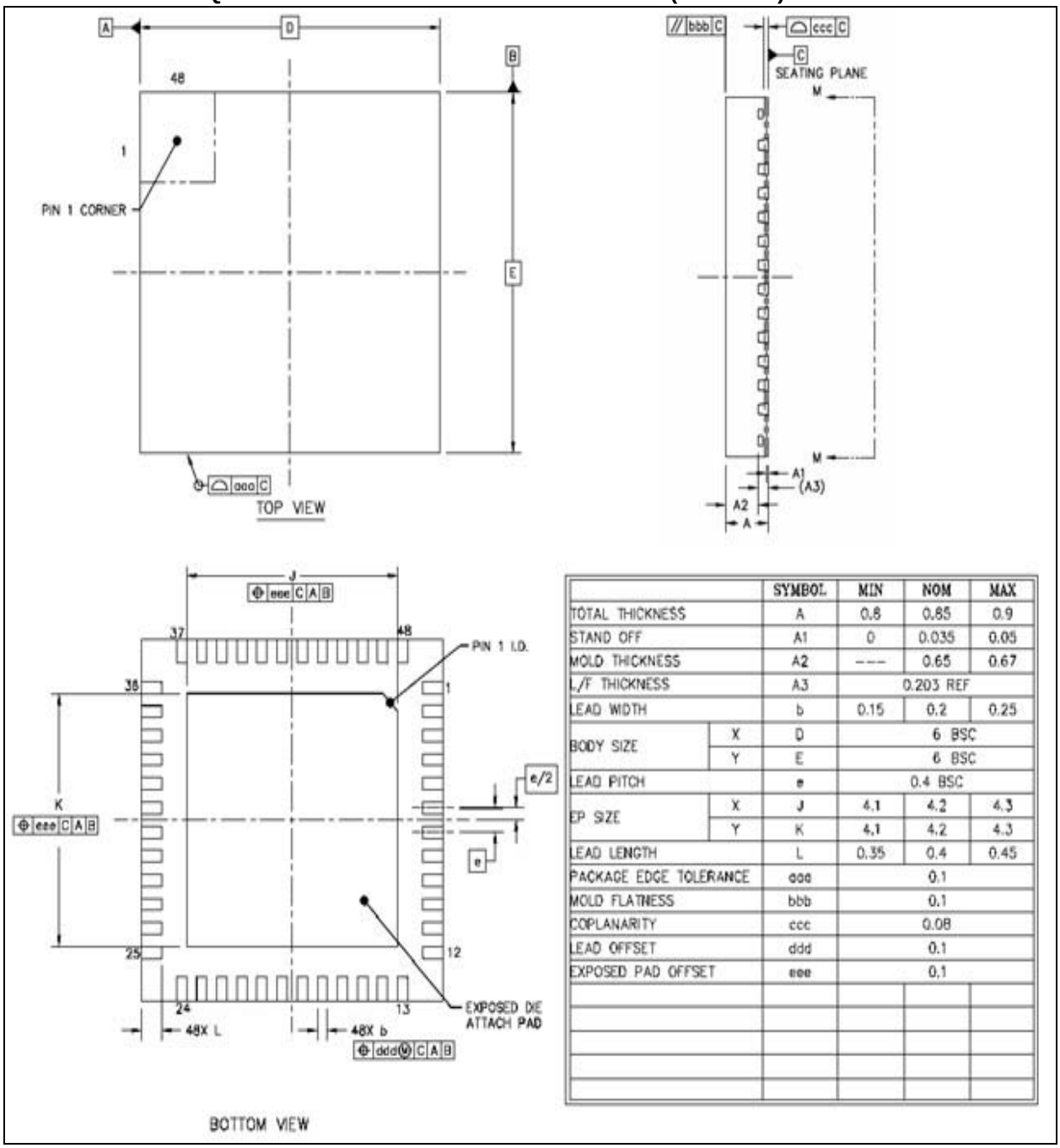
NOTES:

4.0 PACKAGE INFORMATION

The following are package marking information of the IS1870SF module.

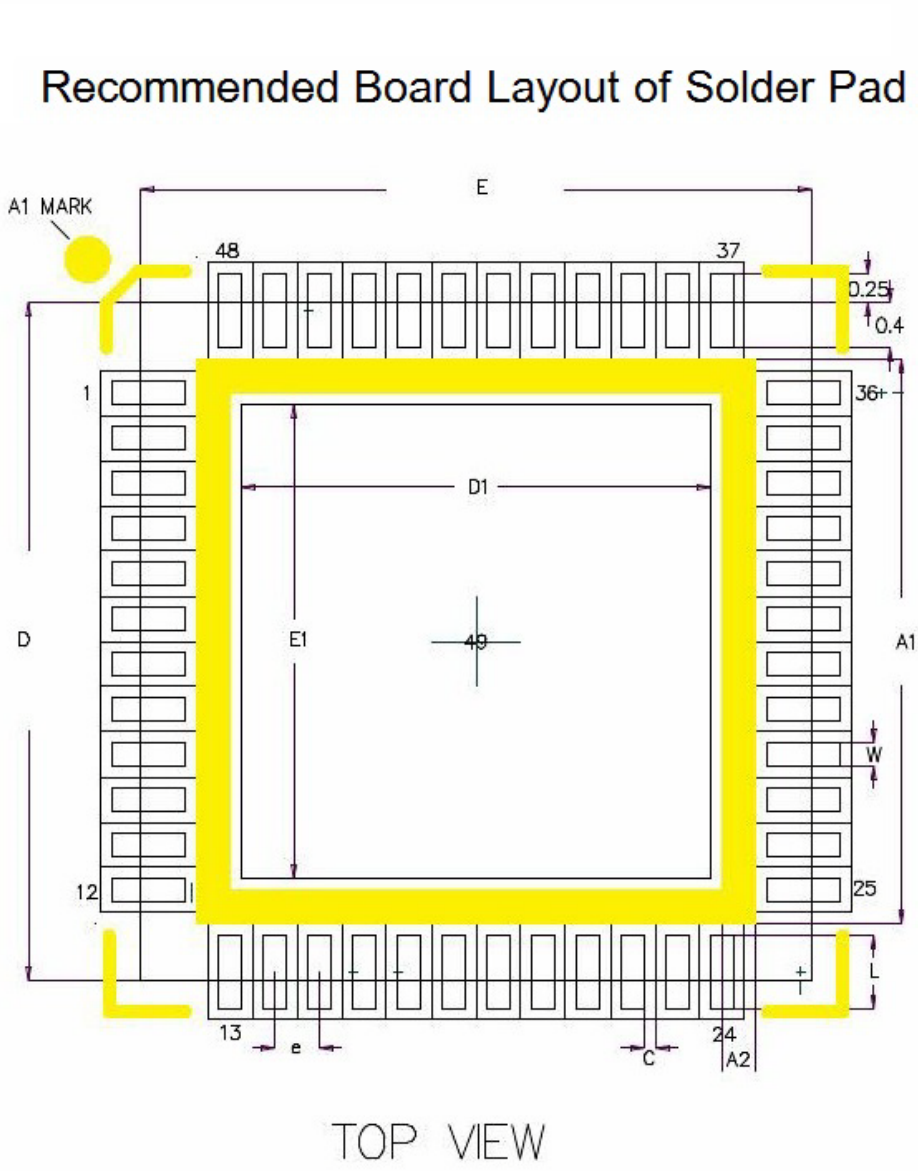
4.1 QFN48 6x6 Chip Outline (IS1870SF)

FIGURE 4-1: QFN48 6X6 PACKAGE SIZE INFORMATION (IS1870SF)



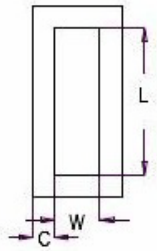
		SYMBOL	MIN	NOM	MAX
TOTAL THICKNESS		A	0.8	0.85	0.9
STAND OFF		A1	0	0.035	0.05
MOLD THICKNESS		A2	---	0.65	0.67
L/F THICKNESS		A3		0.203 REF	
LEAD WIDTH		b	0.15	0.2	0.25
BODY SIZE	X	D		6 BSC	
	Y	E		6 BSC	
LEAD PITCH		e		0.4 BSC	
EP SIZE	X	J	4.1	4.2	4.3
	Y	K	4.1	4.2	4.3
LEAD LENGTH		L	0.35	0.4	0.45
PACKAGE EDGE TOLERANCE		aaa		0.1	
MOLD FLATNESS		bbb		0.1	
COPLANARITY		ccc		0.08	
LEAD OFFSET		ddd		0.1	
EXPOSED PAD OFFSET		eee		0.1	

FIGURE 4-2: QFN48 6X6 FOOTPRINT INFORMATION (IS1870SF)



	SYMBOL	COMMON DIMENSIONS		
		MIN.	NOR.	MAX.
SILKSCREEN TOP L	A1		5	REF
SILKSCREEN TOP W	A2		0.3	REF
BODY SIZE	D		6	BSC
	E		6	BSC
EXPOSED PAD SIZE	D1		4.2	BSC
	E1		4.2	BSC
LEAD LENGTH	L		0.65	
LEAD WIDTH	W		0.2	
SOLDER MASKER OPEN	c		0.1	
LEAD PICTH	e		0.4	
LEAD COUNT	n1		48	

UNIT : MM

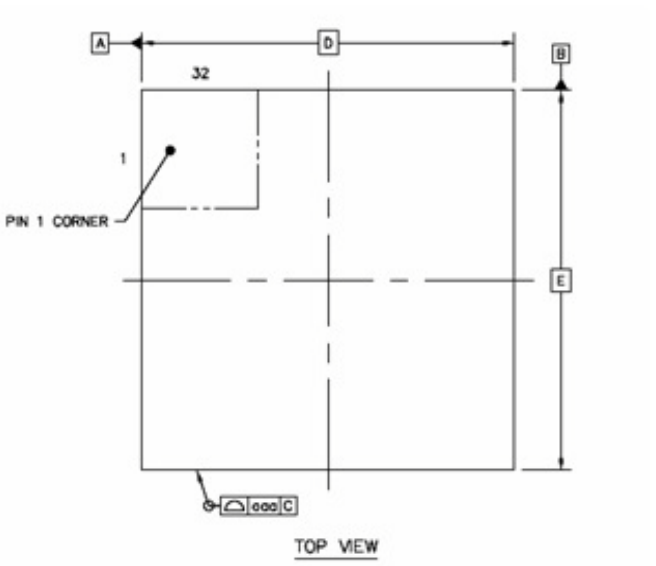


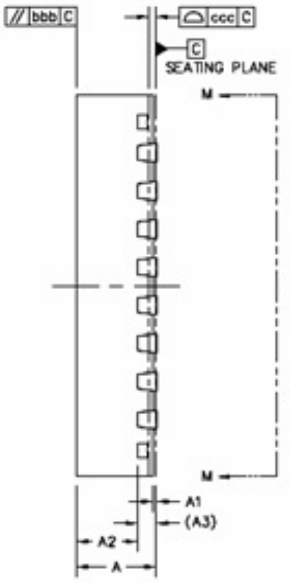
SOLDERMASK OPENING OUTSIDE OF LAND

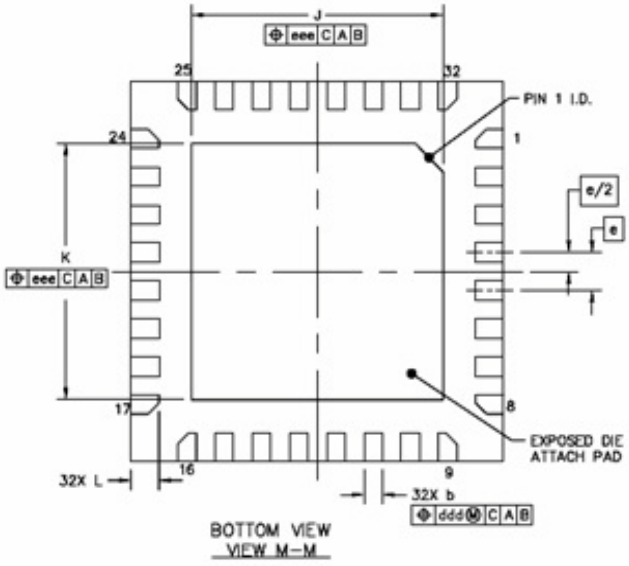
SCALE 2:1

4.2 QFN32 4x4 Chip Outline (IS1871SF)

FIGURE 4-3: QFN32 4X4 PACKAGE SIZE INFORMATION (IS1871SF)

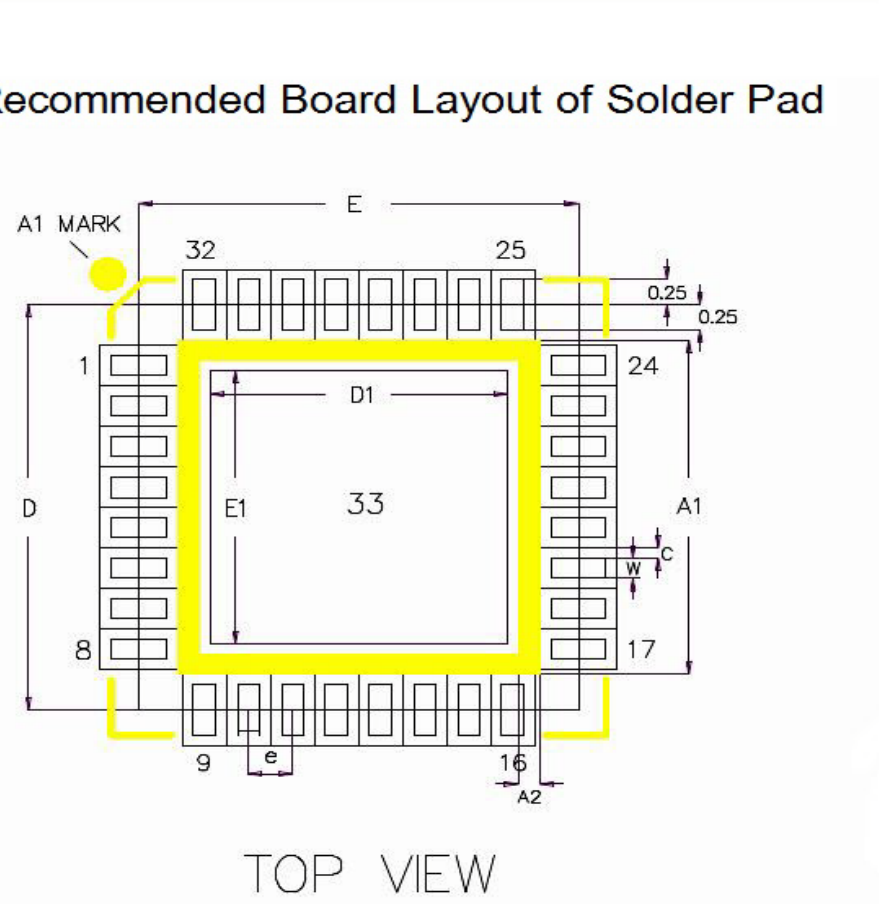






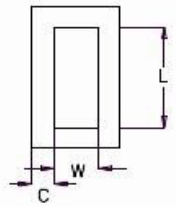
		SYMBOL	MIN	NOM	MAX
TOTAL THICKNESS		A	0.8	0.85	0.9
STAND OFF		A1	0	0.035	0.05
MOLD THICKNESS		A2	---	0.65	0.67
L/F THICKNESS		A3		0.203 REF	
LEAD WIDTH		b	0.15	0.2	0.25
BODY SIZE	X	D		4 BSC	
	Y	E		4 BSC	
LEAD PITCH		e		0.4 BSC	
EP SIZE	X	J	2.6	2.7	2.8
	Y	K	2.6	2.7	2.8
LEAD LENGTH		L	0.25	0.3	0.35
PACKAGE EDGE TOLERANCE		aaa		0.1	
MOLD FLATNESS		bbb		0.1	
COPLANARITY		ccc		0.08	
LEAD OFFSET		ddd		0.1	
EXPOSED PAD OFFSET		eee		0.1	

FIGURE 4-4: QFN32 FOOTPRINT INFORMATION (IS1871SF)



	SYMBOL	COMMON DIMENSIONS		
		MIN.	NOR.	MAX.
SLKSCREEN TOP L	A1		3.3	REF
SLKSCREEN TOP W	A2		0.2	REF
BODY SIZE	D		4	BSC
	E		4	BSC
EXPOSED PAD SIZE	D1		2.7	BSC
	E1		2.7	BSC
LEAD LENGTH	L		0.5	
LEAD WIDTH	W		0.2	
SOLDER MASKER OPEN	c		0.1	
LEAD PICTH	e		0.4	
LEAD COUNT	n1		32	

UNIT : MM

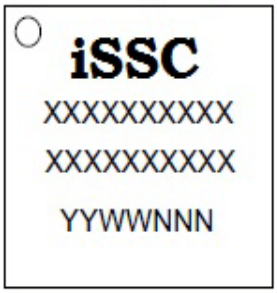


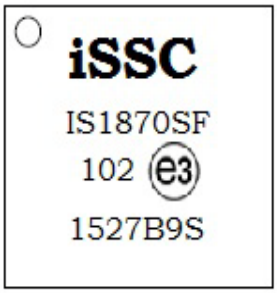
SOLDERMASK OPENING OUTSIDE OF LAND

SCALE 2:1

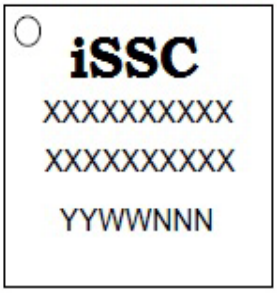
4.3 Package Marking Information

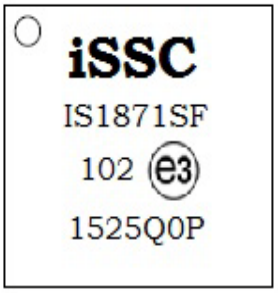
48-Lead QFN (6x6x0.9 mm)





32-Lead QFN (4x4x0.9 mm)





Legend:	XX...X	Customer-specific information
	Y	Year code (last digit of calendar year)
	YY	Year code (last 2 digits of calendar year)
	WW	Week code (week of January 1 is week '01')
	NNN	Alphanumeric traceability code
		Pb-free JEDEC designator for Matte Tin (Sn)
	*	This package is Pb-free. The Pb-free JEDEC designator (e3) can be found on the outer packaging for this package.

Note: In the event the full Microchip part number cannot be marked on one line, it will be carried over to the next line, thus limiting the number of available characters for customer-specific information.

NOTES:

5.0 REFLOW PROFILE AND STORAGE CONDITION

This chapter describes reflow profiles and stencil information of the IS1870/71 SoC, see Figure 5-1 and Figure 5-2.

5.1 Stencil of SMT Assembly Suggestion

5.1.1 STENCIL TYPE & THICKNESS

- Laser cutting
- Stainless steel
- Thickness: 0.5 mm Pitch, thickness < 0.15 mm

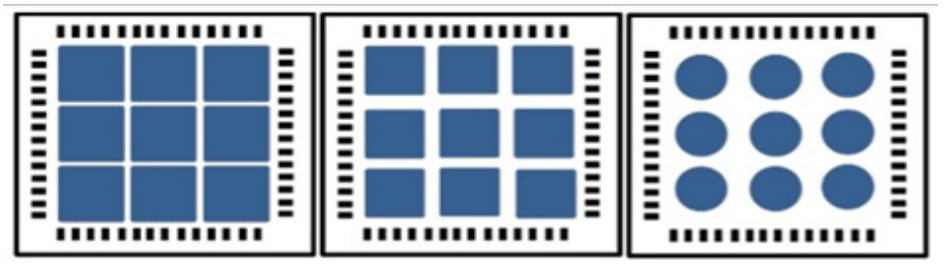
5.1.2 APERTURE SIZE AND SHAPE FOR TERMINAL PAD

- Aspect ratio (width/thickness) >1.5
- Aperture shape
  - The stencil aperture is designed to match the pad size on the PCB.
  - Oval-shape opening should be used to get the optimum paste release.
  - Rounded corners to minimize clogging.
  - Positive taper walls (5° tapering) with bottom opening larger than the top.

5.1.3 APERTURE DESIGN FOR THERMAL PAD

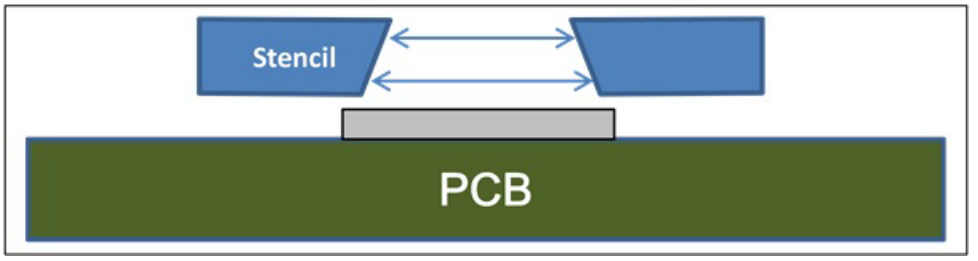
- Small multiple openings should be used instead of one big opening.
- 60~80% solder paste coverage
- Rounded corners to minimize clogging
- Positive taper walls (5° tapering) with bottom opening larger than the top

FIGURE 5-1: REFLOW PROFILE



Do not recommend Coverage 91% | Recommend Coverage 77% | Recommend Coverage 65%

FIGURE 5-2: STENCIL TYPE

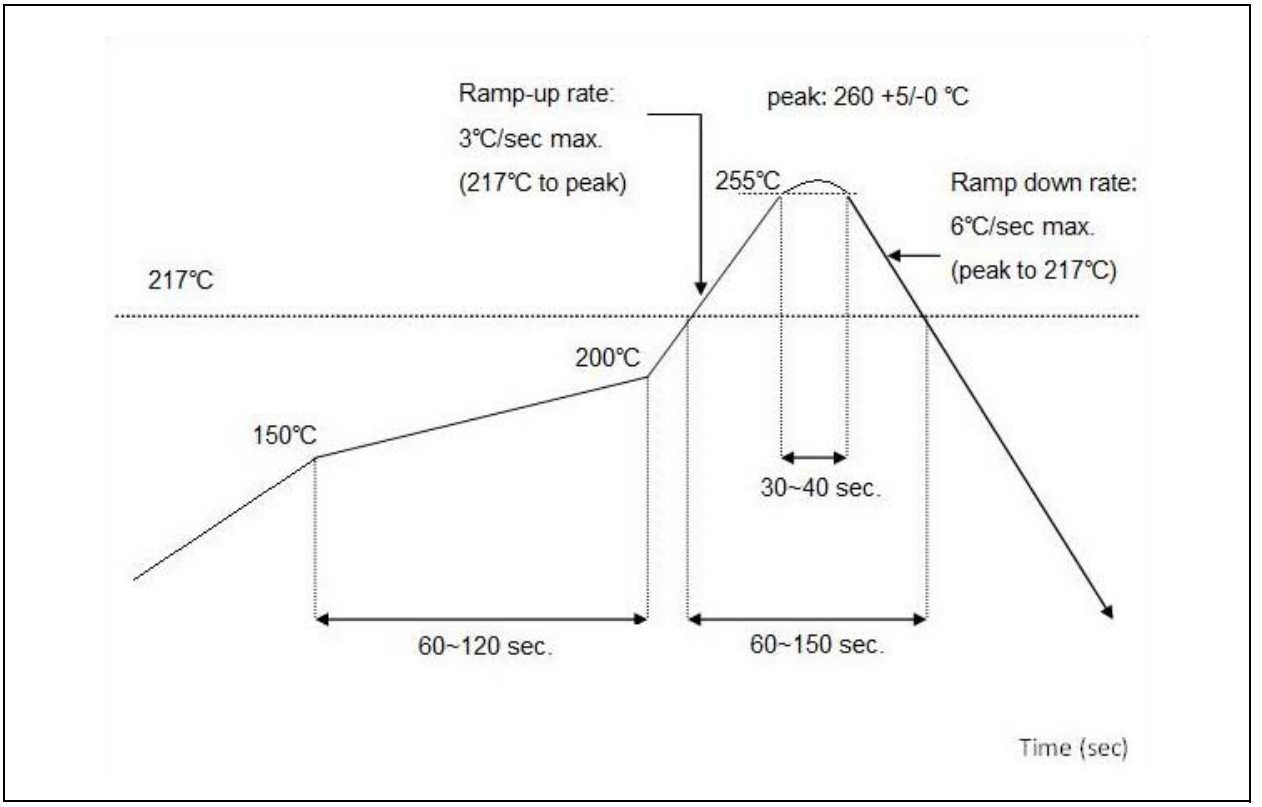


5.2 260 ℃ Reflow Profile

Figure 5-3 illustrates the reflow profile and the following are its specific features:

- Standard Condition: IPC/JEDEC J-STD-020
- Preheat: 150~200 ℃ ~60~120 seconds
- Average ramp-up rate (217 ℃ to peak): 3 ℃ /sec max.
- Temperature maintained above 217: 60~150 seconds
- Time within 5 ℃ of peak temperature: 30 ~ 40 seconds.
- Peak temperature:260 +5/-0 ℃
- Ramp-down rate (peak to 217 ℃): 6 ℃ /sec. max.
- Time 25 ℃ to peak temperature: 8 minutes max.
- Cycle interval: 5 minutes

FIGURE 5-3: REFLOW PROFILE



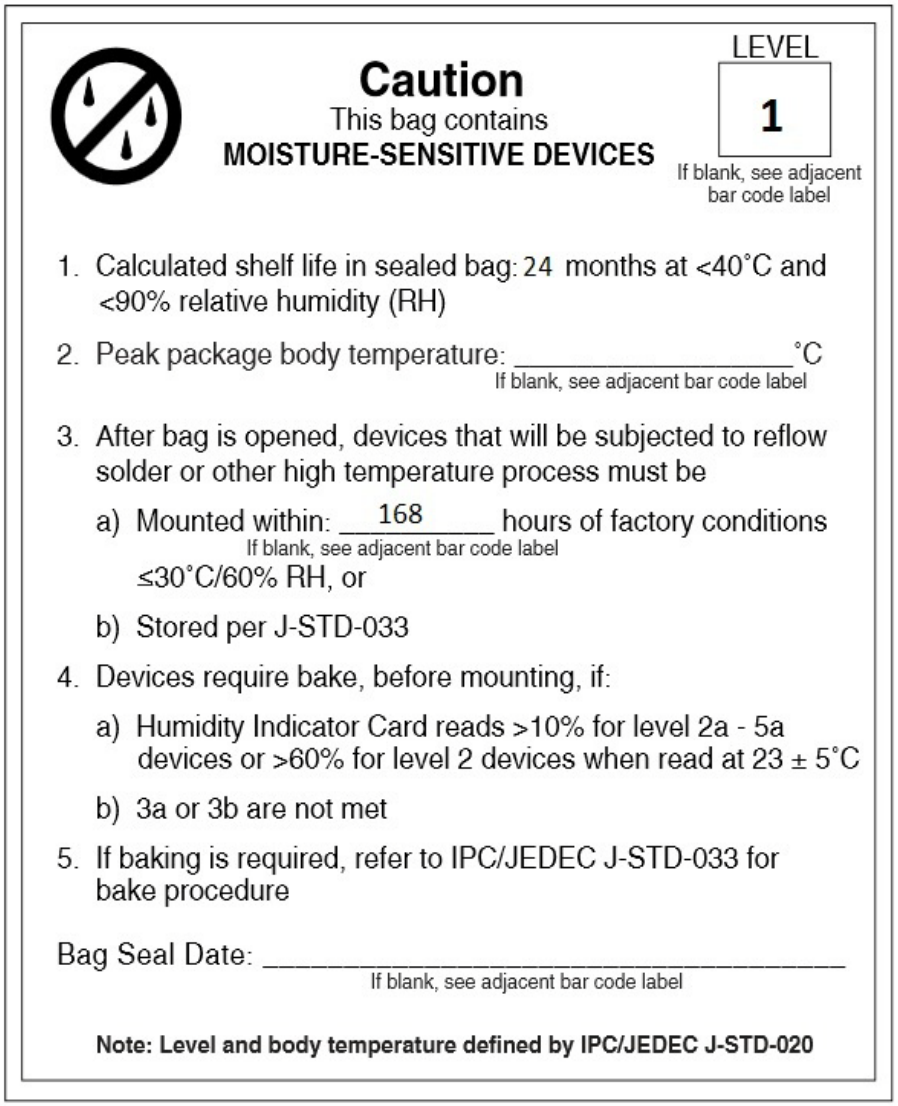
5.3 Storage Condition

Users need to follow these specific storage conditions for the IS1870x SoC.

- Calculated shelf life in the sealed bag: 24 months at <40 ℃ and <90% Relative Humidity (RH).
- After the bag is opened, devices that are subjected to reflow solder or other high temperature process must be mounted within 168 hours of factory conditions, i.e <30 ℃ /60% RH.

Figure 5-4 shows chip bag labeling details. Please note only point no. 1, 3, and 4 are applicable for the 1870x.

FIGURE 5-4: CHIP BAG LABEL



NOTES:

6.0 ORDERING GUIDE

Table 6-1 describes the ordering information for the IS1870/71.

TABLE 6-1: ORDERING GUIDE

Device	Bluetooth Version	Package	Part No.
IS1870	Bluetooth Low Energy SoC, BLE 4.2 compliant	48-lead QFN, 6x6x0.9mm, 0.4 mm pitch	IS1870SF
IS1871	Bluetooth Low Energy SoC, BLE 4.2 compliant	32-lead QFN, 4x4x0.9mm, 0.4 mm pitch	IS1871SF

NOTES:

APPENDIX A: REFERENCE CIRCUIT

A typical application circuit of the IS1870 and IS1871 are shown in Figure A-1 and Figure A-2., which lists the RF matching circuit, PMU power tree, LED option, test points, and configuration table. The GPIOs can be configured to general I/O functions or the function of ADC, PTS, PWM, and external 32.768 KHz crystal.

FIGURE A-1: IS1870 APPLICATION CIRCUIT

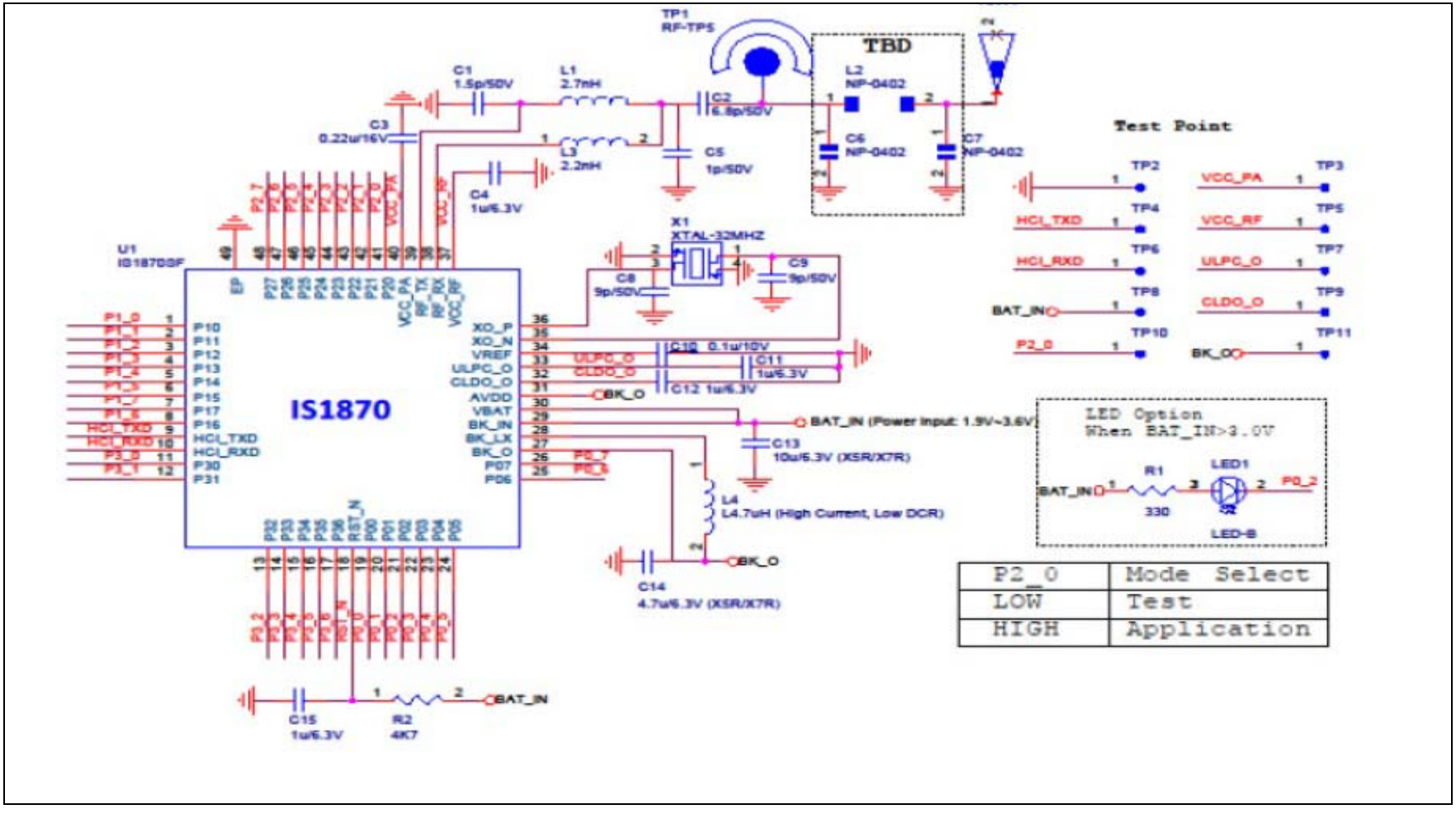
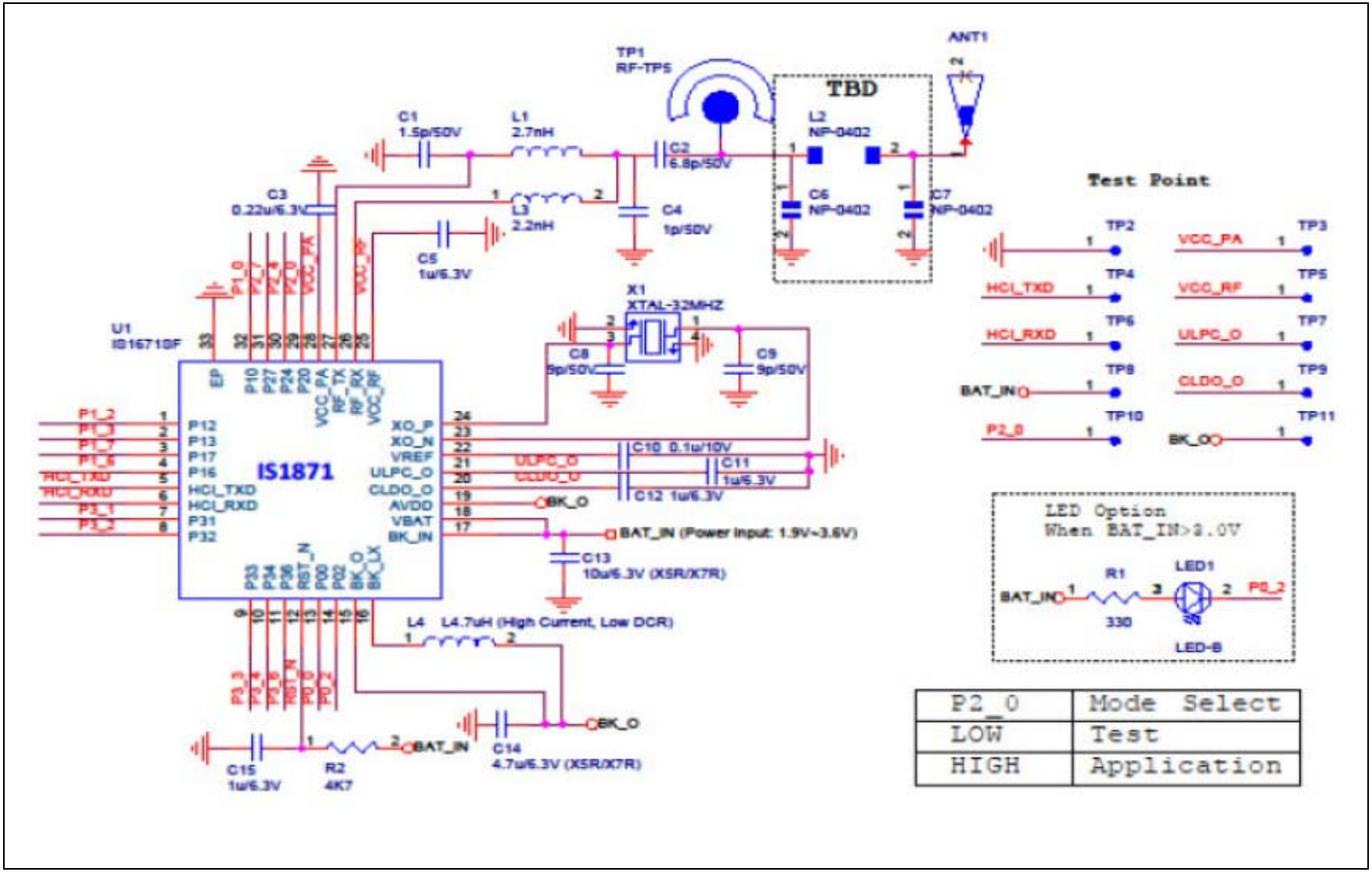


FIGURE A-2: IS1871 APPLICATION CIRCUIT



P2_0	Mode Select
LOW	Test
HIGH	Application

APPENDIX B: LAYOUT GUIDELINES

B.1 RF Matching

The RF traces (including Tx, Rx, and antenna path) on the PCB should match 50Ω impedance. In Figure A-1, value of L1, L3, C1, C2, and C5 are fixed. The antenna matching components C6, C7, and L2 should be adjusted to match the 50Ω 2.4 GHz antenna.

B.2 PMU

PMU section (V_{BAT}, BK_IN, BK_O, BK_LX, AV_{DD}, ULP-C_O, CLDO_O, V_{REF}) components should be kept close to the IS1870/71 as possible.

Table C-1 provides a detailed specification of L4. Layout trace of buck L&C to be given special consideration. For additional information on PCB Design Guidelines, please contact your local Microchip sales office.

The L4 and C14 of Buck section, shown in Figure A-1, should be selected carefully. Capacitor C14 is either 4.7 uF/6.3V, X5R, or X7R type. The inductor L4 need to be high current (I_{DC}>300mA) and low DCR(<1Ω) type.

B.3 Crystal

The XI 32 MHz crystal specification should be within the +/-10 ppm range, see Figure A-1.

APPENDIX C: BILL OF MATERIAL

TABLE C-1: IS1870 CIRCUIT BILL OF MATERIAL

Item	Quantity	Specification	Part Number	Manufacturer	Note
1	1	ANT AT5020-B2R8HAA 2.4 GHZ L5.0 W2.0	ANT1	ACX	—
2	1	CHIP CAP C 1.5P 50V C 0402 NPO	C1	WALSIN	—
3	1	CHIP CAP C 6.8P 50V C 0402 NPO	C2	WALSIN	—
4	1	CHIP CAP C 0.22U 16V K 0402 X5R	C3	WALSIN; TDK	—
5	4	CHIP CAP C 1U 6.3V K 0402 X5R	C4, C10, C11, C12	WALSIN; TDK	—
6	1	CHIP CAP C 1P 50V C 0402 NPO	C5	WALSIN	—
7	2	CHIP CAP C 9P 50V C 0402 NPO	C8, C9	WALSIN	—
8	1	CHIP CAP C 10U 6.3V M 0603 X5R	C13	WALSIN; TDK	—
9	1	CHIP CAP C 4.7U 6.3V K 0603 X5R	C14	WALSIN; TDK	—
10	1	LED BLUE HT-F194NB5 VF2.8V 5mA 0603 INGAN	LED1	HARVATEK	—
11	1	CHIP IND 2.7 nH S 0402	L1	ACX	—
12	1	CHIP IND 2.2 nH S 0402	L3	ACX	—
13	1	CHIP IND 4.7 uH K 420 mA 1.2*1.8*1.0	L4	ZenithTek	DCR: 0.97Ω IDC: 400 mA Irms: 420 mA
14	1	CHIP RES 330 5% 1/16W 0402	R1	EVER OHMS	—
15	1	IS1870/71	U1		—
16	1	XTAL 32M 9 pF 3.2*2.5 10 ppm -40℃ FUND. SMD	X1	SIWARD	—

APPENDIX D: REVISION HISTORY

Revision A (October 2015)

This is the initial released version of this document.

Revision B (October 2015)

This revision includes the following changes as well as minor updates to text and formatting, which were incorporated throughout the document.

TABLE D-1: MAJOR SECTION UPDATES

Section	Update Description
Section "Features"	The section has been updated with new information.
Section "Packages"	The section is updated with the package information
Section 1.0 "Device Overview"	Updated Figure 1-1 and Figure 1-2. Added Table 1-1

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