

IS31AP4991

1.2W AUDIO POWER AMPLIFIER WITH ACTIVE-LOW STANDBY MODE

November 2011

GENERAL DESCRIPTION

The IS31AP4991 has been designed for demanding audio applications such as mobile phones and permits the reduction of the number of external components.

It is capable of delivering 1.2W of continuous RMS output power into an 8Ω load @ 5V.

An externally-controlled standby mode reduces the supply current to much less than 1μA. It also includes internal thermal shutdown protection.

The unity-gain stable amplifier can be configured by external gain setting resistors.

FEATURES

- Operating from $V_{CC} = 2.7V \sim 5.5V$
- 1.2W output power @ $V_{CC} = 5V$, THD+N= 1%, $f = 1kHz$, with 8Ω load
- Ultra-low consumption in standby mode (much less than 1μA)
- 65dB PSRR @217Hz in grounded mode
- Near-zero click-and-pop
- Ultra-low distortion (0.025% @0.5W, 1kHz)
- SOP-8 and MSOP-8 package

APPLICATIONS

- Mobile phones
- PDAs
- Portable electronic devices
- Notebook computer

TYPICAL APPLICATION CIRCUIT

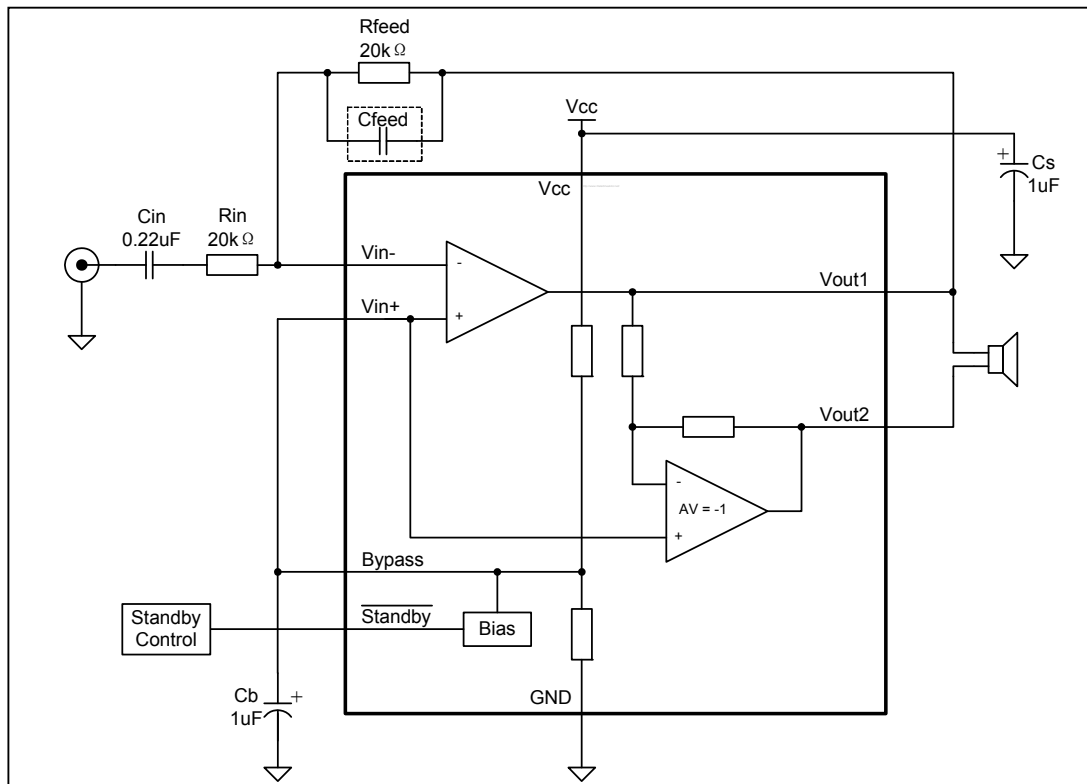
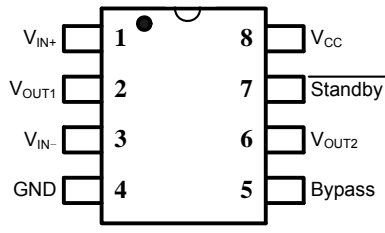
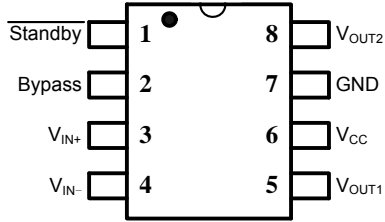


Figure 1 Typical Application Circuit

IS31AP4991

PIN CONFIGURATION

Package	Pin Configuration (Top View)
SOP-8	
MSOP-8	

PIN DESCRIPTION

Pin	No.		Description
	SOP	MSOP	
V_{IN+}	1	3	Positive input of the first amplifier.
V_{OUT1}	2	5	Negative output of the IS31AP4991. Connected to the load and to the feedback resistor R_{feed-} .
V_{IN-}	3	4	Negative input of the first amplifier, receives the audio input signal. Connected to the feedback resistor R_{feed} and to the input resistor R_{in} .
GND	4	7	Ground.
Bypass	5	2	Bypass capacitor pin which provides the common mode voltage ($V_{CC}/2$).
V_{OUT2}	6	8	Positive output of the IS31AP4991. Connected to the load.
$\overline{\text{Standby}}$	7	1	The device enters shutdown mode when a low level is applied on this pin.
V_{CC}	8	6	Positive analog supply of the chip.

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- the user assume all such risks; and
- potential liability of Integrated Silicon Solution, Inc is adequately protected under the circumstances



IS31AP4991

ORDERING INFORMATION

Industrial Range: -40°C to +85°C

Order Part No.	Package	QTY/Reel
IS31AP4991-GRLS2-TR	SOP-8, Lead-free	2500
IS31AP4991-SLS2-TR	MSOP-8, Lead-free	2500

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ABSOLUTE MAXIMUM RATINGS (Notes 1)

Supply voltage, V_{DD}	-0.3V ~ +6.0V
Voltage at any input pin	-0.3V ~ $V_{DD}+0.3V$
Junction temperature, T_{JMAX}	-40°C ~ +150°C
Storage temperature range, T_{stg}	-65°C ~ +150°C
Operating temperature ratings	-40°C ~ +85°C
Thermal resistance, θ_{JA} (SOP-8)	58°C/W
θ_{JA} (MSOP-8)	160°C/W
Power dissipation (Note 2)	Internally Limited

Note 1: Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other condition beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Note 2: The maximum power dissipation must be derated at elevated temperatures and is dictated by T_{JMAX} , θ_{JA} , and the ambient temperature T_A . The maximum allowable power dissipation is $P_{DMAX} = (T_{JMAX} - T_A) / \theta_{JA}$ or the number given in Absolute Maximum Ratings, whichever is lower. For the IS31AP4990D, see power derating curves for additional information.

ELECTRICAL CHARACTERISTICS

The following specifications apply for $C_{in} = 0.22\mu F$, $R_{in} = R_{feed} = 20k\Omega$, $C_b = 1\mu F$, unless otherwise specified. Limits apply for $T_A = 25^\circ C$. $V_{CC} = 5V$ (Note 3 or specified)

Symbol	Parameter	Condition	Typ.	Limit	Unit
I_{CC}	Quiescent power supply current	$V_{CC} = 0V$, $I_o = 0A$, no Load	4.8		mA (max)
I_{STBY}	Standby current	$V_{STBY} = GND$, $R_L = \infty$		1	μA (max)
V_{STBYH}	Shutdown voltage input high	$V_{CC} = 5.5V$		1.4	V(min)
V_{STBYL}	Shutdown voltage input low	$V_{CC} = 2.7V$		0.4	V(max)
V_{OS}	Output offset voltage			15	mV (max)
P_o	Output power (8 Ω)	THD+N = 1%; f = 1kHz	1.18		W
		THD+N = 10%; f = 1kHz	1.46		
T_{WU}	Wake-up time (Note 4)	$C_b = 1\mu F$	115		ms
THD+N	Total harmonic distortion+noise (Note 4)	$P_o = 0.5W_{rms}$; f = 1kHz	0.025		%
PSRR	Power supply rejection ratio (Note 4)	$V_{ripple\ p-p} = 200mV$ Input Grounded	f = 217Hz	65	dB
			f = 1kHz	77	

The following specifications apply for $C_{in} = 0.22\mu F$, $R_{in} = R_{feed} = 20k\Omega$, $C_b = 1\mu F$, unless otherwise specified. Limits apply for $T_A = 25^\circ C$. $V_{CC} = 3V$ (Note 3 or specified)

Symbol	Parameter	Condition	Typ.	Limit	Unit
I_{CC}	Quiescent power supply current	$V_{CC} = 0V$, $I_o = 0A$, no Load	3.8		mA(max)
I_{STBY}	Standby current	$V_{STBY} = GND$, $R_L = \infty$		1	μA (max)
P_o	Output power (8 Ω)	THD+N = 1%; f = 1kHz	405		mW
		THD+N = 10%; f = 1kHz	502		
T_{WU}	Wake-up time (Note 4)	$C_b = 1\mu F$	102		ms
THD+N	Total harmonic distortion+noise (Note 4)	$P_o = 0.3W_{rms}$; f = 1kHz	0.027		%

Note 3: Production testing of the device is performed at 25°C. Functional operation of the device and parameters specified over other temperature range, are guaranteed by design, characterization and process control.

Note 4: Guaranteed by design.

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TYPICAL PERFORMANCE CHARACTERISTIC

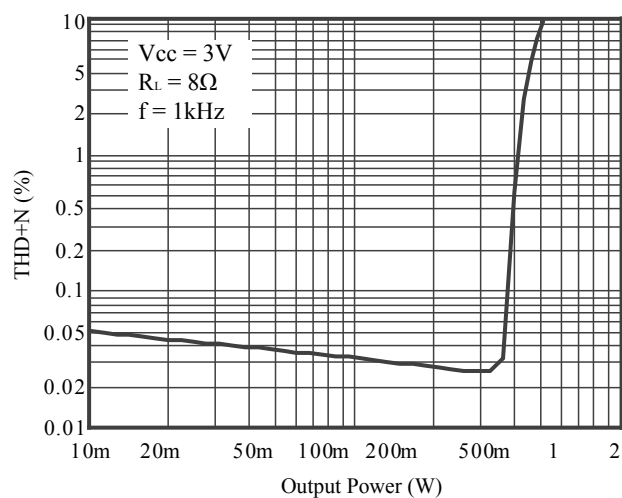


Figure 2 THD+N vs. Output Power

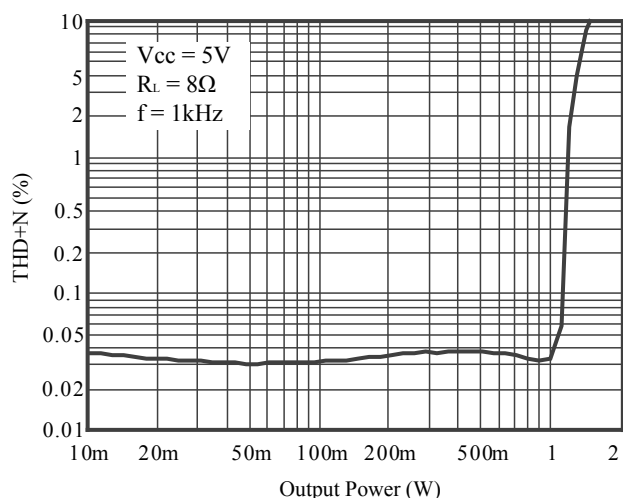


Figure 3 THD+N vs. Output Power

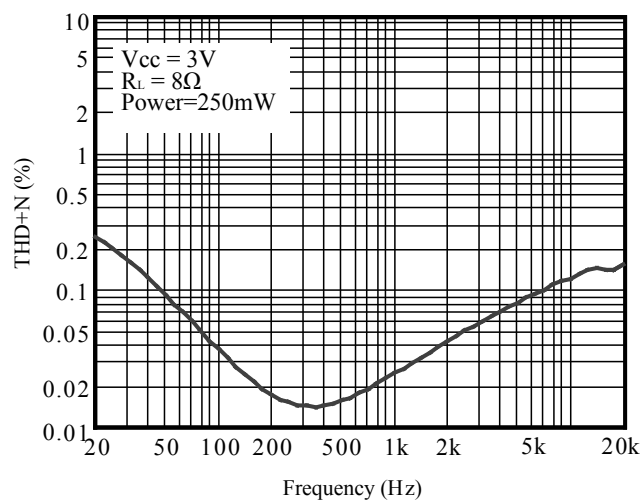


Figure 4 THD+N vs. Frequency

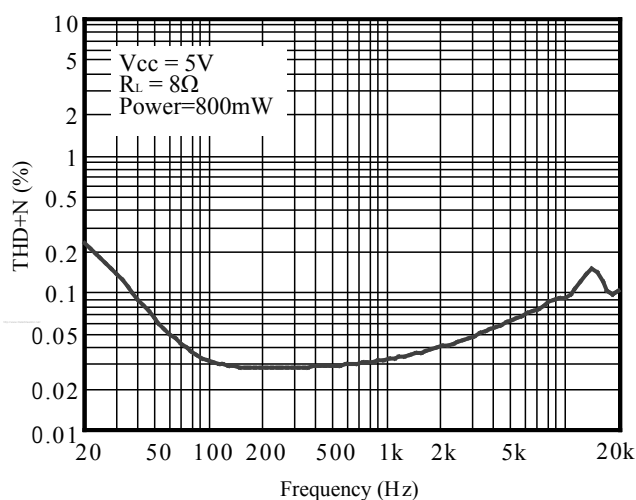


Figure 5 THD+N vs. Frequency

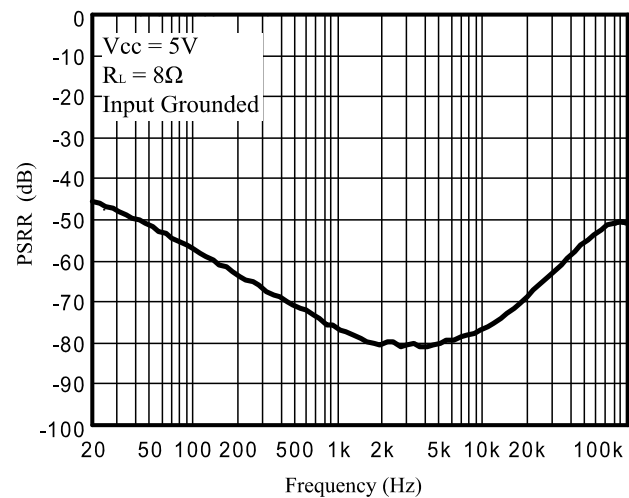


Figure 6 PSRR vs. Frequency

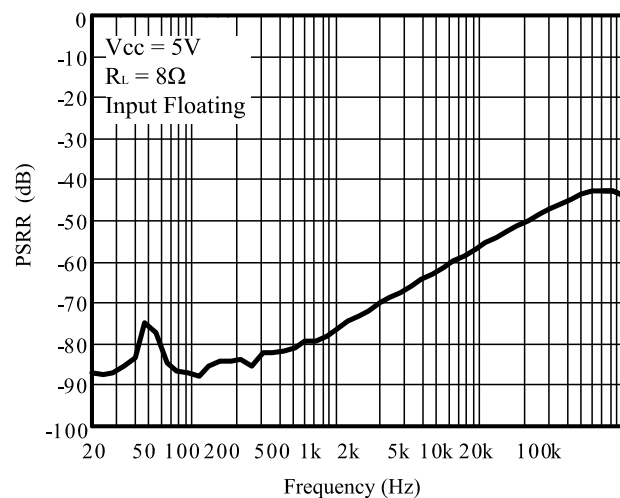


Figure 7 PSRR vs. Frequency

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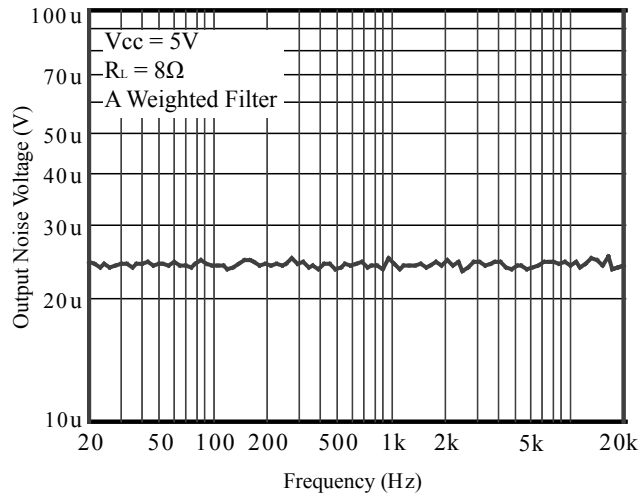


Figure 8 Noise Floor

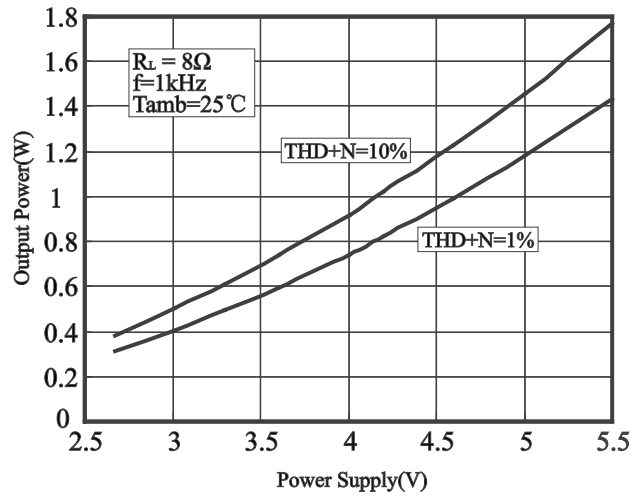


Figure 9 Output Power vs. Power Supply

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APPLICATION INFORMATION

BTL CONFIGURATION PRINCIPLE

The IS31AP4991 is a monolithic power amplifier with a BTL output type. BTL (bridge tied load) means that each end of the load is connected to two single-ended output amplifiers. Thus, we have:

Single-ended output 1 = $V_{out1} = V_{out}$ (V)

Single ended output 2 = $V_{out2} = -V_{out}$ (V)

and

$V_{out1} - V_{out2} = 2V_{out}$ (V)

The output power is:

$$P_{out} = \frac{(2V_{out_{RMS}})^2}{R_L}$$

For the same power supply voltage, the output power in BTL configuration is four times higher than the output power in single ended configuration.

GAIN IN A TYPICAL APPLICATION SCHEMATIC

The typical application schematic is shown in Figure 1 on page 1.

In the flat region (no C_{in} effect), the output voltage of the first stage is (in Volts):

$$V_{out1} = (-V_{in}) \frac{R_{feed}}{R_{in}}$$

For the second stage: $V_{out2} = -V_{out1}$ (V)

The differential output voltage is (in Volts):

$$V_{out2} - V_{out1} = 2V_{in} \frac{R_{feed}}{R_{in}}$$

The differential gain, G_v , is given by:

$$G_v = \frac{V_{out2} - V_{out1}}{V_{in}} = 2V_{in} \frac{R_{feed}}{R_{in}}$$

V_{out2} is in phase with V_{in} and V_{out1} is phased 180° with V_{in} . This means that the positive terminal of the loudspeaker should be connected to V_{out2} and the negative to V_{out1} .

LOW AND HIGH FREQUENCY RESPONSE

In the low frequency region, C_{in} starts to have an effect. C_{in} forms with R_{in} a high-pass filter with a -3dB cut-off frequency. F_{CL} is in Hz.

$$F_{CL} = \frac{1}{2\pi R_{in} C_{in}}$$

In the high frequency region, you can limit the bandwidth by adding a capacitor (C_{feed}) in parallel with R_{feed} . It forms a low-pass filter with a -3dB cut-off frequency. F_{CH} is in Hz.

$$F_{CH} = \frac{1}{2\pi R_{feed} C_{feed}}$$

DECOUPLING OF THE CIRCUIT

Two capacitors are needed to correctly bypass the IS31AP4991: a power supply bypass capacitor C_s and a bias voltage bypass capacitor C_b .

C_s has particular influence on the THD+N in the high frequency region (above 7kHz) and an indirect influence on power supply disturbances. With a value for C_s of 1μF, you can expect THD+N levels similar to those shown in the datasheet.

In the high frequency region, if C_s is lower than 1μF, it increases THD+N and disturbances on the power supply rail are less filtered.

On the other hand, if C_s is higher than 1μF, those disturbances on the power supply rail are more filtered.

C_b has an influence on THD+N at lower frequencies, but its function is critical to the final result of PSRR (with input grounded and in the lower frequency region).

If C_b is lower than 1μF, THD+N increases at lower frequencies and PSRR worsens.

If C_b is higher than 1μF, the benefit on THD+N at lower frequencies is small, but the benefit to PSRR is substantial.

Note that C_{in} has a non-negligible effect on PSRR at lower frequencies. The lower the value of C_{in} , the higher the PSRR is.

WAKE-UP TIME (t_{wu})

When the standby is released to put the device ON, the bypass capacitor C_b will not be charged immediately. As C_b is directly linked to the bias of the amplifier, the bias will not work properly until the C_b voltage is correct. The time to reach this voltage is called wake-up time or t_{wu} and specified in the electrical characteristics table with $C_b = 1\mu F$.

POP PERFORMANCE

Pop performance is intimately linked with the size of the input capacitor C_{in} and the bias voltage bypass capacitor C_b .

The size of C_{in} is dependent on the lower cut-off frequency and PSRR values requested. The size of C_b is dependent on THD+N and PSRR values requested at lower frequencies.

Moreover, C_b determines the speed with which the amplifier turns ON.

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CLASSIFICATION REFLOW PROFILES

Profile Feature	Pb-Free Assembly
Preheat & Soak	
Temperature min (T _{smin})	150°C
Temperature max (T _{smax})	200°C
Time (T _{smin} to T _{smax}) (t _s)	60-120 seconds
Average ramp-up rate (T _{smax} to T _p)	3°C/second max.
Liquidous temperature (T _L)	217°C
Time at liquidous (t _L)	60-150 seconds
Peak package body temperature (T _p)*	Max 260°C
Time (t _p)** within 5°C of the specified classification temperature (T _c)	Max 30 seconds
Average ramp-down rate (T _p to T _{smax})	6°C/second max.
Time 25°C to peak temperature	8 minutes max.

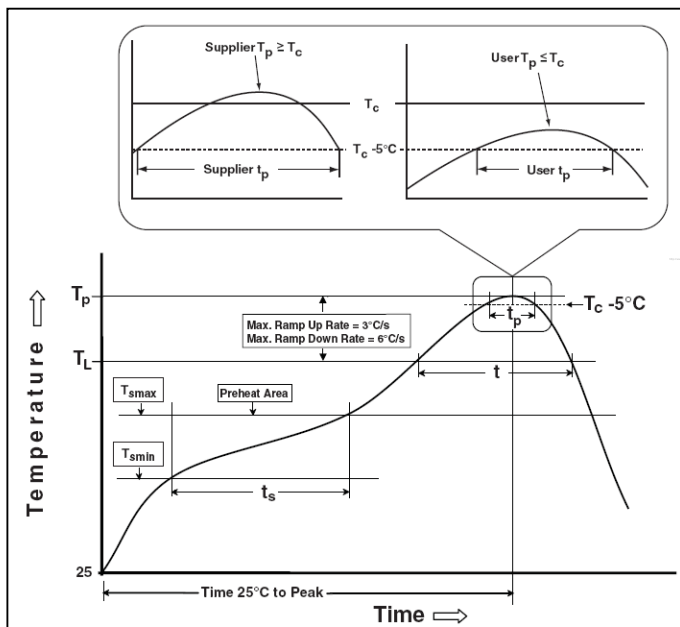
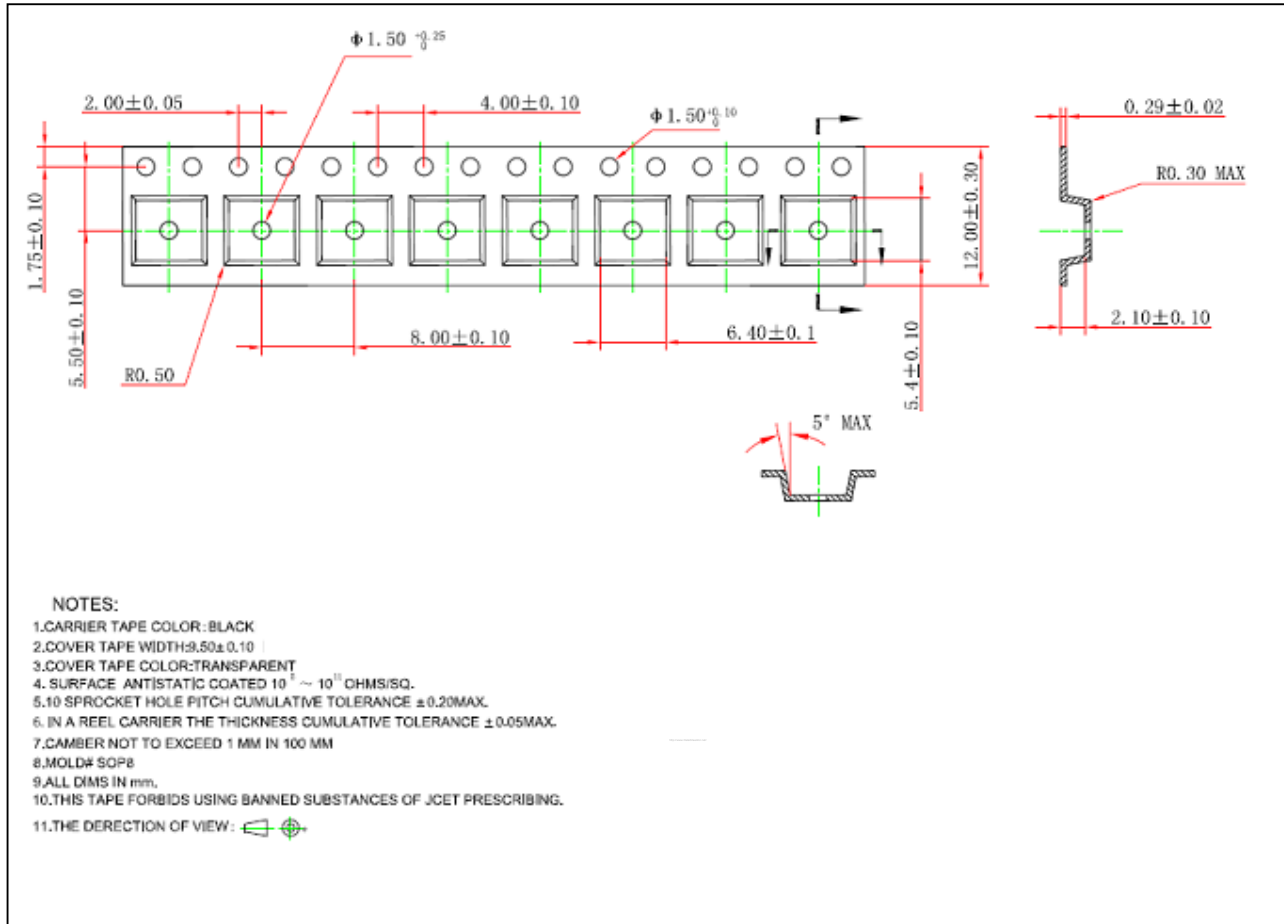


Figure 10 Classification Profile

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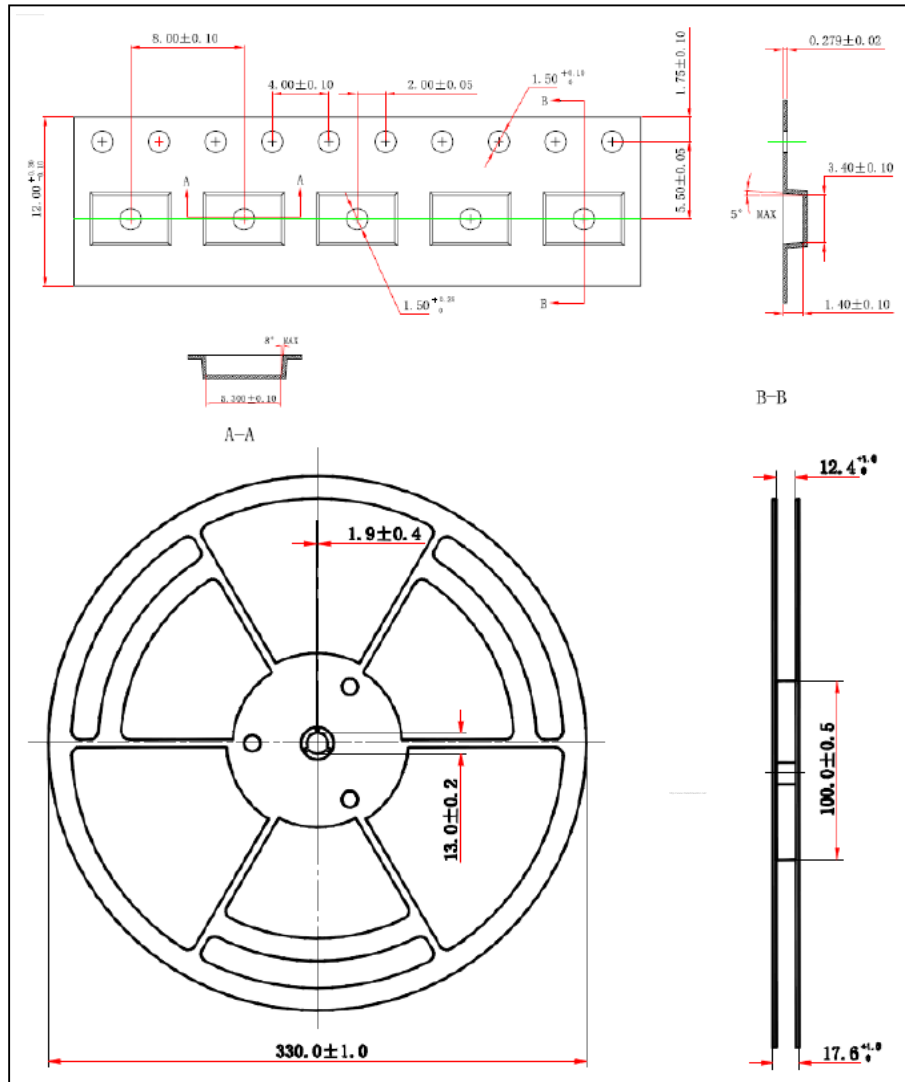
TAPE AND REEL INFORMATION

SOP-8



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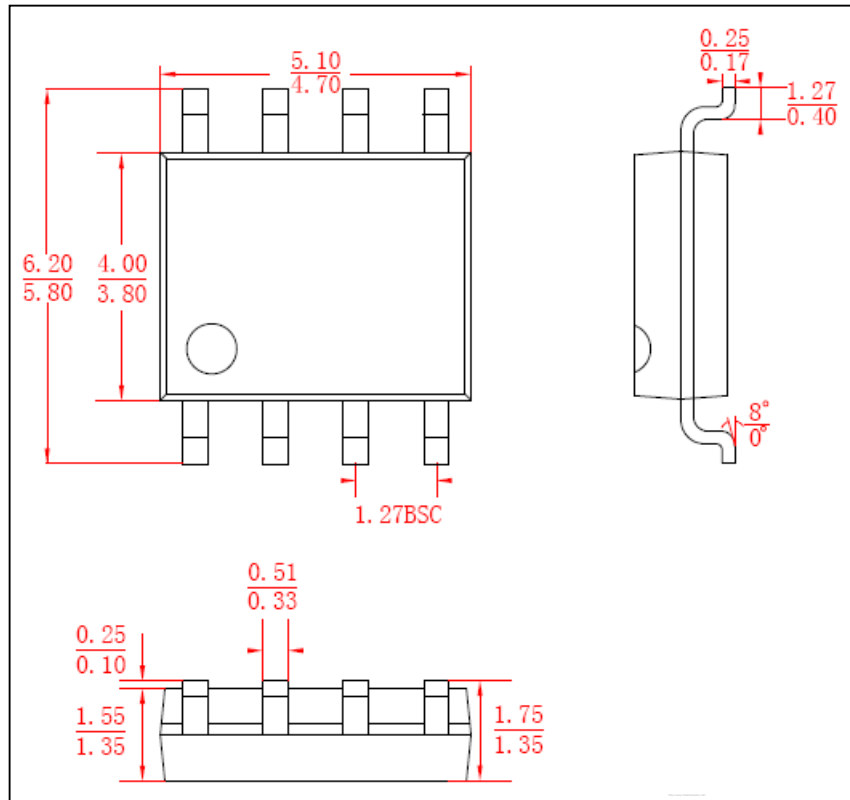
MSOP-8



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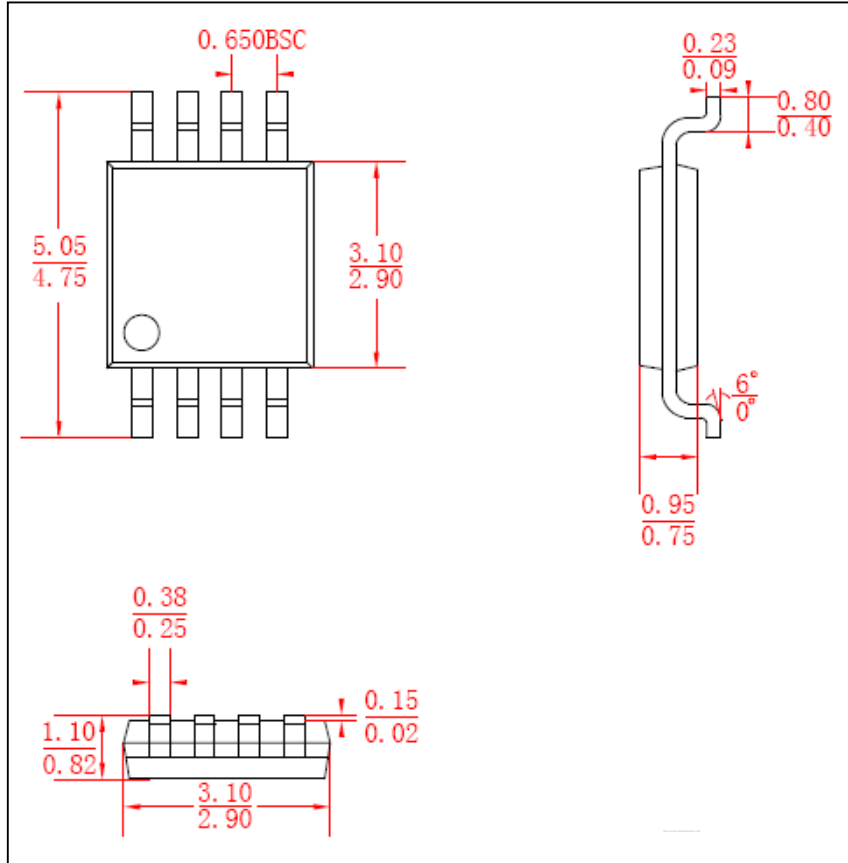
PACKAGE INFORMATION

SOP-8



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MSOP-8



Note: All dimensions in millimeters unless otherwise stated.