IS31FL3197

CHARGE PUMP RGBW LED DRIVER WITH PROGRAMMABLE SELF-RUNNING PATTERNS

May 2022

GENERAL DESCRIPTION

The IS31FL3197 is a charge pump LED driver with programmable sequence operation for automated RGBW lighting effects. It is capable of driving 4 LEDs up to 10mA (adjustable in 256 current levels and 4096 PWM levels) from a small coin size battery supply.

The built−in charge pump structure will automatically toggle between 1x, 1.5x or 2x operation depending on the battery's state of charge. This DC/DC converter operates at a high switching frequency which enables the use of small external capacitors and achieves a 90% peak efficiency. To conserve battery life, the charge pump goes into high impedance mode whenever the IS31FL3197 is shutdown.

The IS31FL3197 can operate in either "Current Level & PWM mode" or "Pattern" mode. In Current Level & PWM mode, the output current of each output is independently programmed and controlled in 4096 steps to achieve color mixing and the PWM duty cycle of each output is also independently programmed and controlled in 4096 steps to simplify color mixing or for smoothly diming control. In Pattern mode, the timing characteristics for RGB channels output can be individually adjusted to maintain a pre-established pattern sequence without requiring any additional MCU interaction, thus saving valuable system resources.

The IS31FL3197 is available in a small QFN-16 (4mm×4mm) and WLCSP-16 (1.88mm×1.8mm, 0.45mm ball pitch, 0.2mm ball diameter) packages. It operates from 2.0V to 3.3V over the temperature range of -40°C to +85°C.

With automated lighting effects and a DC/DC charge pump, the small package IS31FL3197 is ideal for low power battery applications.

FEATURES

- 2.0V to 3.3V supply voltage
- Charge pump
  - 1x, 1.5x, 2x operating modes
  - Highly efficient across battery state of charge
  - 1MHz constant frequency
- Power saving operating
  - Quiescent operating current 700μA (Typ.)
  - Shutdown current 1μA (Typ.)
- Support four LEDs - RGBW
  - Resistor sets maximum 10mA output current per LED
  - Each LED has 8-bit programmable current levels
  - Each LED has 12-bit programmable PWM levels
- LEDs operate with pre-established patterns
  - Once programmed runs without micro
  - OUT1~OUT3 have their own fade ON/OFF timing registers (TS~T4) with independent start/stop/crossfade
  - Fixed number of iterations or non-stop operation
  - Crossfade of one color to another
- Fast 400kHz I2C bus interface
  - Automatic address increment function
  - 4 selectable I2C address locations
- Over-temperature protection
- QFN-16 (4mm×4mm) and WLCSP-16 (1.88mm×1.8mm, 0.45mm ball pitch, 0.2mm ball diameter) packages
- Operating temperature T_A = -40°C ~ +85°C

APPLICATIONS

- Internet-of-Things (IOT)
- Electronic Shelf Labeling (ESL)
- Low-power battery applications
- Hand-held devices requiring visual notifications

TYPICAL APPLICATION CIRCUIT

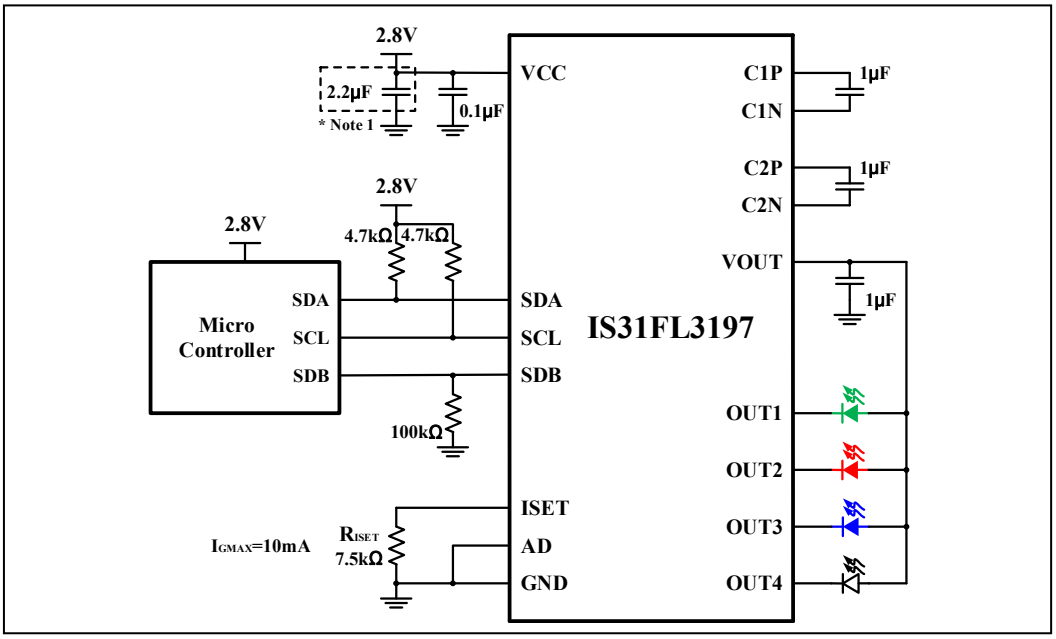


Figure 1 Typical Application Circuit (V_{CC}= 2.8V)

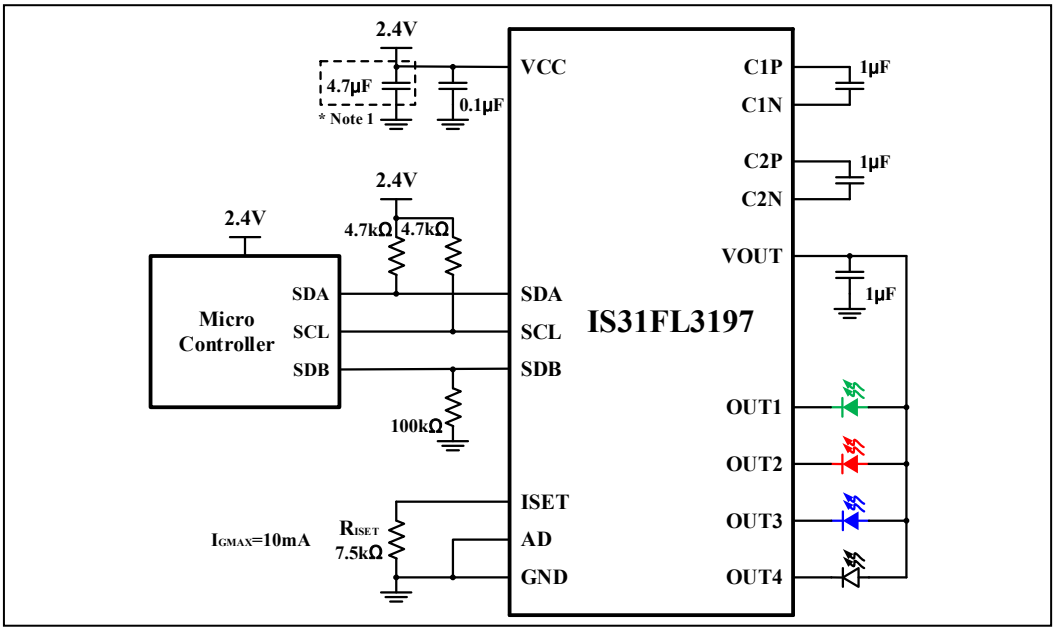
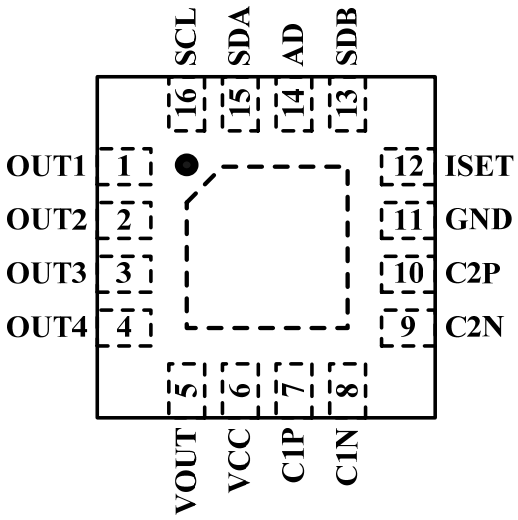
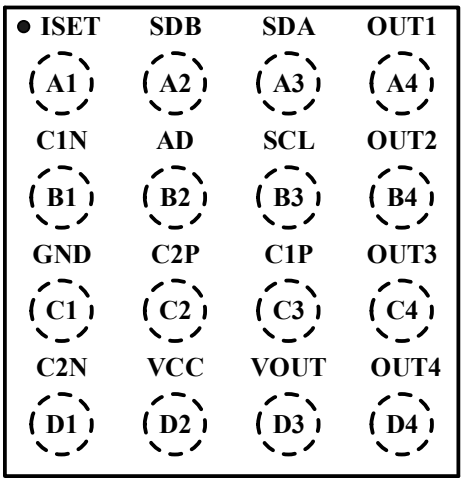


Figure 2 Typical Application Circuit (V_{CC}= 2.4V)

Note 1: This capacitor at the power supply is to ensure that the VCC remains above 2V for normal startup. It should be placed as close as possible to the VCC pin. For the selection of this capacitance value, please refer to “POWER ON SEQUENCE” under “TYPICAL APPLICATION INFORMATION”.

PIN CONFIGURATION

Package	Pin Configuration (Top View)
QFN-16	
WLCSP-16	

PIN DESCRIPTION

QFN	WLCSP	Pin	Description
1~4	A4, B4, C4, D4	OUT1~OUT4	LED current sink pins, connect the corresponding LED cathode to this pin. The anode of the associated LED must to be connected to the VOUT pin.
5	D3	VOUT	Charge pump output supplies the LED current. In shutdown mode this pin is high impedance. Connect a 1μF capacitor from VOUT to GND.
6	D2	VCC	Power supply input, requires 1.0μF and 0.1μF capacitor between this pin and ground pin.
7,8	C3, B1	C1P, C1N	Stage 1 charge pump flying capacitor, C1N negative terminal, C1P positive terminal. (Note 2)
9,10	D1, C2	C2N, C2P	Stage 2 charge pump flying capacitor, C2N negative terminal, C2P positive terminal. (Note 2)
11	C1	GND	Ground reference signal for the charge pump and the output current control. A PCB ground plane strongly recommended.
12	A1	ISET	Connect external resistor R_{ISET} to ground to set global max current I_{GMAX}.
13	A2	SDB	Pull below 0.4V to activate low power shutdown mode.
14	B2	AD	I2C address setting.
15	A3	SDA	I2C data pin. The SDA byte is used to program the device operating mode.
16	B3	SCL	I2C serial clock associated with SDA signal.
		Thermal Pad	Connect to GND.

Note 2: The flying capacitors should be placed as close as possible to the IC and the signal trace between the capacitor and CP terminals kept as short as possible.

ORDERING INFORMATION

Industrial Range: -40°C to +85°C

Order Part No.	Package	QTY/Reel
IS31FL3197-QFLS2-TR	QFN-16, Lead-free	2500
IS31FL3197-CLS2-TR	WLCSP-16, Lead-free	3000

ABSOLUTE MAXIMUM RATINGS

Supply voltage, V_{CC}, V_{OUT}	-0.3V ~ +3.7V
Voltage at any input pin	-0.3V ~ V_{CC}+0.3V
Maximum junction temperature, T_{JMAX}	+150°C
Operating temperature range, T_A=T_J	-40°C ~ +85°C
Storage temperature range, T_{STG}	-65°C ~ +150°C
Package thermal resistance, junction to ambient (4-layer standard test PCB based on JESD 51-2A), θ_{JA}	53.7°C/W (QFN) 73°C/W (WLCSP)
ESD (HBM) ESD (CDM)	±8kV ±750V

Note 3: Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other condition beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

T_A = 25°C, V_{CC} = 2.0V ~ 3.0V, unless otherwise noted. Typical value is T_A = 25°C, V_{CC} = 2.8V.

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
V_{CC}	Supply voltage		2.0		3.3	V
I_{CC}	Quiescent operating current	1x mode, no load, all four channels disable (01h=0x01)		700	820	μA
		1.5x mode, no load		1.7	2.4	mA
		Sleep 1 Mode: CP stops, Bandgap working and all OUTx are off without any bias		42	54	μA
		Sleep 2 Mode: CP, Bandgap stop and all OUTx are off without any bias		0.5	1	μA
I_{SDB}	Shutdown current	V_{SDB}= 0V		0.5	1	μA
		V_{SDB}= V_{CC}, software shutdown		0.5	1	μA
I_{LED}	Current per channel	PWM Control Mode, PWM= 0x0FFF, Current Register 10mA	9.4	10	10.6	mA
ΔI_{MAT}	Output current error between bits (Note 3)	Any two outputs V_{CC}= 2.8V, I_{OUT}= 10mA	-4		+4	%
ΔI_{ACC}	Output current error between devices (Note 4)	Any two outputs V_{CC}= 2.8V, I_{OUT}= 10mA	-6		+6	%
V_{HR}	Current sink headroom voltage	I_{OUT}= 10mA		150	250	mV
V_{OVP}	Output voltage compliance (OVP)	Output Voltage Clamp	3.74	3.9	4.06	V
Charge Pump Characteristics						
t_{ST}	Soft-start time	Charge Pump Start time (C_{OUT}= 1μF) 3.0V < V_{CC}= nominal< 5.5V		64		μs
f_{CLK}	Charge pump operating frequency		900	1000	1120	kHz

ELECTRICAL CHARACTERISTICS (CONTINUE)

T_A= -40°C ~ +85°C, V_{CC} = 2.8V, unless otherwise noted. Typical value is T_A= 25°C.

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
Logic Electrical Characteristics (SDA, SCL, AD, SDB)						
V_{IL}	Logic “0” input voltage	V_{CC} = 2.0V~3.3V	0		0.4	V
V_{IH}	Logic “1” input voltage	V_{CC} = 2.0V~3.3V	1.4		V_{CC}	V
I_{IL}	Logic “0” input current	V_{INPUT} = 0V (Note 6)		5		nA
I_{IH}	Logic “1” input current	V_{INPUT} = V_{IO} (Note 6)		5		nA

DIGITAL INPUT SWITCHING CHARACTERISTICS (NOTE 5)

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
f_{SCL}	Serial-Clock frequency				400	kHz
t_{BUF}	Bus free time between a STOP and a START condition		1.3			μs
$t_{HD, STA}$	Hold time (repeated) START condition		0.6			μs
$t_{SU, STA}$	Repeated START condition setup time		0.6			μs
$t_{SU, STO}$	STOP condition setup time		0.6			μs
$t_{HD, DAT}$	Data hold time				-	μs
$t_{SU, DAT}$	Data setup time		100			ns
t_{LOW}	SCL clock low period		1.3			μs
t_{HIGH}	SCL clock high period		0.7			μs
t_R	Rise time of both SDA and SCL signals, receiving	(Note 6)		20+0.1C_b	300	ns
t_F	Fall time of both SDA and SCL signals, receiving	(Note 6)		20+0.1C_b	300	ns

Note 4: I_{OUT} mismatch (bit to bit) $\triangle I_{MAT}$ is calculated:

$$\Delta I_{MAT} = \left(\frac{I_{OUTn}(n=1\sim 4)}{\left(\frac{I_{OUT1}+I_{OUT2}+I_{OUT3}+I_{OUT4}}{4} \right)} - 1 \right) \times 100\%$$

Note 5: I_{OUT} accuracy (device to device) $\triangle I_{ACC}$ is calculated:

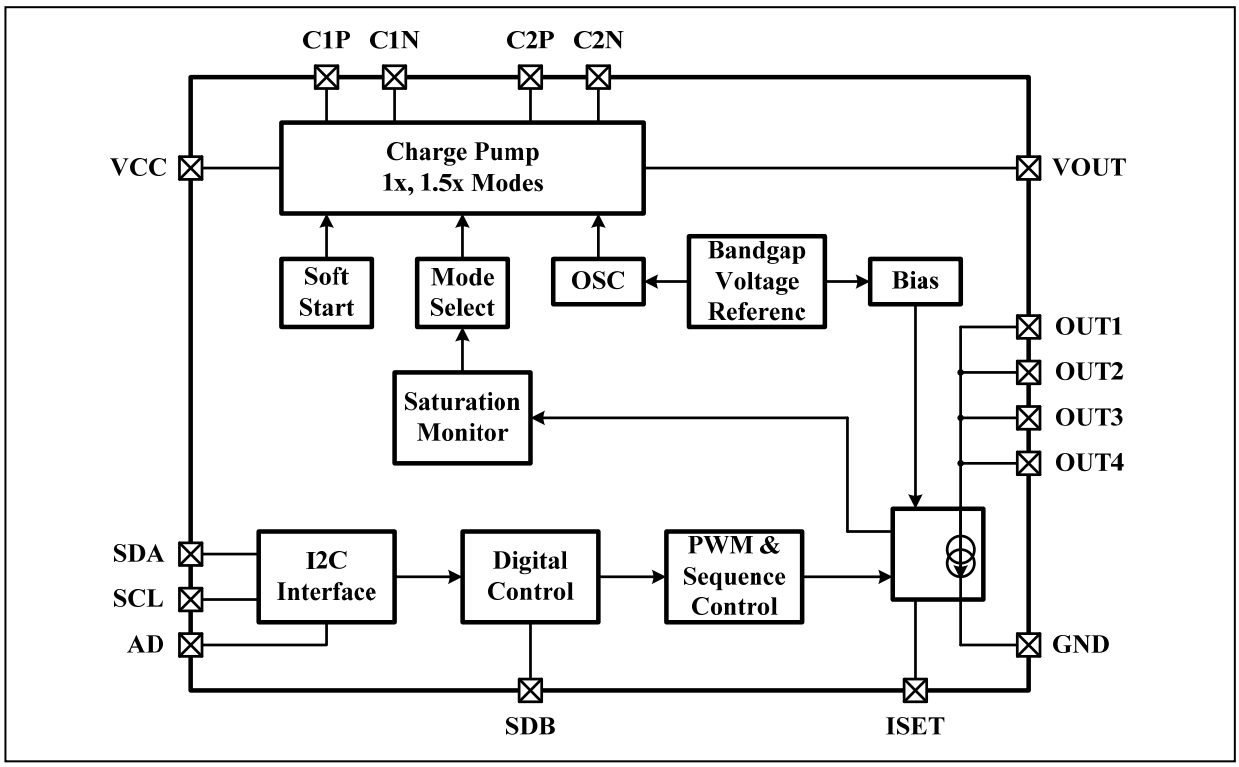
$$\Delta I_{ACC} = \left(\frac{\left(\frac{I_{OUT1}+I_{OUT3}+I_{OUT3}+I_{OUT4}}{4} - I_{OUT(IDEAL)} \right)}{I_{OUT(IDEAL)}} \right) \times 100\%$$

Where $I_{OUT(IDEAL)}$= 10mA.

Note 6: Guaranteed by design.

Note 7: C_b = total capacitance of one bus line in pF. $I_{SINK} \leq$ 6mA. t_R and t_F measured between 0.3×V_{CC} and 0.7×V_{CC}.

FUNCTION BLOCK DIAGRAM



DETAILED DESCRIPTION

I2C INTERFACE

The IS31FL3197 uses a serial bus, which conforms to the I2C protocol, to control the chip's functions with two wires: SCL and SDA. The IS31FL3197 has a constant 7-bit slave address (A7:A1), followed by the R/W bit, A0. Set A0 to "0" for a write command and set A0 to "1" for a read command. The value of bits A1 and A2 are decided by the connection of the AD pin.

The complete slave address is:

Table 1 Slave Address:

AD	A7:A3	A2:A1	A0
GND	10100	00	0/1
SCL		01	
SDA		10	
VCC		11	

AD connected to GND, A2:A1=00;
AD connected to VCC, A2:A1=11;
AD connected to SCL, A2:A1=01;
AD connected to SDA, A2:A1=10;

The SCL line is uni-directional. The SDA line is bi-directional (open-drain) with a pull-up resistor (typically 4.7kΩ). The maximum clock frequency specified by the I2C standard is 400kHz. In this discussion, the master is the microcontroller and the slave is the IS31FL3197.

The timing diagram for the I2C is shown in Figure 2. The SDA is latched in on the stable high level of the SCL. When there is no interface activity, the SDA line should be held high.

The "START" signal is generated by lowering the SDA signal while the SCL signal is high. The start signal will alert all devices attached to the I2C bus to check the incoming address against their own chip address.

The 8-bit chip address is sent next, most significant bit first. Each address bit must be stable while the SCL level is high.

After the last bit of the chip address is sent, the master checks for the IS31FL3197's acknowledge. The master releases the SDA line high (through a pull-up resistor). Then the master sends an SCL pulse. If the IS31FL3197 has received the address correctly, then it holds the SDA line low during the SCL pulse. If the SDA line is not low, then the master should send a "STOP" signal (discussed later) and abort the transfer.

Following acknowledge of IS31FL3197, the register address byte is sent, most significant bit first. IS31FL3197 must generate another acknowledge indicating that the register address has been received.

Then 8-bit of data byte are sent next, most significant bit first. Each data bit should be valid while the SCL level is stable high. After the data byte is sent, the IS31FL3197 must generate another acknowledge to indicate that the data was received.

The "STOP" signal ends the transfer. To signal "STOP", the SDA signal goes high while the SCL signal is high.

ADDRESS AUTO INCREMENT

To write multiple bytes of data into IS31FL3197, load the address of the data register that the first data byte is intended for. During the IS31FL3197 acknowledge of receiving the data byte, the internal address pointer will increment by one. The next data byte sent to IS31FL3197 will be placed in the new address, and so on (Figure 5).

READING PORT REGISTERS

To read the device data, the bus master must first send the IS31FL3197 address with the R/W bit set to "0", followed by the command byte, which determines which register is accessed. After a restart, the bus master must then send the IS31FL3197 address with the R/W bit set to "1". Data from the register defined by the command byte is then sent from the IS31FL3197 to the master (Figure 6).

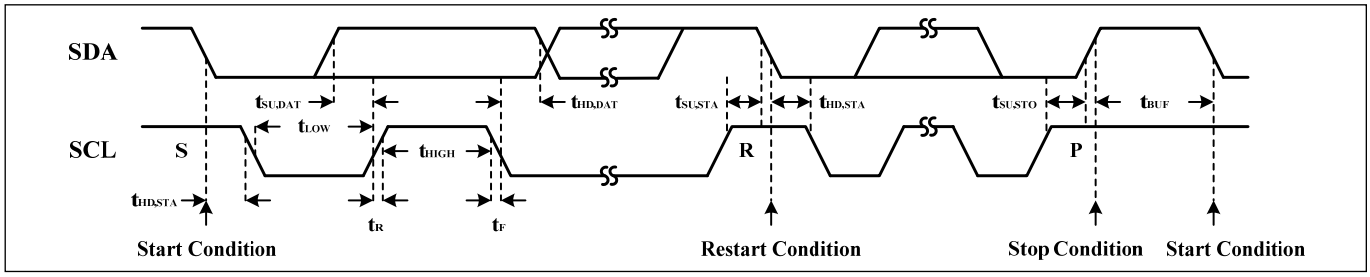


Figure 3 Interface Timing

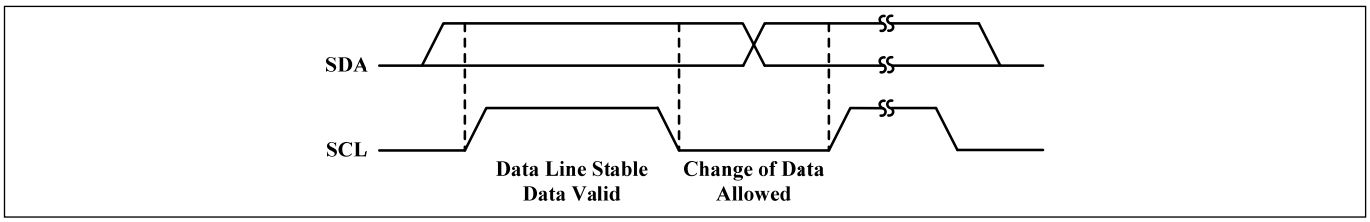


Figure 4 Bit Transfer

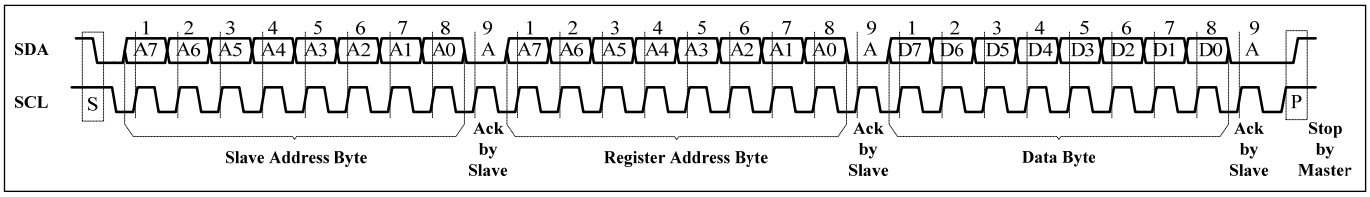


Figure 5 Writing to IS31FL3197 (Typical)

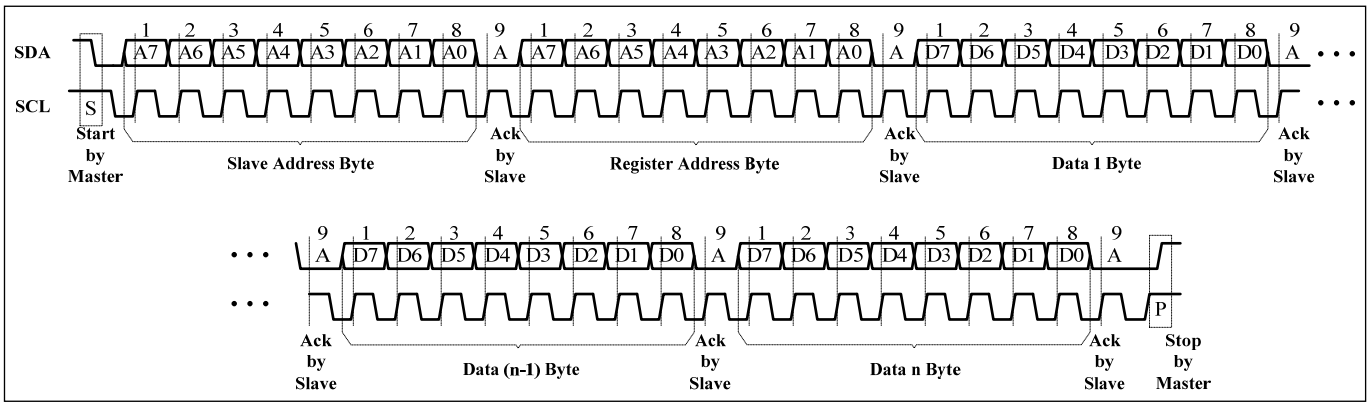


Figure 6 Writing to IS31FL3197 (Automatic Address Increment)

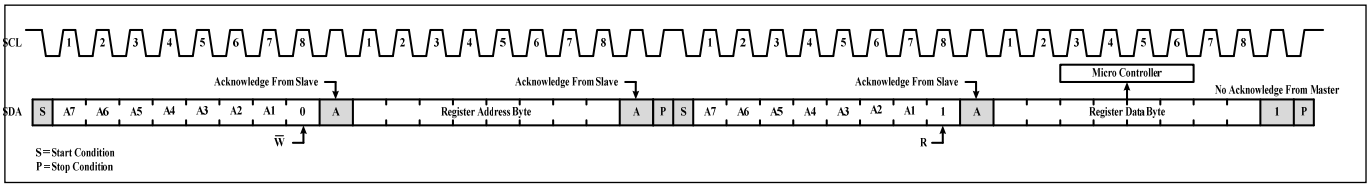


Figure 7 Reading from IS31FL3197

Table 2 Registers Definitions

Address	Name	Function	R/W	Table	Default
00h	Product ID	For read only, read result is Slave address	R	-	-
01h	Shutdown Control Register	Set power down mode and outputs shutdown control	R/W	3	1111 0000
02h	Operation Configure Register	Set output operation mode	R/W	4	0000 0000
03h	Charge Pump Setting Register -1	Set change pump parameters	R/W	5	0000 0000
04h	Charge Pump Setting Register -2	Set change pump parameters	R/W	6	0011 0000
05h	Current Band Register	Set current band of each Output	R/W	7	0101 0101
06h	Color Hold Function Register	Set the hold function of each Output	R/W	8	0000 0000
07h	Phase Delay Register	Phase delay mode setting	R/W	9	0000 0000
0Fh	Pattern State Register	For reading the pattern running state	R	10	0000 0000
10h~13h	OUT1~OUT4 Current Level Register	Output current level data register	R/W	11	0000 0000
10h~12h	Color 1 Setting Register of Pattern	Output current level data register-Color 1	R/W	12	0000 0000
14h~16h	Color 2 Setting Register of Pattern	Output current level data register-Color 2	R/W		0000 0000
17h~19h	Color 3 Setting Register of Pattern	Output current level data register-Color 3	R/W		0000 0000
1Ah~21h	PWM Register	Set PWM data	R/W	13	0000 0000
22h	Pattern TS &T1 Setting Register	Set the TS~T1 time	R/W	14	0000 0000
23h	Pattern T2 &T3 Setting Register	Set the T2~T3 time	R/W	15	0000 0000
24h	Pattern TP &T4 Setting Register	Set the TP~T4 time	R/W	16	0000 0000
25h	Crossfade Setting Register 1	Set the Crossfade enable	R/W	17	0000 0000
26h	Crossfade Setting Register 2	Set the Crossfade time	R/W	18	0000 0000
27h	Pattern Color Enable Register	Set the color enable/disable	R/W	19	0000 0001
28h	Pattern Color Cycle Times Register	Set color repeat time	R/W	20	0000 0000
29h	Pattern Register	Set next step and Gamma of each pattern	R/W	21	0000 0000
2Ah	Pattern Loop Times Register	Set the loop time of Pattern	R/W	22	0000 0000
2Bh	Color Update Register	Update color data	R/W	-	0000 0000
2Ch	PWM Update Register	Update PWM data	R/W	-	0000 0000
2Dh	Pattern Update Register	Update the time data and start to run pattern	R/W	-	0000 0000
3Fh	Reset Register	Reset the registers value to default	W	-	0000 0000

Table 3 01h Shutdown Control Register

Bit	D7:D4	D3	D2:D1	D0
Name	EN4:EN1	-	SLE	SSD
Default	1111	0	00	0

The Shutdown Control Register sets software shutdown and sleep modes of IS31FL3197.

The Output Enable Register enables/disables the outputs independently. The ENx is only effective when SSD= “1”.

Sleep 1 (power saving standby 1) Mode: CP in 1x mode and all OUTx are off without any bias. I_SLEEP1= 42μA (Typ.)

Sleep 2 (power saving standby 2) Mode: CP off and all OUTx are off without any bias. I_SLEEP2= 1μA (Typ.)

When SLE bits are set to “01” or “10”, IS31FL3197 puts itself in Sleep 1 or Sleep 2 Modes if all OUTx outputs are off for >30s. MCU command to the IS31FL3197 will wake it up and disable the sleep mode.

SSD	**Software Shutdown Enable**
0	Software shutdown mode
1	Normal operation

SLE	**Sleep Mode Enable**
00/11	Sleep mode disable
01	Sleep1 mode enable
10	Sleep2 mode enable

ENx	**Output Enable Control**
0	Output disable
1	Output enable

Table 4 02h Operating Configure Register

Bit	D7	D6	D5:D4	D3:D2	D1:D0
Name	-	MOD4	MOD3	MOD2	MOD1
Default	-	0	00	00	00

The Operating Configure Register sets output operation modes of IS31FL3197.

MODx	**OUT1~OUT3 LED Mode**
00	PWM & Current Level Mode
01	Pattern Mode (not available for OUT4)
1x	Current Level Mode

MOD4	**OUT4 LED Mode**
0	PWM & Current Level Mode
1	Current Level Mode

When the OUTx works in PWM Mode, means the output current is controlled by PWM Registers (1Ah~21h).

When the OUTx works in Pattern Mode, means the output current is controlled by Color Setting Registers (10h~12h, 14h~16h, 17h~19h).

When the OUTx works in Current Level Mode, means the output current is controlled by Current Level Register (10h~13h).

Notice that OUT4 is not available in Pattern Mode.

Table 5 03h Charge Pump Setting Register-1

Bit	D7:D6	D5:D4	D3:D2	D1:D0
Name	-	CPPM	-	CPM
Default	00	00	00	00

The Charge Pump Setting Register-1 sets the charge pump working mode.

CPPM	**Charge Pump Power up Mode**
00/10	1x mode
01	1.5x mode
11	2x mode

CPM	**Charge Pump Working Mode**
00	Auto mode
01	1x mode
10	1.5x mode
11	2x mode

Table 6 04h Charge Pump Setting Register-2

Bit	D7	D6:D4	D3:D0
Name	-	HRT	CPDE4:CPDE1
Default	0	011	0000

The Charge Pump Setting Register-2 sets headroom detect threshold voltage and enables OUTx charge pump detection. Disable charge pump detection on OUTx if LED anode not connected to VOUT or OUTx floating.

CPDEx	**Charge Pump Detection Enable of OUTx**
0	Enable
1	Disable

HRT	Headroom Threshold Voltage
000	50mV
001	100mV
010	125mV
011	150mV
100	175mV
101	200mV
110	250mV
111	300mV

Table 7 05h Current Band Register

Bit	D7:D6	D5:D4	D3:D2	D1:D0
Name	CB4	CB3	CB2	CB1
Default	01	01	01	01

The Current Band Register stores the current band or maximum output peak current of each LED output.

I_{GMAX} is the maximum current output decided by R_{ISET}, when R_{ISET}=7.5kΩ, I_{GMAX}=10mA.

I_{BAND} is maximum current decided by all registers include Current Level Register and PWM register.

When CBx is "01", I_{BAND}= I_{GMAX} ×1/2=5mA.

CBx	Current Band Setting
00	Band 1: 0mA~I_{GMAX} ×1/4, I_{BAND}= I_{GMAX} × 1/4
01	Band 2: 0mA~ I_{GMAX} ×1/2, I_{BAND}= I_{GMAX} × 1/2
10	Band 3: 0mA~ I_{GMAX} ×3/4, I_{BAND}= I_{GMAX} × 3/4
11	Band 4: 0mA~ I_{GMAX}, I_{BAND}= I_{GMAX}

Table 8 06h Color Hold Function Register

Bit	D7:D2	D1	D0
Name	-	CHF	HT
Default	0000 00	0	0

The Color Hold Function Register configures hold time for each output in Pattern Mode.

HT	Hold Time Selection
0	Hold at end of T4 when color loop done (always off)
1	Hold at end of T2 when color loop done (always on)

CHF	Hold Function Enable
0	hold function disable
1	hold function enable

Table 9 07h Phase Delay Register

Bit	D7:D1	D0
Name	-	PD
Default	0000 000	0

IS31FL3197 features the output current phase delay function, default is mode 1

PD	Phase Delay Mode
0	Phase delay mode 1
1	Phase delay mode 2

Table 10 0Fh Pattern State Register (Read Only)

Bit	D7	D6	D5	D4	D3	D2:D0
Name	PS	CS3	CS2	CS1	-	TS
Default	0	0	0	0	0	000

The Pattern State Register stores the pattern status. PS is the pattern enabled or not, CSx is the color enable or not, TS will show the running position of Pattern.

TS	Time State
000	Running at TS
001	Running at T1
010	Running at T2
011	Running at T3
100	Running at TP
101	Running at T4
110	Running at TC

CSx	Color State
0	Not running at Color x
1	Running at Color x

PS	Pattern State
0	Not running at Pattern
1	Running at Pattern

Table 11 10h/11h/12h/13h OUT1/OUT2/OUT3/OUT4 Current Level Register

Bit	D7:D0
Name	CL
Default	0000 0000

The output current may be computed using the Formula (1):

$$I_{OUT} = I_{BAND} \times \frac{CL}{256} \qquad (1)$$

$$I_{LED} = I_{OUT} \times \frac{PWM}{4096} \quad (2)$$

$$CL = \sum_{n=0}^{7} D[n] \cdot 2^n \quad (3)$$

Where D[n] stands for the individual bit value, 1 or 0, in location n, I_{BAND} is defined by the CB bits in Current Band Register (05h), PWM is the value of 1Ah~21h, I_{OUT} is the peak current of the outputs. I_{LED} is the average current of the outputs.

When IS31FL3197 operates in Current Level Mode, PWM = 4096.

When IS31FL3197 operates in PWM & Current Level Mode, the value of CL and PWM will decide the output current together.

When IS31FL3197 operates in Pattern Mode, PWM changes to make the auto breathing effect.

For example: in Current Level node only, if D7:D0 = 10110101,

$I_{OUT} = I_{BAND} (2^7 + 2^5 + 2^4 + 2^2 + 2^0)/256$

Table 12 10h~12h Color 1 Setting Register of Pattern (OUT1~OUT3)

Bit	D7:D0
Name	COL1_Oy
Default	0000 0000

14h~16h Color 2 Setting Register of Pattern (OUT1~OUT3)

Bit	D7:D0
Name	COL2_Oy
Default	0000 0000

17h~19h Color 3 Setting Register of Pattern (OUT1~OUT3)

Bit	D7:D0
Name	COL3_Oy
Default	0000 0000

Color Setting Registers store the color setting for each output in Pattern Mode. Check Pattern Color Setting section for more information about the color setting registers.

When IS31FL3197 operates in Pattern Mode, the value of Color Registers will decide the output current of each output in 256 levels.

The output current may be computed using the Formula (4):

$$I_{OUT} = I_{BAND} \times \frac{COLx\_Oy}{256} \quad (4)$$

$$COLx\_Oy = \sum_{n=0}^{7} D[n] \cdot 2^n \quad (5)$$

Where D[n] stands for the individual bit value, 1 or 0, in location n.

For example: if D7:D0 = 10110101,

$I_{OUT} = I_{BAND} (2^7 + 2^5 + 2^4 + 2^2 + 2^0)/256$

I_{OUT} is the peak current of the outputs. I_{BAND} is defined by the CB bits in Current Band Register (05h).

Need to write Color Update Register (2Bh) to update the data.

Table 13 1Ah~21h PWM Register

Reg	1Bh (1Dh, 1Fh, 21h)	1Ah (1Ch, 1Eh, 20h)
Bit	D3:D0	D7:D0
Name	PWM_H	PWM_L
Default	0000	0000 0000

When IS31FL3197 operates only in PWM & Current Level Mode, each output has 2 bytes to modulate the PWM duty in 4096 steps, in Pattern Mode, the PWM cannot be accessed.

I_{OUT} and the value of the PWM Registers decide the average current of each LED noted I_{LED}.

I_{OUT} is computed by Formula (6):

$$I_{LED} = I_{BAND} \times \frac{CL}{256} \times \frac{PWM}{4096} \quad (6)$$

Where I_{OUT} is the peak current of the outputs. I_{LED} is the average current of the outputs. I_{BAND} is defined by the CB bits in Current Band Register (05h), CL is defined by the CL bit in Current Level Register.

$$PWM = \sum_{n=0}^{11} D[n] \cdot 2^n \quad (7)$$

Where D[n] stands for the individual bit value, 1 or 0, in location n.

For example: if PWM_H = 00001001, PWM_L = 10110101,

$I_{LED} = I_{BAND} (2^{11} + 2^8 + 2^7 + 2^5 + 2^4 + 2^2 + 2^0)/4096$

PWM Registers need to update by writing PWM Update Register (2Ch).

Table 14 22h Pattern TS &T1 Setting Register

Bit	D7:D3	D4:D0
Name	T1	TS
Default	0000	0000

The TS & T1 Setting Registers set the TS and T1 time in Pattern Mode.

TS	Pattern Start Time Selection
0000	0.03s
0001	0.13s
0010	0.26s
0011	0.38s
0100	0.51s
0101	0.77s
0110	1.04s
0111	1.60s
1000	2.10s
1001	2.60s
1010	3.10s
1011	4.20s
1100	5.20s
1101	6.20s
1110	7.30s
1111	8.30s

T1	Rise Time Selection
0000	0.03s
0001	0.13s
0010	0.26s
0011	0.38s
0100	0.51s
0101	0.77s
0110	1.04s
0111	1.60s
1000	2.10s
1001	2.60s
1010	3.10s
1011	4.20s
1100	5.20s
1101	6.20s
1110	7.30s
1111	8.30s

Table 15 23h Pattern T2 &T3 Setting Register

Bit	D7:D3	D4:D0
Name	T3	T2
Default	0000	0000

The T2 & T3 Setting Registers set the T2 and T3 time in Pattern Mode.

T2	Hold Time Selection
0000	0.03s
0001	0.13s
0010	0.26s
0011	0.38s
0100	0.51s
0101	0.77s
0110	1.04s
0111	1.60s
1000	2.10s
1001	2.60s
1010	3.10s
1011	4.20s
1100	5.20s
1101	6.20s
1110	7.30s
1111	8.30s

T3	Fall Time Selection
0000	0.03s
0001	0.13s
0010	0.26s
0011	0.38s
0100	0.51s
0101	0.77s
0110	1.04s
0111	1.60s
1000	2.10s
1001	2.60s
1010	3.10s
1011	4.20s
1100	5.20s
1101	6.20s
1110	7.30s
1111	8.30s

Table 16 24h Pattern TP &T4 Setting Register

Bit	D7:D4	D3:D0
Name	T4	TP
Default	0000	0000

The TP & T4 Setting Registers set the TP and T4 time in Pattern Mode.

TP	Time between Pulses
0000	0.03s
0001	0.13s
0010	0.26s
0011	0.38s
0100	0.51s
0101	0.77s
0110	1.04s
0111	1.60s
1000	2.10s
1001	2.60s
1010	3.10s
1011	4.20s
1100	5.20s
1101	6.20s
1110	7.30s
1111	8.30s

T4	Off Time Selection
0000	0.03s
0001	0.13s
0010	0.26s
0011	0.38s
0100	0.51s
0101	0.77s
0110	1.04s
0111	1.60s
1000	2.10s
1001	2.60s
1010	3.10s
1011	4.20s
1100	5.20s
1101	6.20s
1110	7.30s
1111	8.30s

Table 17 25h Color Crossfade Enable Register

Bit	D7:D3	D2	D1	D0
Name	-	CFE3	CFE2	CFE1
Default	00000	0	0	1

Crossfade to next color function for each color in Pattern Mode. These enable status only active after T2 of each color (no need to update).

CFEx	Crossfade Enable Selection
0	Color x crossfade to next disable
1	Color x crossfade to next enable

Table 18 26h Crossfade Setting Register

Bit	D7:D4	D3:D0
Name	-	TC
Default	0000	0110

The Crossfade Setting Registers set the color crossfade time in Pattern Mode.

TC	Crossfade Time between Colors
00xx	0.51s
0100	0.51s
0101	0.77s
0110	1.04s
0111	1.60s
1000	2.10s
1001	2.60s
1010	3.10s
1011	4.20s
1100	5.20s
1101	6.20s
1110	7.30s
1111	8.30s

Table 19 27h Pattern Color Enable Register

Bit	D7:D3	D2	D1	D0
Name	-	CE3	CE2	CE1
Default	00000	0	0	1

Color Enable Register enables the color function for each color in Pattern Mode.

CEx	Color Enable Selection
0	Color x disable
1	Color x enable

Table 20 28h Pattern Color Cycle Times Register

Bit	D7:D6	D5:D4	D3:D2	D1:D0
Name	-	CCT3	CCT2	CCT1
Default	00	00	00	00

Pattern Color Cycle Times Register sets color loop times for each color.

CCTx	Color Cycle Times Selection
00	Endless
01	1 time
10	2 times
11	3 times

Table 21 29h Pattern Register

Bit	D7:D4	D3:D2	D1:D0
Name	MTPLT	GAM	-
Default	0000	00	00

GAM controls the gamma of pattern. MTPLT controls the loop of Pattern.

GAM	Gamma Selection
00/11	Gamma=2.4
01	Gamma=3.5
10	Linearity

MTPLT	Multi-Pulse Loop Time
0000	endless
0001	1 time
…	
1111	15 times

Table 22 2Ah Pattern Loop Times Register

Bit	D7	D6:D0
Name	PLT_H	PLT_L
Default	0	000 0000

If PLT_H(D7) =0, PLT_L! = 0

Pattern loop times:

$$Looptime = \sum_{n=0}^{6} D[n] \times 2^n \qquad (8)$$

If PLT_H(D7) =0, PLT_L=0, endless

If PLT_H(D7) =1, PLT_L! = 0

Pattern loop times:

$$Looptime = 16 \times \sum_{n=0}^{6} D[n] \times 2^n \qquad (9)$$

If PLT_H(D7) =1, PLT_L=0, endless

Where D[n] stands for the individual bit value.

2Bh Color Update Register

Write “0xC5” to 2Bh will update the data of 10h~13h/14h~16h/17h~19h.

2Ch PWM Update Register

Write “0xC5” to 2Ch will update the data of 1Ah~21h.

2Dh Pattern time Update Register

Write “0xC5” to 2Dh will update the data of 22h~24h.

3Fh Reset Register

Once user writes “0xC5” to the Reset Register, IS31FL3197 will reset all registers to their default value. On initial power-up, the IS31FL3197 registers are reset to their default values for a blank display.

TYPICAL APPLICATION INFORMATION

GENERAL DESCRIPTION

IS31FL3197 is a 4-channel fun LED driver which features two-dimensional auto breathing mode. It has Pattern Mode and Current Lever Mode for RGBW lighting effects.

The IS31FL3197 LED driver integrates a switched capacitor charge pump to power three LEDs with a programmable regulated current, up to 10mA (Max.) per channel. It only requires five external components; supply decoupling capacitor, an output bypass capacitor, 2 flying capacitors and a RISET.

Upon power up, the built-in charge pump converter will initialize in the 1x mode. To prevent a large in-rush current; the IS31FL3197 will first charge the CP capacitor to near VCC. The 1x mode provides maximum efficiency and minimum noise. The IS31FL3197 will remain in this mode until one of the LED current source drivers begins to drop out of regulation. When this drop out occurs the IS31FL3197 will switch to 2x mode after a soft-start period. The part will return to 1x mode whenever it is shut down.

The current delivered through the LED load is controlled by an internal configurable low dropout current source.

POWER ON SEQUENCE

IS31FL3197 provides a power-on reset feature that is controlled by VBAT supply voltage. When the VBAT supply voltage exceeds 2V (maximum), the internal circuit starts to work. The reset signal will be generated to perform a power-on reset (POR) operation, which will reset all control circuits and configuration registers until the internal power voltage become stable.

Before SDB pull high, the I2C operation is allowed. The SDB rising edge will reset the I2C bus.

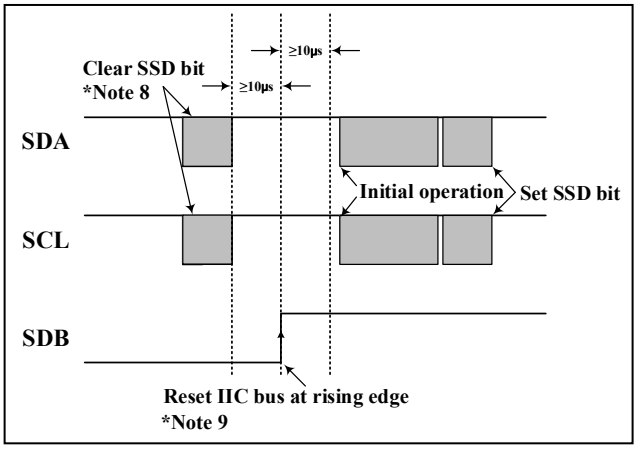


Figure 8 SDB Pin Sequence

Note 8: I2C operation is allowed when SDB is low.

Note 9: There should be no I2C operation 10μs before and after SDB rinsing edge.

When power on, the charging of the flying capacitors (CP) and output capacitance (C_{OUT})

In some cases, like a mouse, when plug-out and quickly plug-in back the USB power, the LED will flicker for a very short time. The reason is the power is not lower than the POR voltage point (usually lower than 2.0V), and the device still stores the previous setting data, if user pull-up the SDB high when power up, following with the initial operation, the LED will be ON between SDB rising edge and Current Level initial effective, to avoid this, as above figure, a writing to 01h is recommended to shut down the chip before pull-high the SDB pin.

The IS31FL3197 charge pump circuit may result in a risk of power supply voltage (VCC) dipping below 2V if the bypass capacitance on VCC pin is not enough. As below, Figure 9, there is about 70mA inrush current and supply voltage (VCC) may drop from 2.2V to about 1.44V when the VCC bypass capacitance is only 0.1μF. IS31FL3197 normal VCC power supply voltage range is 2.0V~3.3V, and if it drops to 1.44V (lower than 2V), a power-on reset (POR) may be triggered and IS31FL3197 will not startup properly and the charge pump output (VOUT) will have no output (as illustrated in Figure 8, low supply voltage application start-up waveform).

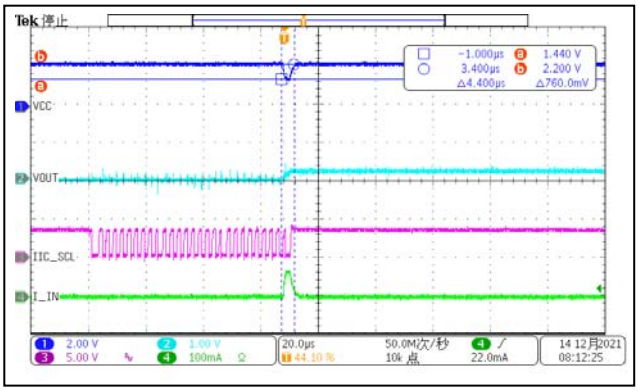


Figure 9 Low Supply Voltage Application Start-up

The reason for this is that the IS31FL3197 has a charge pump structure, where it is necessary to charge the flying capacitors (CP) and output capacitance (COUT) when IS31FL3197 starts up (or is released from shutdown mode).

The charging inrush current at startup charges the flying capacitors (CP) and output capacitor (COUT). Due to the internal resistance of the power supply (VCC) and the impedance of PCB layout traces, the inrush current can cause the supply voltage to drop.

For the above startup risk, there are two suggested methods (of hardware and software) to avoid this.

In terms of hardware, the risk can be avoided by adjusting the power supply capacitor's capacitance value. The power supply capacitor is used for energy storage and filtering, and selecting appropriate capacitance value can ensure that the voltage remains above 2V during IS31FL3197's startup.

The recommended capacitance values for power supply capacitor under different supply voltages are listed in below table:

Table 23 Recommended Capacitance Values vs. VCC

VCC	Capacitance Values
3.3V	2.2μF+0.1μF
3.0V	2.2μF+0.1μF
2.7V	4.7μF+0.1μF
2.4V	4.7μF+0.1μF
2.2V	10μF+0.1μF
2.0V	10μF+10μF+0.1μF or 22μF+0.1μF

In terms of software, in normal case, after SDB pin is pulled to high, normal operation is to write 01h once to release shutdown mode. As illustrated in Figure 10, writing Shutdown Control Register (01h) only 1 time will make the VCC dropped to 1.36V (lower than 2V), a power-on reset (POR) may be triggered and IS31FL3197 will not startup properly and the charge pump output (VOUT) has no output (as illustrated in Figure 10).

It is recommended to write the Shutdown Control Register (01h) triple times, each time with delay time of about 150us-5ms to startup the IS31FL3197 3 times. This increases the charging time for the COUT and flying capacitors and ensure the IC can start up normally.

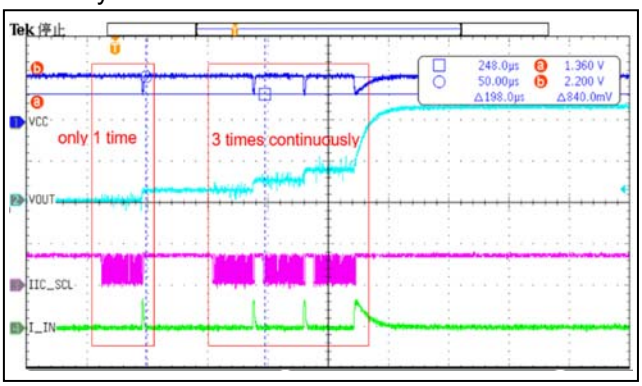


Figure 10 Software Suggestion Sequence

As illustrated above in Figure 10, to ensure the effectiveness of the software method, there needs to be a recommended delay time interval of about 150us to 5ms after each startup command write is performed 3 times successively to the IS31FL3197.

CHARGE PUMP

The converter is based on a 3-stage charge pump technique to efficiently generate a DC voltage to supply the RGBW LED current. The system regulates the current flowing into each LED, not the DC VOUT value. The built−in OVP circuit continuously monitors the VOUT voltage and stops the charge pump when the voltage is above 3.9V. It resumes normal operation when the voltage drops below 3.9V. The IS31FL3197 can operate under no load conditions.

The integrated capacitive charge pump is designed for $V_{OUT}= V_{CC} \times$ Mode, where Mode = 1, 1.5 or 2. The charge pump converter only needs four external components: supply decoupling capacitor, output bypass capacitor and two flying capacitors.

To maintain the lowest output resistance, use capacitors with low ESR. The charge-pump output resistance is a function of CP and COUT's ESR and the internal switch resistance. Minimizing the charge-pump capacitor's ESR minimizes the total resistance.

Using larger flying capacitors (CP) reduces the output impedance and improves efficiency however, above a certain point, increasing CP's capacitance has a negligible effect because the output resistance becomes dominated by the internal switch resistance and capacitor ESR. But when space is a constraint, it may be necessary to sacrifice low output resistance for the sake of small capacitor size.

Increasing the output capacitance (C_{OUT}) reduces the output ripple voltage. Decreasing its ESR reduces both output resistance and ripple. Smaller capacitance values can be used with light loads. Use the following equation to calculate the peak-to-peak ripple:

$V_{RIPPLE} = I_{OUT}/(f_{OSC} \times C_{OUT}) + 2 \times I_{OUT} \times ESRCOUT$ (10)

A bypass capacitor on the incoming supply will reduce its AC impedance and the impact of the charge pump switching noise. A 0.1μF bypass capacitor is sufficient.

ISET MAXIMUM OUTPUT CURRENT

The maximum output current of OUT1~OUT4 can be adjusted by the external resistor, R_{ISET}, as described in Formula (11).

$$I_{GMAX} = \frac{75}{R_{ISET}} \qquad (11)$$

The recommended value of R_{ISET} is 7.5kΩ.

When R_{ISET}=7.5kΩ, I_{GMAX}=10mA.

There are four programmed current bands which can be set by the Current Band Register (05h). It is used to set the maximum current of each output, I_{BAND}.

By setting the MODx bits of the Operating Configure Register (02h) to “1x” (MOD1~MOD3) or “1” (MOD4), the corresponding output will operate in Current Level Mode.

The minimum I_{OUT} of each out is 2.5mA and to achieve this, when minimum CBx of 05h is “00” (I_{BAND}=1/4 I_{GMAX}), maximum R_{ISET} is 7.5kΩ, when minimum CBx of 05h is “01” (I_{BAND}=2/4 I_{GMAX}), maximum R_{ISET} is 15kΩ, when minimum CBx of 04h is “01” (I_{BAND}=3/4 I_{GMAX}), maximum R_{ISET} is 22.5kΩ, when minimum CBx of 04h is “00” (I_{BAND}=4/4 I_{GMAX}), maximum R_{ISET} is 30kΩ.

If R_{ISET} is smaller than 7.5kΩ, the output current will increase according the Formula 8, recommend absolute minimum RISET is 6.25kΩ (CBx of 05h is “00”, I_{GMAX}=12mA).

PWM CONTROL

The PWM Registers (1Ah~21h) can modulate LED brightness of each channels with 4096 steps. For example, if the data in PWM_H Register is “0000 0000” and in PWM_L Register is “0000 0100”, then the PWM is 4/4096.

Writing new data continuously to the registers can modulate the brightness of the LEDs to achieve a breathing effect.

CURRENT LEVEL MODE

The Current Level Registers (10h~13h) are active and can modulate LED peak current IOUT of each output with 256 steps independently. For example, if the data in Current Lever Register is “0000 0100”, then the current level is the fourth step, with a current level of 4/256.

In Current Level Mode, user doesn’t need to turn on the CEx of 27h, a new value must be written to the Current Level registers to change the output current. Writing new data continuously to the registers can modulate the brightness of the LEDs to achieve breathing, blinking, or any other effects that the user defines.

PWM & CURRENT LEVEL MODE

PWM & Current Level Mode is the combination of PWM and Current Level Mode. In this mode, the Current Level Registers (10h~13h) adjust the peak current (I_{OUT}) of the outputs, the PWM Registers (1Ah~21h) adjust the duty cycle of the output current, the finial result is the output average current ILED.

PATTERN MODE

By setting the MOD1~MOD3 bits of the Operating Configure Register (02h) to “01”, the corresponding output will operate in Pattern Mode. In Pattern Mode, the timing characteristics for output current - current rising (T1), holding (T2), falling (T3) and off time (TS, TP, T4), can be adjusted individually so that each output can independently maintain a pre-established pattern achieving mixing color breathing or a single color breathing without requiring any additional interface activity, thus saving valuable system resources.

PATTERN COLOR SETTING

In Pattern Mode, the LED color is defined by COLx_Oy (x, y= 1, 2, 3) bits in Color Setting Registers (10h~19h). There are 3 RGB current combinations to generate 3 pre-defined colors for display. More than one of the 3 pre-defined colors can be chosen by setting CEx bits in Color Enable Register (27h). When CEx is set, the color x is allowed to be displayed in current pattern.

In Current Level Mode, the output current (OUT1~OUT4) is configured by the Current Level Register (10h~13h) as Table 23.

Table 24 Color Register of Current Level Mode

Mode	OUT1	OUT2	OUT3	OUT4
Current Level	10h	11h	12h	13h

In PWM Mode, the output current (OUT1~OUT4) is configured by the PWM Register (1Ah~21h) as Table 24.

Table 25 PWM Register of PWM & Current Level Mode

Mode	OUT1	OUT2	OUT3	OUT4
PWM_H	1Bh	1Dh	1Fh	21h
PWM_L	1Ah	1Ch	1Eh	20h

In Pattern Mode, the output current (OUT1~OUT3) is configured by the Color Setting Register of Pattern as Table 25.

Table 26 Color Register of Pattern Mode

Pattern Mode	Color Enable	OUT1	OUT2	OUT3
Pattern	CE1(27h)	10h	11h	12h
	CE2(27h)	14h	15h	16h
	CE3(27h)	17h	18h	19h

PATTERN TIME SETTING

User should configure the related pattern time setting registers according to actual timing requirements via I2C interface before starting pattern. The pattern time is including TS, T1~T4 and TP. And the pattern has three continue lighting cycle as Color 1~Color 3. Please check the LED OPERATING MODE section for more about the time setting.

GAMMA CORRECTION

In order to perform a better visual LED breathing effect, the device integrates gamma correction to the Pattern Mode. The gamma correction causes the

change in intensity to appear more linear to the human eye.

Gamma correction, also known as gamma compression or encoding, is used to encode linear luminance to match the non-linear characteristics of display. Since the IS31FL3197 can modulate the brightness of the LEDs with 256 steps, a gamma correction function can be applied when computing each subsequent LED intensity setting such that the changes in brightness matches the human eye's brightness curve.

The IS31FL3197 provides three gamma corrections which can be set by GAM bits of Pattern Registers (29h) for each pattern. The gamma correction is shown as below.

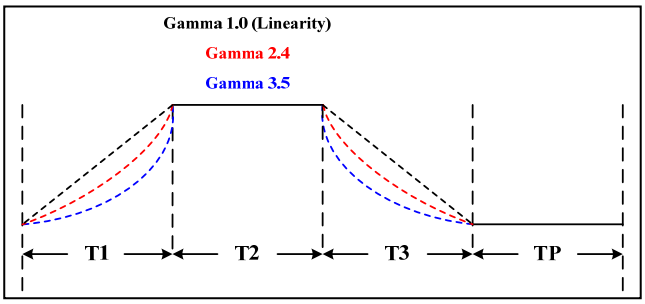


Figure 11 Gamma Correction

CROSSFADE

The IS31FL3197 features the crossfade effect which supports one color crossfade to another. This feature works based on Pattern Mode, it will skip the T3, TP and next color's T1, replacing with a color crossfade effect.

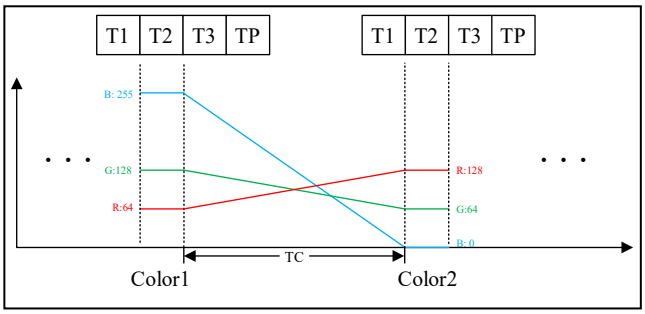


Figure 12 Color Crossfade Example

To enable color crossfade effect, the CFEx bit of Color Crossfade Enable Register need to set to "1", for example, if trying to let color 1 crossfade to color 2, the CFE1 should be set to "1".

Crossfade effect will change one color to another linear and smoothly, for example, if color 1 of RGB is (RGB=64:128:255), color 2 is (RGB=128:64:0), for red color LED, the current level will change from 64 to 128, the crossfade algorithm will calculate the variation, which is 128-64=+64, and make the result become linear change from initial value(64) to target value(128) in time slot of TC which is defined in Crossfade Setting Register(26h). At the same time green LED (G) and blue (B) will do same work to make color 1 crossfade to color 2 smoothly.

SHUTDOWN MODE

Shutdown mode can either be used as a means of reducing power consumption or generating a flashing display (repeatedly entering and leaving shutdown mode). During shutdown mode all registers retain their data.

Software Shutdown

By setting SSD bit of the Shutdown Register (00h) to "0", the IS31FL3197 will operate in software shutdown mode, wherein it will consume only 1μA (typ.) current. When the IS31FL3197 is in software shutdown mode, all current sources are switched off.

Hardware Shutdown

The chip enters hardware shutdown mode when the SDB pin is pulled low, wherein they consume only 1μA (Typ.) current. When set SDB high, the rising edge will reset the I2C module, but the register information retains.

LED OPERATING MODE

The IS31FL3197 has three operating modes which can be chosen by the MODx bits of Operating Configure Register (02h).

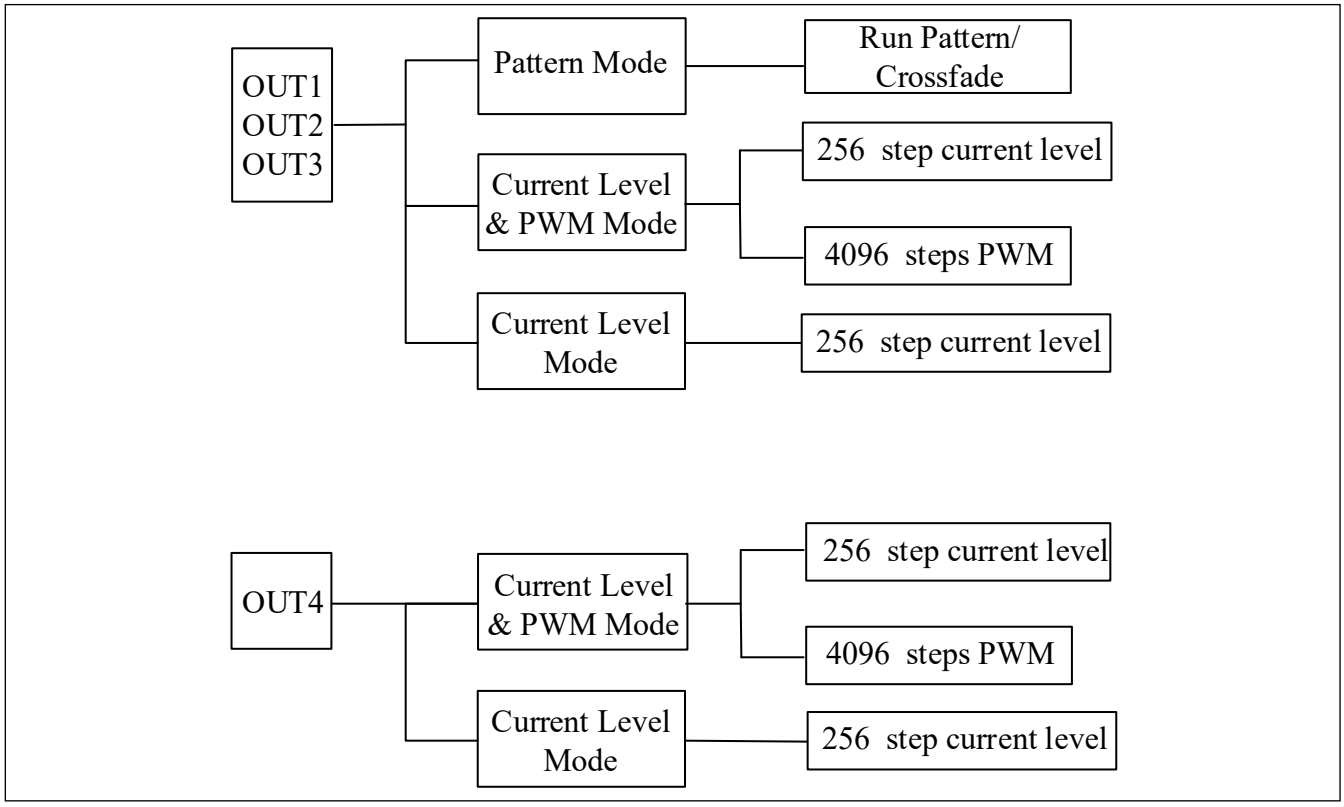


Figure 13 Operating Mode Map

Pattern Mode

If MODx=10 (Pattern Mode), OUT1~OUT3 can operate in Pattern Mode only and run the pattern.

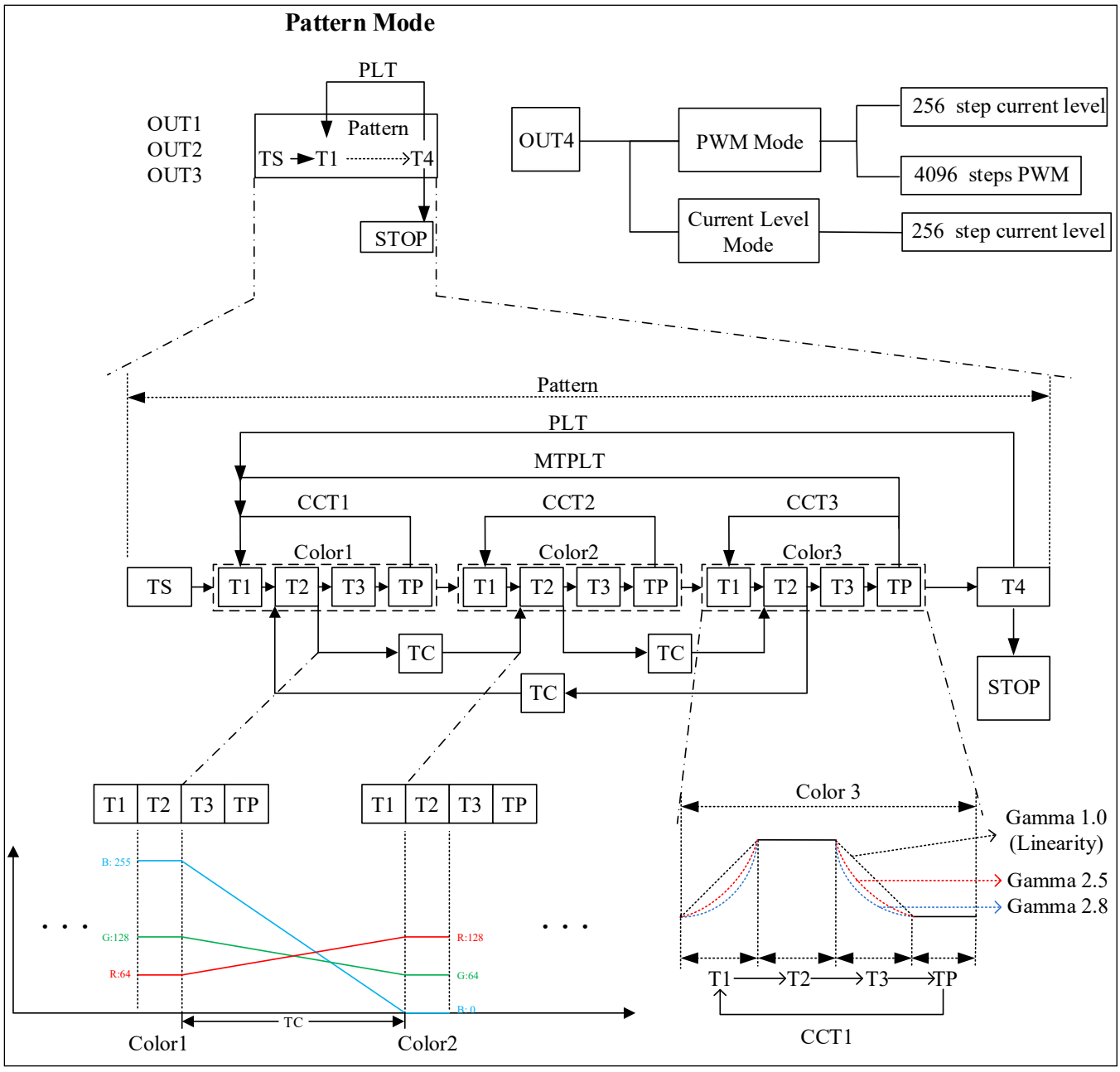


Figure 14 Pattern Mode

CLASSIFICATION REFLOW PROFILES

Profile Feature	Pb-Free Assembly
Preheat & Soak Temperature min (Tsmin) Temperature max (Tsmax) Time (Tsmin to Tsmax) (ts)	150°C 200°C 60-120 seconds
Average ramp-up rate (Tsmax to Tp)	3°C/second max.
Liquidous temperature (TL) Time at liquidous (tL)	217°C 60-150 seconds
Peak package body temperature (Tp)*	Max 260°C
Time (tp)** within 5°C of the specified classification temperature (Tc)	Max 30 seconds
Average ramp-down rate (Tp to Tsmax)	6°C/second max.
Time 25°C to peak temperature	8 minutes max.

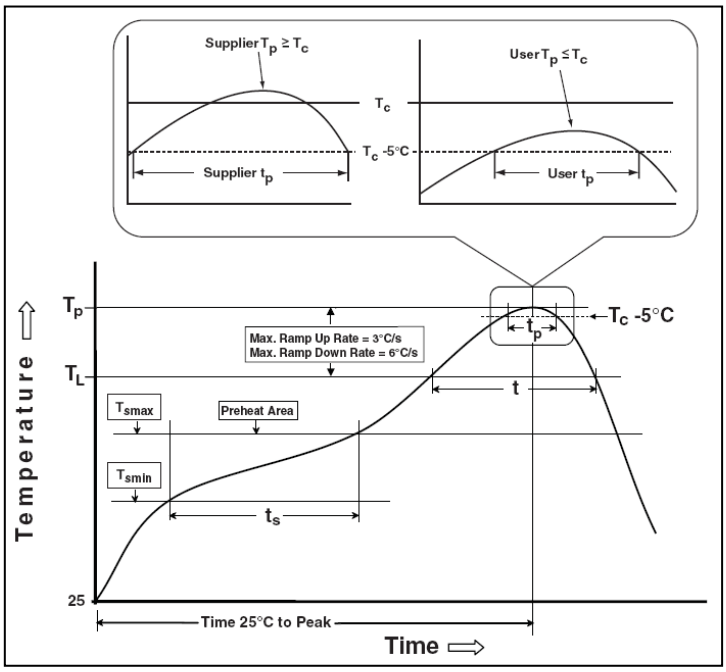
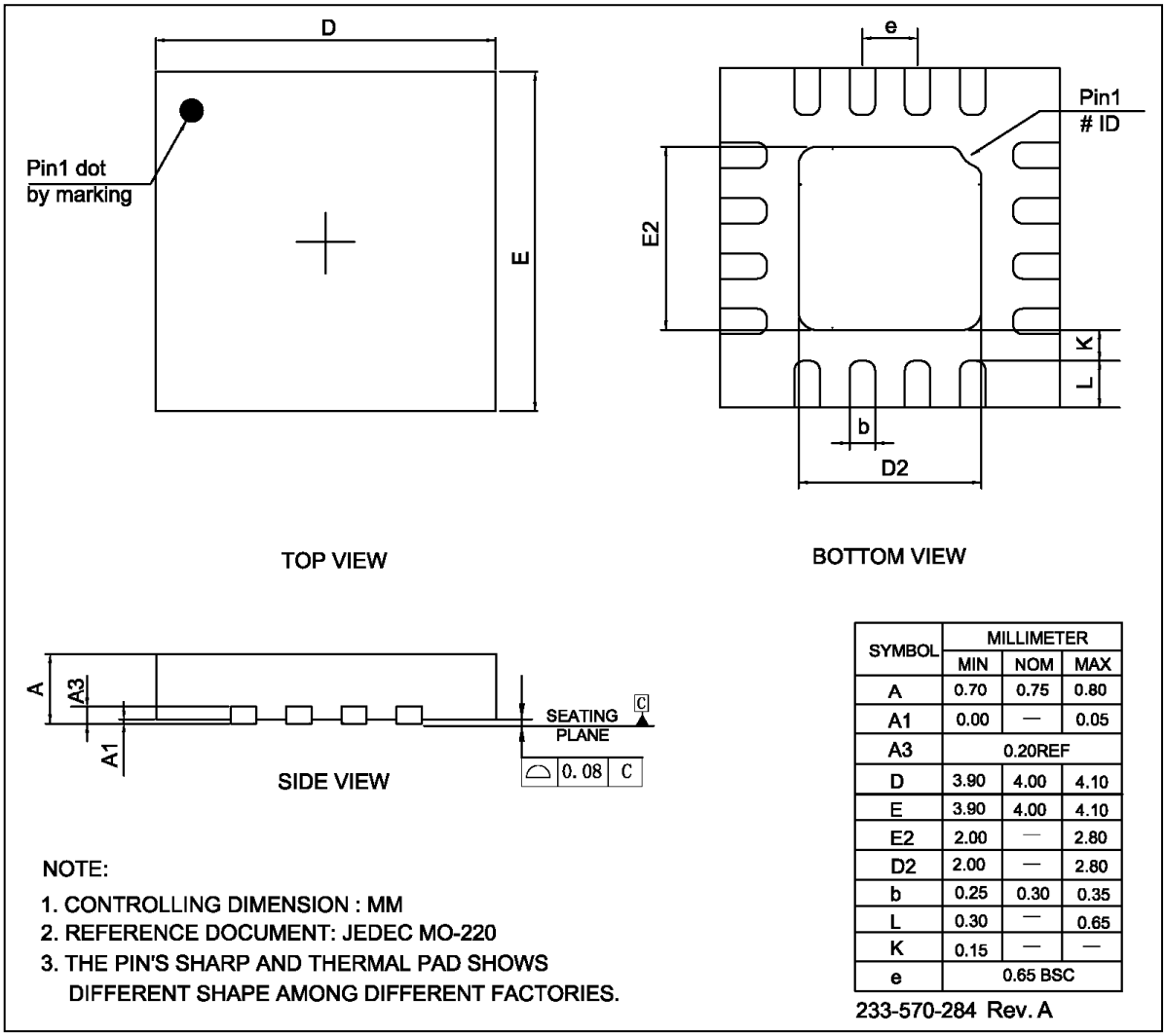


Figure 15 Classification Profile

PACKAGE INFORMATION

QFN-16



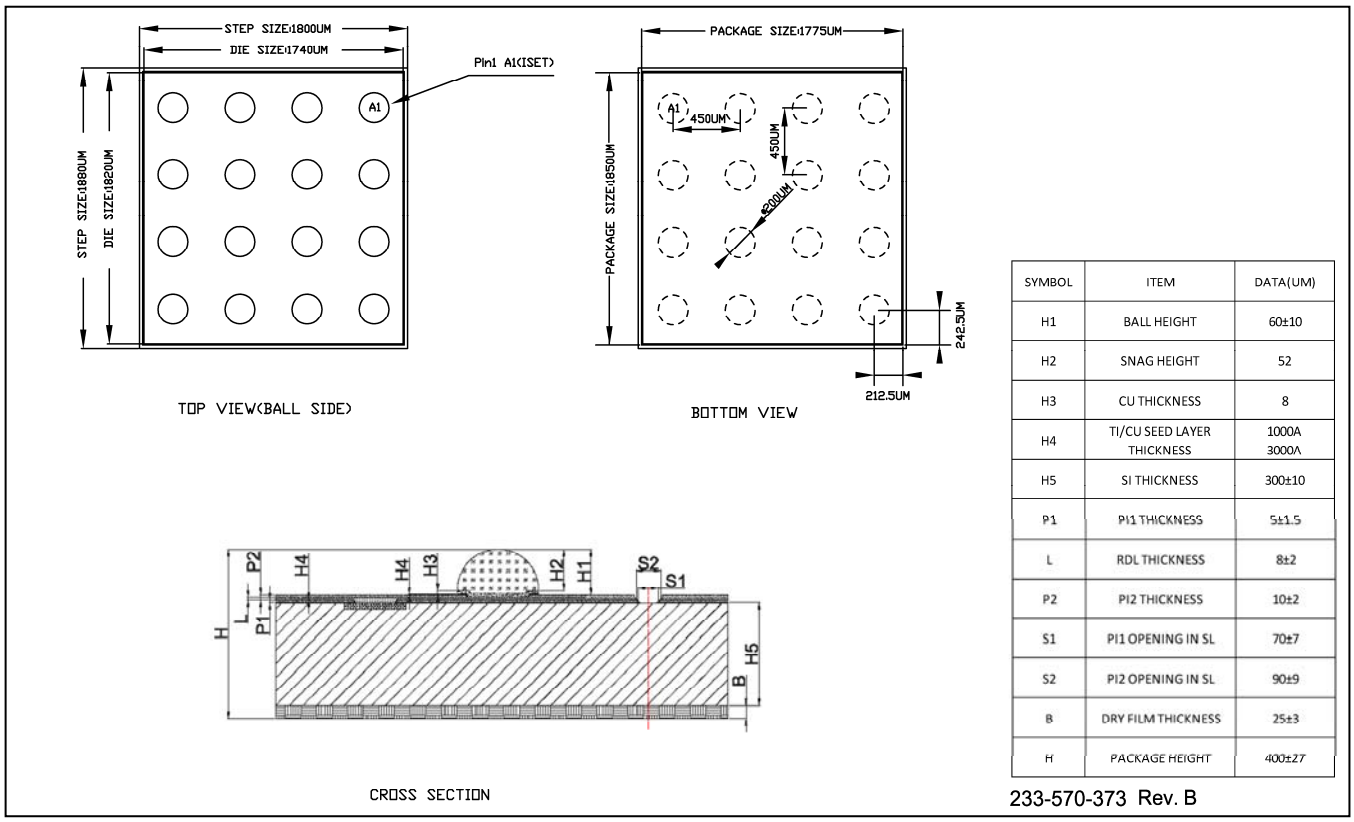
SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	0.70	0.75	0.80
A1	0.00	—	0.05
A3		0.20REF	
D	3.90	4.00	4.10
E	3.90	4.00	4.10
E2	2.00	—	2.80
D2	2.00	—	2.80
b	0.25	0.30	0.35
L	0.30	—	0.65
K	0.15	—	—
e		0.65 BSC	

NOTE:

1. CONTROLLING DIMENSION : MM
2. REFERENCE DOCUMENT: JEDEC MO-220
3. THE PIN'S SHARP AND THERMAL PAD SHOWS DIFFERENT SHAPE AMONG DIFFERENT FACTORIES.

233-570-284 Rev. A

WLCSP-16

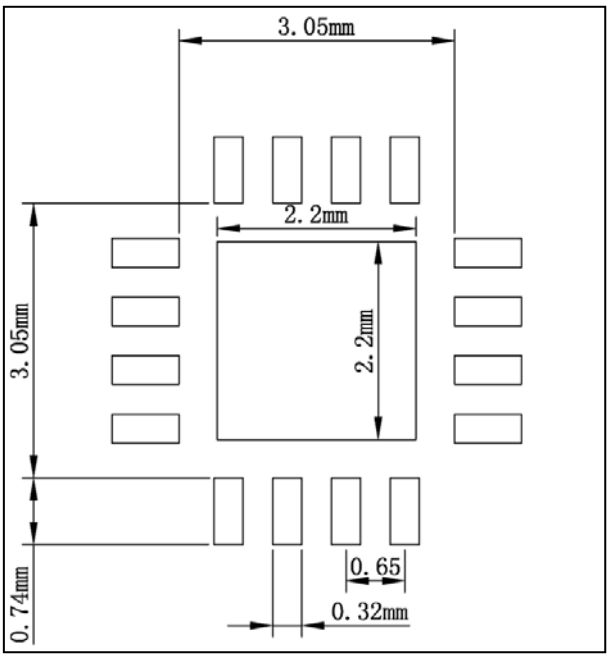


SYMBOL	ITEM	DATA(UM)
H1	BALL HEIGHT	60±10
H2	SNAG HEIGHT	52
H3	CU THICKNESS	8
H4	TI/CU SEED LAYER THICKNESS	1000A 3000A
H5	SI THICKNESS	300±10
P1	PI1 THICKNESS	5±1.5
L	RDL THICKNESS	8±2
P2	PI2 THICKNESS	10±2
S1	PI1 OPENING IN SL	70±7
S2	PI2 OPENING IN SL	90±9
B	DRY FILM THICKNESS	25±3
H	PACKAGE HEIGHT	400±27

233-570-373 Rev. B

RECOMMENDED LAND PATTERN

QFN-16



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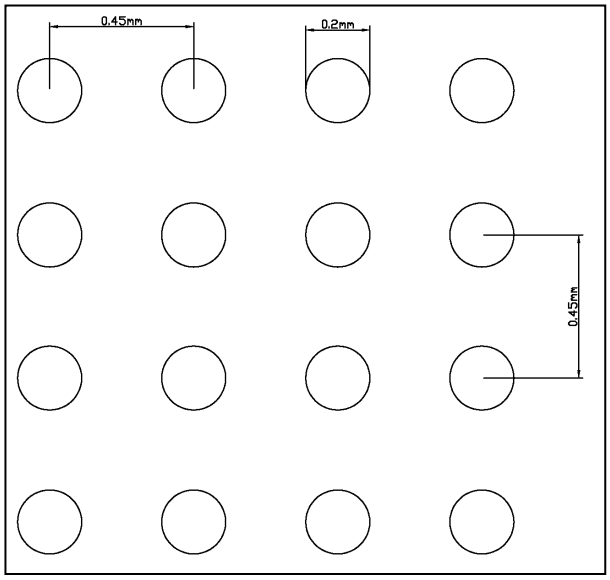

Note:

1. Land pattern complies to IPC-7351.
2. All dimensions in MM.
3. This document (including dimensions, notes & specs) is a recommendation based on typical circuit board manufacturing parameters. Since land pattern design depends on many factors unknown (eg. User's board manufacturing specs), user must determine suitability for use.

REVISION HISTORY

Revision	Detail Information	Date
0A	1. Update typical application circuit 2. Update EC table 3. Add crossfade effect details	2019.12.05
A	Release to mass production	2020.07.28
B	1. Update typical application circuit 2. Update TYPICAL APPLICATION INFORMATION (Add POWER ON SEQUENCE) 3. Update ABSOLUTE MAXIMUM RATINGS (Supply voltage VCC from -0.3V ~+3.6V to -0.3V ~ +3.7V)	2022.04.20