IS31FL3206

12-CHANNEL LED DRIVER; SELECTABLE PWM FREQUENCY

June 2024

GENERAL DESCRIPTION

IS31FL3206 is comprised of 12 constant current channels each with independent PWM control, designed for driving LEDs, PWM frequency can be 24kHz (default) or 3.6kHz. The output current of each channel can be set at up to 38mA (Max.) by an external resistor and independently scaled by a factor of 1, 11/12, 9/12 and 7/12. The average LED current of each channel can be changed in 256 steps by changing the PWM duty cycle through an I2C interface.

The chip can be turned off by pulling the SDB pin low or by using the software shutdown feature to reduce power consumption.

IS31FL3206 is available in QFN-20 (3mm × 3mm) package. It operates from 2.7V to 5.5V over the temperature range of -40°C to +125°C.

FEATURES

- 2.7V to 5.5V supply
- Each channel output current up to 38mA
- Accuracy between channels and ICs: <±6% (Max.)
- I2C interface, automatic address increment function
- Four selectable I2C addresses
- Internal reset register
- Modulate LED brightness with 256 steps PWM
- Each channel can be controlled independently
- Each channel can be scaled independently by 1, 11/12, 9/12 and 7/12
- PWM frequency selectable
  - 24kHz (default)
  - 3.6kHz
- -40°C to +125°C temperature range
- QFN-20 (3mm × 3mm) package
- RoHS & Halogen-Free Compliance
- TSCA Compliance

APPLICATIONS

- AI-speakers and smart home devices
- LED in home appliances
- LED display for hand-held devices

TYPICAL APPLICATION CIRCUIT

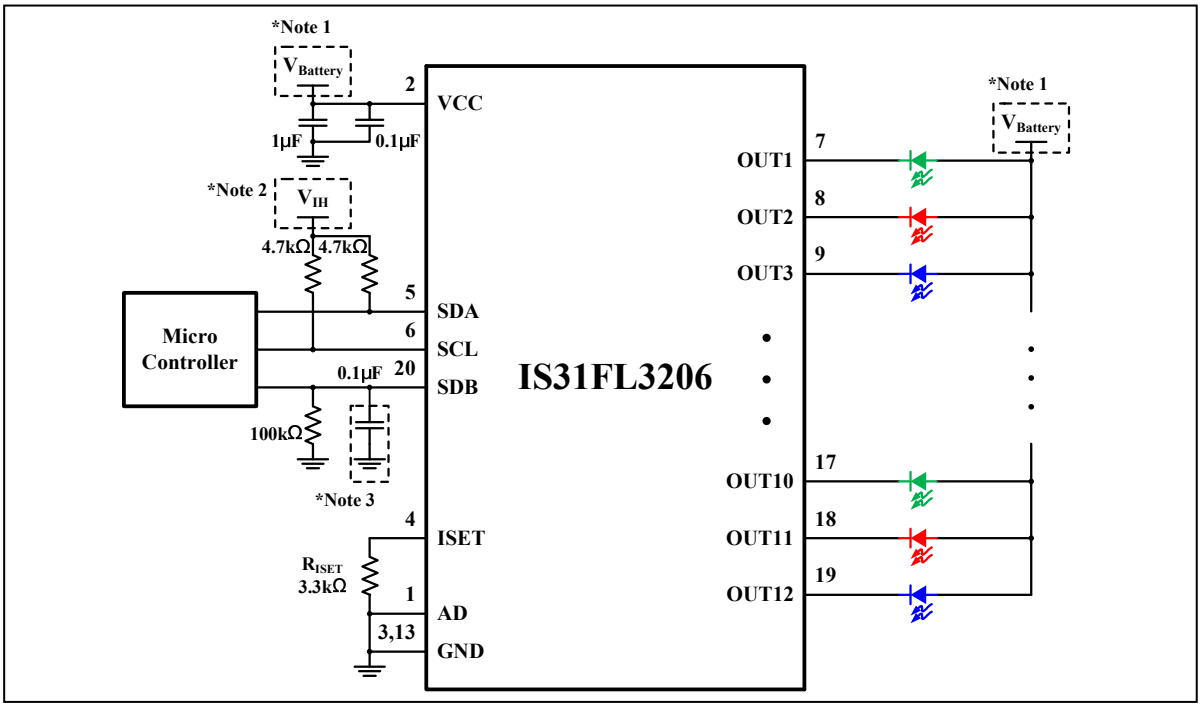


Figure 1 Typical Application Circuit (V_{CC}= Battery)

TYPICAL APPLICATION CIRCUIT(CONTINUED)

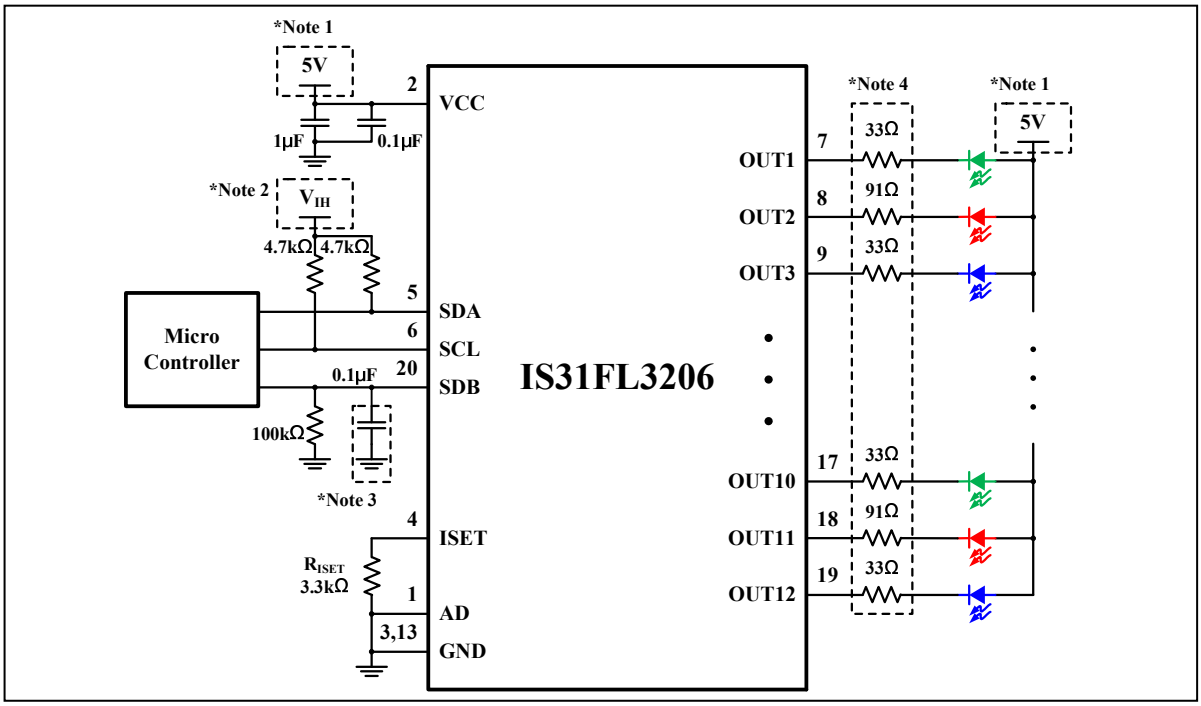


Figure 2 Typical Application Circuit (V_{CC}= 5V)

Note 1: V_{LED+} should be same as VCC voltage.

Note 2: V_{IH} is the high level voltage for IS31FL3206, which is usually same as V_{CC} of Micro Controller, e.g. if V_{CC} of Micro Controller is 3.3V, V_{IH}=3.3V. If V_{CC}=5V and V_{IH} is lower than 2.8V, recommend to add a level shift circuit for SDA and SCL.

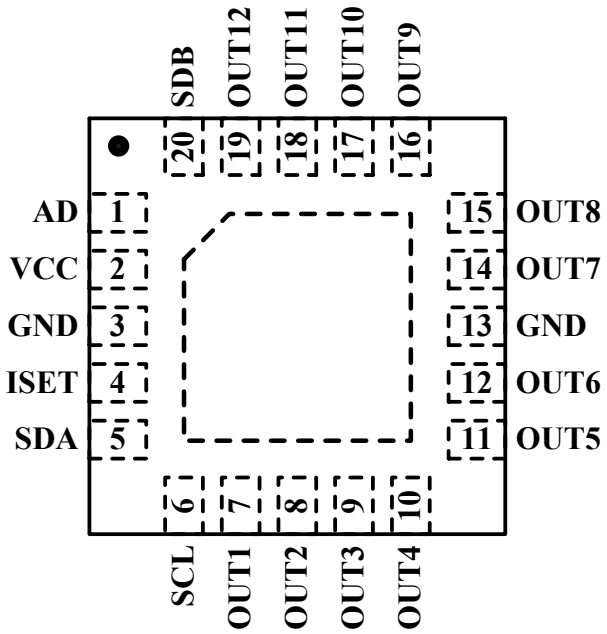
Note 3: A 0.1μF capacitor is necessary for passing the EFT test.

Note 4: These resistors are optional to help reduce the power of IS31FL3206 only (values are for V_{LED+}=5V).

Note 5: The maximum output current is set to 38mA when R_{ISET}= 2kΩ. Please refer to current setting section in application information.

Note 6: The IC should be placed far away from the antenna in order to prevent the EMI.

PIN CONFIGURATION

Package	Pin Configuration (Top View)
QFN-20	

PIN DESCRIPTION

No.	Pin	Description
1	AD	I2C address setting.
2	VCC	Power supply.
3, 13	GND	Ground.
4	ISET	Input terminal used to connect an external resistor. This regulates the global output current.
5	SDA	I2C serial data.
6	SCL	I2C serial clock.
7~12	OUT1~OUT6	Output channel 1~6 for LEDs.
14~19	OUT7 ~ OUT12	Output channel 7~12 for LEDs.
20	SDB	Shutdown the chip when pulled low.
	Thermal Pad	Connect to GND.

ORDERING INFORMATION

Industrial Range: -40°C to +125°C

Order Part No.	Package	QTY/Reel
IS31FL3206-QFLS4-TR	QFN-20, Lead-free	2500

ABSOLUTE MAXIMUM RATINGS

Supply voltage, V_{CC}	-0.3V ~ +6.0V
Voltage at SCL, SDA, SDB, OUT1 to OUT12	-0.3V ~ V_{CC}+0.3V
Maximum junction temperature, T_{JMAX}	+150°C
Storage temperature range, T_{STG}	-65°C ~ +150°C
Operating temperature range, T_A=T_J	-40°C ~ +125°C
Package thermal resistance, junction to ambient (4-layer standard test PCB based on JESD 51-2A), θ_{JA}	57.9°C/W
ESD (HBM) ESD (CDM)	±8kV ±1kV

Note 7: Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other condition beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

Typical values are T_A = 25°C, V_{CC} = 3.6V.

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
V_{CC}	Supply voltage		2.7		5.5	V
I_{MAX}	Maximum global output current	V_{CC} = 4.2V, V_{OUT} = 0.8V R_{ISET} = 2kΩ, SL = "010000" (Note 8)		38		mA
I_{OUT}	Output current	V_{OUT} = 0.6V R_{ISET} = 3.3kΩ, SL = "010000"		23		mA
ΔI_{MATCH}	Output current mismatch between channels	V_{OUT} = 0.6V R_{ISET}= 3.3kΩ, SL = "010000" (Note 9)	-6		6	%
V_{HR}	Headroom voltage	R_{ISET} = 3.3kΩ, I_{OUT}=20mA SL = "010000"		0.4	0.6	V
I_{CC}	Quiescent power supply current	R_{ISET} = 3.3kΩ		5	6.5	mA
I_{SD}	Shutdown current	V_{SDB} = 0V or software shutdown T_A = 25°C, V_{CC} = 3.6V		2	3	μA
f_{OUT}	PWM frequency of output	0x27=0x00		24		kHz
		0x27=0x01		3.6		kHz
I_{OZ}	Output leakage current	V_{SDB} = 0V or software shutdown, V_{OUT}= V_{CC}= 5.5V			0.2	μA
T_{SHDN}	Thermal shutdown	(Note 10)		160		°C
$T_{SHDNHYST}$	Hysteresis	(Note 10)		20		°C
V_{ISET}	Output voltage of ISET pin			1.3		V
Logic Electrical Characteristics (SDA, SCL, SDB, AD)						
V_{IL}	Logic "0" input voltage	V_{CC} = 2.7V~5.5V			0.4	V
V_{IH}	Logic "1" input voltage	V_{CC} = 2.7V~5.5V	1.4			V
I_{IL}	Logic "0" input current	V_{INPUT} = 0V (Note 10)		5		nA
I_{IH}	Logic "1" input current	V_{INPUT} = V_{CC} (Note 10)		5		nA

DIGITAL INPUT SWITCHING CHARACTERISTICS (NOTE 10)

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
f_{SCL}	Serial-Clock frequency				400	kHz
t_{BUF}	Bus free time between a STOP and a START condition		1.3			μs
$t_{HD, STA}$	Hold time (repeated) START condition		0.6			μs
$t_{SU, STA}$	Repeated START condition setup time		0.6			μs
$t_{SU, STO}$	STOP condition setup time		0.6			μs
$t_{HD, DAT}$	Data hold time (Note 11)				0.9	μs
$t_{SU, DAT}$	Data setup time (Note 12)		100			ns
t_{LOW}	SCL clock low period		1.3			μs
t_{HIGH}	SCL clock high period		0.7			μs
t_R	Rise time of both SDA and SCL signals, receiving (Note 13)			20+0.1C_b	300	ns
t_F	Fall time of both SDA and SCL signals, receiving (Note 13)			20+0.1C_b	300	ns

Note 8: The recommended minimum value of R_{ISET} is 2kΩ, or it may cause a large current.

Note 9: $\Delta I_{MATCH}= (I_{OUT}- I_{AVG})/I_{AVG}\times100\%$. $I_{AVG}= (I_{OUT1}+I_{OUT2}+\ldots I_{OUT12})/12$.

Note 10: Guaranteed by design.

Note 11: The minimum $t_{HD, DAT}$ measured start from V_{IL}(max) of SCL signal. The maximum $t_{HD,DAT}$ has only to be met if the device does not stretch the LOW period (t_{LOW}) of the SCL signal. V_{IL}(max)

Note 12: A Fast-mode I2C-bus device can be used in a Standard-mode I2C-bus system, but the requirement $t_{SU,DAT}\geq$ 250 ns must then be met. This will automatically be the case if the device does not stretch the LOW period of the SCL signal. If such a device does stretch the LOW period of the SCL signal, it must output the next data bit to the SDA line t_R max + $t_{SU,DAT}$ = 1000 + 250 = 1250ns (according to the Standard-mode I2C-bus specification) before the SCL line is released.

Note 13: C_b= total capacitance of one bus line in pF. $I_{SINK} \leq$ 6mA. t_R and t_F measured between 0.3 × V_{CC} and 0.7 × V_{CC}. Guaranteed by design.

DETAILED DESCRIPTION

I2C INTERFACE

The IS31FL3206 uses a serial bus, which conforms to the I2C protocol, to control the chip's functions with two wires: SCL and SDA. The IS31FL3206 has a 7-bit slave address (A7:A1), followed by the R/W bit, A0. Since IS31FL3206 only supports write operations, A0 must always be "0". The value of bits A1 and A2 are decided by the connection of the AD pin.

The complete slave address is:

Table 1 Slave Address (Write Only):

Bit	A7:A3	A2:A1	A0
Value	11011	AD	0

AD connected to GND, AD = 00;
AD connected to VCC, AD = 11;
AD connected to SCL, AD = 01;
AD connected to SDA, AD = 10;

The SCL line is uni-directional. The SDA line is bi-directional (open-collector) with a pull-up resistor (typically 4.7kΩ). The maximum clock frequency specified by the I2C standard is 400kHz. In this discussion, the master is the microcontroller and the slave is the IS31FL3206.

The timing diagram for the I2C is shown in Figure 3. The SDA is latched in on the stable high level of the SCL. When there is no interface activity, the SDA line should be held high.

The "START" signal is generated by lowering the SDA signal while the SCL signal is high. The start signal will alert all devices attached to the I2C bus to check the incoming address against their own chip address.

The 8-bit chip address is sent next, most significant bit first. Each address bit must be stable while the SCL level is high.

After the last bit of the chip address is sent, the master checks for the IS31FL3206's acknowledge. The master releases the SDA line high (through a pull-up resistor). Then the master sends an SCL pulse. If the IS31FL3206 has received the address correctly, then it holds the SDA line low during the SCL pulse. If the SDA line is not low, then the master should send a "STOP" signal (discussed later) and abort the transfer.

Following acknowledge of IS31FL3206, the register address byte is sent, most significant bit first. IS31FL3206 must generate another acknowledge indicating that the register address has been received.

Then 8-bit of data byte are sent next, most significant bit first. Each data bit should be valid while the SCL level is stable high. After the data byte is sent, the IS31FL3206 must generate another acknowledge to indicate that the data was received.

The "STOP" signal ends the transfer. To signal "STOP", the SDA signal goes high while the SCL signal is high.

ADDRESS AUTO INCREMENT

To write multiple bytes of data into IS31FL3206, load the address of the data register that the first data byte is intended for. During the IS31FL3206 acknowledge of receiving the data byte, the internal address pointer will increment by one. The next data byte sent to IS31FL3206 will be placed in the new address, and so on. The auto increment of the address will continue as long as data continues to be written to IS31FL3206 (Figure 6).

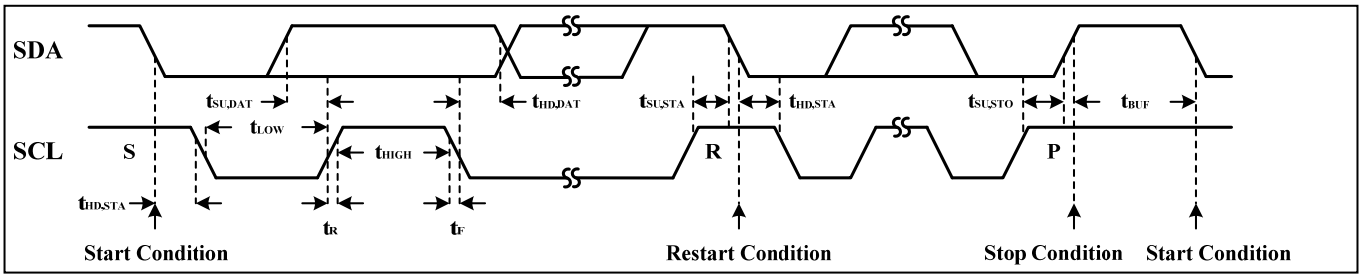


Figure 3 Interface Timing

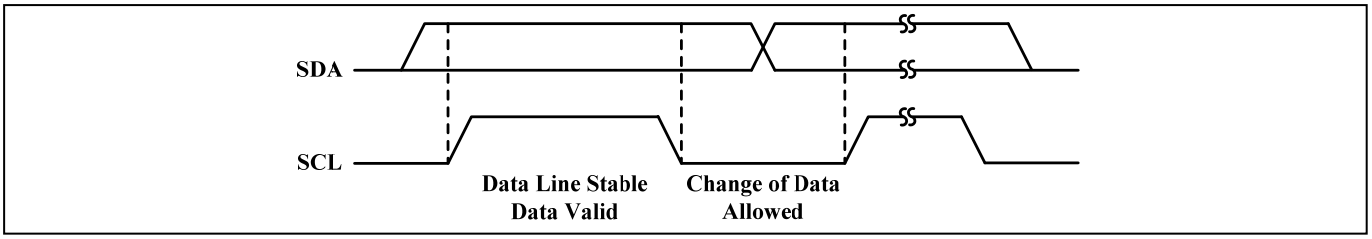


Figure 4 Bit Transfer

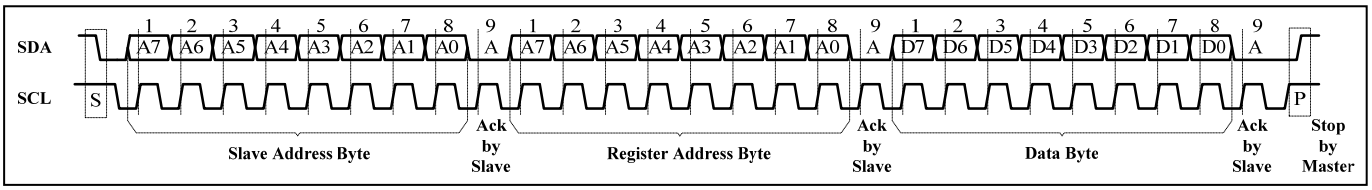


Figure 5 Writing to IS31FL3206 (Typical)

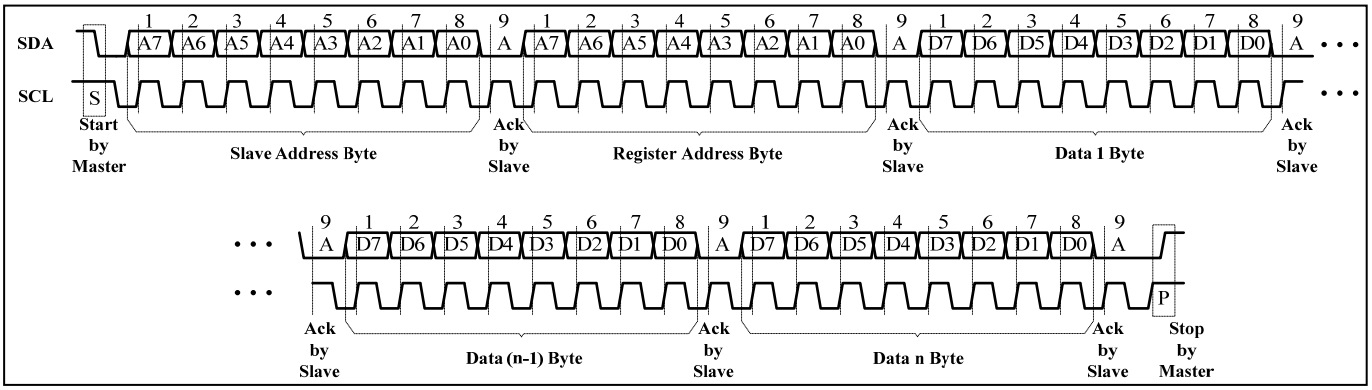


Figure 6 Writing to IS31FL3206 (Automatic Address Increment)

REGISTERS DEFINITIONS

Table 2 Register Function

Address	Name	Function	R/W	Table	Default
00h	Shutdown Register	Set software shutdown mode	W	3	0000 0000
04h~0Fh	PWM Register	12 channels PWM duty cycle data register	W	4	
13h	Update Register	Load PWM Register and LED Control Register's data	W	-	0000 0000
17h~22h	LED Control Register	Channel 1 to 12 enable bit and current setting	W	5	0000 0000
26h	Global Control Register	Set all channels enable	W	6	
27h	Output Frequency Setting Register	Set all channels operating frequency	W	7	
2Fh	Reset Register	Reset all registers into default value	W	-	0000 0000

Table 3 00h Shutdown Register

Bit	D7:D1	D0
Name	-	SSD
Default	0000 000	0

The Shutdown Register sets software shutdown mode of IS31FL3206.

SSD	Software Shutdown Enable
0	Software shutdown mode
1	Normal operation

Table 4 04h~0Fh PWM Register (OUT1~OUT12)

Bit	D7:D0
Name	PWM
Default	0000 0000

The PWM Registers adjusts LED luminous intensity in 256 steps.

The value of a channel's PWM Register decides the average output current for each output, OUT1~OUT12. The average output current may be computed using the Formula (1):

$$I_{OUT} = \frac{I_{MAX}}{256} \cdot \sum_{n=0}^{7} D[n] \cdot 2^n \qquad (1)$$

Where "n" indicates the bit location in the respective PWM register.

For example: D7:D0 = 10110101,

$$I_{OUT} = I_{MAX} (2^0+2^2+2^4+2^5+2^7)/256$$

The I_{OUT} of each channel is setting by the SL bit of LED Control Register (14h~1Fh). Please refer to the detail information in Page 11.

13h PWM Update Register

The data sent to the PWM Registers and the LED Control Registers will be stored in temporary registers. A write operation of "0000 0000" value to the Update Register is required to update the registers (04h~0Fh, 17h~22h).

Table 5 17h~22h LED Control Register (OUT1~OUT12)

Bit	D7:D6	D5:D0
Name	-	SL
Default	00	00 0000

The LED Control Registers store the on or off state of each LED and set the output current.

SL	HEX	Output Current (I_{OUT})
010000	0x10	$I_{OUT}=I_{MAX}$
010001	0x11	$I_{OUT}=11/12\ I_{MAX}$
010010	0x12	$I_{OUT}=9/12\ I_{MAX}$
010011	0x13	$I_{OUT}=7/12\ I_{MAX}$
00xxxx	0x0x	$I_{OUT}=0$
Others	Not allowed	

Table 6 26h Global Control Register

Bit	D7:D1	D0
Name	-	G_EN
Default	0000 000	0

The Global Control Register set all channels enable.

G_EN	Global LED Enable
0	Normal operation
1	Shutdown all LEDs

Table 7 27h Output Frequency Setting Register

Bit	D7:D1	D0
Name	-	OFS
Default	0000 000	0

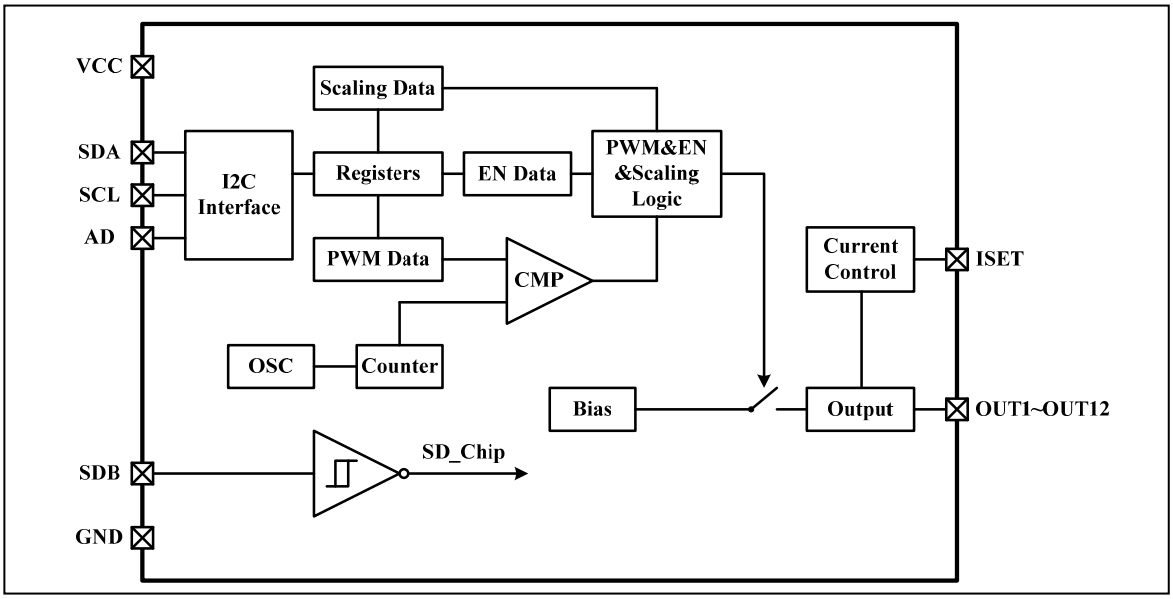
The Output Frequency Setting Register selects a fixed PWM operating frequency for all output channels.

OFS	Output Frequency Setting
0	24kHz
1	3.6kHz

2Fh Reset Register

Once user writes “0000 0000” data to the Reset Register, IS31FL3206 will reset all registers to default value. On initial power-up, the IS31FL3206 registers are reset to their default values for a blank display.

FUNCTIONAL BLOCK DIAGRAM



TYPICAL APPLICATION INFORMATION

PWM CONTROL

The PWM Registers (04h~0Fh) can modulate LED brightness of 12 channels with 256 steps. For example, if the data in PWM Register is “0000 0100”, then the PWM is the fourth step.

Writing new data continuously to the registers can modulate the brightness of the LEDs to achieve a breathing effect.

RISET

The maximum output current of OUT1~OUT12 can be adjusted by the external resistor, R_{ISET}, as described in Formula (2).

$$I_{MAX} = x \cdot \frac{V_{ISET}}{R_{ISET}} \qquad (2)$$

x = 58.5, V_{OUT} = 0.8V, V_{ISET} = 1.3V.

The recommended minimum value of R_{ISET} is 2kΩ.

CURRENT SETTING

The current of each LED can be set independently by the SL bit of LED Control Register (17h~22h). The maximum global current is set by the external register R_{ISET}.

When channels drive different quantity of LEDs, adjust maximum output current according to quantity of LEDs to ensure average current of each LED is the same.

For example, set R_{ISET}= 3.3kΩ then I_{MAX}= 23mA.

GAMMA CORRECTION

In order to perform a better visual LED breathing effect we recommend using a gamma corrected PWM value to set the LED intensity. This results in a reduced number of steps for the LED intensity setting, but causes the change in intensity to appear more linear to the human eye.

Gamma correction, also known as gamma compression or encoding, is used to encode linear luminance to match the non-linear characteristics of display. Since the IS31FL3206 can modulate the brightness of the LEDs with 256 steps, a gamma correction function can be applied when computing each subsequent LED intensity setting such that the changes in brightness matches the human eye's brightness curve.

Table 8 32 Gamma Steps With 256 PWM Steps

C(0)	C(1)	C(2)	C(3)	C(4)	C(5)	C(6)	C(7)
0	1	2	4	6	10	13	18
C(8)	C(9)	C(10)	C(11)	C(12)	C(13)	C(14)	C(15)
22	28	33	39	46	53	61	69
C(16)	C(17)	C(18)	C(19)	C(20)	C(21)	C(22)	C(23)
78	86	96	106	116	126	138	149
C(24)	C(25)	C(26)	C(27)	C(28)	C(29)	C(30)	C(31)
161	173	186	199	212	226	240	255

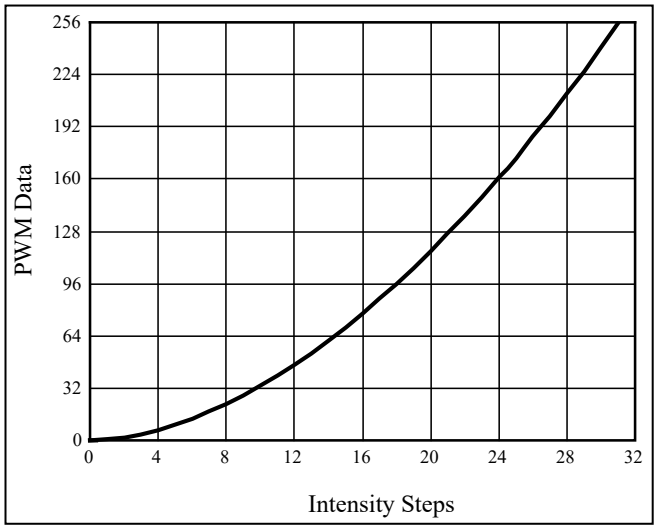


Figure 7 Gamma Correction (32 Steps)

Choosing more gamma steps provides for a more continuous looking breathing effect. This is useful for very long breathing cycles. The recommended configuration is defined by the breath cycle T. When T=1s, choose 32 gamma steps, when T=2s, choose 64 gamma steps. The user must decide the final number of gamma steps not only by the LED itself, but also based on the visual performance of the finished product.

Table 9 64 Gamma Steps With 256 PWM Steps

C(0)	C(1)	C(2)	C(3)	C(4)	C(5)	C(6)	C(7)
0	1	2	3	4	5	6	7
C(8)	C(9)	C(10)	C(11)	C(12)	C(13)	C(14)	C(15)
8	10	12	14	16	18	20	22
C(16)	C(17)	C(18)	C(19)	C(20)	C(21)	C(22)	C(23)
24	26	29	32	35	38	41	44
C(24)	C(25)	C(26)	C(27)	C(28)	C(29)	C(30)	C(31)
47	50	53	57	61	65	69	73
C(32)	C(33)	C(34)	C(35)	C(36)	C(37)	C(38)	C(39)
77	81	85	89	94	99	104	109
C(40)	C(41)	C(42)	C(43)	C(44)	C(45)	C(46)	C(47)
114	119	124	129	134	140	146	152
C(48)	C(49)	C(50)	C(51)	C(52)	C(53)	C(54)	C(55)
158	164	170	176	182	188	195	202
C(56)	C(57)	C(58)	C(59)	C(60)	C(61)	C(62)	C(63)
209	216	223	230	237	244	251	255

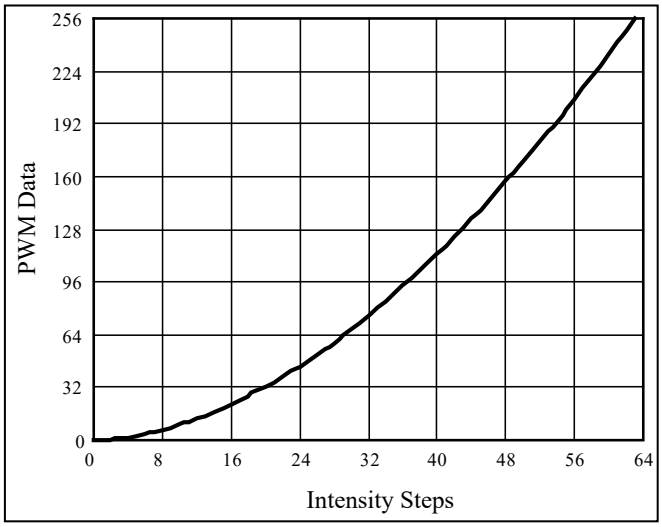


Figure 8 Gamma Correction (64 Steps)

Note, the data of 32 gamma steps is the standard value and the data of 64 gamma steps is the recommended value.

SHUTDOWN MODE

Shutdown mode can be used as a means of reducing power consumption. During shutdown mode all registers retain their data.

Software Shutdown

By setting SSD bit of the Shutdown Register (00h) to "0", the IS31FL3206 will operate in software shutdown mode. When the IS31FL3206 is in software shutdown mode, all current sources are switched off.

Hardware Shutdown

The chip enters hardware shutdown mode when the SDB pin is pulled low.

PWM FREQUENCY SELECT

The IS31FL3206 output channels operate with a default PWM frequency of 24kHz. Because all the OUTx channels are synchronized, the DC supply will experience large instantaneous current surges when the OUTx channels turn ON. These current surges will generate an AC ripple on the power supply which cause stress to the decoupling capacitors.

When the AC ripple is applied to a monolithic ceramic capacitor chip (MLCC) it will expand and contract causing the PCB to flex and generate audible hum in the range of between 20Hz to 20kHz, To avoid this hum, there are many countermeasures, such as selecting the capacitor type and value which will not cause the PCB to flex and contract.

An additional option for avoiding audible hum is to set the IS31FL3206's output PWM frequency above the audible range. The Output Frequency Setting Register 27h bit D0 can be used to set the switching frequency to 24kHz (Default), which is beyond the audible range. Figure 9 below shows the variation of output PWM frequency across supply voltage and temperature.

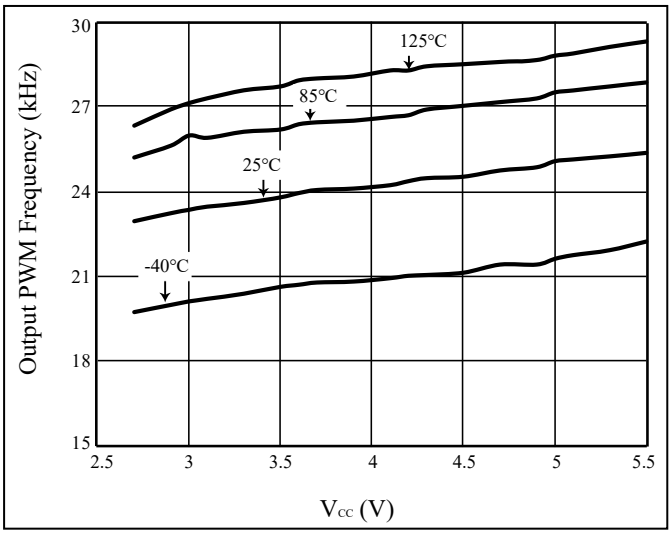


Figure 9 Output PWM Frequency vs. V_{CC}

CLASSIFICATION REFLOW PROFILES

Profile Feature	Pb-Free Assembly
Preheat & Soak Temperature min (Tsmin) Temperature max (Tsmax) Time (Tsmin to Tsmax) (ts)	150°C 200°C 60-120 seconds
Average ramp-up rate (Tsmax to Tp)	3°C/second max.
Liquidous temperature (TL) Time at liquidous (tL)	217°C 60-150 seconds
Peak package body temperature (Tp)*	Max 260°C
Time (tp)** within 5°C of the specified classification temperature (Tc)	Max 30 seconds
Average ramp-down rate (Tp to Tsmax)	6°C/second max.
Time 25°C to peak temperature	8 minutes max.

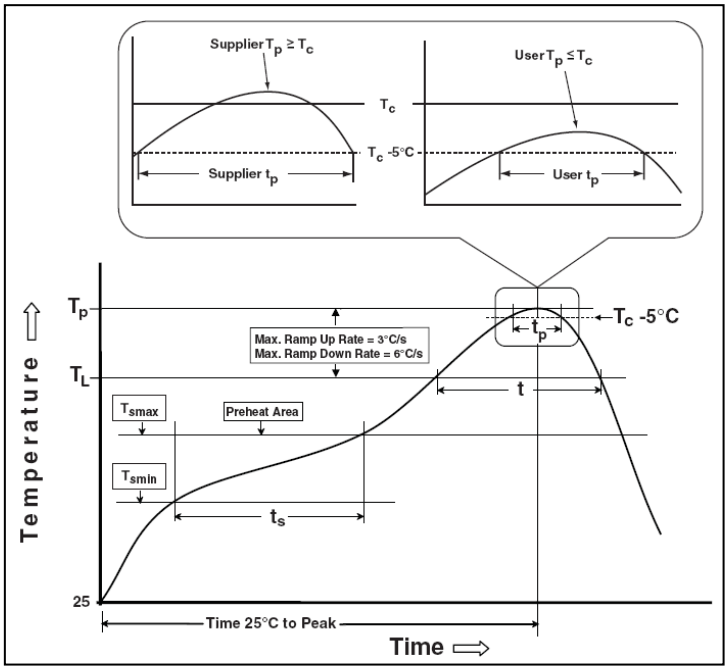
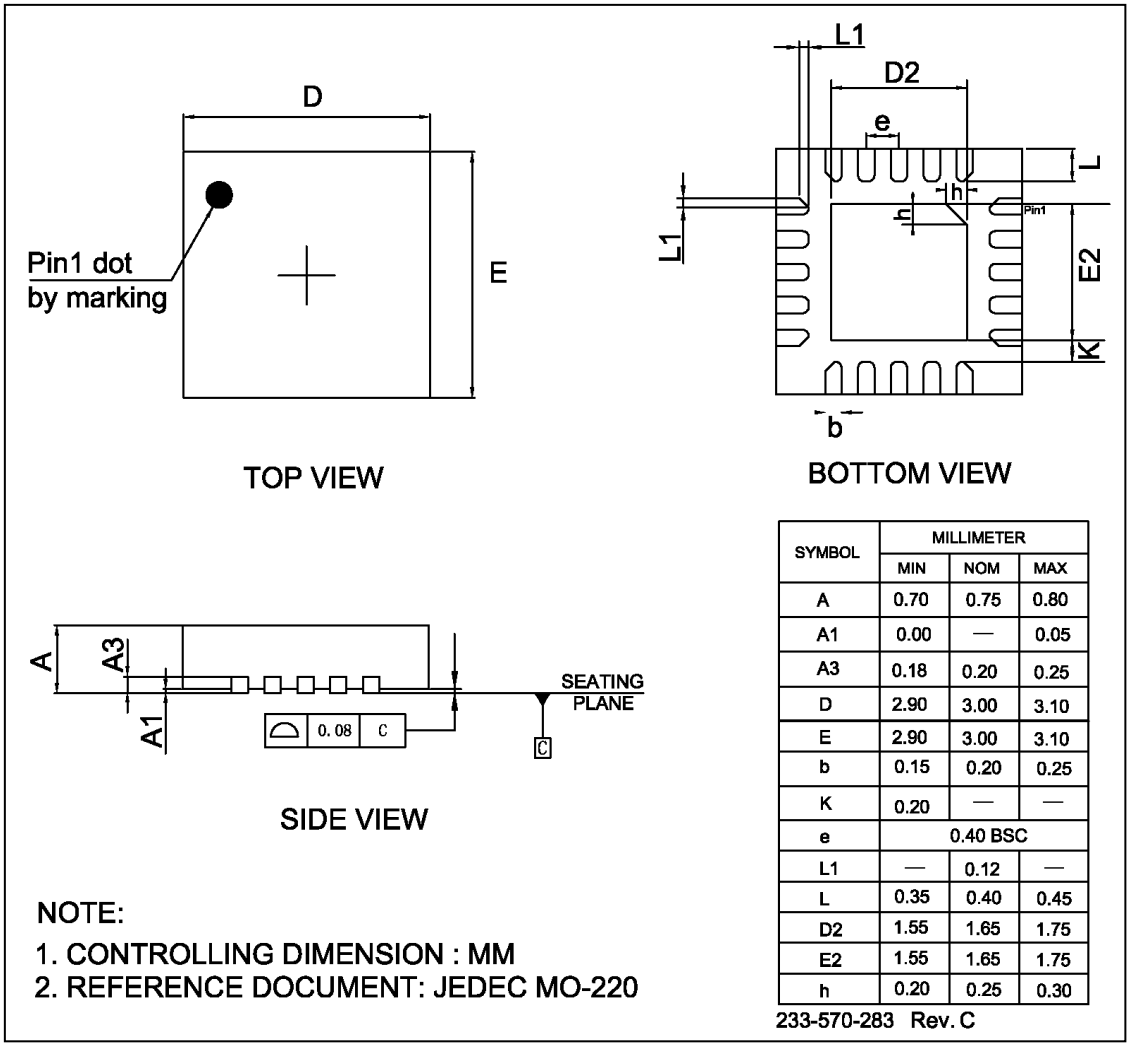


Figure 10 Classification Profile

PACKAGE INFORMATION

QFN-20



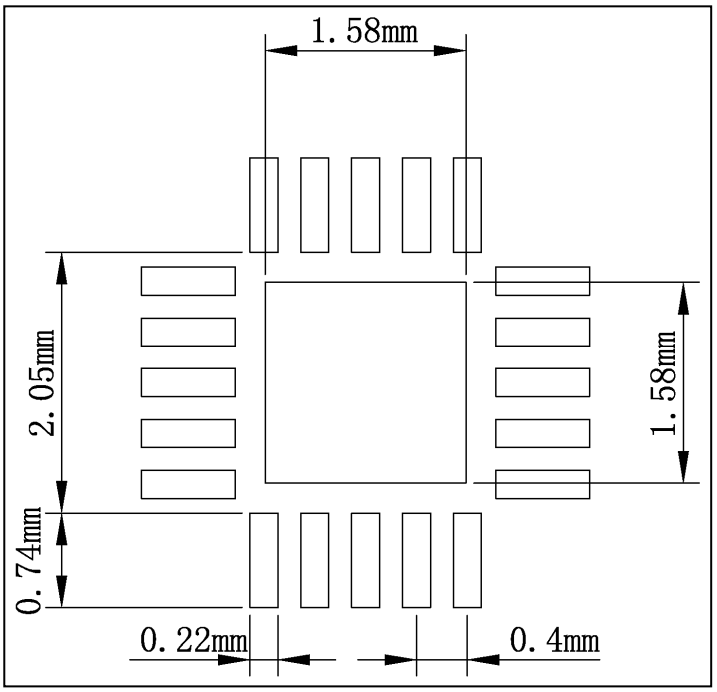
SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	0.70	0.75	0.80
A1	0.00	—	0.05
A3	0.18	0.20	0.25
D	2.90	3.00	3.10
E	2.90	3.00	3.10
b	0.15	0.20	0.25
K	0.20	—	—
e	0.40 BSC		
L1	—	0.12	—
L	0.35	0.40	0.45
D2	1.55	1.65	1.75
E2	1.55	1.65	1.75
h	0.20	0.25	0.30

NOTE:
1. CONTROLLING DIMENSION : MM
2. REFERENCE DOCUMENT: JEDEC MO-220

233-570-283 Rev. C

RECOMMENDED LAND PATTERN

QFN-20



Note:

1. Land pattern complies to IPC-7351.
2. All dimensions in MM.
3. This document (including dimensions, notes & specs) is a recommendation based on typical circuit board manufacturing parameters. Since land pattern design depends on many factors unknown (eg. User's board manufacturing specs), user must determine suitability for use.

REVISION HISTORY

Revision	Detail Information	Date
0A	Initial release.	2018.05.04
0B	Update ELECTRICAL CHARACTERISTICS table.	2018.05.16
A	Release to final. Update typical application circuit.	2019.03.08
B	Update registers' R/W information.	2019.08.26
C	1.Update to new Lumissil logo 2.Update POD and add RoHS	2024.06.04