24 CHANNEL LED DRIVER

January 2024

GENERAL DESCRIPTION

IS31FL3224 is an LED driver with 24 high voltage (16V) constant current channels. Each channel can be pulse width modulated (PWM) with 7-bit/8-bit precision for smooth LED brightness control. The maximum output current of each channel is designed to be 40mA, which can be adjusted by three 7-bit/8-bit global control registers group (one group for R for CS 3×n, one group for G for channels 3×n+1, and one group for B for channels 3×n+2, n=0~7, for example: one group for R is CS0, CS3, CS6 … CS21. one group for G is CS1, CS4, CS7 … CS22 and one group for B is CS2, CS5, CS8 … CS23). Proprietary algorithms are used in IS31FL3224 to minimize power bus noise caused by passive components on the power bus such as MLCC decoupling capacitor. All registers can be programmed via HSB (high speed series bus, up to 10MHz), DSB (Manchester encoded, daisy chained serial bus, up to 2MHz), SPI (12MHz) bus or I2C (1MHz) interface.

IS31FL3224 can be turned off with minimum current consumption by pulling the SDB pin low.

IS31FL3224 is available in QFN-40 (5mm×5mm) package and can work over temperature range from -40°C to +125°C.

FEATURES

- V_{CC}= 3.0V to 5.5V
- Support 24 constant current channels, tolerate up to 18V, nominal operation voltage up to 16V
- Constant-current output range: 40mA
- Current output range (open drain (OD) mode): 100mA× 24 channels
- Interface (MODE pins)
  - DSB (Daisy Chained Serial Bus, 2MHz)
  - HSB (High Speed Series Bus: 10MHz)
  - SPI (12MHz)
  - I2C (1MHz)
- For DSB and HSB
  - Built-in PWM generator: 7-bit/ch
  - 7-bit × 3 global current adjustment
- For SPI and IIC
  - Built-in PWM generator: 8-bit/ch
  - 8-bit × 3 global current adjustment
- Power noise reduction method
  - 4-groups delay to minimize the power ripple (See application information section for more detail)
  - Power Noise Reduction (PNR): Left, Right, Middle
- Spread spectrum
- Programmable detection of open/short, detected LED and store detected LED information in registers for ease of manufacturing/debugging
- Over temperature (thermal shutdown) protection
- Over current protection
- Under voltage protection
- Software shutdown mode
- Operating temperature: -40°C to 125°C
- QFN-40 (5mm×5mm) package
- RoHS & Halogen-Free Compliance
- TSCA Compliance

APPLICATIONS

- Pachinko
- White goods
- Gaming machine

TYPICAL APPLICATION CIRCUIT

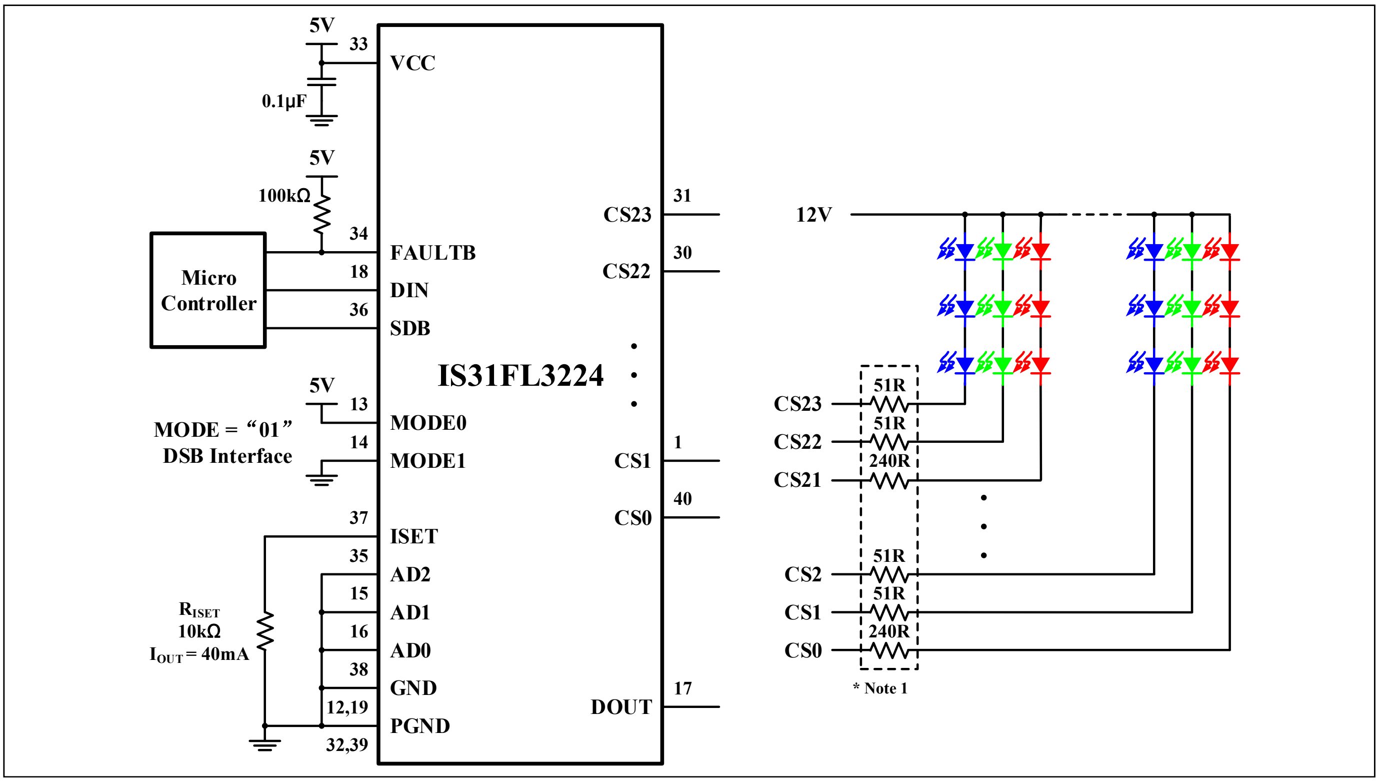


Figure 1 Typical Application Circuit (DSB Interface)

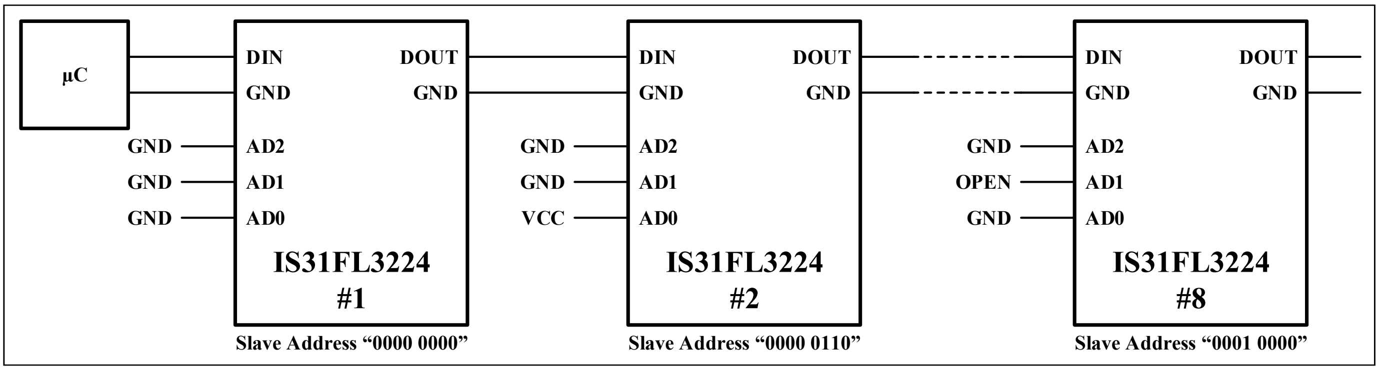


Figure 2 DSB Cascade Connection

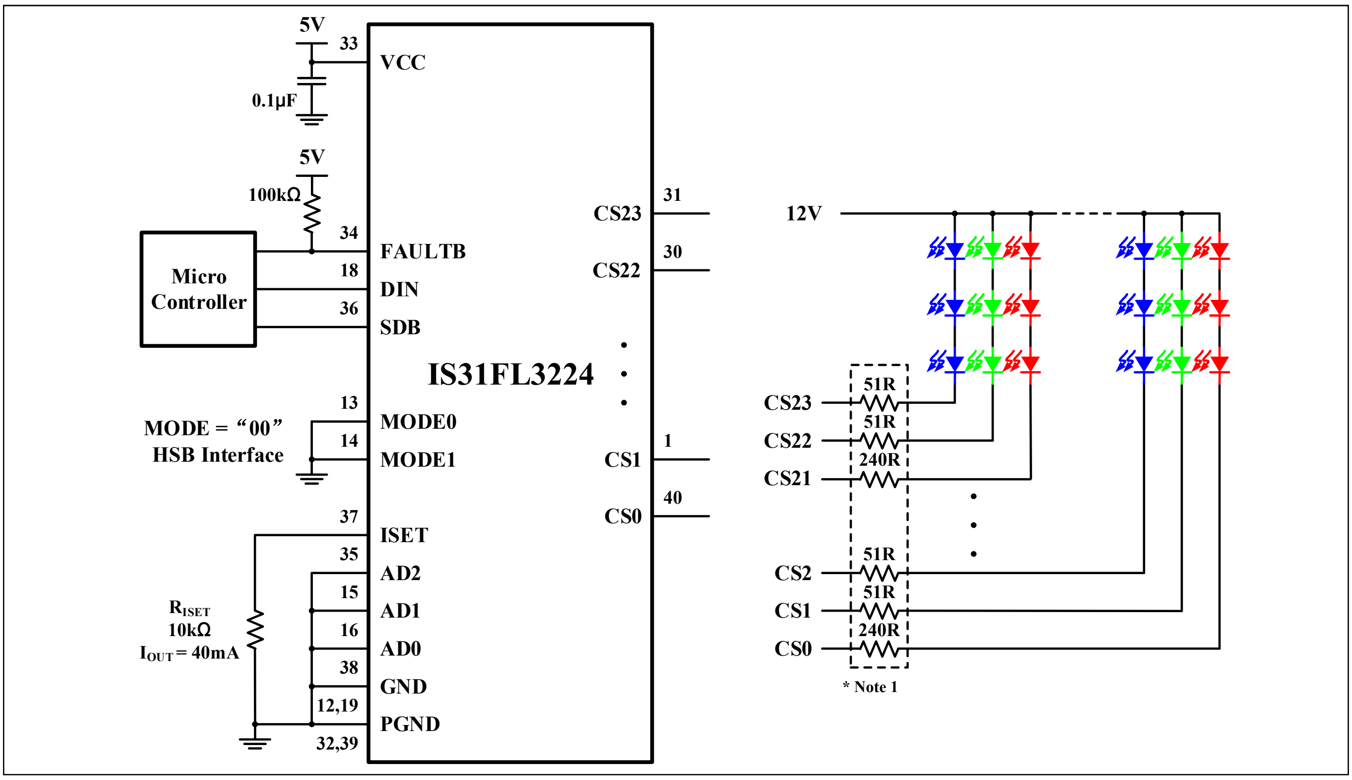


Figure 3 Typical Application Circuit (HSB Interface)

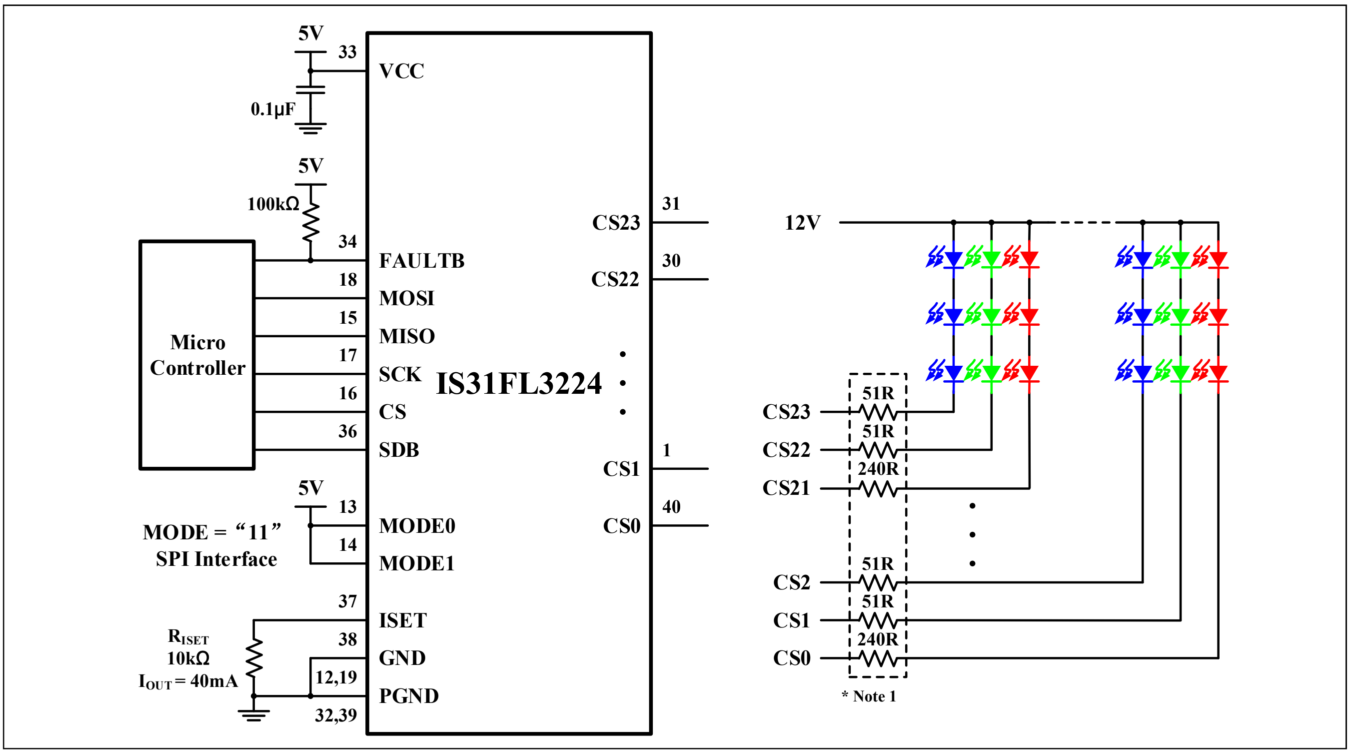


Figure 4 Typical Application Circuit (SPI Interface)

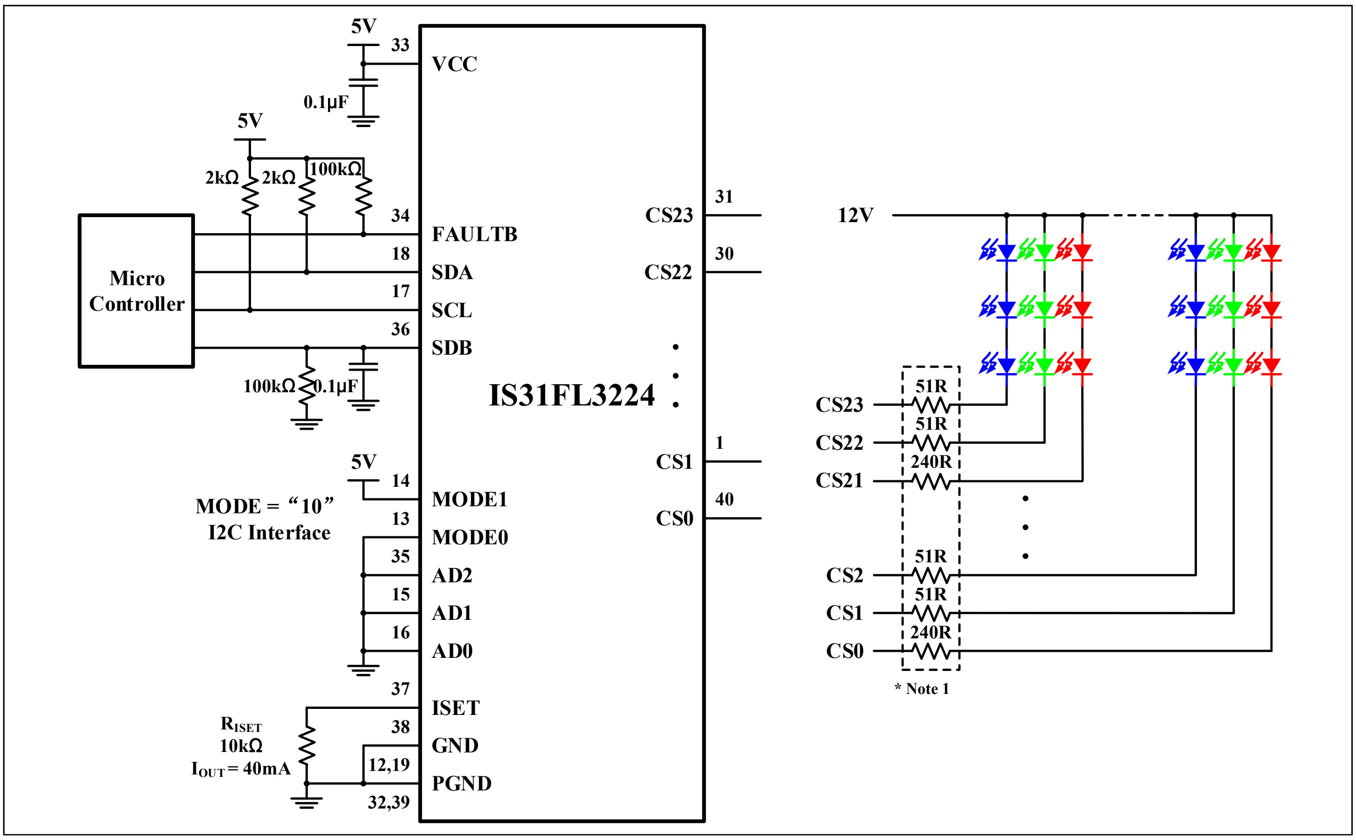
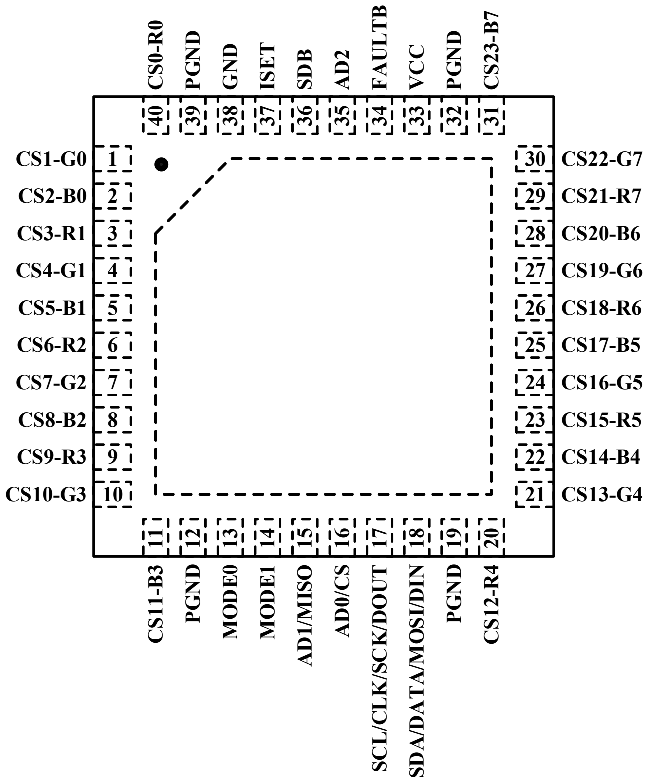


Figure 5 Typical Application Circuit (I2C Interface)

Note 1: These resistors in series with LED are for offloading the thermal dissipation ($P=I^2R$) away from the IS31FL3224 (resistor values are for PV_{CC}= 12V).

PIN CONFIGURATION

Package	Pin Configuration (Top View)
QFN-40	

PIN DESCRIPTION

No.	Pin	Description
1~11,20~31,40	CS[23:0]-Xx	X=R, G or B, x=0, 1, 2, current sink pin for LEDs.
12,19,32,39	PGND	Power GND.
38	GND	Analog GND.
34	FAULTB	Interrupt output pin. Register 9Eh can read the function of the FAULTB pin and active low when the interrupt event (FAULTB pull low) happens. Can be NC (float) if interrupt function is not used.
13,14	MODE [0:1]	Interface select pins.
37	ISET	Set the maximum IOUT current.
15	AD1/MISO	Address select pin/SPI output data.
16	AD0/CS	Address select pin/CS signal of SPI.
17	SCL/CLK/ SCK /DOUT	I2C clock/ HSB clock/ SPI clock /DSB Data out.
18	SDA/DATA/ MOSI/DIN	I2C input data /HSB input data / SPI input data/ DSB input data.
35	AD2	Address select pin.
36	SDB	Shutdown pin.
33	VCC	Analog and digital circuits.
	Thermal Pad	Connect to GND.

ORDERING INFORMATION
Industrial Range: -40°C to +125°C

Order Part No.	Package	QTY/Reel
IS31FL3224-QFLS4-TR	QFN-40, Lead-free	2500

ABSOLUTE MAXIMUM RATINGS

Supply voltage, V_{CC}	-0.3V ~ +6.0V
Voltage at CSx pin	-0.3V ~ +18V
Voltage at any input pin	-0.3V ~ VCC+0.3V
Maximum junction temperature, T_{JMAX}	+150°C
Storage temperature range, T_{STG}	-65°C ~+150°C
Operating temperature range, T_A=T_J	-40°C ~ +125°C
Package thermal resistance, junction to ambient (4-layer standard test PCB based on JESD 51-2A), $θ_{JA}$	32.2°C/W
ESD (HBM) ESD (CDM)	±3kV ±750V

Note 2: Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other condition beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

The following specifications apply for V_{CC}= 5V, T_A= 25°C, unless otherwise noted.

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
V_{CC}	Supply voltage		3.0		5.5	V
$I_{CC}(V_{CC})$	Quiescent power supply current	R_{ISET}=10.0kΩ, V_{SDB}=V_{CC}=5V, GCC=0x00		3.2	4.5	mA
I_{SD}	Shutdown current	V_{SDB}= 0V		2.4	3	μA
		V_{SDB}= V_{CC}, GCC= 0x00, SSD= 0		2.2	3	mA
I_{OUT}	Maximum constant current of CSx	R_{ISET}= 10kΩ, GCCR= GCCG= GCCB= 0xFE	36.5	40	43.5	mA
I_{OUT_MAX}	Maximum current of CSx	OD mode, PWM= 0xFF		100		mA
$ΔI_{MAT}$	Output current error between outputs (Note 3)	I_{OUT}= 40mA	-8		8	%
$ΔI_{ACC}$	Output current error between devices (Note 4)	I_{OUT}= 40mA	-8		8	%
V_{HR}	Current sink headroom voltage CSx	R_{ISET}= 10kΩ, I_{SINK}= 40mA		350	500	mV
I_{OZ}	CSx out leakage	V_CSx= 16V			0.2	μA
f_{PWM}	PWM frequency	PWMF= 32kHz	29.5	31.5	33.5	kHz

ELECTRICAL CHARACTERISTICS (CONTINUED)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
Logic Electrical Characteristics (SDB, DATA/DIN, CLK/DOUT, SEL, AD [2:0])						
V_{IL}	Logic "0" input voltage	V_{CC}= 3.0V~5.5V			0.25V_{CC}	V
V_{IH}	Logic "1" input voltage	V_{CC}= 3.0V~5.5V	0.5V_{CC}			V
V_{HYS}	Input Schmitt trigger hysteresis	V_{CC}= 3.6V		0.2		V
V_{AD}	Input for AD[2:0], AD= VCC	V_{CC}= 3.0V~5.5V	V_{CC}-0.3		V_{CC}	V
	Input for AD[2:0], AD= Open	V_{CC}= 3.0V~5.5V	GND+1.6		V_{CC}-0.6	V
	Input for AD[2:0], AD= ISET	V_{CC}= 3.0V~5.5V	ISET-0.3		ISET+0.3	V
	Input for AD[2:0], AD= GND	V_{CC}= 3.0V~5.5V	GND		GND+0.3	V
I_{IL}	Logic "0" input current	V_{INPUT}= L (Note 5)		5		nA
I_{IH}	Logic "1" input current	V_{INPUT}= H (Note 5)		5		nA

DIGITAL INPUT HSB SWITCHING CHARACTERISTICS (NOTE 5)

Symbol	Parameter	Min.	Typ.	Max.	Units
f_{C_HSB}	Clock frequency	-		10	MHz
t_{DVCH}	Data in set-up time	10		-	ns
t_{CHDX}	Data in hold time	10		-	ns
t_{CH}	Clock high time	50		-	ns
t_{CL}	Clock low time	50		-	ns

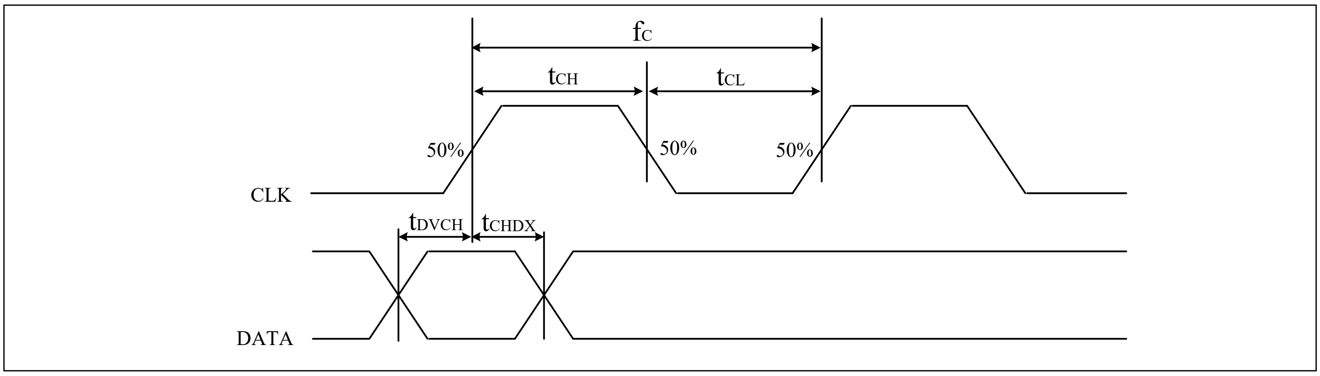


Figure 6 HSB Input Timing

DIGITAL INPUT DSB SWITCHING CHARACTERISTICS (NOTE 5)

Symbol	Parameter	Min.	Typ.	Max.	Units
t_{pLH}	DATAIN-DATAOUT propagation delay time C_L=15pF, t_r = t_f =15ns	-		20	ns
t_{pHL}	DATAIN-DATAOUT propagation delay time C_L=15pF, t_r = t_f =15ns	-		20	ns

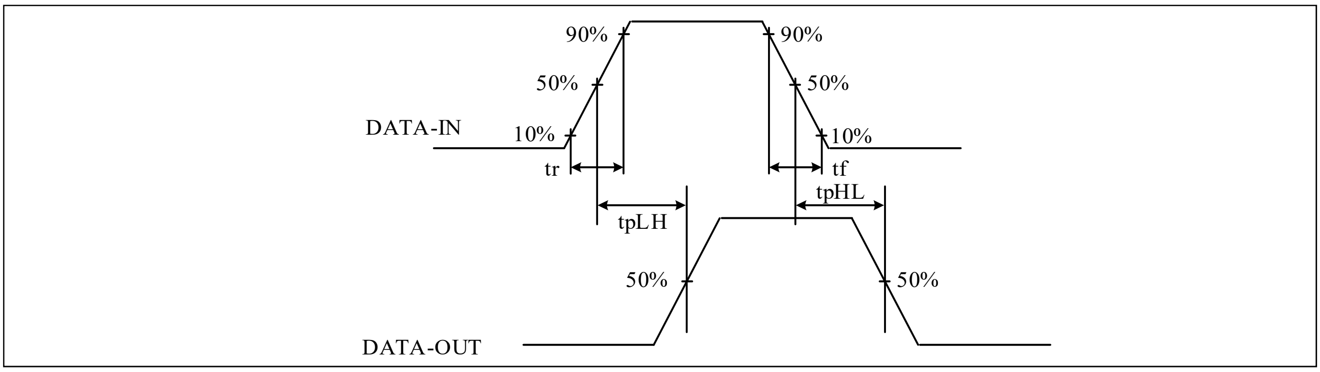


Figure 7 $t_{pH}L/t_{pLH}$ for DSB

DIGITAL INPUT SPI SWITCHING CHARACTERISTICS (NOTE 5)

Symbol	Parameter	Min.	Typ.	Max.	Units
f_{C_SPI}	Clock frequency	-		12	MHz
t_{SLCH}	CS active set-up time	34			ns
t_{SHCH}	CS not active set-up time	17			ns
t_{SHSL}	CS detect time	167			ns
t_{CHSH}	CS active hold time	34			ns
t_{CHSL}	CS not active hold time	17			ns
t_{CH}	Clock high time	34			ns
t_{CL}	Clock low time	34			ns
t_{CLCH}	Clock rise time			9	ns
t_{CHCL}	Clock fall time			9	ns
t_{DVCH}	Data in set-up time	7			ns
t_{CHDX}	Data in hold time	9			ns
t_{SHQZ}	Output disable time			34	ns
t_{CLQV}	Clock low to output valid			39	ns
t_{CLQX}	Output hold time	0			ns
t_{QLQH}	Output rise time			17	ns
t_{QLQH}	Output fall time			17	ns

DIGITAL INPUT I2C SWITCHING CHARACTERISTICS (NOTE 5)

Symbol	Parameter	Fast Mode			Fast Mode Plus			Units
		Min.	Typ.	Max.	Min.	Typ.	Max.	
f_{SCL}	Serial-clock frequency	-		400	-		1000	kHz
t_{BUF}	Bus free time between a STOP and a START condition	1.3		-	0.5		-	μs
$t_{HD, STA}$	Hold time (repeated) START condition	0.6		-	0.26		-	μs
$t_{SU, STA}$	Repeated START condition setup time	0.6		-	0.26		-	μs
$t_{SU, STO}$	STOP condition setup time	0.6		-	0.26		-	μs
$t_{HD, DAT}$	Data hold time	-		-	-		-	μs
$t_{SU, DAT}$	Data setup time	100		-	50		-	ns
t_{LOW}	SCL clock low period	1.3		-	0.5		-	μs
t_{HIGH}	SCL clock high period	0.7		-	0.26		-	μs
t_R	Rise time of both SDA and SCL signals, receiving	-		300	-		120	ns
t_F	Fall time of both SDA and SCL signals, receiving	-		300	-		120	ns

Note 3: I_{OUT} mismatch (bit to bit) $\triangle I_{MAT}$ is calculated:

$$\Delta I_{MAT} = \pm\left(\frac{I_{OUT(MAX)} - I_{OUT(MIN)}}{\left(\frac{I_{OUT0}+I_{OUT1}+\ldots+I_{OUT23}}{24}\times 2\right)}\right)\times 100\%$$

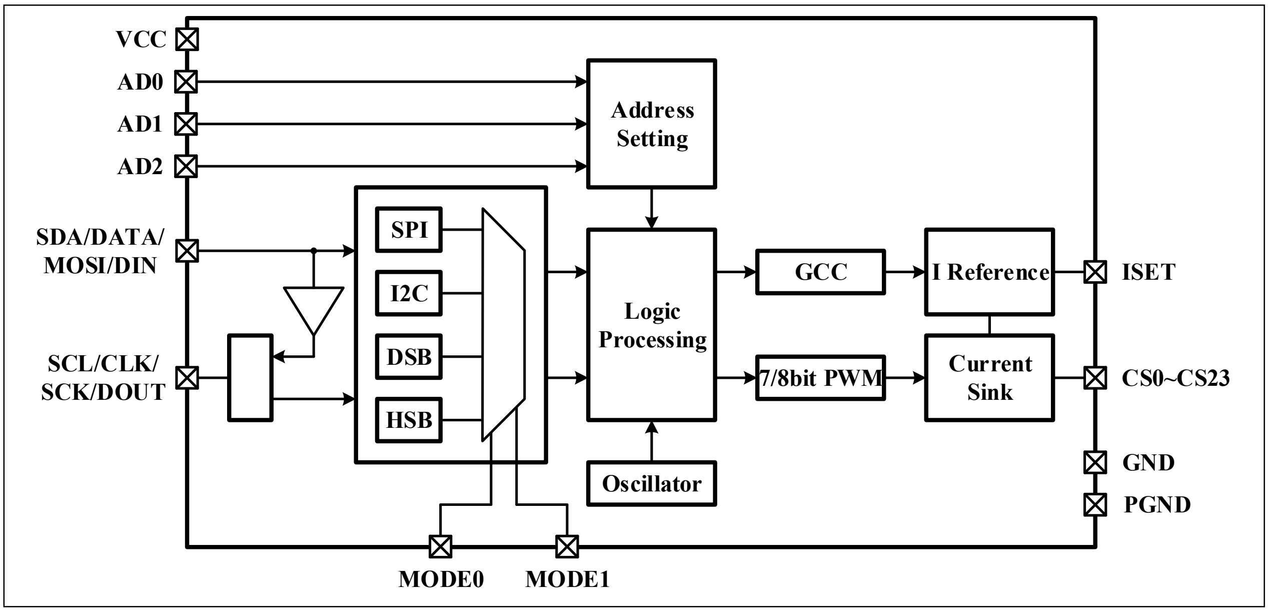
Note 4: I_{OUT} accuracy (device to device) $\triangle I_{ACC}$ is calculated:

$$\Delta I_{ACC} = \pm MAX\left(\frac{I_{OUT(MIN)} - I_{OUT(IDEAL)}}{I_{OUT(IDEAL)}}\right)\times 100\%$$

Where $I_{OUT(IDEAL)}$= 40mA when R_{ISET}= 10kΩ.

Note 5: Guaranteed by design.

FUNCTIONAL BLOCK DIAGRAM



DETAILED DESCRIPTION

IS31FL3224 has two MODE pins which can select the interface of IS31FL3224.

Table 1 Interface Setting

MODE [1:0]	Interface
00	HSB, high speed serial bus
01	DSB, daisy chain serial bus
10	I2C
11	SPI

HSB INTERFACE (HIGH SPEED SERIAL BUS)

When MODEx pins are connected as MODE[1:0]= “00”, the device will be programmed in HSB, high speed serial bus, the IS31FL3224 should be programmed using the following format:

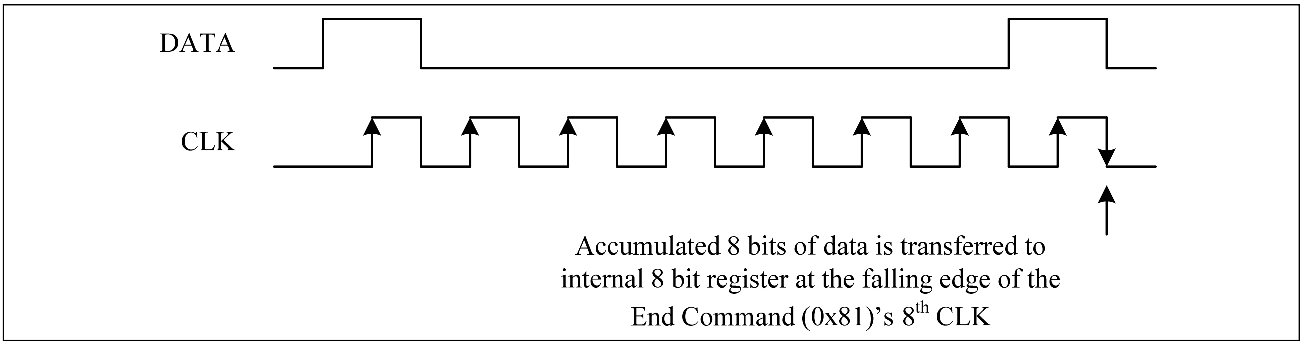


Figure 8 Data State To The Transition State

About data setting of the registers please refer to DATA SETTING MODE section.

DSB INTERFACE (DAISY CHAIN SERIAL BUS)

When MODEx pins are connected as MODE[1:0]= “01”, the device will be programmed in DSB, daisy chain serial bus.

The IS31FL3224 uses DIN signal. As compared with 2 wires data signal synchronous with the clock signal in conventional products, this product assigns each data state to the transition state (H to L or L to H) as shown below.

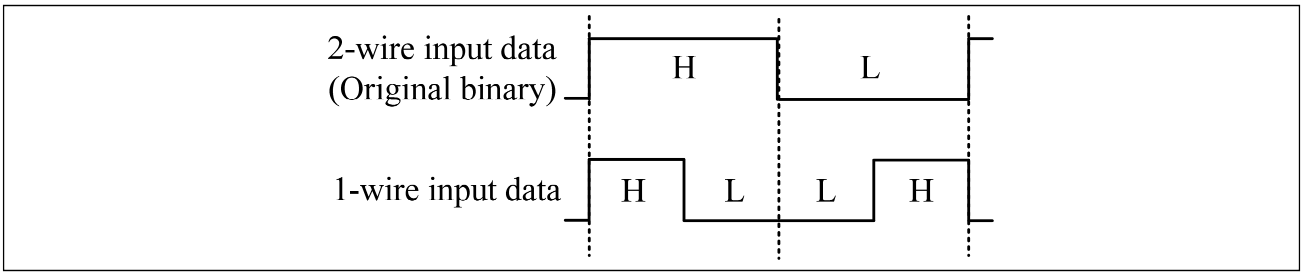


Figure 9 Data state to the transition state

About data setting of the registers please refer to DATA SETTING MODE section.

DATA SETTING MODE (For HSB AND DSB)

For setting data, select from (1) Normal Programming Mode, (2) Special Programming Mode, if all outputs are controlled, Special Programming Mode is recommended.

(1) Normal Programming Mode

Start Command [11111111]	**Slave Address 8 bits**	**Register Address 8 bits**	**Data byte 8 bits**	**End Command [10000001]**

Figure 10 Programming One Register

Start Command [11111111]	Slave Address 8 bits	Register Address1 8 bits	Data byte1 8 bits	Register Address2 8 bits	Data byte2 8 bits	•••	End Command [10000001]

Figure 11 Programming More Than One Register

Normal Programming Mode should be set as the following flow:

"Start Command (11111111)"->"Slave address(8 bits)" -> "Register(8 bits)" -> "Data byte(8 bits)" -> "End Command (10000001)" or

"Start Command (11111111)"->"Slave address(8 bits)" -> "Register 1 (8 bits)" -> "Data byte1 (8 bits)" -> "Register 2 (8 bits)" -> "Data byte2 (8 bits)" -> …-> "End Command (10000001)"

Input data from DATA signal is written to the shift register at the rising edge of CLK every 8 bit.

This data is transferred at the falling edge of the End Command (0x81)'s eighth CLK.

(2) Special Programming Mode

When data of 01100000 is input to the sub address, the operation moves to the special mode where all channels are selected in order. Data of 24 channels should be input.

(If data of more than 24 channels are provided, the 25th and subsequent data are treated as invalid. If data of less than 24 channels are provided, those data are written to the channels in order and the remaining channels retain the previous data.)

To return to the normal mode, input data from the start command (ALL "H" 8-bit). In case of using this mode configuration, volume of data can be omitted.

Start Command [11111111]	Slave Address	Register-address (Special mode set) [01100000]	Data CS0	Data CS1	•••	Data CS23	End Command [10000001]

Figure 12 Programming in Special Programming Mode

SLAVE ADDRESSES (For HSB and DSB)

Input voltages and logic states of the AD2, AD1 and AD0 pins are determined as follows.

(High order bit = 0. Low order bit = 0 (Except of all selection))

VCC= "11", ISET= "01", Open= "10", GND= "00"

Table 2 Slave Address (For HSB and DSB)

A7	A6:A5	A4:A3	A2:A1	A0	Remark
0	AD2	AD1	AD0	0	ADx=VCC, ISET, Open or GND, "00000000" ~ "01111110"
0	xx	xx	xx	1	All Select, Broadcast address.

Total support "00000000" ~ "01111110", 64 addresses

When A7:A0= "0xxx xxx1" all slave device are selected.

The All Select slave address allows every device. This special slave address is to facilitate a system broadcast mode.

SPI INTERFACE

When MODEx pins are connected as MODE[1:0]= "11", the device will be programmed SPI bus.

IS31FL3224 uses a SPI protocol to control the chip's function with four wires: CS, SCK, MOSI and MISO. SPI transfer starts form CS pin from high to low controlled by Master (Microcontroller), and IS31FL3224 latches data when clock rising.

The maximum SCK frequency supported in IS31FL3224 is 12MHz.

Table 3 SPI Command byte

A7	A6:A4	A4:A0	Remark
0	011	0000	Write address
1	011	0000	Read address

ADDRESS AUTO INCREMENT

To write multiple bytes of data bytes to the IS31FL3224, it is necessary to initiate the process by loading the specific address corresponding to the data register intended for the initial data byte. During the 8th rising edge of receiving the data byte, the internal address pointer will increment by one. The next data byte sent to IS31FL3224 will be placed in the new address, and so on. The auto increment of the address will continue as long as data continues to be written to IS31FL3224 (Figure 16).

READING OPERATION

The D7 of the Command Byte needs to be set to "1". If read one register, as shown in Figure 17, read the MISO data after sending the command byte and register address. If read more registers, as shown in Figure 18, the register address will auto increase during the 8th rising edge of receiving the last bit of the previous register data.

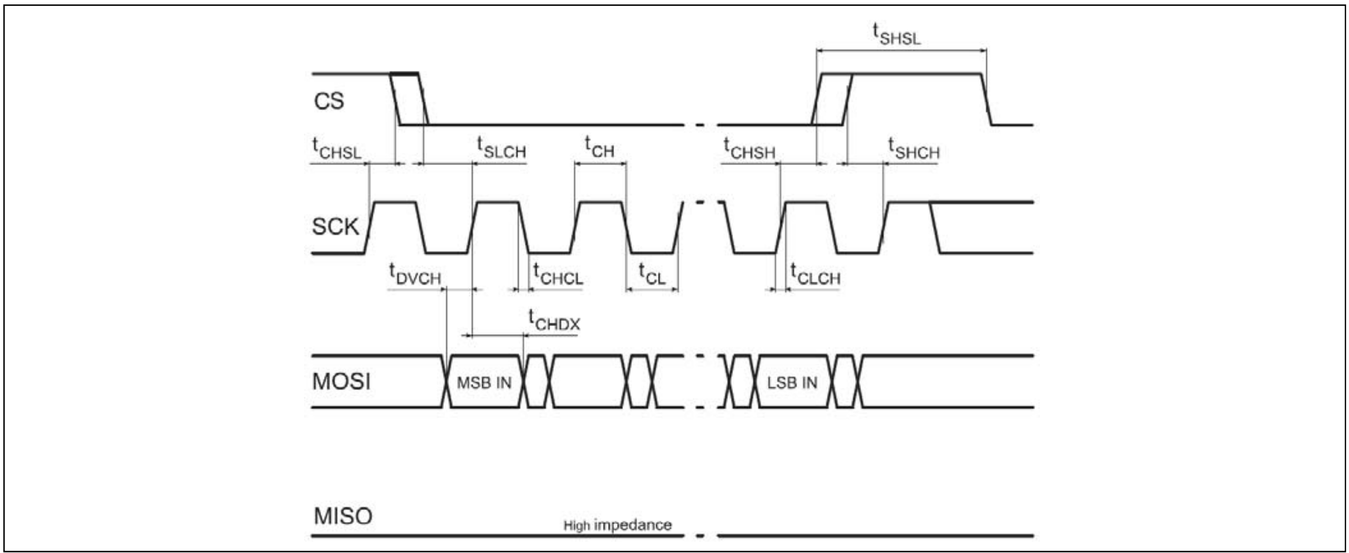


Figure 13 SPI Input Timing

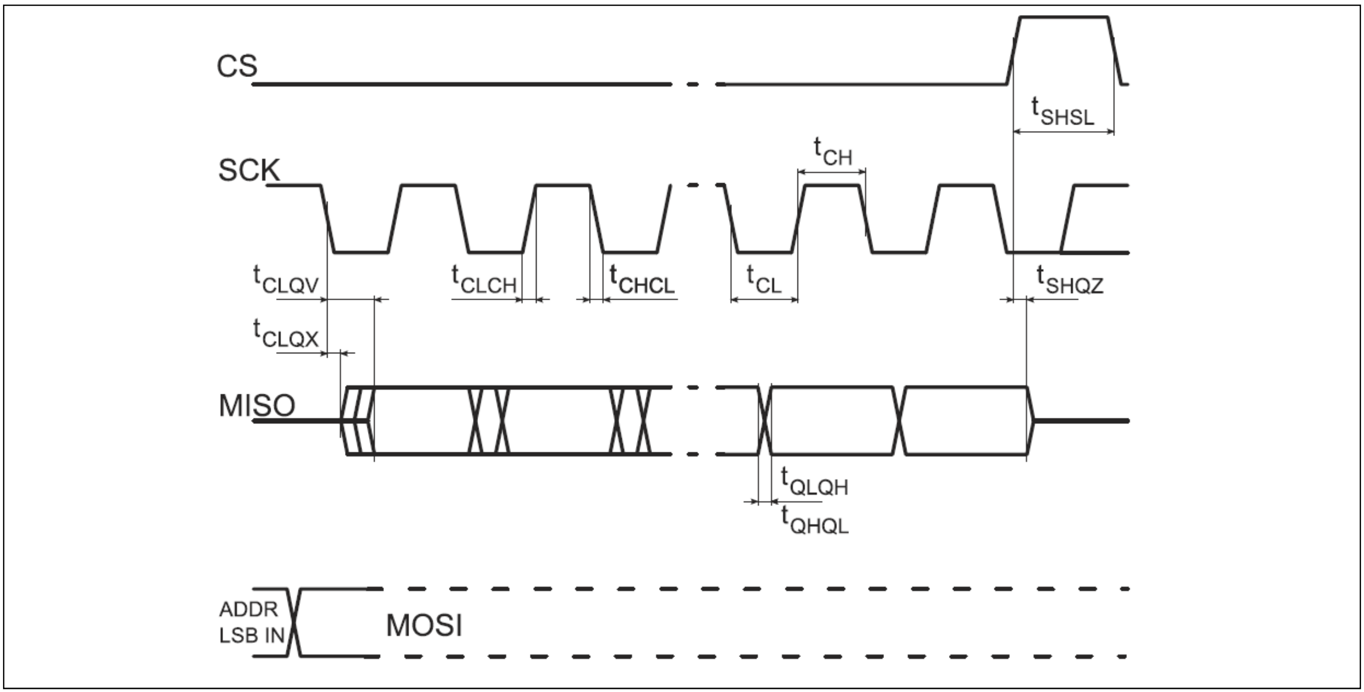


Figure 14 SPI Input Timing

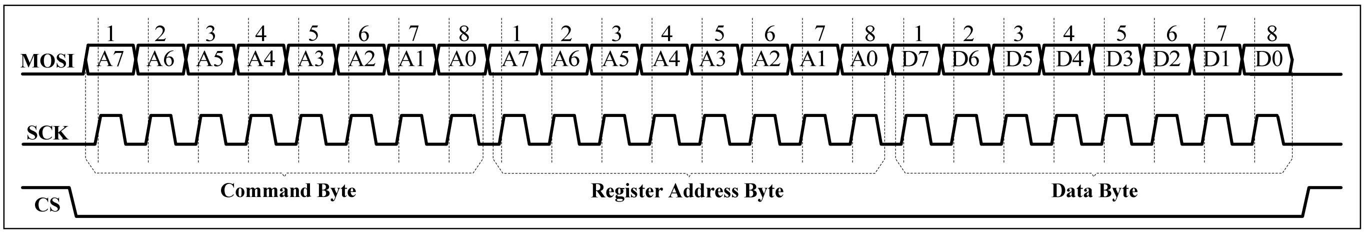


Figure 15 SPI writing to IS31FL3224 (Typical)

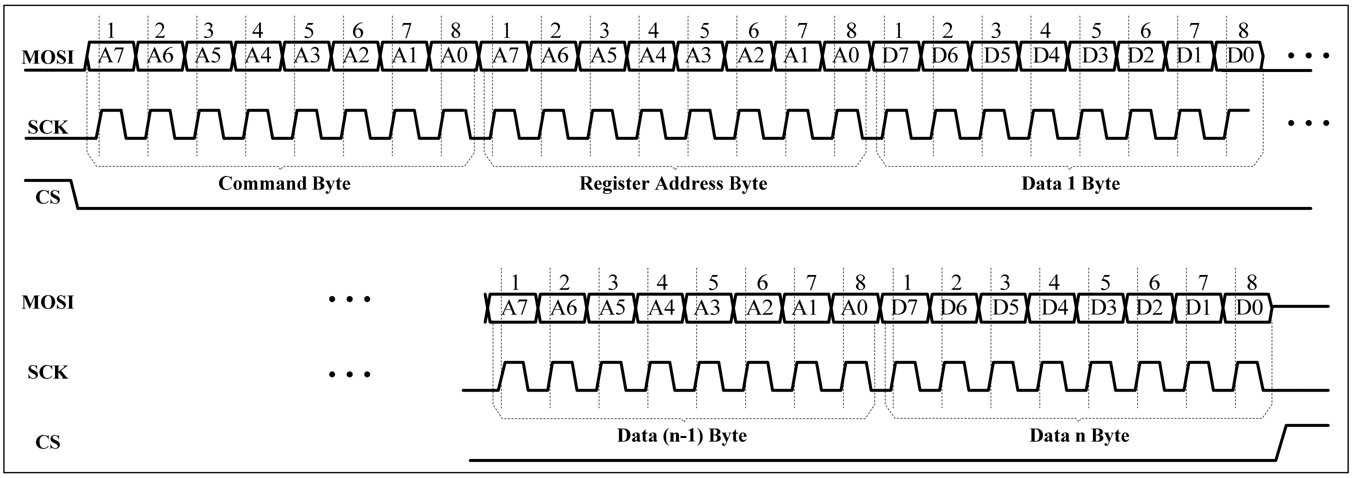


Figure 16 SPI Writing to IS31FL3224 (Automatic Address Increment)

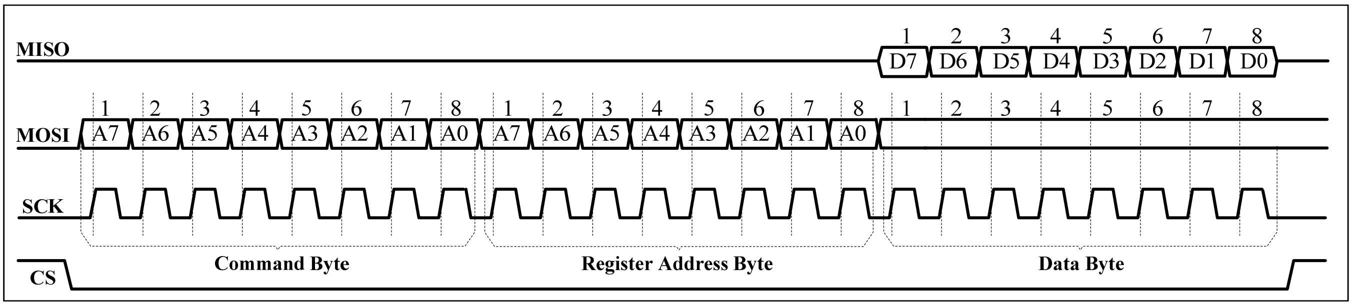


Figure 17 SPI Reading From IS31FL3224 (Typical)

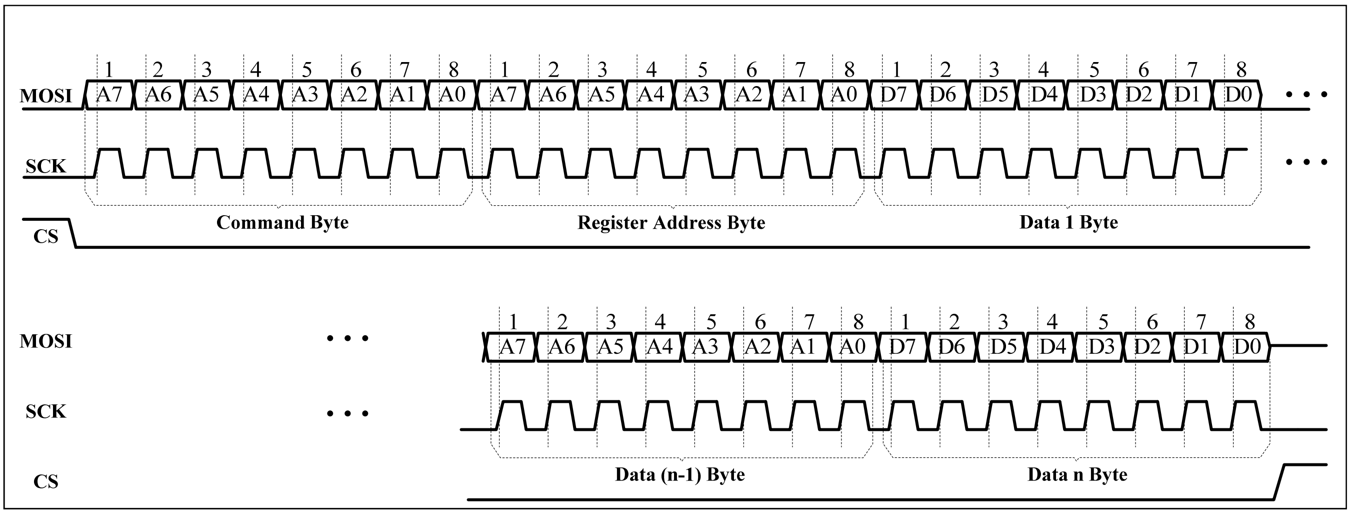


Figure 18 SPI Reading From IS31FL3224 (Automatic Address Increment)

I2C INTERFACE

When MODEx pins are connected as MODE[1:0]= "10", the device will be programmed I2C bus.

IS31FL3224 uses a serial bus, which conforms to the I2C protocol, to control the chip's functions with two wires: SCL and SDA. The IS31FL3224 has a 7-bit slave address (A7:A1), followed by the R/W bit, A0. Set A0 to "0" for a write command and set A0 to "1" for a read command. The value of bits from A6 to A1 is decided by the connection of the ADx pins.

Input voltages and logic states of the AD2, AD1 and AD0 pins are determined as follows.

Table 4 Slave Address

A7	A6:A5	A4:A3	A2:A1	A0	Remark
1	AD2	AD1	AD0	0	ADx=VCC, ISET, Open or GND, "10000000" ~ "11111100" AD[2:0] must not all connect to VCC
1	AD2	AD1	AD0	1	Read address
1	11	11	11	0	Broadcast address, all slaves will ack

ADx connected to VCC, ADx = 11;

ADx connected to ISET, ADx = 01;

ADx is open, ADx = 10;

ADx connected to GND, ADx = 00;

Total support "10000000"~"11111100", 63 addresses.

When A7:A0= "1111 1110" all slave devices are selected.

The SCL line is uni-directional. The SDA line is bi-directional (open-drain) with a pull-up resistor (typically 2kΩ). The maximum clock frequency specified by the I2C standard is 1MHz. In this discussion, the master is the microcontroller and the slave is the IS31FL3224.

The timing diagram for the I2C is shown in Figure 19. The SDA is latched in on the stable high level of the SCL. When there is no interface activity, the SDA line should be held high.

The "START" signal is generated by lowering the SDA signal while the SCL signal is high. The start signal will alert all devices attached to the I2C bus to check the incoming address against their own chip address.

The 8-bit chip address is sent next, most significant bit first. Each address bit must be stable while the SCL level is high.

After the last bit of the chip address is sent, the master checks for the IS31FL3224's acknowledge. The master releases the SDA line high (through a pull-up resistor). Then the master sends an SCL pulse. If the IS31FL3224 has received the address correctly, then it holds the SDA line low during the SCL pulse. If the SDA line is not low, then the master should send a "STOP" signal (discussed later) and abort the transfer.

Following acknowledge of IS31FL3224, the register address byte is sent, most significant bit first. IS31FL3224 must generate another acknowledge indicating that the register address has been received.

Then 8-bit of data byte are sent next, most significant bit first. Each data bit should be valid while the SCL level is stable high. After the data byte is sent, the IS31FL3224 must generate another acknowledge to indicate that the data was received.

The "STOP" signal ends the transfer. To signal "STOP", the SDA signal goes high while the SCL signal is high.

ADDRESS AUTO INCREMENT

To write multiple bytes of data bytes to the IS31FL3224, it is necessary to initiate the process by loading the specific address corresponding to the data register intended for the initial data byte. During the IS31FL3224 acknowledge of receiving the data byte, the internal address pointer will increment by one. The next data byte sent to IS31FL3224 will be placed in the new address, and so on. The auto increment of the address will continue as long as data continues to be written to IS31FL3224 (Figure 22).

READING OPERATION

Most of the registers can be read.

To read the register, after I2C start condition, the bus master must send the IS31FL3224 device address with the R/$\overline{W}$ bit set to "0", followed by the register address which determines which register is accessed. Then restart I2C, the bus master should send the IS31FL3224 device address with the R/$\overline{W}$ bit set to "1". Data from the register defined by the command byte is then sent from the IS31FL3224 to the master (Figure 23).

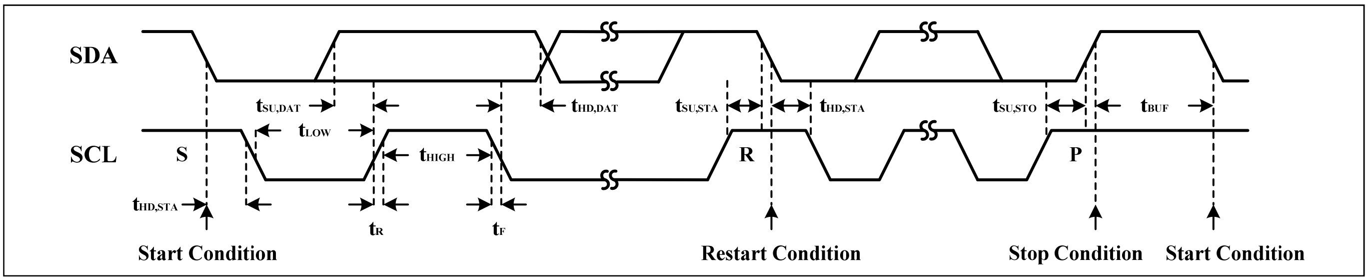


Figure 19 I2C Interface Timing

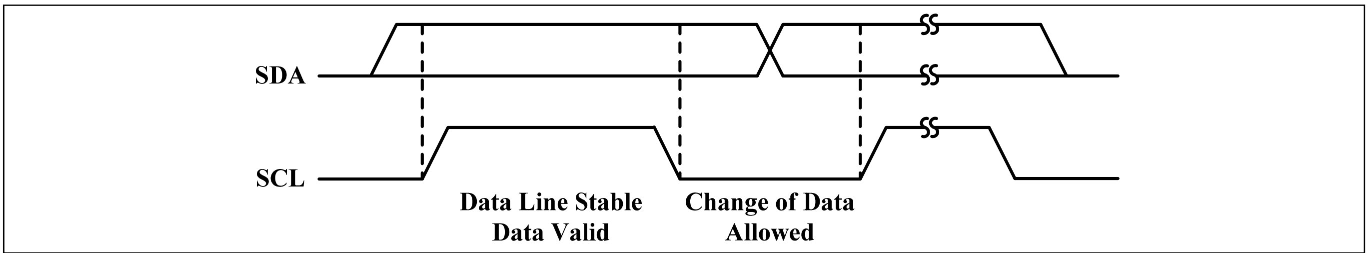


Figure 20 I2C Bit Transfer

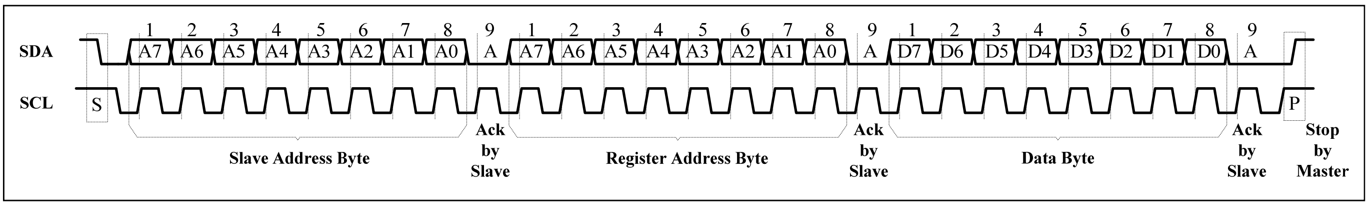


Figure 21 I2C Writing to IS31FL3224 (Typical)

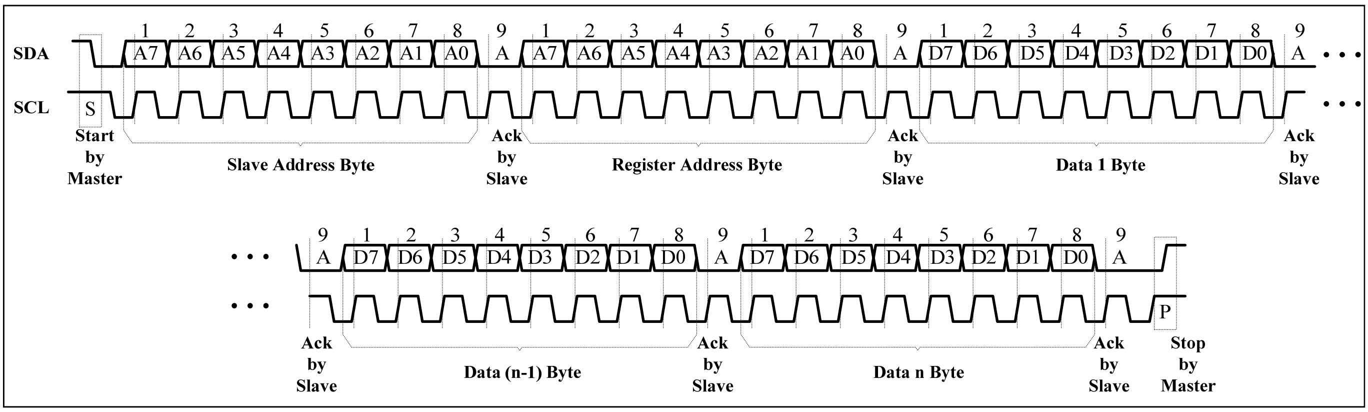


Figure 22 I2C Writing to IS31FL3224 (Automatic Address Increment)

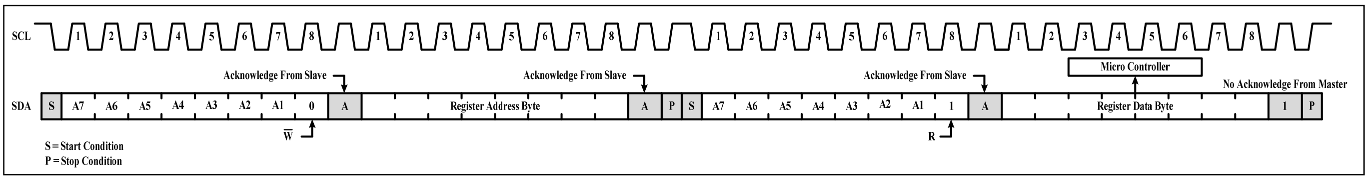


Figure 23 I2C Reading from IS31FL3224

REGISTER DEFINITIONS

Address	Name	Function	Table	R/W	Default
PWM Register					
02h~30h	PWM Register	Set PWM value for CS0-CS23	5	W/R	0000 0000
32h	PWM Update Register	Update PWM by SPI and I2C only		W	0000 0000
4Ah	All Channel Select	Set global channel		W	0000 0000
60h	Special Mode	Set Auto Address increase Write mode by HSB and DSB only		W	0000 0000
Function Register					
8Eh	Command Register Write Lock	To unlock function registers	-	W	0000 0000
90h	Configuration Register	Set operating mode	7	W/R	0000 0010
92h	Global Current Control Registers	Set global current for R channels	8	W/R	1111 1110
94h		Set global current for G channels		W/R	
96h		Set global current for B channels		W/R	
98h	Spread Spectrum Register	Set spread spectrum function	9	W/R	0000 0000
9Ah	Power Noise Reduction (PNR) Register	Power noise reduction setting	10	W/R	1001 0000
9Ch	Temperature Status and Open/Short Detect Register	Temperature thermal roll off and Open/Short Detect setting	11	W/R	0000 0000
9Eh	Fault State Register	For reading the fault state by SPI and I2C only	12	R	0000 0000
A0h~A4h	Open/Short Status Registers	Store the Open/Short information of LED by SPI and I2C only	13~15	R	0000 0000
B0h	OD mode Register	Select CS mode	-	W	0000 0000
B2h	OD mode Register Write Lock	To unlock B0h registers	-	W	0000 0000
BEh	Software Reset Register	Enable software reset function	-	W	0000 0000

Note 6: Follow the sequence to write PWM registers:

HSB/DSB mode: “Start Command”->“Slave address” -> 02=“0xXX” -> … -> “End Command”.

Follow the sequence to write function registers:

HSB/DSB mode: “Start Command”->“Slave address” -> 8Eh=“0xC6” ->90h= “0xXX” ->…-> “End Command”, 8Eh set to “0xC6” is to unlock the 90h.

When in SPI and I2C mode, the PWM data need to be updated with the writing 0x00 to 32h register.

Note 7: R is only for IIC and SPI.

Note 8: The read PWM register has the actual PWM value. If the write PWM register is not updated, the read value will not change.

Table 5 PWM Register

Data bytes set PWM value.

HEX	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Register	Remark
02h	0	0	0	0	0	0	1	0	/CS00	
04h	0	0	0	0	0	1	0	0	/CS01	
06h	0	0	0	0	0	1	1	0	/CS02	
…									…	
30h	0	0	1	1	0	0	0	0	/CS23	
40h	0	1	0	0	0	0	0	0	Global	Default Local
60h	0	1	1	0	0	0	0	0	Special	Default Normal

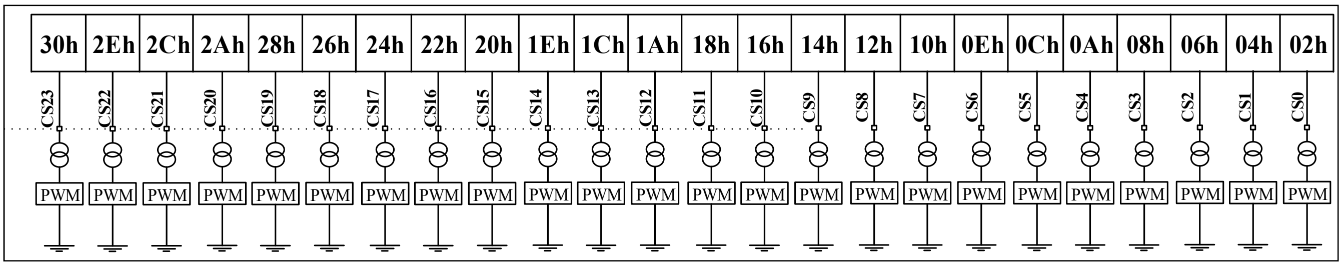


Figure 24 PWM Register

60h is for HSB and DSB interface only. Data bytes set PWM value. (Bit 0 must be "0" for HSB and DSB mode.)

Table 6 Data Bytes: PWM Value

Data bytes set PWM value. (Bit 0 must be zero for HSB and DSB mode)

HEX	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	PWM Dimming (for reference only)
00	0	0	0	0	0	0	0	0	0/128, OFF (Default)
02	0	0	0	0	0	0	1	0	1/128
04	0	0	0	0	0	1	0	0	2/128
… …									
FC	1	1	1	1	1	1	0	0	126/128
FE	1	1	1	1	1	1	1	0	127/128

Data bytes set PWM value. (For SPI and I2C mode, Bit 0 can be "1")

HEX	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	PWM Dimming (for reference only)
00	0	0	0	0	0	0	0	0	0/256, OFF (Default)
01	0	0	0	0	0	0	0	1	1/256
02	0	0	0	0	0	0	1	0	2/256
… …									
FE	1	1	1	1	1	1	1	0	254/256
FF	1	1	1	1	1	1	1	1	255/256

32h PWM Update Register

The data sent to the PWM Registers and the LED Control Registers will be stored in temporary registers. A write operation of "0000 0000" value to the Update Register is required to update the registers (02h~30h).

FUNCTION REGISTER

8Eh Function Unlock Register

Write Function Unlock Register with 0xC6 to unlock the Function Register (90h~9Ch).

Table 7 90h Configuration Register

Bit	D7	D6:D4	D3:D2	D1	D0
Name	TSD	PWMF	SDTV	SSD	-
Default	0	000	00	1	0

The Configuration Register sets operating mode of IS31FL3224. When SSD is "0", IS31FL3224 works in software shutdown mode. When SSD is set to "1", IS31FL3224 works in normal operate mode.

TSD	Thermal shutdown disable
0	Enable
1	Disable

PWMF	PWM Frequency
000	32kHz (default)
001	32kHz
010	16kHz
011	8kHz
100	4kHz
101	2kHz
110	1kHz
111	500Hz

SSD	Software Shutdown Control
0	Software shutdown
1	Normal operation

SDTV	Short detect threshold voltage
00	3.6V
01	7.4V
10	10.7V
11	12.8V

Table 8 92h/94h/96h Global Current Control Register

Bit	D7:D0
Name	GCCX
Default	1111 1110

The Global Current Control Registers modulate all CSx (x=0~23) GCCX current which is noted as IOUT in 128 or 256 steps.

92h is for R channels, GCCR, CS0, CS3, CS6 … CS21

92h is for G channels, GCCG, CS1, CS4, CS7 … CS22

94h is for B channels, GCCB, CS2, CS5, CS8 … CS23.

For HSB and DSB mode, I_{OUT} is computed by the Formula (1):

$$I_{OUT(PEAK)} = \frac{400}{R_{ISET}} \times \frac{GCC}{128} \qquad (1)$$

$$GCC = \sum_{n=1}^{7} D[n] \cdot 2^n$$

Where D[n] stands for the individual bit value, 1 or 0, in location n.

For SPI and I2C mode, I_{OUT} is computed by the Formula (2):

$$I_{OUT(PEAK)} = \frac{400}{R_{ISET}} \times \frac{GCC}{256} \qquad (2)$$

$$GCC = \sum_{n=0}^{7} D[n] \cdot 2^n$$

Where D[n] stands for the individual bit value, 1 or 0, in location n.

Table 9 98h Spread Spectrum Register

Bit	D7:D6	D5:D4	D3	D2:D1	D0
Name	RNG	CLT	SSP	GPC	-
Default	00	00	0	00	0

Spread Spectrum Register sets the spread spectrum (SSP) and synchronization function of IS31FL3224. The spread spectrum range is ±5%. When SSP enabled, the spread spectrum function will be enabled and the CLT bits will adjust the cycle time of spread spectrum function.

RNG	Spread spectrum range
00	±5%
01	±15%
10	±24%
11	±34%

CLT	Spread Spectrum Cycle Time
00	1980μs
01	1200μs
10	820μs
11	Not allowed

SSP	Spread Spectrum Function Enable
0	Disable
1	Enable

GPC	Global PWM Control
00	Function off (default)
01	Not allowed
10/11	All channel's PWM= 0x00 (10 : HSB & DSB: 0/128) (10/11: SPI & I2C: 0/256)

Table 10 9Ah Power Noise Reduction (PNR) Register

Bit	D7:D6	D5:D4	D3:D2	D1:D0
Name	PNR_B	PNR_G	PNR_R	-
Default	10	01	00	00

IS31FL3224 implements a proprietary PWM algorithm which spreads PWM rising and falling edges of each channel to minimize power line disturbance, hence, to minimize power rail noise. Traditionally, all channels start PWM cycle at the same time, creating a large LED current switching transient on the power bus. Using this Power Noise Reduction (PNR) method, some LED rising and falling edges can be cancelled, some are spread at different time point, minimizing simultaneously switching power transient noise. The timing and definition are shown in the following figure.

Between each adjacent channel with the same starting PWM cycles, an internal clock delay is inserted to further spread the edges.

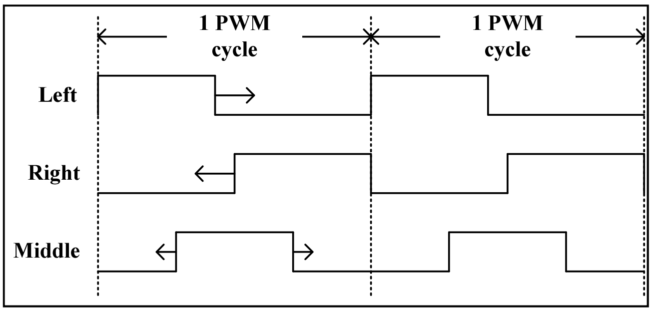


Figure 25 PWM Counting Position Definition

The PWM counting direction is programmable for each color group, for all R channel, G channel and B channel, defined by PNR[7:0]. Select different direction for R, G and B can minimize the power rail noise.

PNR_B	PNR for blue channels
00	Left
01	Right
10/11	Middle (default)

PNR_G	PNR for green channels
00	Left
01	Right (default)
10/11	Middle

PNR_R	PNR for red channels
00	Left (default)
01	Right
10/11	Middle

Table 11 9Ch Temperature Status and Open/Short Detect Register

Bit	D7:D6	D5:D4	D3	D2	D1:D0
Name	TS	TROF	OSDE	OSDS	-
Default	00	00	0	0	00

9Ch register sets the temperature status and also it enables/disables the open and short detect/select function. Please check note 9 and note 10 for more details.

TS	Temperature Point, Thermal Roll Off start point
00	140°C
01	120°C
10	100°C
11	90°C

TROF	Percentage Of Output Current
00	100%
01	75%
10	55%
11	30%

OSDE	Open Short Detect Enable
0	Disable
1	Enable

OSDS	Open Short Detect Select
0	Open detection
1	Short detection

Note 9: TS stores the temperature point of the IC. If the IC temperature reaches the temperature point the IC will trigger the thermal roll off and will decrease the current as TROF set percentage.

Note 10: The open and short circuit detection function will be affected by the Power Noise Reduction mode and PWM value. When the Power Noise Reduction is set to Left, the PWM value must be greater than 0x3F.When the Power Noise Reduction is set to Right, the PWM value must be greater than 0xC4.If the Power noise Reduction is set to Middle, the PWM value must be greater than 0x85 to ensure that the open and short as circuit detection function is normal.

Table 12 9Eh Fault State Register

Bit	D7:D6	D3	D2	D1	D0
Name	-	-	OFF	TSDF	-
Default	0000	0	0	0	0

Fault State Register stores thermal shutdown flag and LED open flag.

When OSDE/OSDS bits of 9Ch register are enabled, LED open or short will be detected, if the OFF bit is set to 1.

TSDF	Thermal Shutdown Flag
0	No thermal shutdown happens
1	Thermal shutdown happens

OFF	Open Fault Flag
0	No LED open happens
1	LED open happens

Table 13 A0h Open Short Status Register

Bit	D7:D0
Name	OS7: OS0
Default	0000 0000

Table 14 A2h Open Short Status Register

Bit	D7:D0
Name	OS15: OS8
Default	0000 0000

Table 15 A4h Open Short Status Register

Bit	D7:D0
Name	OS23: OS16
Default	0000 0000

The open/short status registers (A0h, A2h, A4h) store the open/short information of LED string. To get the correct open/short information, several configurations are recommended to set before setting the OSDE bit (D3 of 9Ch):

1 GCCx=0x10, too low or too high GCCx, like GCCx=0x02, may read out incorrect open/short information.

2 PWM=0xFE, too low PWM, like PWM=0x01, may read out incorrect open/short information.

3 The open and short circuit detection function will be affected by the Power Noise Reduction mode as well. When the Power Noise Reduction is set to Left, the PWM value must be greater than 0x3F. When the Power Noise Reduction is set to Right, the PWM value must be greater than 0xC4.If the Power noise Reduction is set to Middle, the PWM value must be greater than 0x85 to ensure that the open and short circuit detection function is normal.

B0h OD Mode Register

Write OD Mode Register with 0xAE to enable the OD Mode and CS to operate in open drain mode.

Write OD Mode Register with any values except 0xAE to the OD mode register to disable OD mode, and CS operates in constant current mode.

B2h OD Mode Unlock Register

Write OD Mode Unlock Register with 0xB6 to unlock the OD Mode Register (B0h)

BEh Software Reset Register

Write Software Reset Register with 0x00 will reset all the register to default value.

APPLICATION INFORMATION

PWM CONTROL

After setting the I_{OUT} and GCCX the brightness of each LEDs (LED average current (I_{LED})) can be modulated with 128 or 256 steps by PWM Register, as described in Formula below.

Where D[n] stands for the individual bit value, 1 or 0, in location n.

For HSB and DSB mode, I_{OUT} is computed by the Formula (1):

$$I_{OUT(PEAK)} = \frac{400}{R_{ISET}} \times \frac{GCC}{128} \quad (1)$$

$$GCC = \sum_{n=1}^{7} D[n] \cdot 2^n$$

Where D[n] stands for the individual bit value, 1 or 0, in location n.

For SPI and I2C mode, I_{OUT} is computed by the Formula (2):

$$I_{OUT(PEAK)} = \frac{400}{R_{ISET}} \times \frac{GCC}{256} \quad (2)$$

$$GCC = \sum_{n=0}^{7} D[n] \cdot 2^n$$

Where D[n] stands for the individual bit value, 1 or 0, in location n.

For HSB and DSB mode, the final average current of LED, I_{LED} is computed as Formula (4):

$$I_{LED} = \frac{PWM}{128} \times I_{OUT(PEAK)} \quad (4)$$

$$PWM = \sum_{n=1}^{7} D[n] \cdot 2^n$$

Where PWM is PWM Registers (02h~30h) data showing in Table 5.

For SPI and I2C mode, the final average current of LED, I_{LED} is computed as Formula (5).

$$I_{LED} = \frac{PWM}{256} \times I_{OUT(PEAK)} \quad (5)$$

$$PWM = \sum_{n=0}^{7} D[n] \cdot 2^n$$

Where PWM is PWM Registers (02h~30h) data showing in Table 5.

For example, for SPI and I2C mode, if R_{ISET}= 10kΩ, PWM= 255, and GCC= 255, then

$$I_{OUT(PEAK)} = \frac{400}{10k\Omega} \times \frac{255}{256} = 39.84mA$$

$$I_{LED} = I_{OUT(PEAK)} \times \frac{PWM}{256}$$

OPERATING MODE

IS31FL3224 can only operate in PWM Mode. The brightness of each LED can be modulated with 256 steps by PWM registers. For example, if the data in PWM Register is “0000 0100”, then the PWM is the fourth (SPI and I2C mode) or second step (HSB and DSB mode).

Writing new data continuously to the registers can modulate the brightness of the LEDs to achieve a breathing effect.

OPEN AND SHORT DETECT FUNCTION

IS31FL3224 has open and short detect bit for each LED.

The open/short status registers (A0h, A2h, A4h) store the open/short information of LED string. To get the correct open/short information, several configurations are recommended to set before setting the OSDE bit (D3 of 9Ch):

1. GCCX=0x10, too low or too high GCCX, like GCCX=0x01, may read out incorrect open/short information.
2. PWM=0xFE, too low PWM, like PWM=0x01, may read out incorrect open/short information.
3. The open and short circuit detection function will be affected by the Power Noise Reduction mode as well. When the Power Noise Reduction is set to Left, the PWM value must be greater than 0x3F. When the Power Noise Reduction is set to Right, the PWM value must be greater than 0xC4.If the Power noise Reduction is set to Middle, the PWM value must be greater than 0x85 to ensure that the short circuit detection function is normal.

4-GROUPS DELAY FUNCTION

The IS31FL3224 configuration entails the establishment of four distinct groups delay, each comprising six channels. Specifically, channels CS0 through CS5 are allocated to Group 1, channels CS6 through CS11 to Group 2, channels CS12 through CS17 to Group 3, and channels CS18 through CS24 to Group 4. To mitigate the power ripple that may arise from concurrently activating numerous channels, a deliberate delay of one clock cycle is instituted between these groups. PWM frequency (PWMF) is set at 500Hz, and temporal duration of this delay is set as 1/500/256, which approximates to 7.8 microseconds (7.8μs). This temporal segregation into groups, coupled with the calibrated delay, serves as an effective strategy to ameliorate power fluctuations associated with the concurrent activation of multiple channels within the IS31FL3224 configuration. This delay might seem extremely short, almost like a quick blink of an eye, but it serves an important purpose. It helps to spread power consumption over time, reducing the chances of sudden, large spikes in power usage. This, in turn, helps maintain a more stable and consistent power supply, which can be crucial in various applications where precise control of lighting or display elements is necessary.

INTERFACE RESET

The HSB/DSB/SPI/I2C will be reset if the SDB pin is pull-high from 0V to logic high, at the operating SDB rising edge, the interface operation is not allowed.

SHUTDOWN MODE

Shutdown mode can be used as a means of reducing power consumption. During shutdown mode all registers retain their data.

Software Shutdown

By setting SSD bit of the Configuration Register (90h) to "0", the IS31FL3224 will operate in software shutdown mode. When the IS31FL3224 is in software shutdown, all current sources are switched off, so that Put the LED out. All registers can be operated, Typical current consume is 2.14mA when VCC=5V.

Hardware Shutdown

The chip enters hardware shutdown when the SDB pin is pulled low. All analog circuits are disabled during hardware shutdown, typical the current consume is 2.4μA when V_{CC}=5V.

The chip releases hardware shutdown when the SDB pin is pulled high. During hardware shutdown state Function Register can be operated.

If V_{CC} has a risk drop below 1.75V but above 0.1V during SDB pulled low, please re-initialize all Function Registers before SDB pulled high.

LAYOUT

The IS31FL3224 consumes lots of power so good PCB layout will help improve the reliability of the chip. Please consider below factors when layout the PCB.

Power Supply Lines

When designing the PCB layout pattern, the first step should consider about the supply line and GND connection, especially those traces with high current, also the digital and analog blocks' supply line and GND should be separated to avoid the noise from digital block affect the analog block.

At least one 0.1μF capacitor, if possible with a 0.47μF or 1μF capacitor is recommended to connected to the ground at each power supply pins of the chip, and it needs to close to the chip and the ground net of the capacitor should be well connected to the GND plane.

R_{ISET}

R_{ISET} should be close to the chip and the ground side should well connect to the GND plane.

Thermal Consideration

The over temperature of the chip may result in deterioration of the properties of the chip. IS31FL3224 has a thermal pad but the chip could be very hot if the power is very large. So do consider the ground area connects to the GND pins and thermal pad. Other traces should keep away and ensure the ground area below the package is integrated, and the back layer should be connected to the thermal pad through 9 or 16 vias to be maximize area size of ground plane.

The package thermal resistance, θ_{JA}, determines the amount of heat that can pass from the silicon die to the surrounding ambient environment. The θ_{JA} is a measure of the temperature rise created by power dissipation and is usually measured in degree Celsius per watt (°C/W).

When operating the chip at high ambient temperatures, or when driving maximum load current, care must be taken to avoid exceeding the package power dissipation limits. The maximum power dissipation can be calculated using the following Formula (6):

$$P_{D(MAX)} = \frac{T_{J(MAX)} - T_A}{\theta_{JA}} \qquad (6)$$

So,

$$P_{D(MAX)} = \frac{125°C - 25°C}{32.2°C/W} \approx 3.11W$$

Figure 26 shows the power derating of the IS31FL3224 on a JEDEC boards (in accordance with JESD 51-5 and JESD 51-7) standing in still air.

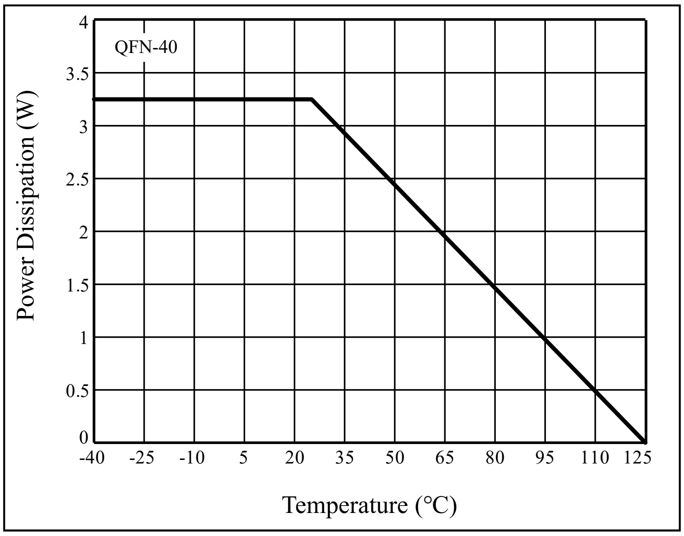


Figure 26 Dissipation Curve

Current Rating Example

For a R_{ISET}= 10kΩ application, the current rating for each net is as follows:

• VCC pins= 40mA×24= 960mA, recommend trace width: 0.3mm~0.5mm.

• CSx pins= 40mA, recommend trace width: 0.1016mm~0.254mm.

• All other pins < 15mA, recommend trace width: 0.1016mm~0.254mm.

CLASSIFICATION REFLOW PROFILES

Profile Feature	Pb-Free Assembly
Preheat & Soak Temperature min (Tsmin) Temperature max (Tsmax) Time (Tsmin to Tsmax) (ts)	150°C 200°C 60-120 seconds
Average ramp-up rate (Tsmax to Tp)	3°C/second max.
Liquidous temperature (TL) Time at liquidous (tL)	217°C 60-150 seconds
Peak package body temperature (Tp)*	Max 260°C
Time (tp)** within 5°C of the specified classification temperature (Tc)	Max 30 seconds
Average ramp-down rate (Tp to Tsmax)	6°C/second max.
Time 25°C to peak temperature	8 minutes max.

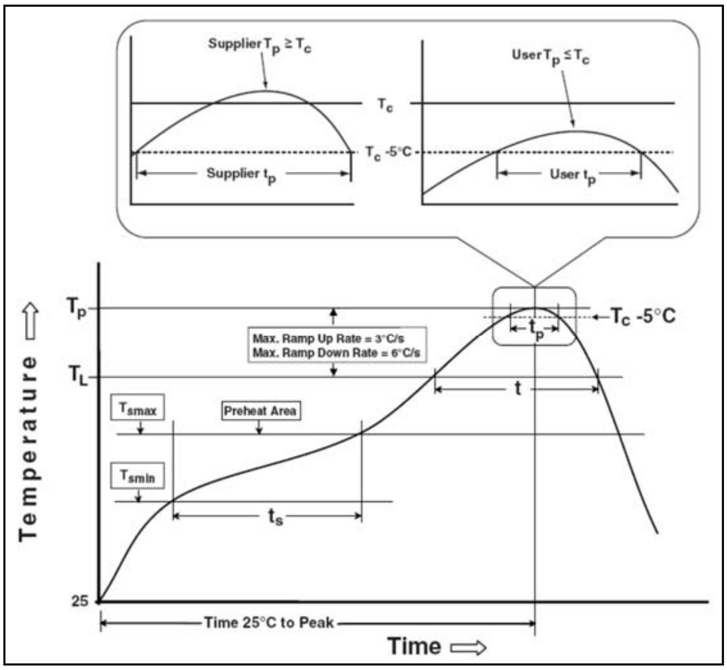
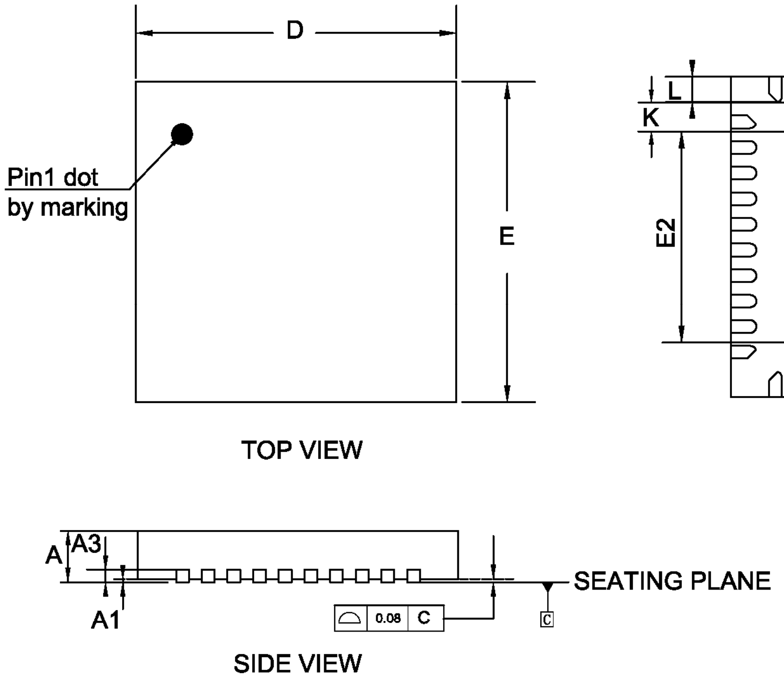


Figure 27 Classification profile

PACKAGE INFORMATION

QFN-40



SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	0.70	0.75	0.80
A1	0	0.02	0.05
A3	0.18	0.20	0.25
K	0.20	-	-
b	0.15	0.20	0.25
D	4.90	5.00	5.10
E	4.90	5.00	5.10
D2	3.15	-	3.80
E2	3.15	-	3.80
L	0.30	0.40	0.50
e	0.40BSC		

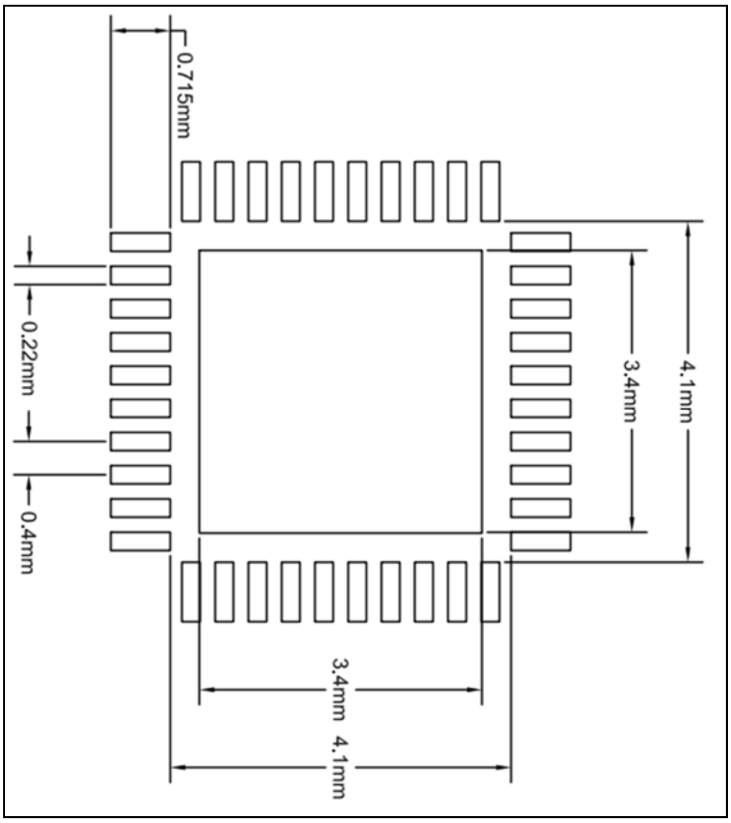
233-570-291 Rev.B

NOTE:

1. CONTROLLING DIMENSION : MM
2. REFERENCE DOCUMENT: JEDEC MO-220
3. THE PIN'S SHARP AND THERMAL PAD SHOWS DIFFERENT SHAPE AMONG DIFFERENT FACTORIES.

RECOMMENDED LAND PATTERN

QFN-40



Note:

1. Land pattern complies to IPC-7351.
2. All dimensions in MM.
3. This document (including dimensions, notes & specs) is a recommendation based on typical circuit board manufacturing parameters. Since land pattern design depends on many factors unknown (eg. User's board manufacturing specs), user must determine suitability for use.

REVISION HISTORY

Revision	Detail Information	Date
0A	Initial release	2023.09.06
0B	1.GENERAL DESCRIPTION section of SPI frequency changed to SPI (12MHz). 2.Modify EC table data and information. 3.Modify the description error in FEATURES.	2023.11.09
A	Modify EC table data and information. Release to mass production.	2023.12.22