IS31FL3294

4-LED LED DRIVER

June 2024

GENERAL DESCRIPTION

The IS31FL3294 is a 4 LED current sink LED driver programmed via 1MHz I2C compatible interface. Each LED can be dimmed individually with 4096 steps PWM data and each current sink has 8-bit DC scaling (Color Calibration) data which allowing 4096 steps of linear PWM dimming and 256 steps of DC current adjustable level.

The IS31FL3294 operates from 2.7V to 5.5V and features a very low shutdown and operational current.

The IS31FL3294 can operate in either "Current Level & PWM mode" or "Pattern" mode. In Current Level & PWM mode, the output current of each output is independently programmed and controlled in 4096 steps to achieve color mixing and the PWM duty cycle of each output is also independently programmed and controlled in 4096 steps to simplify color mixing or for smoothly diming control. In Pattern mode, the timing characteristics for RGB channels output can be individually adjusted to maintain a pre-established pattern sequence without requiring any additional MCU interaction, thus saving valuable system resources.

IS31FL3294 is available in UTQFN-12 (2mm×2mm) package. It operates from 2.7V to 5.5V over the temperature range of -40°C to +125°C.

FEATURES

- Supply voltage range: 2.7V to 5.5V
- 4 current sinks, I_{OUT}= 40mA (Max.)
- Ultra-low operational current (200μA Typ. at V_{CC}=3.6V)
  - Power-saving mode: 1μA (Typ.) with SDB high and all LEDs off
- Accurate color rendition
  - 12-bit/8+4-bit PWM/channel
  - 8-bit correction/channel
  - 6-bit global current adjust
- SDB rising edge reset I2C module
- 1MHz I2C-compatible interface
- Auto breath function
  1) 3 patterns auto breath
  2) Fade IN/ Fade OUT time up to 8s.
  3) Single Pulse/Multi pulse/Manual control modes for auto breath.
  4) 3 color pre-configure registers for color breath
- UTQFN-12 (2mm×2mm) package
- RoHS & Halogen-Free Compliance
- TSCA Compliance

APPLICATIONS

- Hand-held devices for LED display
- Gaming device (Mouse, Mouse MAT etc.)
- IOT device (AI speaker etc.)

TYPICAL APPLICATION CIRCUIT

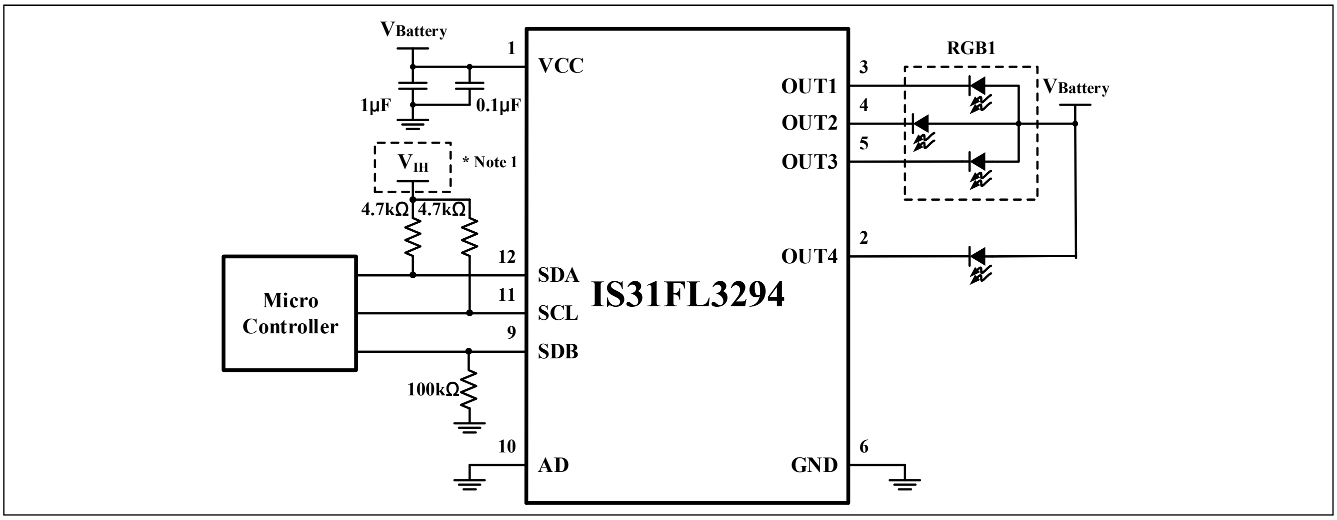
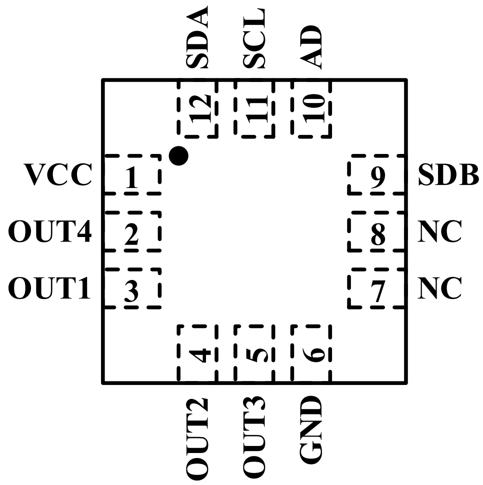


Figure 1 Typical Application Circuit

Note 1: V_{DD} is the high level voltage for IS31FL3294, which is usually same as VCC of Micro Controller, e.g. if V_{CC} of Micro Controller is 3.3V, V_{IH}= 3.3V. If V_{CC}= 5V and V_{IH} is lower than 2.8V, recommend to add level shift circuit.

PIN CONFIGURATION

Package	Pin Configuration (Top View)
UTQFN-12	

PIN DESCRIPTION

No.	Pin	Description
1	VCC	Power supply.
3, 4, 5, 2	OUT1~OUT4	Current source outputs.
6	GND	Ground.
7, 8	NC	No connect
9	SDB	Shutdown the chip when pulled to low.
10	AD	I2C address setting.
11	SCL	I2C serial clock.
12	SDA	I2C serial data.
	Thermal Pad	Connect to GND.

ORDERING INFORMATION
Industrial Range: -40°C to +125°C

Order Part No.	Package	QTY/Reel
IS31FL3294-UTLS4-TR	UTQFN-12, Lead-free	3000

ABSOLUTE MAXIMUM RATINGS

Supply voltage, V_{CC}	-0.3V ~+6.0V
Voltage at any input pin	-0.3V ~ V_{CC}+0.3V
Maximum junction temperature, T_{JMAX}	+150°C
Storage temperature range, T_{STG}	-65°C ~+150°C
Operating temperature range, T_A=T_J	-40°C ~ +125°C
Package thermal resistance, junction to ambient (4-layer standard test PCB based on JESD 51-2A), $θ_{JA}$	126.1°C/W
ESD (HBM) ESD (CDM)	±2kV ±750V

Note 2: Stresses beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other condition beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

The following specifications apply for V_{CC}= 5V, T_A= 25°C, unless otherwise noted.

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
V_{CC}	Supply voltage		2.7		5.5	V
I_{CC}	Quiescent power supply current	V_{CC}=3.6V, V_{SDB}=$V_{CC,}$ aLL channels PWM=0x00, 12-bit mode, PFS= 220Hz		0.2	0.24	mA
		V_{CC}=5V, V_{SDB}=$V_{CC,}$ aLL channels PWM=0x00, 12-bit mode, PFS= 220Hz		0.26	0.29	
		V_{CC}=3.6V, V_{SDB}=$V_{CC,}$ aLL channels PWM=0x00, 8+4-bit mode, PFS= 23kHz		0.4	0.47	
		V_{CC}=5V, V_{SDB}=$V_{CC,}$ aLL channels PWM=0x00, 8+4-bit mode, PFS= 23kHz		0.55	0.6	
I_{SD}	Shutdown current	V_{CC}=5V, V_{SDB}=0V		0.4	2	μA
		V_{CC}=3.6V, V_{SDB}=0V		0.3	1	
		V_{SDB}= V_{CC}=5V, Configuration Register written “0000 0000		0.4	2	
		V_{SDB}= V_{CC}=3.6V, Configuration Register written “0000 0000		0.3	1	
I_{OUT}	Constant current of channel	GCC=0x3F, CL=0xFF, IMAX=0	27.5	30	32.5	mA
		GCC=0x3F, CL=0xFF, IMAX=1		40		
f_{OUT}	PWM frequency of output	OSC= 1.8MHz, PFS=00, PWM Resolution= 12-bit	200	220	240	Hz
		OSC= 1.8MHz, PFS=01, PWM Resolution= 12-bit	400	440	480	Hz
		OSC= 6MHz, PFS=10, PWM Resolution= 8+4-bit	21	23	25.3	kHz
$ΔI_{MAT}$	Between channels	I_{OUT}=30mA (Note 3)	-6.5		6.5	%
$ΔI_{ACC}$	Between device to device	I_{OUT}=30mA (Note 4)	-6.5		6.5	%
$ΔI_{MAT}$	Between channels	I_{OUT}=3mA (LCAI=1) (Note 3)	-7		7	%
$ΔI_{ACC}$	Between device to device	I_{OUT}=3mA (LCAI=1) (Note 4)	-7		7	%
V_{HR}	Current sink headroom voltage	I_{OUT} =30mA		250	330	mV

ELECTRICAL CHARACTERISTICS (CONTINUE)

The following specifications apply for V_{CC}= 5V, T_A= 25°C, unless otherwise noted.

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
T_{SD}	Thermal shutdown	(Note 5)		165		°C
T_{SD_HY}	Thermal shutdown hysteresis	(Note 5)		18		°C
Logic Electrical Characteristics (SDA, SCL, SDB, AD)						
V_{IL}	Logic “0” input voltage	V_{CC}= 2.7V~5.5V	GND		0.4	V
V_{IH}	Logic “1” input voltage	V_{CC}= 2.7V~5.5V	1.4		V_{CC}	V
I_{IL}	Logic “0” input current	V_{INPUT}= 0V (Note 5)		5		nA
I_{IH}	Logic “1” input current	V_{INPUT}= V_{CC} (Note 5)		5		nA

DIGITAL INPUT I2C SWITCHING CHARACTERISTICS (NOTE 5)

Symbol	Parameter	Fast Mode			Fast Mode Plus			Units
		Min.	Typ.	Max.	Min.	Typ.	Max.	
f_{SCL}	Serial-clock frequency	-		400	-		1000	kHz
t_{BUF}	Bus free time between a STOP and a START condition	1.3		-	0.5		-	μs
$t_{HD, STA}$	Hold time (repeated) START condition	0.6		-	0.26		-	μs
$t_{SU, STA}$	Repeated START condition setup time	0.6		-	0.26		-	μs
$t_{SU, STO}$	STOP condition setup time	0.6		-	0.26		-	μs
$t_{HD, DAT}$	Data hold time	-		-	-		-	μs
$t_{SU, DAT}$	Data setup time	100		-	50		-	ns
t_{LOW}	SCL clock low period	1.3		-	0.5		-	μs
t_{HIGH}	SCL clock high period	0.7		-	0.26		-	μs
t_R	Rise time of both SDA and SCL signals, receiving (Note 6)	-		300	-		120	ns
t_F	Fall time of both SDA and SCL signals, receiving (Note 6)	-		300	-		120	ns

Note 3: I_{OUT} mismatch (bit to bit) $\triangle I_{MAT}$ is calculated:

$$\Delta I_{MAT} = \left(\frac{I_{OUTn}(n = 1 \sim 4)}{\left(\frac{I_{OUT1}+I_{OUT2}+I_{OUT3}+I_{OUT4}}{4}\right)} - 1 \right) \times 100\%\Delta$$

Note 4: I_{OUT} accuracy (device to device) $\triangle I_{ACC}$ is calculated:

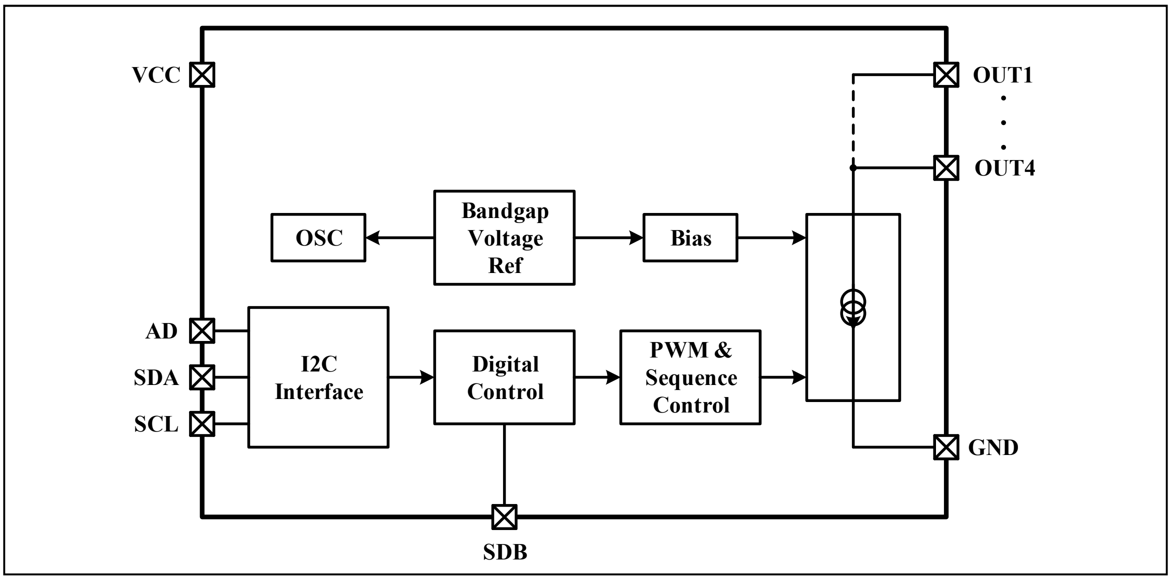
$$\Delta I_{ACC} = \left(\frac{\left(\frac{I_{OUT1}+I_{OUT2}+I_{OUT3}+I_{OUT4}}{4} - I_{OUT(IDEAL)}\right)}{I_{OUT(IDEAL)}} \right) \times 100\%$$

Where $I_{OUT(IDEAL)}$= 30mA or 3mA.

Note 5: Guaranteed by design.

Note 6: C_b = total capacitance of one bus line in pF. I_{SINK} ≤ 6mA. T_R and t_F measured between 0.3×V_{CC} and 0.7×V_{CC}.

FUNCTION BLOCK DIAGRAM



DETAILED DESCRIPTION

I2C INTERFACE

IS31FL3294 uses a serial bus, which conforms to the I2C protocol, to control the chip's functions with two wires: SCL and SDA. The IS31FL3294 has a 7-bit slave address (A7:A1), followed by the R/W bit, A0. Set A0 to "0" for a write command and set A0 to "1" for a read command. The value of bits A1 and A2 are decided by the connection of the AD pin.

Table 1 Slave Address

AD	A7:A3	A2:A1	A0
GND	1110 1	00	0/1
SCL		01	
SDA		10	
VCC		11	

AD connected to GND, A2:A1=00;

AD connected to VCC, A2:A1=11;

AD connected to SCL, A2:A1=01;

AD connected to SDA, A2:A1=10;

The SCL line is uni-directional. The SDA line is bi-directional (open-drain) with a pull-up resistor (typically 2kΩ). The maximum clock frequency specified by the I2C standard is 1MHz. In this discussion, the master is the microcontroller and the slave is the IS31FL3294.

The timing diagram for the I2C is shown in Figure 2. The SDA is latched in on the stable high level of the SCL. When there is no interface activity, the SDA line should be held high.

The "START" signal is generated by lowering the SDA signal while the SCL signal is high. The start signal will alert all devices attached to the I2C bus to check the incoming address against their own chip address.

The 8-bit chip address is sent next, most significant bit first. Each address bit must be stable while the SCL level is high.

After the last bit of the chip address is sent, the master checks for the IS31FL3294's acknowledge. The master releases the SDA line high (through a pull-up resistor). Then the master sends an SCL pulse. If the IS31FL3294 has received the address correctly, then it holds the SDA line low during the SCL pulse. If the SDA line is not low, then the master should send a "STOP" signal (discussed later) and abort the transfer.

Following acknowledge of IS31FL3294, the register address byte is sent, most significant bit first. IS31FL3294 must generate another acknowledge indicating that the register address has been received.

Then 8-bit of data byte are sent next, most significant bit first. Each data bit should be valid while the SCL level is stable high. After the data byte is sent, the IS31FL3294 must generate another acknowledge to indicate that the data was received.

The "STOP" signal ends the transfer. To signal "STOP", the SDA signal goes high while the SCL signal is high.

ADDRESS AUTO INCREMENT

To write multiple bytes of data into IS31FL3294, load the address of the data register that the first data byte is intended for. During the IS31FL3294 acknowledge of receiving the data byte, the internal address pointer will increment by one. The next data byte sent to IS31FL3294 will be placed in the new address, and so on. The auto increment of the address will continue as long as data continues to be written to IS31FL3294 (Figure 5).

READING OPERATION

Most of the registers can be read.

To read the register, after I2C start condition, the bus master must send the IS31FL3294 device address with the R/ bit set to "0", followed by the register address which determines which register is accessed. Then restart I2C, the bus master should send the IS31FL3294 device address with the R/ bit set to "1". Data from the register defined by the command byte is then sent from the IS31FL3294 to the master (Figure 6).

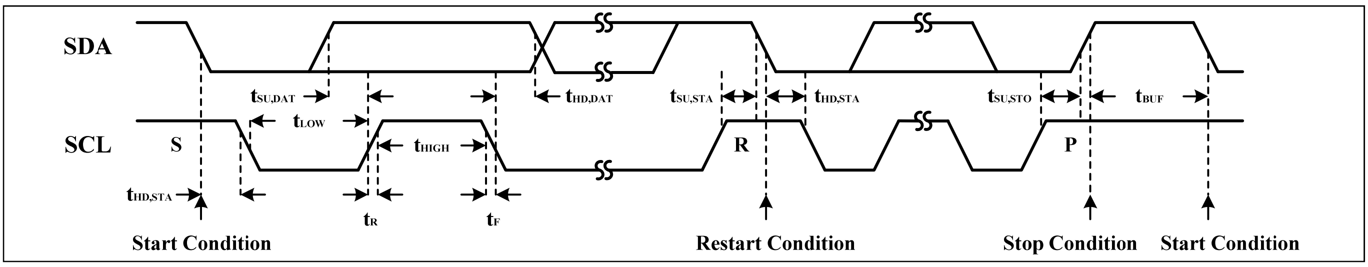


Figure 2 I2C Interface Timing

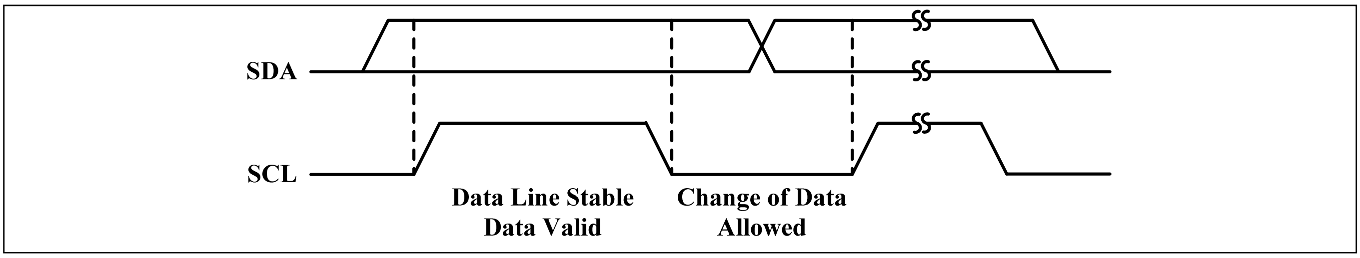


Figure 3 I2C Bit Transfer

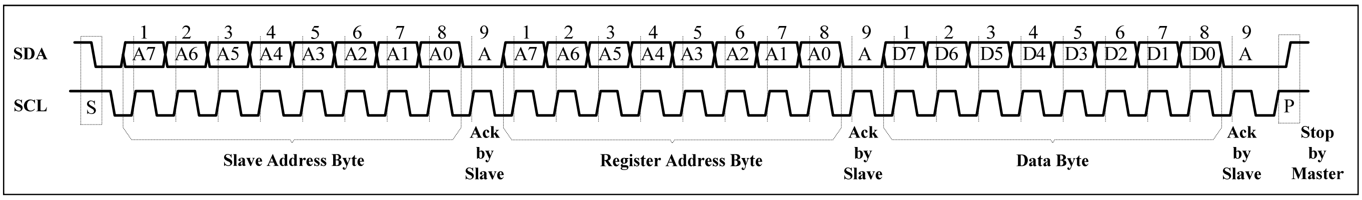


Figure 4 I2C Writing to IS31FL3294 (Typical)

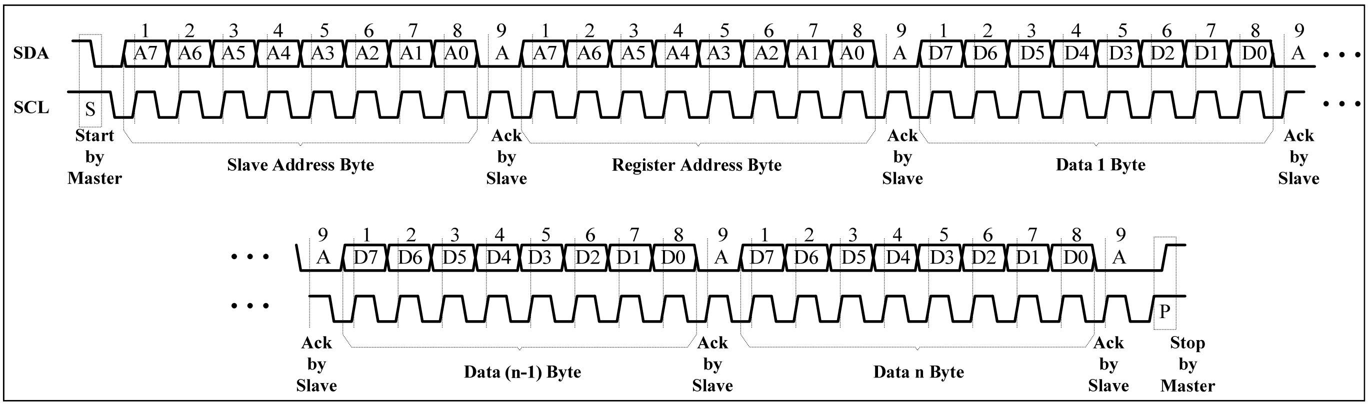


Figure 5 I2C Writing to IS31FL3294 (Automatic Address Increment)

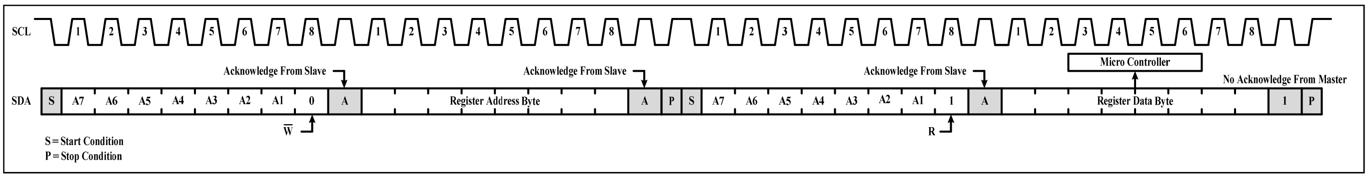


Figure 6 I2C Reading from IS31FL3294

Table 2 Registers Definitions

Address	Name	Function	R/W	Table	Default
00h	Product ID	For read only, read result is Slave address	R	-	-
01h	Shutdown Control Register	Set power down mode and outputs shutdown control	R/W	3	0010 0000
02h	Output Enable Register 1	Enable output 1~4	R/W	4	0001 1111
04h	Operation Configure Register 1	Set output 1~3 operation mode	R/W	5	0000 0000
05h	Operation Configure Register 2	Set output 4 operation mode	R/W	6	0000 0000
07h	Global Current Control Register	Set global current	R/W	7	0011 1111
08h	Hold Function Register	Set the hold function of each Output	R/W	8	0000 0000
0Bh	PWM Frequency Adjust Unlock Register	Unlock the 0Ch	W	-	0000 0000
0Ch	PWM Frequency Adjust Register	Adjust the PWM Frequency	R/W	9	0000 0000
0Dh~0Fh	3 Pattern State Register	For reading the pattern running state	R	10	0000 0000
10h~13h	OUT1~OUT4 Current Level Register	Output current level data register	R/W	11	0000 0000
10h~13h	Color 1 Setting Register of Pattern	Output current level data register-Color 1	R/W	12	0000 0000
20h~23h	Color 2 Setting Register of Pattern	Output current level data register-Color 2	R/W		0000 0000
30h~33h	Color 3 Setting Register of Pattern	Output current level data register-Color 3	R/W		0000 0000
19/29/39h	Pattern TS &T1 Setting Register	Set the TS~T1 time	R/W	15	0000 0000
1A/2A/3Ah	Pattern T2 &T3 Setting Register	Set the T2~T3 time	R/W	16	0000 0000
1B/2B/3Bh	Pattern TP &T4 Setting Register	Set the TP~T4 time	R/W	17	0000 0000
1C/2C/3Ch	Pattern Color Enable Register	Set the color enable/disable	R/W	18	0000 0001
1D/2D/3Dh	Pattern Color Cycle Times Register	Set color repeat time	R/W	19	0000 0000
1E/2E/3Eh	Pattern Register	Set next step and Gamma of each pattern	R/W	20	0000 0001
1F/2F/3Fh	Pattern Loop Times Register	Set the loop time of Pattern	R/W	21	0000 0000
40h~47h	PWM Register	Set PWM data	R/W	13	0000 0000
52h	Color Update Register	Update color data	R/W	-	0000 0000
53h	PWM Update Register	Update PWM data	R/W	-	0000 0000
54/55/56h	Pattern Update Register	Update the time data and start to run pattern	R/W	-	0000 0000
5Fh	Reset Register	Reset the registers value to default	W	-	0000 0000

Table 3 01h Shutdown Control Register

Bit	D7	D6	D5	D4	D3:D2	D1	D0
Name	LCAI	IMAX	MS	-	PFS	SLE	SSD
Default	0	0	1	0	00	0	0

The Shutdown Control Register sets software shutdown and sleep modes of IS31FL3294.

When the SLE bit is set to "1", the IS31FL3294 enters Sleep Mode if all OUTx outputs are off for >20s. All OUTx are off without any bias. I_SLEEP = 1μA (Typ.). When the IS31FL3294 is in sleep mode, the SLE bit needs to be set to "0" so that the IS31FL3294 will wake up and disable the sleep mode.

The PFS bit sets the PWM resolution. PWM mode can operate at 220Hz (12-bit, 8+4-bit mode), 440Hz (12-bit, 8+4-bit mode) and 23kHz (8+4-bit mode).

When MS set to "1", the IS31FL3294 in the Master mode.

SSD Software Shutdown Enable
0 Software shutdown mode
1 Normal operation

SLE Sleep Mode Enable
0 Sleep mode disable
1 Sleep mode enable (20s after no output current)

PFS PWM Frequency Select
00 220Hz (Force 220Hz in Pattern Mode or PWM mode)
01 440Hz (12-bit PWM mode)
1x 23kHz (8+4-bit PWM mode, 23kHz)

LCAI Low Current Accuracy Improve
0 Default maximum 30mA
1 1/3 output current, and improve low current accuracy

IMAX Enable $I_{OUT(MAX)}$=40mA
0 Default 30mA
1 $I_{OUT(MAX)}$=40mA

MS Master Slave
0 Master mode disable
1 Master mode enable

Table 4 02h Output Enable Register 1

Bit	D7:D4	D3	D2	D1	D0
Name	-	EN4	EN3	EN2	EN1
Default	0001	1	1	1	1

The Output Enable Register enables/disables the outputs independently. The ENx is only effective when SSD= "1".

ENx Output Enable Control
0 Output disable
1 Output enable

Table 5 04h Operating Configure Register 1

Bit	D7	D6	D5:D4	D3:D2	D1:D0
Name	-	RGB	MOD3	MOD2	MOD1
Default	0	0	00	00	00

Table 6 05h Operating Configure Register 2

Bit	D7:D2	D1:D0
Name	-	MOD4
Default	0000000	00

The MODx (x=1~4) bits sets output operation modes of IS31FL3294.

When RGB= "1", RGB Mode enables, OUT1~OUT4 running in RGB Mode, the MODx (x=1~4) bits are invalid. When RGB= "0", OUT1~OUT4 are controlled by the MODx (x=1~4) bits.

RGB Enable RGB Mode
0 Disable
1 Enable

MODx OUT1~OUT4 LED Mode
00 PWM & Current Level Mode
01 Pattern Mode
1x Current Level Mode

When the OUTx works in PWM Mode & Current Level Mode, means the output current is controlled by PWM Registers (40h~47h).

When the OUTx works in Pattern Mode, it means the output current is controlled by Color Setting Registers.

When the OUTx works in Current Level Mode, it means the output current is controlled by Current Level Register.

Table 7 07h Global Current Control Register

Bit	D7:D6	D5:D0
Name	-	GCC
Default	00	11 1111

GCC registers control I_{OUT} as shown in Formula (1).
If GCC=0x3F, CL=0xFF, I_{OUT}= $I_{OUT(MAX)}$

$$I_{OUT} = 30mA \times \frac{GCC}{64} \times \frac{CL}{256} \quad (1)$$

$$GCC = \sum_{n=0}^{7} D[n] \cdot 2^n \quad (2)$$

When IMAX= “1”, the 30mA will become 40mA.

Table 8 08h Hold Function Register

Bit	D7:D6	D5	D4	D3	D2	D1	D0
Name	-	HFE3	HTS3	HFE2	HTS2	HFE1	HTS1
Default	00	0	0	0	0	0	0

The Hold Function Register configures hold time for each output in Pattern Mode.

HTS Hold Time Selection
0 Hold at end of T4 when Pattern loop done (always off)
1 Hold at end of T2 when Pattern loop done (always on)08”

HFE Hold Function Enable
0 hold function disable
1 hold function enable

0Bh PWM Frequency Adjust Unlock Register

Write “0xA5” to 0Bh to unlock the PWM Frequency Adjust Register (0Ch).

Table 9 0Ch PWM Frequency Adjust Register

Bit	D7:D3	D2:D0
Name	-	PFA
Default	000	000

Before access to 0Ch, the 0Bh need to be written with 0xA5 to unlock it.

The PFA bits adjust the PWM Frequency, for example, if PWM frequency is 23kHz at 8+4-bit PWM mode, if PFA is “000”, the PWM frequency is 23kHz, if PFA is “001”, the PWM frequency is 28.08kHz (+22.07%).

PFA PWM Frequency Adjust
000 0%
001 +22.07%
010 +36.29%
011 +57.04%
100 -51.58%
101 -44.48%
110 -30.89%
111 -15.22%

Table 10 0Dh~0Fh Pattern State Register (Read Only)

Bit	D7:D0
Name	Pattern State
Default	0000 0000

The Pattern State Register stores the pattern status. 0Dh register is used for pattern 1, 0Eh for pattern 2, similarly 0Fh for pattern 3.

Below table shows the pattern running state.

Read Result	D7:D0	Pattern State	Color	Time
0x90	1001 0000	Running	-	TS
0x91	1001 0001	Running	Color1	T1
0x92	1001 0010	Running	Color1	T2
0x93	1001 0011	Running	Color1	T3
0xA4	1010 0100	Running	Color1	TP
0xA1	1010 0001	Running	Color2	T1
0xA2	1010 0010	Running	Color2	T2
0xA3	1010 0011	Running	Color2	T3
0xC4	1100 0100	Running	Color2	TP
0xC1	1100 0001	Running	Color3	T1
0xC2	1100 0010	Running	Color3	T2
0xC3	1100 0011	Running	Color3	T3
0x94	1001 0100	Running	Color3	TP
0x95	1001 0101	Running	-	T4
0x00	0000 0000	Not running	-	-

Note 7: These reading results are only applicable for the condition: the color 1, color 2 and color 3 in one pattern are all enabled (1Ch/2Ch/3Ch = 0x07).

Table 11 10h~13h OUT1~OUT4 Current Level Register

Bit	D7:D0
Name	CL
Default	0000 0000

The output current may be computed using the Formula (1):

$$I_{OUT} = 30mA \times \frac{GCC}{64} \times \frac{CL}{256} \quad (1)$$

$$CL = \sum_{n=0}^{7} D[n] \cdot 2^n \quad (3)$$

$$I_{LED} = 30mA \times \frac{GCC}{64} \times \frac{CL}{256} \times \frac{PWM}{4096} \quad (4)$$

Where D[n] stands for the individual bit value, 1 or 0, in location n, PWM is the value in 40h~51h, I_{OUT} is the peak current of the outputs. I_{LED} is the average current of the outputs.

When IMAX= “1”, the 30mA will become 40mA.

When IS31FL3294 operates in Current Level Mode, PWM = 4096 in above equation.

For example: in Current Level node only, if D7:D0 = 10110101,

I_{OUT} = 30mA × $(2^7 + 2^5 + 2^4 + 2^2 + 2^0)/256$

When IS31FL3294 operates in PWM & Current Level Mode, the value of CL and PWM will decide the output current together.

Table 12-1 10h~13h Color 1 Setting Register of Pattern (OUT1~OUT4)

Bit	D7:D0
Name	COL1_Oy
Default	0000 0000

Table 12-2 20h~23h Color 2 Setting Register of Pattern (OUT1~OUT4)

Bit	D7:D0
Name	COL2_Oy
Default	0000 0000

Table 12-3 30h~33h Color 3 Setting Register of Pattern (OUT1~OUT4)

Bit	D7:D0
Name	COL3_Oy
Default	0000 0000

Color Setting Registers store the color setting for each output in Pattern Mode. Check Pattern Color Setting section for more information about the color setting registers.

When IS31FL3294 operates in Pattern Mode, the value of Color Registers will decide the output current of each output in 256 levels.

The output current may be computed using the Formula (4):

$$I_{OUT} = 30\,mA \times \frac{COLx\_Oy}{256} \quad (5)$$

$$COLx\_Oy = \sum_{n=0}^{7} D[n] \cdot 2^n \quad (6)$$

Where D[n] stands for the individual bit value, 1 or 0, in location n.

For example: if D7:D0 = 10110101,

I_{OUT} = 30mA×$(2^7 + 2^5 + 2^4 + 2^2 + 2^0)/256$

I_{OUT} is the peak current of the outputs.

Need to write Color Update Register (52h) to update the data.

Table 13 40h~47h PWM Register

Reg	41h, 43h, 45h, 47h		40h, 42h, 44h, 46h
Bit	D7:D4	D3:D0	D7:D0
Name	-	PWM_H	PWM_L
Default	0000	0000	0000 0000

When IS31FL3294 operates in PWM & Current Level Mode, each output has 2 bytes to modulate the PWM duty as below Table 17 in 4096 steps, in Pattern Mode, the PWM cannot be accessed.

The value of the PWM Registers decides the average current of each LED noted I_{LED}.

The value of the PWM Registers decides the average current of each LED noted I_{LED}.

I_{LED} computed by Formula (1):

$$I_{LED} = 30mA \times \frac{GCC}{64} \times \frac{CL}{256} \times \frac{PWM}{4096} \quad (7)$$

Where I_{OUT} is the peak current of the outputs. I_{LED} is the average current of the outputs.

$$PWM = \sum_{n=0}^{11} D[n] \cdot 2^n$$

Where D[n] stands for the individual bit value, 1 or 0, in location n.

For example: if PWM_H = 00001001, PWM_L = 10110101, N=4096, GCC=63, CL=255,

I_{LED} = 30mA×$(2^{11} + 2^8 + 2^7 + 2^5 + 2^4 + 2^2 + 2^0)/4096$

Table 14 Register of PWM & Current Level Mode

Mode	Register	OUT1	OUT2
PWM & Current Level	PWM_H	41h	43h
	PWM_L	40h	42h
	CL	10h	11h
	Register	OUT3	OUT4
	PWM_H	45h	47h
	PWM_L	44h	46h
	CL	12h	13h

Table 15 19/29/39h Pattern TS &T1 Setting Register

Bit	D7:D3	D4:D0
Name	T1	TS
Default	0000	0000

The TS & T1 Setting Registers set the TS and T1 time in Pattern Mode. 19h register is used for pattern 1, 29h for pattern 2, similarly 39h for pattern 3.

TS	**Pattern Start Time Selection**
0000	0.04s
0001	0.16s
0010	0.31s
0011	0.46s
0100	0.61s
0101	0.92s
0110	1.25s
0111	1.92s
1000	2.52s
1001	3.12s
1010	3.72s
1011	5.04s
1100	6.24s
1101	7.44s
1110	8.76s
1111	9.96s

T1	**Rise Time Selection**
0000	0.04s
0001	0.16s
0010	0.31s
0011	0.46s
0100	0.61s
0101	0.92s
0110	1.25s
0111	1.92s
1000	2.52s
1001	3.12s
1010	3.72s
1011	5.04s
1100	6.24s
1101	7.44s
1110	8.76s
1111	9.96s

Table 16 1A/2A/3Ah Pattern T2 &T3 Setting Register

Bit	D7:D3	D4:D0
Name	T3	T2
Default	0000	0000

The T2 & T3 Setting Registers set the T2 and T3 time in Pattern Mode. 1Ah register is used for pattern 1, 2Ah for pattern 2, similarly 3Ah for pattern 3

T2	**Hold Time Selection**
0000	0.04s
0001	0.16s
0010	0.31s
0011	0.46s
0100	0.61s
0101	0.92s
0110	1.25s
0111	1.92s
1000	2.52s
1001	3.12s
1010	3.72s
1011	5.04s
1100	6.24s
1101	7.44s
1110	8.76s
1111	9.96s

T3	**Fall Time Selection**
0000	0.04s
0001	0.16s
0010	0.31s
0011	0.46s
0100	0.61s
0101	0.92s
0110	1.25s
0111	1.92s
1000	2.52s
1001	3.12s
1010	3.72s
1011	5.04s
1100	6.24s

1101	7.44s
1110	8.76s
1111	9.96s

Table 17 1B/2B/3Bh Pattern TP &T4 Setting Register

Bit	D7:D4	D3:D0
Name	T4	TP
Default	0000	0000

The TP & T4 Setting Registers set the TP and T4 time in Pattern Mode. 1Bh register is used for pattern 1, 2Bh for pattern 2, similarly

It should be noted that the sleep mode effective time is 20s, it starts at the end of T3. If T4+TP is too long, pattern loop will stop. When sleep mode is enabled, T4 & TP do no longer than 4.20s.

TP	Time between Pulses
0000	0.04s
0001	0.16s
0010	0.31s
0011	0.46s
0100	0.61s
0101	0.92s
0110	1.25s
0111	1.92s
1000	2.52s
1001	3.12s
1010	3.72s
1011	5.04s
1100	6.24s
1101	7.44s
1110	8.76s
1111	9.96s

T4	Off Time Selection
0000	0.04s
0001	0.16s
0010	0.31s
0011	0.46s
0100	0.61s
0101	0.92s
0110	1.25s
0111	1.92s
1000	2.52s
1001	3.12s
1010	3.72s
1011	5.04s
1100	6.24s
1101	7.44s
1110	8.76s
1111	9.96s

Table 18 1C/2C/3Ch Pattern Color Enable Register

Bit	D7:D3	D2	D1	D0
Name	-	CE3	CE2	CE1
Default	00000	0	0	1

Color Enable Register enables the color function for each color in Pattern Mode. 1Ch register is used for pattern 1, 2Ch for pattern 2, similarly 3Ch for pattern 3.

CEx	Color Enable Selection
0	Color x disable
1	Color x enable

Table 19 1D/2D/3Dh Pattern Color Cycle Times Register

Bit	D7:D6	D5:D4	D3:D2	D1:D0
Name	-	CCT3	CCT2	CCT1
Default	00	00	00	00

Pattern Color Cycle Times Register sets Color loop times for each color. 1Dh register is used for pattern 1, 2Dh for pattern 2, similarly 3Dh for pattern 3.

CCTx	Color Cycle Times Selection
00	Endless
01	1 time
10	2 times
11	3 times

Table 20-1 1Eh Pattern Register

Bit	D7:D4	D3	D2	D1:D0
Name	MTPLT1	GAM1	-	NXT1
Default	0000	0	0	01

GAM controls the gamma of pattern. MTPLT controls the loop of Pattern.

GAM1	Gamma Selection
0	Gamma=2.4
1	Linearity

MTPLT1 Multi-Pulse Loop Time
0000 endless
0001 1 time
…
1111 15 times

NXT1 Pattern 1 Next
01 Go to Pattern 2 (Only effective in RGB mode)
00/10/11 Just stop

Table 20-2 2Eh Pattern Register

Bit	D7:D4	D3	D2	D1:D0
Name	MTPLT2	GAM2	-	NXT2
Default	0000	0	0	01

GAM controls the gamma of pattern. MTPLT controls the loop of Pattern.

GAM2 Gamma Selection
0 Gamma=2.4
1 Linearity

MTPLT2 Multi-Pulse Loop Time
0000 Endless
0001 1 time
…
1111 15 times

NXT2 Pattern 2 Next
01 Go to Pattern 1 (Only effective in RGB mode)
10 Go to Pattern 3 (Only effective in RGB mode)
00/11 Just stop

Table 20-3 3Eh Pattern Register

Bit	D7:D4	D3	D2	D1:D0
Name	MTPLT3	GAM3	-	NXT3
Default	0000	0	0	01

GAM controls the gamma of pattern. MTPLT controls the loop of Pattern.

GAM3 Gamma Selection
0 Gamma=2.4
1 Linearity

MTPLT3 Multi-Pulse Loop Time
0000 endless
0001 1 time
…
1111 15 times

NXT3 Pattern 3 Next
01 Go to Pattern 1 (Only effective in RGB mode)
10 Go to Pattern 2 (Only effective in RGB mode)
00/11 Just stop

Table 21 1F/2F/3Fh Pattern Loop Times Register

Bit	D7	D6:D0
Name	PLTx_H	PLTx_L
Default	0	000 0000

Pattern loop Times register sets the loop time of the pattern. 1Fh register is used for pattern 1, 2Fh for pattern 2, similarly 3Fh for pattern 3.
If PLT_H(D7)=0, PLT_L!=0
Pattern loop times:

$$Looptime = \sum_{n=0}^{6} D[n] \times 2^n \qquad (8)$$

If PLT_H(D7)=0, PLT_L=0, endless
If PLT_H(D7)=1, PLT_L!=0
Pattern loop times:

$$Looptime = 16 \times \sum_{n=0}^{6} D[n] \times 2^n \qquad (9)$$

If PLT_H(D7)=1, PLT_L=0, endless

52h Color Update Register

Write "0xC5" to 52h will update the data of 10h~18h/20h~28h/30h~38h.

53h PWM Update Register

Write "0xC5" to 53h will update the data of 40~51h.

54/55/56h Pattern time Update Register

Write "0xC5" to 54/55/56h will update the data of 19h~1Fh/29h~2Fh/39h~3Fh.

5Fh Reset Register

Once user writes "0xC5" to the Reset Register, IS31FL3294 will reset all registers to their default value. On initial power-up, the IS31FL3294 registers are reset to their default values for a blank display.

TYPICAL APPLICATION INFORMATION

GENERAL DISCRIPTION

IS31FL3294 is a 4-channel fun LED driver with auto breathing mode. It has Pattern Mode and Current Lever Mode for RGB lighting effects.

CURRENT SETTING

The maximum output current is 30mA. When IMAX="1", the 30mA will become 40mA. The Global Current Control register GCC can be used to set a lower current. The 8-bit CL registers (10h~13h) control the individual currents for each of the outputs.

For example, OUT1, OUT2 and OUT3 drive an RGB LED, OUT1 is Red LED, OUT2 is Green LED and OUT 3 is Blue LED. If GCC and CL bits are the same, then the RGB LED may appear a pinkish, or not so white. The CL bits can be used to adjust the IOUTx current so the RGB LED appears closer to a pure white color. We call this CL bit adjustment by another name: white balance register.

PWM FREQUENCY SELECT

The IS31FL3294 output channels operate with a default 12-bit PWM resolution and the PWM frequency of 220Hz. Because all the OUTx channels are synchronized, the DC power supply will experience large instantaneous current surges when the OUTx channels turn ON. These current surges will generate an AC ripple on the power supply which cause stress to the decoupling capacitors. When the AC ripple is applied to a monolithic ceramic capacitor chip (MLCC) it will expand and contract causing the PCB to flex and generate audible hum in the range of between 20Hz to 20kHz, to avoid this hum, there are many countermeasures, such as selecting the capacitor type and value which will not cause the PCB to flex and contract.

An additional option for avoiding audible hum is to set the IS31FL3294's output PWM frequency above the audible frequency range. The Control Register (00h) can be used to set the switching frequency to 220Hz/440Hz/23KHz. Combination settings of the PFS bits will result in different PWM frequency, select a value higher than 20kHz to avoid the audible frequency range.

PWM CONTROL

The PWM Registers (40h~47h) can modulate LED brightness of each channels with 4096 steps. For example, if the data in PWM_H Register is "0000 0000" and in PWM_L Register is "0000 0100", then the PWM is 4/4096.

Writing new data continuously to the registers can modulate the brightness of the LEDs to achieve a breathing effect.

CURRENT LEVEL MODE

The Current Level Registers (10h~13h) are active and can modulate LED peak current IOUT of each output with 256 steps independently. For example, if the data in Current Lever Register is "0000 0100", then the current level is the fourth step, with a current level of 4/256.

In Current Level Mode, user doesn't need to turn on the CEx of 1Ch, a new value must be written to the Current Level registers to change the output current. Writing new data continuously to the registers can modulate the brightness of the LEDs to achieve breathing, blinking, or any other effects that the user defines.

In Current Level Mode, the output current (OUT1~OUT4) is configured by the Current Level Register (10h~14h).

PWM & CURRENT LEVEL MODE

PWM & Current Level Mode is the combination of PWM and Current Level Mode. In this mode, the Current Level Registers (10h~13h) adjust the peak current (I_{OUT}) of the outputs, the PWM Registers (40h~47h) adjust the duty cycle of the output current, the finial result is the output average current I_{LED}.

Table 14 Register of PWM & Current Level Mode

Mode	Register	OUT1	OUT2
PWM & Current Level	PWM_H	41h	43h
	PWM_L	40h	42h
	CL	10h	11h
	Register	OUT3	OUT4
	PWM_H	45h	47h
	PWM_L	44h	46h
	CL	12h	13h

RGB MODE

By setting the RGB bits of the Operating Configure Register 1 (04h) to "1", the IS31FL3294 will operate in One Shot Programming mode. In this mode 4 channels (1 group RGB and 1 single color LED) can be modulated breathing cycle independently by TS~TP (Figure 10). Setting different TS~T4 can achieve RGB breathing with auto color changing. OUT1~OUT4 running in Pattern 1 to Pattern 3. The maximum intensity of each RGB can be adjusted independently by the Color Setting Registers (10h~13h/20h~23h/30h~33h) (Table 25).

Table 22 Color Register of RGB Mode

Pattern Mode	Color Enable	OUT1	OUT2	OUT3	OUT4
Pattern 1	CE1(1Ch)	10h	11h	12h	13h
	CE2(1Ch)	20h	21h	22h	23h
	CE3(1Ch)	30h	31h	32h	33h
Pattern 2	CE1(2Ch)	10h	11h	12h	13h
	CE2(2Ch)	20h	21h	22h	23h
	CE3(2Ch)	30h	31h	32h	33h
Pattern 3	CE1(3Ch)	10h	11h	12h	13h
	CE2(3Ch)	20h	21h	22h	23h
	CE3(3Ch)	30h	31h	32h	33h

Note 8: If IS31FL3294 operates in the RGB Mode and then enters into sleep mode, the SLE bit needs to set as "0", that the IS31FL3294 will wake up and disable the sleep mode.

PATTERN MODE

By setting the MOD1~MOD4 bits of the Operating Configure Register (04h/05h) to "01", the corresponding output will operate in Pattern Mode. In Pattern Mode, the timing characteristics for output current – current rising (T1), holding (T2), falling (T3) and off time (TS, TP, T4) (Figure 9), can be adjusted individually so that each output can independently maintain a pre-established pattern achieving mixing color breathing or a single-color breathing without requiring any additional interface activity, thus saving valuable system resources. OUT1~OUT3 running in Pattern 1, OUT4 running in Pattern 2.

PATTERN COLOR SETTING

In Pattern Mode, the LED color is defined by COLx_Oy (x, y= 1, 2, 3) bits in Color Setting Registers (10h~13h/20h~23h/30h~33h). There are 1 RGB current combinations to generate 1 pre-defined colors for display. More than one of the 1 pre-defined colors can be chosen by setting CEx bits in Color Enable Register (1Ch/2Ch/3Ch). When CEx is set, the color x is allowed to be displayed in current pattern.

In Pattern Mode, the output current (OUT1~OUT4) is configured by the Color Setting Register of Pattern as Table 26.

Table 23 Color Register of Pattern Mode

Pattern Mode	Color Enable	OUT1	OUT2
Pattern 1	CE1(1Ch)	10h	11h
	CE2(1Ch)	20h	21h
	CE3(1Ch)	30h	31h
Pattern Mode	**Color Enable**	**OUT3**	**OUT4**
Pattern 2	CE1(2Ch)	12h	13h
	CE2(2Ch)	22h	23h
	CE3(2Ch)	32h	33h

PATTERN TIME SETTING

User should configure the related pattern time setting registers according to actual timing requirements via I2C interface before starting pattern. The pattern time is including TS, T1~T4 and TP. And the pattern has three continue lighting cycle as Color 1~Color 3. Please check the LED OPERATING MODE section for more about the time setting.

GAMMA CORRECTION

In order to perform a better visual LED breathing effect, the device integrates gamma correction to the Pattern Mode. The gamma correction causes the change in intensity to appear more linear to the human eye.

Gamma correction, also known as gamma compression or encoding, is used to encode linear luminance to match the non-linear characteristics of display. Since the IS31FL3294 can modulate the brightness of the LEDs with 256 steps, a gamma correction function can be applied when computing each subsequent LED intensity setting such that the changes in brightness matches the human eye's brightness curve.

The IS31FL3294 provides three gamma corrections which can be set by GAM bits of Pattern Registers (1Eh/2Eh/3Eh) for each pattern. The gamma correction is shown as below.

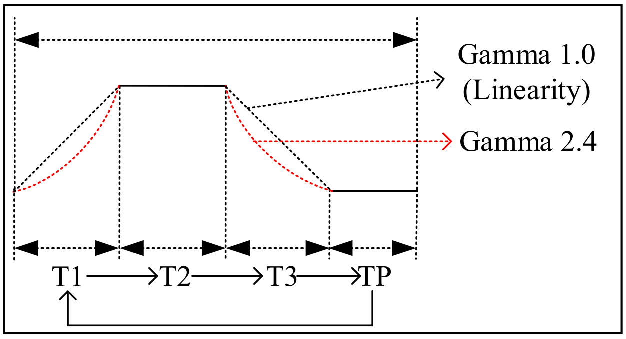


Figure 7 Gamma Correction

SHUTDOWN MODE

Shutdown mode can either be used as a means of reducing power consumption or generating a flashing display (repeatedly entering and leaving shutdown mode). During shutdown mode all registers retain their data.

Software Shutdown

By setting SSD bit of the Shutdown Register (01h) to “0”, the IS31FL3294 will operate in software shutdown mode, wherein it will consume only 0.4μA (Typ.) current. When the IS31FL3294 is in software shutdown mode, all current sources are switched off.

Hardware Shutdown

The chip enters hardware shutdown mode when the SDB pin is pulled low, wherein they consume only 0.4μA (Typ.) current. When set SDB high, the rising edge will reset the I2C module, but the register information retains.

LED OPERATING MODE

The IS31FL3294 has three operating modes which can be chosen by the MODx bits of Operating Configure Register (04h/05h).

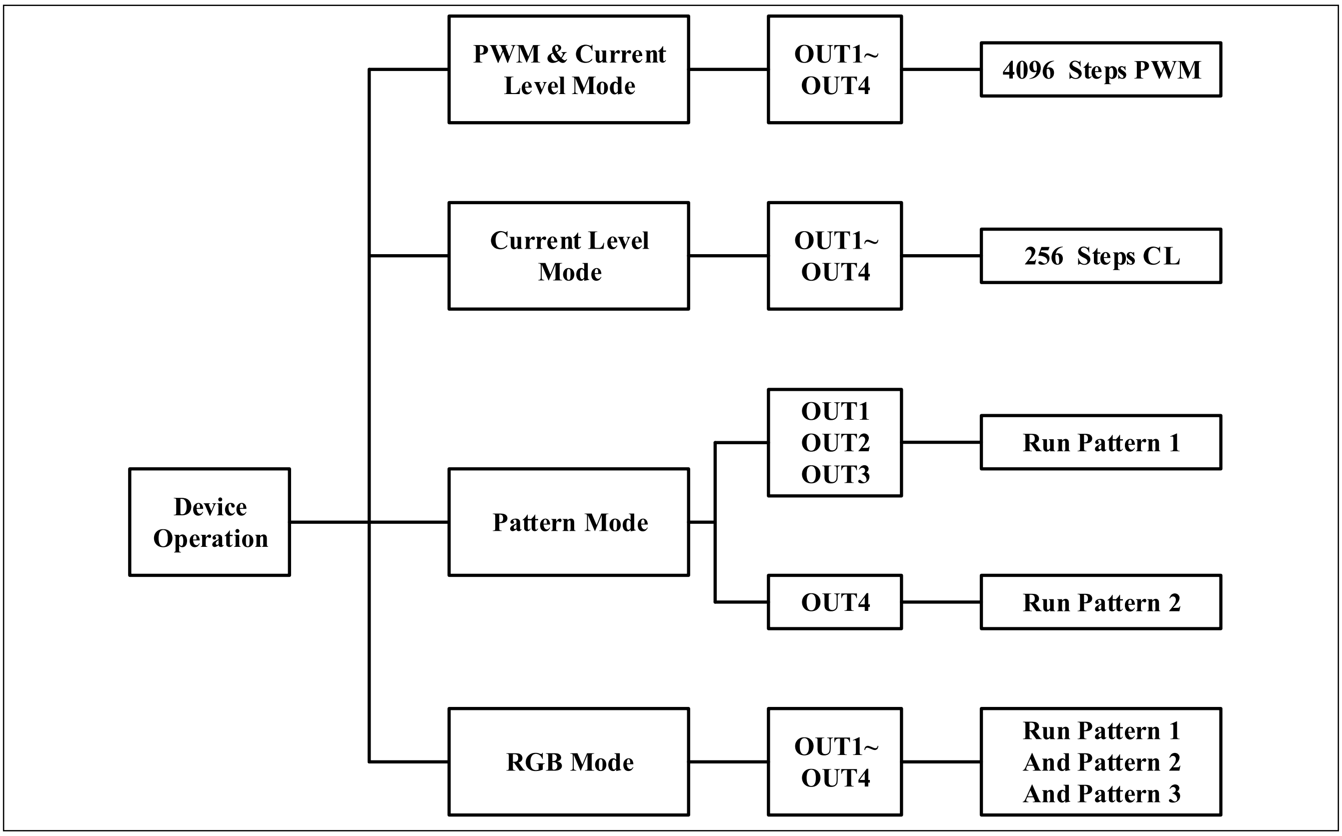


Figure 8 Operating Mode Map

Pattern Mode

If MODx=01 (Pattern Mode), OUT1~OUT3 can operate in Pattern Mode only and run pattern 1, OUT4 run the pattern 2.

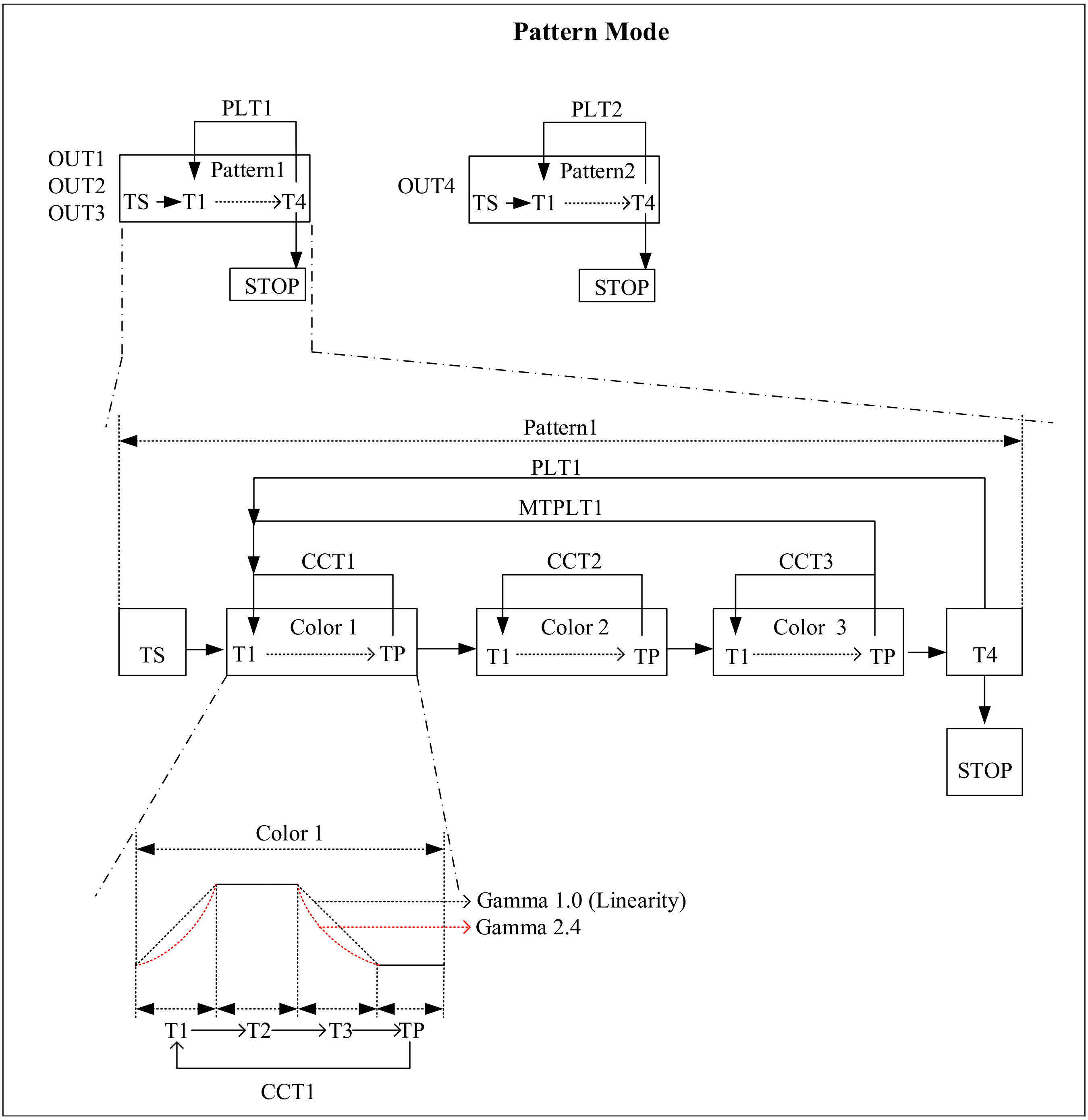


Figure 9 Pattern Mode

RGB Mode

If RGB=1 (RGB Mode), OUT1~OUT4 can operate in Pattern Mode only and run the pattern 1 and pattern 2 and pattern 3.

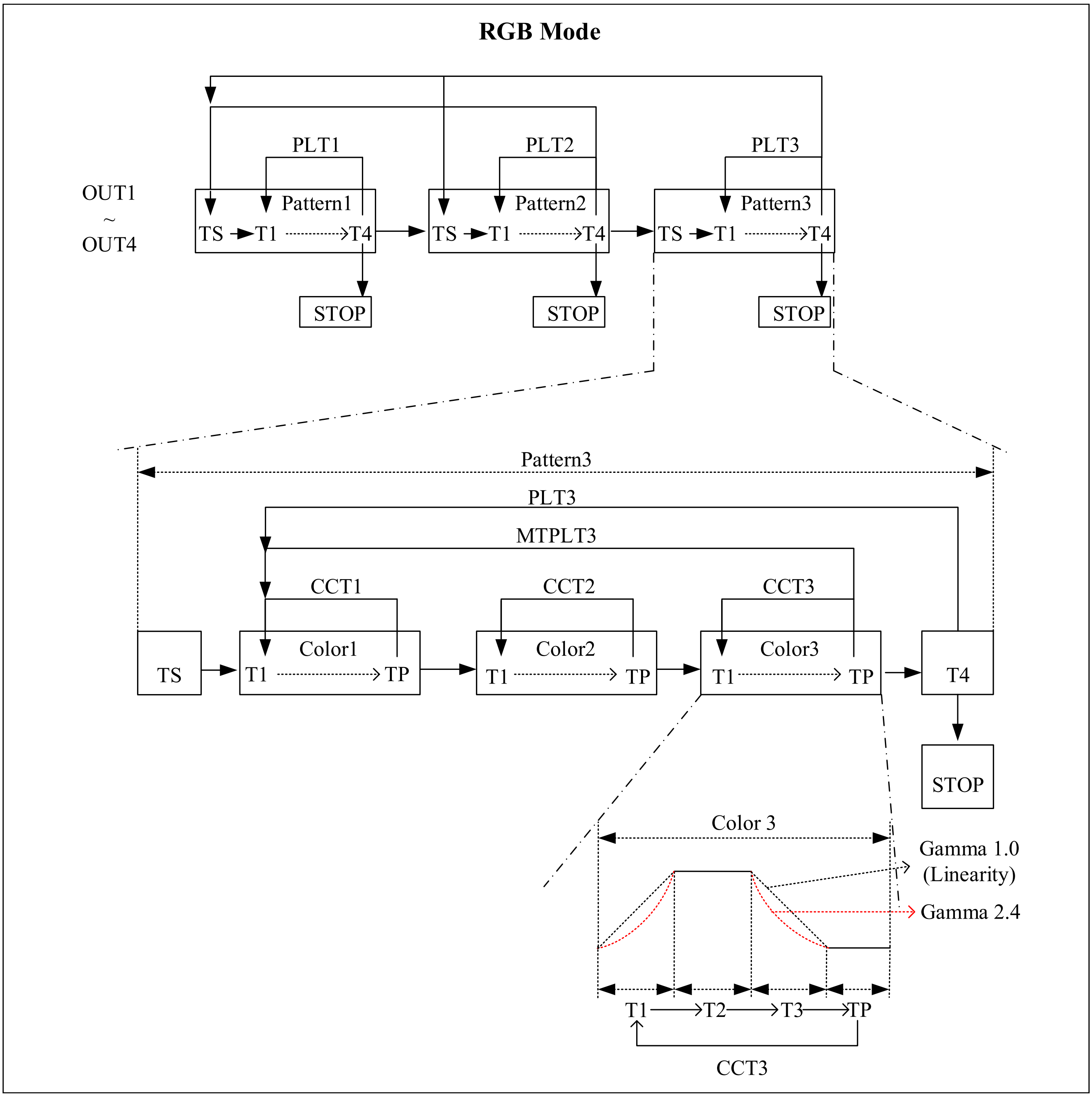


Figure 10 RGB Mode

CLASSIFICATION REFLOW PROFILES

Profile Feature	Pb-Free Assembly
Preheat & Soak Temperature min (Tsmin) Temperature max (Tsmax) Time (Tsmin to Tsmax) (ts)	150°C 200°C 60-120 seconds
Average ramp-up rate (Tsmax to Tp)	3°C/second max.
Liquidous temperature (TL) Time at liquidous (tL)	217°C 60-150 seconds
Peak package body temperature (Tp)*	Max 260°C
Time (tp)** within 5°C of the specified classification temperature (Tc)	Max 30 seconds
Average ramp-down rate (Tp to Tsmax)	6°C/second max.
Time 25°C to peak temperature	8 minutes max.

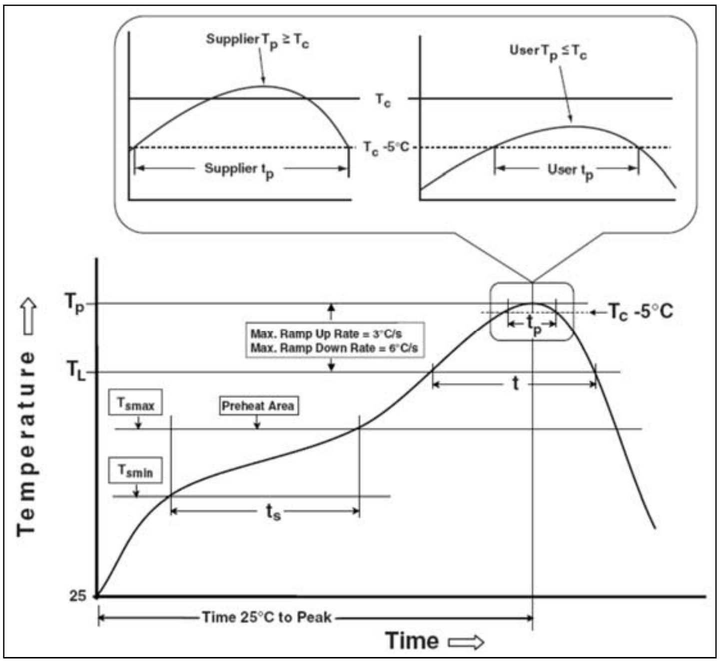
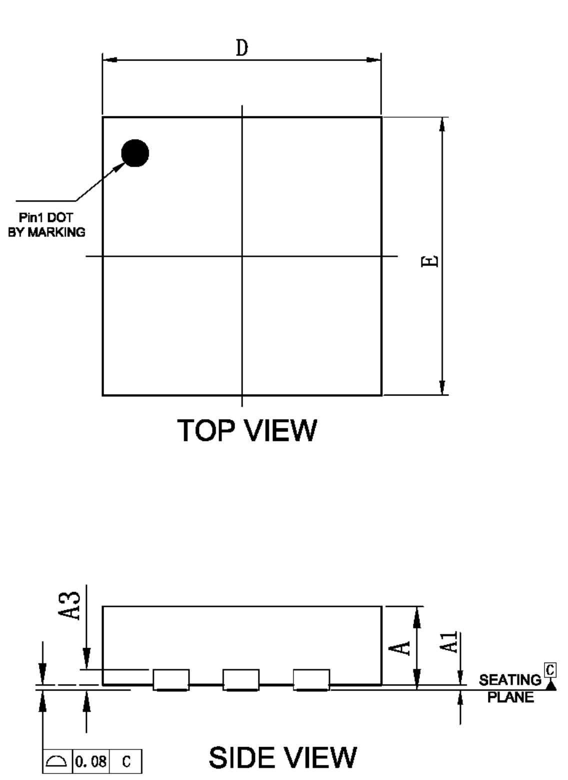
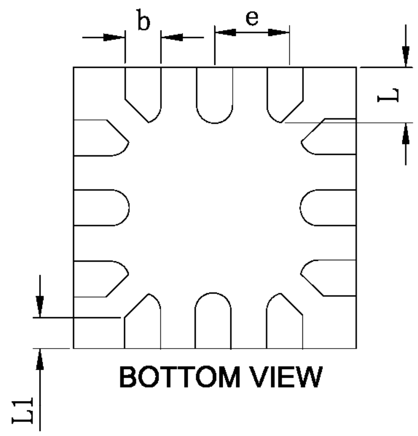


Figure 11 Classification Profile

PACKAGE INFORMATION

UTQFN-12





SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	0.50	0.55	0.60
A1	—	0.02	0.05
b	0.18	0.25	0.30
A3	0.15 Ref		
D	1.95	2.00	2.05
E	1.95	2.00	2.05
e	0.50 BSC		
L	0.30	0.40	0.50
L1	0.232	0.235	0.238

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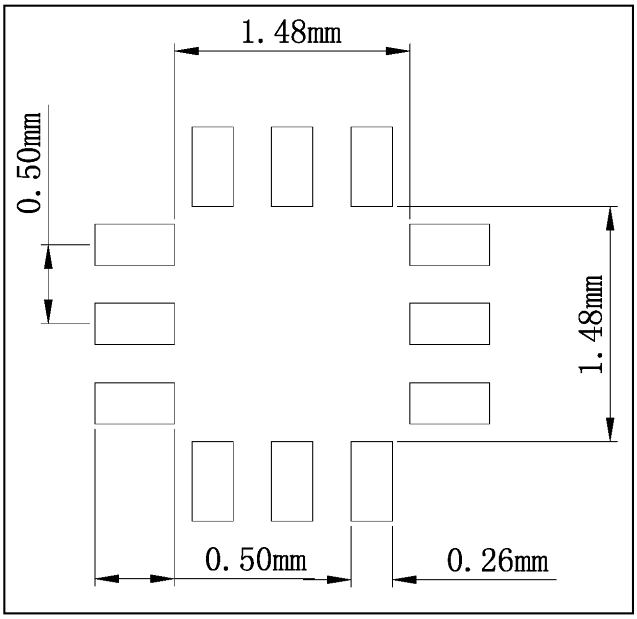
RECOMMENDED LAND PATTERN

UTQFN-12



Note:

1. Land pattern complies to IPC-7351.
2. All dimensions in MM.
3. This document (including dimensions, notes & specs) is a recommendation based on typical circuit board manufacturing parameters. Since land pattern design depends on many factors unknown (eg. User's board manufacturing specs), user must determine suitability for use.

REVISION HISTORY

Revision	Detail Information	Date
0A	Initial release	2022.11.23
A	Release to mass production	2023.03.09
B	Update QTY/Reel to 3000	2023.06.15
C	Correct the definition of 0D~0Fh Pattern State Register	2023.08.16
D	1. Updated Lumissil new Logo 2. Updated registers table 3. Updated description of 01h register 4. Added note 7 and 8	2024.05.21