IS31FL3298

CHARGE PUMP RGB LED DRIVER WITH PROGRAMMABLE SELF-RUNNING PATTERNS

May 2024

GENERAL DESCRIPTION

The IS31FL3298 is a charge pump LED driver with programmable sequence operation for automated RGBW lighting effects. It is capable of driving 9 LEDs up to 20mA (adjustable in 256 current levels and 4096 PWM levels) from battery power supply.

The built−in charge pump structure will automatically toggle between 1x, or 1.5x operation depending on the battery's state of charge. This DC/DC converter operates at a high switching frequency which enables the use of small external capacitors and achieves a 90% peak efficiency. To conserve battery life, the charge pump goes into high impedance mode whenever the IS31FL3298 is shutdown.

The IS31FL3298 can operate in PWM mode, the output current of each output is independently programmed and controlled in 4096 steps to achieve color mixing and the PWM duty cycle of each output is also independently programmed and controlled in 4096 steps to simplify color mixing or for smoothly diming control.

With automated lighting effects and a DC/DC charge pump, the small package IS31FL3298 is ideal for battery applications.

The IS31FL3298 is available in a small WLCSP-25 (0.4mm ball pitch, 0.2mm ball diameter) and QFN-24 (4mm × 4mm) packages. It operates from 2.5V to 5.5V over the temperature range of -40°C to +125°C.

FEATURES

- 2.5V to 5.5V supply voltage
- Charge pump
  - 1x, 1.5x operating modes
  - Highly efficient across battery state of charge
- Power saving operating
  - Quiescent operating current 420μA (Typ.)
  - Shutdown current 0.5μA (Typ.)
- Open/Short detection function
- Support 9 LEDs
  - Maximum 20mA output current per LED
  - 7-bit global current selections (128 levels, 0mA~20mA)
  - Each LED has 8-bit programmable current levels
  - Each LED has 12-bit programmable PWM levels
- Fast 1MHz I2C bus interface
  - Automatic address increment function
  - 3 selectable I2C address locations
- Auto breath function:
  - 3 patterns auto breath for 3×3 channels.
  - Other channels can quit the pattern and control by SL&PWM registers
  - Fade IN/ Fade OUT time length max value up to 10s.
  - 3 color pre-configure registers for color breath
- Over-temperature protection
- WLCSP-25 (0.4mm ball pitch, 0.2mm ball diameter) and QFN-24 (4mm × 4mm) packages
- Operating temperature T_A = -40°C ~ +125°C
- RoHS & Halogen-Free Compliance
- TSCA Compliance

APPLICATIONS

- Internet-of-Things (IOT)
- Electronic cigarette
- Low-power battery applications
- Hand-held devices requiring visual notifications

TYPICAL APPLICATION CIRCUIT

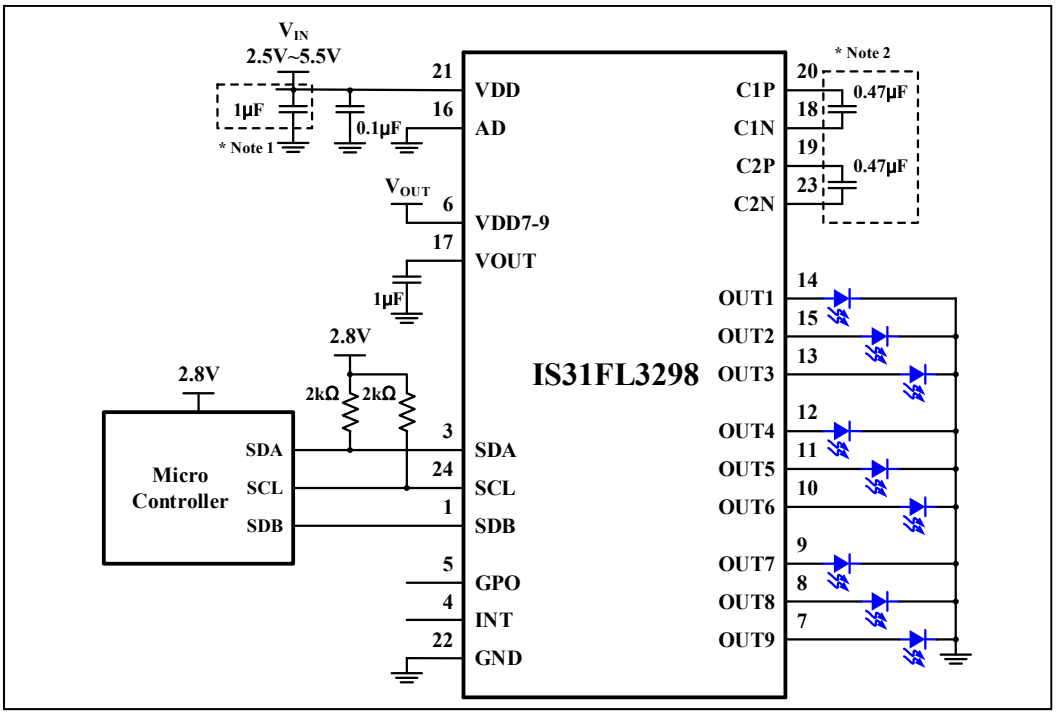


Figure 1 Typical Application Circuit

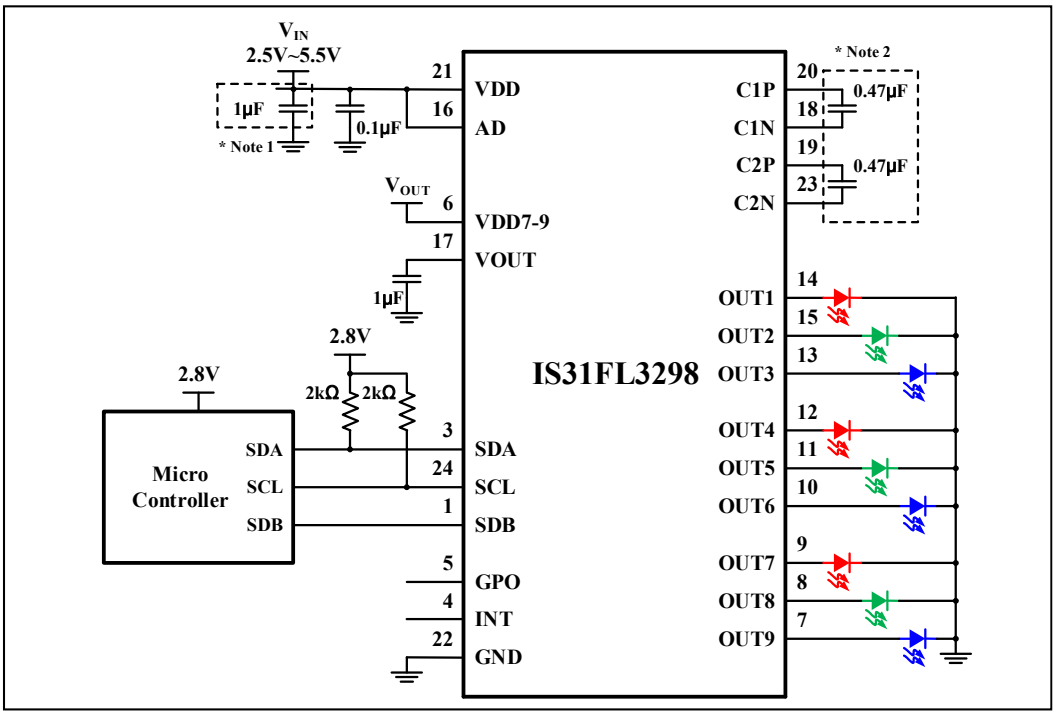
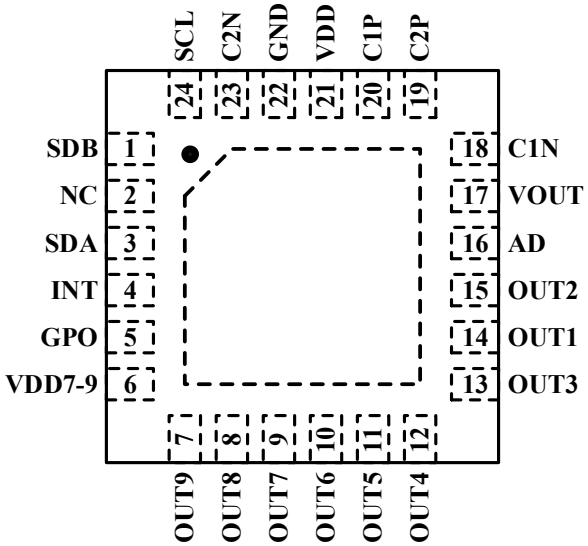
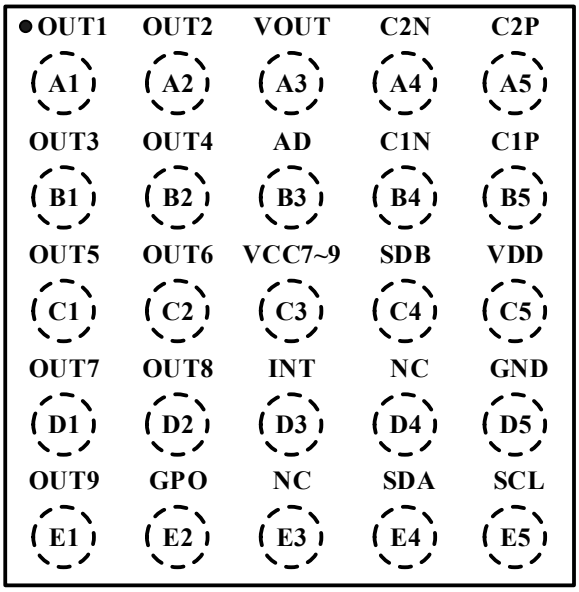


Figure 2 Typical Application Circuit (RGB application)

Note 1: The bypass capacitors should be placed as close as possible to the IC and the V_{CC} and GND trace kept as short as possible.

Note 2: The flying capacitors should be placed as close as possible to the IC and the signal trace between the capacitor and CP terminals kept as short as possible.

PIN CONFIGURATION

Package	Pin Configuration (Top View)
QFN-24	
WLCSP-25	

PIN DESCRIPTION

No.		Pin	Description
QFN	WLCSP		
1	C4	SDB	Pull below 0.4V to activate low power shutdown mode.
2	D4,E3	NC	Not connect. Leave this pin unconnected.
3	E4	SDA	I2C data pin. The SDA byte is used to program the device operating mode.
4	D3	INT	OD/O, Interrupt for microcontroller unit. Leave unconnected if not used.
5	E2	GPO	O, General-purpose output. Leave unconnected if not used.
6	C3	VDD7-9	Power supply for OUT 7-9.
7~15	A1,A2,B1,B2,C1, C2,D1,D2,E1	OUT9~OUT1	LED current source pins, connect the corresponding LED anode to this pin.
16	B3	AD	I2C address setting.
17	A3	VOUT	Charge pump output supplies the LED current. In shutdown mode this pin is high impedance. Connect a 1μF capacitor from VOUT to GND.
18	B4	C1N	Stage 1 charge pump flying capacitor, C1N negative terminal. (Note 2)
19	A5	C2P	Stage 2 charge pump flying capacitor, C2P positive terminal. (Note 2)
20	B5	C1P	Stage 1 charge pump flying capacitor, C1P positive terminal. (Note 2)
21	C5	VDD	Power supply input, requires 1.0μF and 0.1μF capacitor between this pin and ground pin.
22	D5	GND	Ground reference signal for the charge pump and the output current control. A PCB ground plane strongly recommended.
23	A4	C2N	Stage 2 charge pump flying capacitor, C2N negative terminal. (Note 2)
24	E5	SCL	I2C serial clock associated with SDA signal.
		Thermal Pad	Connect to GND.

Note 2: The flying capacitors should be placed as close as possible to the IC and the signal trace between the capacitor and CP terminals kept as short as possible.

ORDERING INFORMATION

Industrial Range: -40°C to +125°C

Order Part No.	Package	QTY/Reel
IS31FL3298-QFLS4-TR	QFN-24, Lead-free	2500
IS31FL3298-CLS4-TR	WLCSP-25, Lead-free	3000

ABSOLUTE MAXIMUM RATINGS

Supply voltage, V_{CC}, $V_{OUT,}$	-0.3V ~ +5.5V
Voltage at any input pin and NC pin	-0.3V ~ V_{CC} +0.3V
Maximum junction temperature, T_{JMAX}	+150°C
Operating temperature range, T_A=T_J	-40°C ~ +125°C
Storage temperature range, T_{STG}	-65°C ~ +150°C
Package thermal resistance, junction to ambient (4-layer standard test PCB based on JESD 51-2A), θ_{JA}	29.6°C/W (QFN) 68°C/W (WLCSP)
ESD (HBM) ESD (CDM)	±6kV ±750V

Note 3: Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other condition beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

T_A = 25°C, V_{CC} = 2.5V ~ 5.5V unless otherwise noted. Typical value is T_A = 25°C, V_{CC} = 3.6V.

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
V_{CC}	Supply voltage		2.5		5.5	V
I_{CC}	Quiescent operating current	1x mode, no load, (01h= 0x21)		420	500	μA
		1.5x mode, no load, (01h= 0x21)		2.5	3.1	mA
		Sleep Mode, no load		0.5	1	μA
I_{SDB}	Shutdown current	V_{SDB}= 0V		0.5	1	μA
		V_{SDB}= V_{CC}, software shutdown		0.5	1	μA
I_{OUT}	Current per channel	DC Mode, GCC= 0x3F， headroom voltage=0.6V	9.5	10	10.5	mA
		DC Mode, GCC= 0x7F headroom voltage=0.6V	19	20	21	mA
f_{OUT}	Output frequency	12bit mode	198	220	242	Hz
			396	440	484	
		8bit mode/8+4bit	21.6	24	26.4	kHz
ΔI_{MAT}	Output current error between bits (Note 4)	Any two outputs headroom voltage=0.6V, I_{OUT}= 10mA, DC Mode	-4		+4	%
ΔI_{ACC}	Output current error between devices (Note 5)	Any two outputs headroom voltage=0.6V, I_{OUT}= 10mA, DC Mode	-4		+4	%
V_{HR}	Current sink headroom voltage	DC Mode, GCC= 0x3F, I_{OUT}= 10mA		150	250	mV
V_{OVP}	Output voltage compliance (OVP)	1.5x mode Output Voltage Clamp	3.74	3.9	4.06	V
V_{SC_FL}	LED short detection threshold	I_{OUT}= 10mA, measured at OUTx to GND, PWM>10%， PWM Frequency = 24kHz		1	1.1	V
V_{OC_FL}	LED string open detection threshold	I_{OUT}= 10mA, measured at (V_{OUTx}-V_{OC_FL}), PWM>10%, PWM Frequency = 24kHz	40	60		mV

ELECTRICAL CHARACTERISTICS (CONTINUE)

T_A = 25°C, V_{CC} = 2.5V ~ 5.5V, unless otherwise noted. Typical value is T_A = 25°C, V_{CC}= 3.6V.

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
Charge Pump Characteristics						
t_{ST}	Soft-start time	Charge Pump start time (C_{OUT}= 1μF)		128		μs
f_{CPO}	Charge pump operating frequency	PWM frequency= 24kHz	900	1000	1120	kHz
		PWM frequency= 220Hz/440Hz	810	900	990	kHz
Logic Electrical Characteristics (SDA, SCL, AD, SDB, GPO, INT)						
V_{IL}	Logic “0” input voltage	V_{CC}= 2.5V~5.5V			0.4	V
V_{IH}	Logic “1” input voltage	V_{CC}= 2.5V~5.5V	1.4			V
I_{IL}	Logic “0” input current	V_{INPUT}= 0V (Note 6)		5		nA
I_{IH}	Logic “1” input current	V_{INPUT}= V_{CC} (Note 6)		5		nA
V_{OL}	Output Low Level (GPO, INT, SDA)	I_{OUT}= 5mA		0.1	0.2	V
V_{OH}	Output High Level (GPO)	I_{OUT}= -5mA	V_{CC} -0.2	V_{CC} -0.1		V
I_L	Output Leakage Current (GPO)	V_{GPO}= V_{CC}			1	μA

DIGITAL INPUT SWITCHING CHARACTERISTICS (NOTE 6)

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
f_{SCL}	Serial-Clock frequency				1	MHz
t_{BUF}	Bus free time between a STOP and a START condition		1.3			μs
$t_{HD, STA}$	Hold time (repeated) START condition		0.6			μs
$t_{SU, STA}$	Repeated START condition setup time		0.6			μs
$t_{SU, STO}$	STOP condition setup time		0.6			μs
$t_{HD, DAT}$	Data hold time				-	μs
$t_{SU, DAT}$	Data setup time		100			ns
t_{LOW}	SCL clock low period		1.3			μs
t_{HIGH}	SCL clock high period		0.7			μs
t_R	Rise time of both SDA and SCL signals, receiving	(Note 7)		20+0.1C_b	300	ns
t_F	Fall time of both SDA and SCL signals, receiving	(Note 7)		20+0.1C_b	300	ns

Note 4: I_{OUT} mismatch (bit to bit) $\triangle I_{MAT}$ is calculated:

$$\Delta I_{MAT} = \left(\frac{I_{OUTn}(n = 1 \sim 9)}{\left(\frac{I_{OUT1} + I_{OUT2} + \cdots + I_{OUT9}}{9}\right)} - 1 \right) \times 100\%$$

Note 5: I_{OUT} accuracy (device to device) $\triangle I_{ACC}$ is calculated:

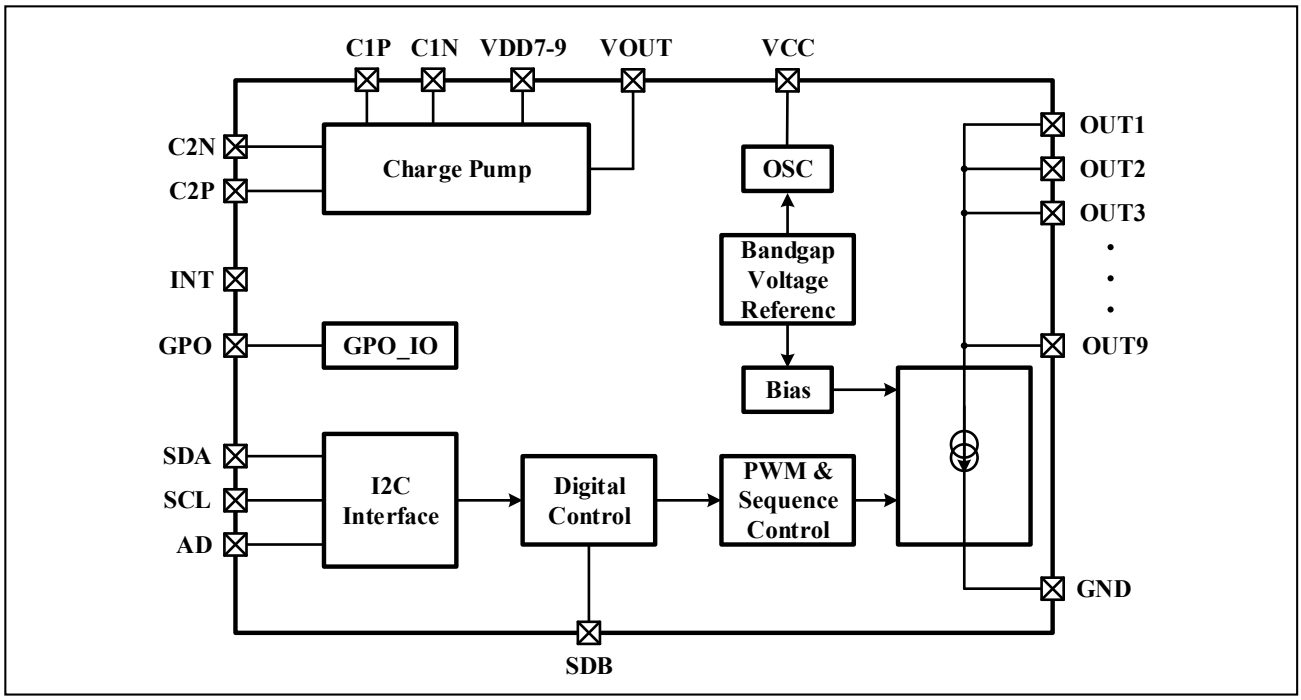
$$\Delta I_{ACC} = \left(\frac{\left(\frac{I_{OUT1} + I_{OUT3} + \cdots + I_{OUT9}}{9} - I_{OUT(IDEAL)}\right)}{I_{OUT(IDEAL)}} \right) \times 100\%$$

Where $I_{OUT(IDEAL)}$= 10mA.

Note 6: Guaranteed by design.

Note 7: C_b = total capacitance of one bus line in pF. I_{SINK} ≤ 6mA. t_R and t_F measured between 0.3× V_{CC} and 0.7× V_{CC}.

FUNCTION BLOCK DIAGRAM



DETAILED DESCRIPTION

I2C INTERFACE

IS31FL3298 uses a serial bus, which conforms to the I2C protocol, to control the chip's functions with two wires: SDA and SCL. The IS31FL3298 has a 7-bit slave address (A7:A1), followed by the R/W bit, A0. Set A0 to "0" for a write command and set A0 to "1" for a read command. The value of bits A1 and A2 are decided by the connection of the AD pin.

Table 1 Slave Address

AD	A7:A3	A2:A1	A0
GND	1110 0	00	0/1
SCL		01	
VDD		11	

AD connected to GND, A2:A1=00;

AD connected to VDD, A2:A1=11;

AD connected to SCL, A2:A1=01;

Note: If AD pin is connected to VOUT pin, when IS31FL3298 is in shutdown mode, V_{OUT} is low, device slave address is 0xE0 (A2:A1=00). After writing the SSD bit as "1" in shutdown control register (01h) by device slave address 0xE0(A2:A1=00), IS31FL3298 run into normal operation mode, V_{OUT} will be pulled high, the slave address will become 0xE6 (A2:A1=11).

The SCL line is uni-directional. The SDA line is bi-directional (open-drain) with a pull-up resistor (typically it is 2kΩ for 1MHz and 4.7kΩ for 400kHz). The maximum clock frequency specified by the I2C standard is 1MHz. In this discussion, the master is the microcontroller and the slave is the IS31FL3298.

The timing diagram for the I2C is shown in Figure 3. The SDA is latched in on the stable high level of the SCL. When there is no interface activity, the SDA line should be held high.

The "START" signal is generated by lowering the SDA signal while the SCL signal is high. The start signal will alert all devices attached to the I2C bus to check the incoming address against their own chip address.

The 8-bit chip address is sent next, most significant bit first. Each address bit must be stable while the SCL level is high.

After the last bit of the chip address is sent, the master checks for the IS31FL3298's acknowledgement. The master releases the SDA line high (through a pull-up resistor). Then the master sends an SCL pulse. If the IS31FL3298 has received the address correctly, then it holds the SDA line low during the SCL pulse. If the SDA line is not low, then the master should send a "STOP" signal (discussed later) and abort the transfer.

Following acknowledge of IS31FL3298, the register address byte is sent, most significant bit first. IS31FL3298 must generate another acknowledge indicating that the register address has been received.

Then 8-bit of data byte are sent next, most significant bit first. Each data bit should be valid while the SCL level is stable high. After the data byte is sent, the IS31FL3298 must generate another acknowledgement to indicate that the data was received.

The "STOP" signal ends the transfer. To signal "STOP", the SDA signal goes high while the SCL signal is high.

ADDRESS AUTO INCREMENT

To write multiple bytes of data into IS31FL3298, load the address of the data register that the first data byte is intended for. During the IS31FL3298 acknowledge of receiving the data byte, the internal address pointer will increment by one. The next data byte sent to IS31FL3298 will be placed in the new address, and so on. The auto increment of the address will continue as long as data continues to be written to IS31FL3298 (Figure 6).

READING OPERATION

Most of the registers can be read.

To read the register, after I2C start condition, the bus master must send the IS31FL3298 device address with the R/$\overline{W}$ bit set to "0", followed by the register address which determines which register is accessed. Then restart I2C, the bus master should send the IS31FL3298 device address with the R/$\overline{W}$ bit set to "1". Data from the register defined by the command byte is then sent from the IS31FL3298 to the master (Figure 7).

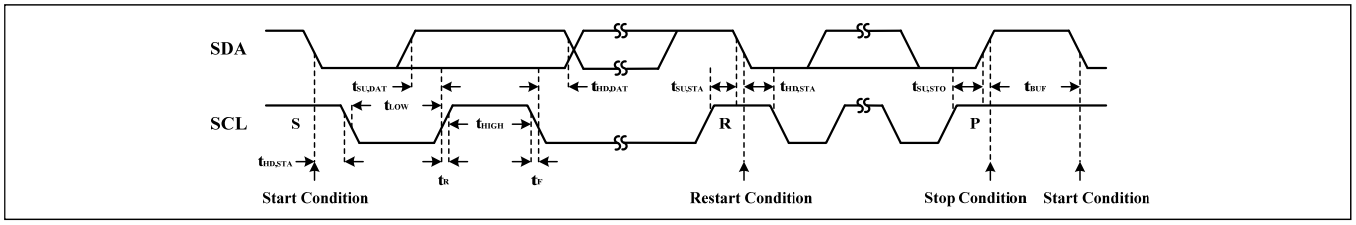


Figure 3 I2C Interface Timing

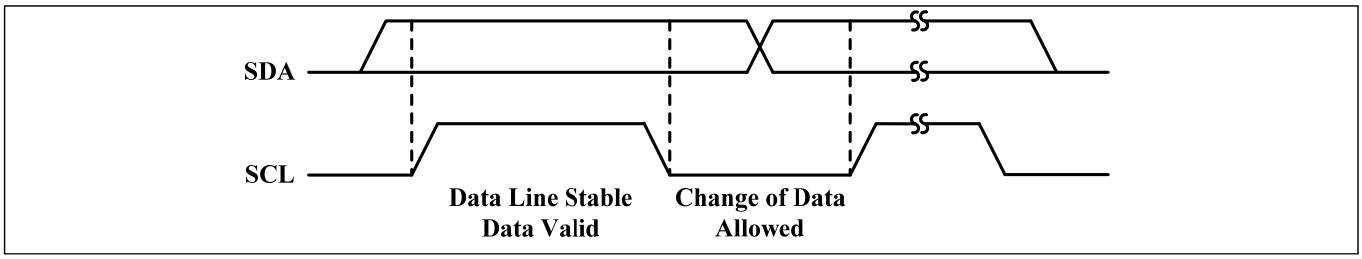


Figure 4 I2C Bit Transfer

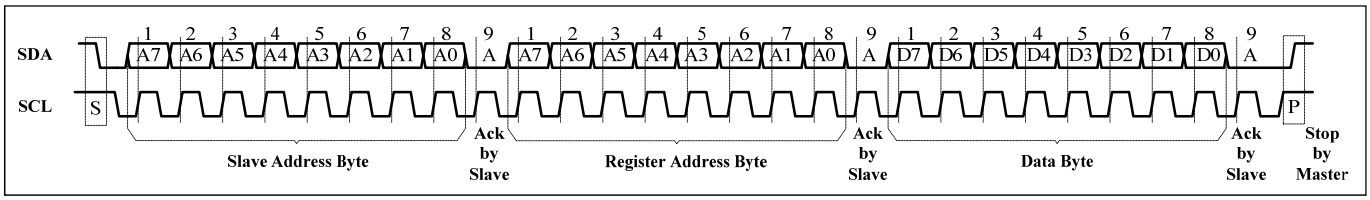


Figure 5 I2C Writing to IS31FL3298 (Typical)

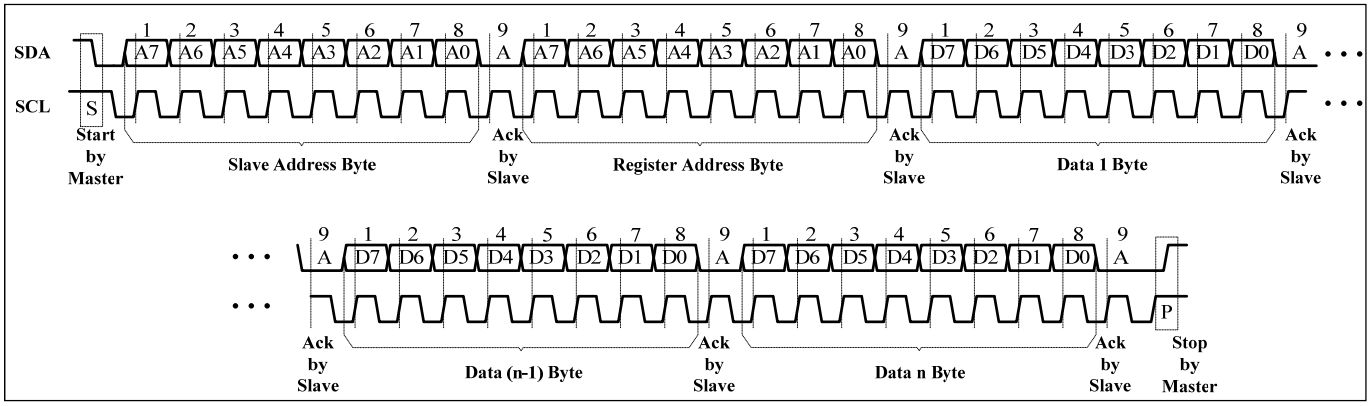


Figure 6 I2C Writing to IS31FL3298 (Automatic Address Increment)

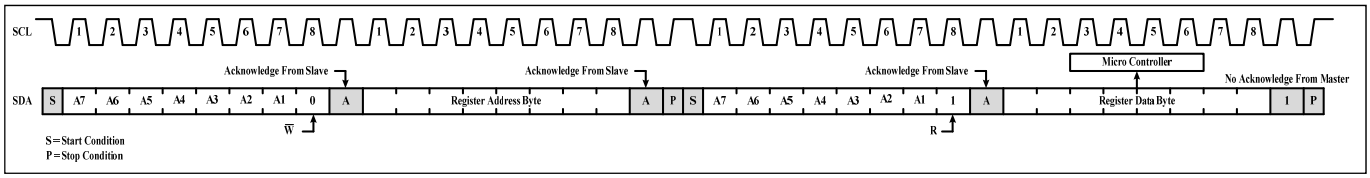


Figure 7 I2C Reading from IS31FL3298

Table 2 Registers Definitions

Address	Name	Function	R/W	Table	Default
00h	Product ID	For read only, read result is Slave address	R	-	-
01h	Shutdown Control Register	Set power down mode and outputs shutdown control	R/W	3	0010 0000
02h	Output Enable Register 1	Enable output 1~6	R/W	4	0111 0111
03h	Output Enable Register 2	Enable output 7~9	R/W	5	0000 0111
04h	Operation Configure Register 1	Set output 1~3 operation mode	R/W	6	0000 0000
05h	Operation Configure Register 2	Set output 4~6 operation mode	R/W	7	0000 0000
06h	Operation Configure Register 3	Set output 7~9 operation mode	R/W	8	0000 0000
07h	Global Current Control Register	Set global current	R/W	9	00111111
08h	Hold Function Register	Set the hold function of each Output	R/W	10	0000 0000
09h	Breathing Mark Function Register	Set the breathing mark time point	R/W	11	0000 0000
0Ah	Charge Pump Setting Register-1	Set change pump parameters	R/W	12	0000 0000
0Bh	Charge Pump Setting Register-2	Set change pump parameters	R/W	13	0011 0000
0Ch	Adjust Register	Adjust the PWM Frequency	R/W	14	0000 0000
0Dh~0Fh	Pattern State Register	For reading the pattern running state	R	15	0000 0000
10h~18h	OUT1~OUT9 Current Level Register	Output current level data register	R/W	16	0000 0000
10h~18h	Color 1 Setting Register of Pattern	Output current level data register-Color 1	R/W	17	0000 0000
20h~28h	Color 2 Setting Register of Pattern	Output current level data register-Color 2	R/W		0000 0000
30h~38h	Color 3 Setting Register of Pattern	Output current level data register-Color 3	R/W		0000 0000
19/29/39h	Pattern TS &T1 Setting Register	Set the TS~T1 time	R/W	18	0000 0000
1A/2A/3Ah	Pattern T2 &T3 Setting Register	Set the T2~T3 time	R/W	19	0000 0000
1B/2B/3Bh	Pattern TP &T4 Setting Register	Set the TP~T4 time	R/W	20	0000 0000
1C/2C/3Ch	Pattern Color Enable Register	Set the color enable/disable	R/W	21	0000 0001
1D/2D/3Dh	Pattern Color Cycle Times Register	Set color repeat time	R/W	22	0000 0000
1E/2E/3Eh	Pattern Register	Set next step and Gamma of each pattern	R/W	23	0000 0001
1F/2F/3Fh	Pattern Loop Times Register	Set the loop time of Pattern	R/W	24	0000 0000
40h~51h	PWM Register	Set PWM data	R/W	25	0000 0000
52h	Color Update Register	Update color data	W	-	0000 0000
53h	PWM Update Register	Update PWM data	W	-	0000 0000
54/55/56h	Pattern Update Register	Update the time data and start to run pattern	W	-	0000 0000
58h	Open Short Detect Enable Register	Open short detect enable	R/W	26	0000 0000
59h/5Ah/5Bh	LED Open Short Status Register	Open short information	R	27	0000 0000
6Fh	Reset Register	Reset the registers value to default	W	-	0000 0000

Table 3 01h Shutdown Control Register

Bit	D7	D6	D5	D4	D3:D2	D1	D0
Name	LCB	-	-	-	PFS	SLE	SSD
Default	0	-	1	0	00	0	0

The Shutdown Control Register sets software shutdown and sleep modes of IS31FL3298.

When LCB bits are set to "0", the I_{OUT} is 10mA when GCC=0x3F. When LCB bit is set to "1", the I_{OUT} is 5mA when GCC=0x3F.

The PFS bit sets the PWM resolution. PWM mode can operate at 220Hz (12-bit), 440Hz (12-bit) and 24kHz (8+4-bit mode).

When SLE bits are set to "1", IS31FL3298 puts itself in Sleep Mode if all OUTx outputs are off for >40s. All OUTx are off without any bias. I_SLEEP= 1μA (Typ.). When the IS31FL3298 in the sleep mode, the SLE bit need to set as "0", that the IS31FL3298 will wake up and disable the sleep mode.

LCB Low Current Bit

0 Default 10mA (GCC=0x3F, CL=0xFF)

1 5mA (GCC=0x3F, CL=0xFF)

PFS PWM Frequency Select

00 12bit at 220Hz (Force 220Hz in Pattern Mode or RGB)

01 12bit at 440Hz

1x 8+4bit mode at 24kHz

SLE Sleep Mode Enable

0 Sleep mode disable

1 Sleep mode enable (40s after no current)

SSD Software Shutdown Enable

0 Software shutdown mode

1 Normal operation

Table 4 02h Output Enable Register 1

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	-	EN6	EN5	EN4	-	EN3	EN2	EN1
Default	0	1	1	1	0	1	1	1

Table 5 03h Output Enable Register 2

Bit	D7:D6	D5:D4	D3	D2	D1	D0
Name	GPO	INTO	VINT	EN9	EN8	EN7
Default	00	00	0	1	1	1

The Output Enable Register enables/disables the outputs independently. The ENx is only effective when SSD= "1".

ENx Output Enable Control

0 Output disable

1 Output enable

GPO Output of GPO pin

10 Output low

11 Output high

0x Output hi-z

INTO Output of INT pin

00 INT pin output for interrupt function (pull to VDD by 100kΩ when VINT=1, depend on 09h)

01 INT pin output for interrupt function (pull to VDD by 100kΩ when VINT=1, depend on 58h)

10 Output low

11 Output hi-z (pull to VDD by 100kΩ when VINT=1)

VINT INT pin Pull high EN

0 Disable, INT pin is no pull, need external pull-up

1 Enable, INT pin is pull to VDD by 100kΩ
It is better if it can pull to SDB voltage

Table 6 04h Operating Configure Register 1

Bit	D7	D6	D5:D4	D3:D2	D1:D0
Name	-	RGB	MOD3	MOD2	MOD1
Default	0	0	00	00	00

Table 7 05h Operating Configure Register 2

Bit	D7:D6	D5:D4	D3:D2	D1:D0
Name	-	MOD6	MOD5	MOD4
Default	00	00	00	00

Table 8 06h Operating Configure Register 3

Bit	D7:D6	D5:D4	D3:D2	D1:D0
Name	-	MOD9	MOD8	MOD7
Default	00	00	00	00

The MODx (x=1~9) bits set output operation modes of IS31FL3298.

When RGB= "1", RGB Mode enables, OUT1~OUT9 running in RGB Mode, the MODx (x=1~9) bits are invalid. When RGB= "0", OUT1~OUT9 are controlled by the MODx (x=1~9) bits.

RGB	Enable RGB Mode
0	Disable
1	Enable

MODx	OUT1~OUT9 LED Mode
00	PWM Mode
01	Pattern Mode
1x	Current Level Mode

When the OUTx works in PWM Mode, means the output current is controlled by PWM Registers (40h~51h) together with Current Level Register (10h~18h).

When the OUTx works in Pattern Mode, means the output current is controlled by Color Setting Registers of Pattern (10h~18h/20h~28h/30h~38h) in.

When the OUTx works in Current Level Mode, means the output current is controlled by Current Level Register (10h~18h), the PWM Registers are invalid (40h~51h).

Table 9 07h Global Current Control Register

Bit	D7	D6:D0
Name	-	GCC
Default	0	011 1111

The Global Current Control Register modulates all OUTx (x=1~9) DC current which is noted as I_{OUT} in 128 steps

I_{OUT} is computed by as shown in Formula (1).

$$I_{OUT} = 20mA \times \frac{GCC}{128} \times \frac{CL}{256} \quad (1)$$

$$GCC = \sum_{n=0}^{6} D[n] \times 2^n \quad (2)$$

$$CL = \sum_{n=0}^{7} D[n] \times 2^n \quad (3)$$

Where D[n] stands for the individual bit value, 1 or 0, in location n. GCC is the value of 07h, CL is the value of 10h~18h.

If GCC=0x3F, CL=0xFF, I_{OUT}=10mA

If GCC=0x7F, CL=0xFF, I_{OUT}=$I_{OUT(MAX)}$=20mA

Table 10 08h Hold Function Register

Bit	D7:D6	D5	D4	D3	D2	D1	D0
Name	-	HFE3	HTS3	HFE2	HTS2	HFE1	HTS1
Default	00	0	0	0	0	0	0

The Hold Function Register configures hold time for each output in Pattern Mode.

HTS	Hold Time Selection
0	Hold at end of T4 when loop done (always off)
1	Hold at end of T2 when loop done (always on)

HFE	Hold Function Enable
0	hold function disable
1	hold function enable

Table 11 09h Breathing Mark Function Register

Bit	D7:D6	D5:D4	D3:D2	D1:D0
Name	-	PAMF	CMF	TMP
Default	00	00	00	00

The PAMF selects the pattern, CMF selects the Color and TMP selects the T1-T4 to have interruption.

Note 8: When only one color is enabled in the Pattern Color Enable Register (1C/2C/3Ch = 0x01, 0x02, or 0x04), the TMP bits can be set to "00" or "1x".

PAMF	Pattern mark (INT pull low) Function
00	Pattern 1
01	Pattern 2
10	Pattern 3

CMF	Pattern mark (INT pull low) Function
00	Color 1
01	Color 2
10	Color 3

TMP	Time point (INT pull low)
00	Start of T2
01	Start of TP
1x	Start of T4

Table 12 0Ah Charge Pump Setting Register-1

Bit	D7:D3	D2	D1:D0
Name	CPDE5:CPDE1	CPPM	CPM
Default	00000	0	00

The Charge Pump Setting Register-1 sets the charge pump working mode.

CPPM	Charge Pump Power up Mode
0	1x mode
1	1.5x mode

CPM	Charge Pump Working Mode
00	Auto mode
01	1x mode
10	1.5x mode

Table 13 0Bh Charge Pump Setting Register-2

Bit	D7	D6:D4	D3:D0
Name	-	HRT	CPDE9:CPDE6
Default	0	011	0000

The Charge Pump Setting Register-2 sets headroom detect threshold voltage and enables OUTx charge pump detection. Disable charge pump detection on OUTx if LED anode not connected to VOUT or OUTx floating.

CPDEx	Charge Pump Detection Enable of OUTx
0	Enable
1	Disable

HRT	Headroom Threshold Voltage
000	V_{OUT}-75mV
001	V_{OUT}-100mV
010	V_{OUT}-125mV
011	V_{OUT}-150mV (Default)
100	V_{OUT}-175mV
101	V_{OUT}-200mV
110	V_{OUT}-225mV
111	V_{OUT}-250mV

Table 14 0Ch Adjust Register

Bit	D7:D3	D2:D0
Name	-	PFA
Default	0000 0	000

The PFA bits adjust the PWM Frequency. When the base PWM Frequency is 24kHz (the PFS bit in 01h register as “1x”), the change ratio as below. If the base PWM Frequency is 220Hz/440Hz (the PFS bit in 01h register as “00/01”), the change ratio will have a small variation.

PFA	PWM Frequency Adjust
000	0%
001	+18.9%
010	+32.17%
011	+47.57%
100	-47.06%
101	-39.86%
110	-26.86%
111	-11.07%

Table 15 0Dh~0Fh Pattern State Register (Read Only)

Bit	D7:D0
Name	Pattern State
Default	0000 0000

The Pattern State Register stores the pattern status.

0Dh register is used for pattern 1, 0Eh for pattern 2, similarly 0Fh for pattern 3.

Below table shows the pattern running state.

Note 9: These reading results are only applicable for the condition: the color 1, color 2 and color 3 in one pattern are all enabled (1C/2C/3Ch = 0x07).

Read Result	D7:D0	Pattern State	Color	Time
0x90	1001 0000	Running	-	TS
0x91	1001 0001	Running	Color1	T1
0x92	1001 0010	Running	Color1	T2
0x93	1001 0011	Running	Color1	T3
0xA4	1010 0100	Running	Color1	TP
0xA1	1010 0001	Running	Color2	T1
0xA2	1010 0010	Running	Color2	T2
0xA3	1010 0011	Running	Color2	T3
0xC4	1100 0100	Running	Color2	TP
0xC1	1100 0001	Running	Color3	T1
0xC2	1100 0010	Running	Color3	T2
0xC3	1100 0011	Running	Color3	T3
0x94	1001 0100	Running	Color3	TP
0x95	1001 0101	Running	-	T4
0x00	0000 0000	Not running	-	-

Table 16 10h~18h OUT1~OUT9 Current Level Register

Bit	D7:D0
Name	CL
Default	0000 0000

The output current may be computed using the Formula (1):

$$I_{OUT} = 20mA \times \frac{GCC}{128} \times \frac{CL}{256} \qquad (1)$$

$$CL = \sum_{n=0}^{7} D[n] \times 2^n \qquad (3)$$

$$I_{LED} = 20mA \times \frac{GCC}{128} \times \frac{CL}{256} \times \frac{PWM}{N} \quad (4)$$

Where D[n] stands for the individual bit value, 1 or 0, in location n, PWM is the value of 40h~51h, I_{OUT} is the peak current of the outputs. I_{LED} is the average current of the outputs.

When IS31FL3298 operates in Current Level Mode, PWM = 4096.

When IS31FL3298 operates in PWM Mode, the value of CL and PWM will decide the output current together.

When IS31FL3298 operates in Pattern Mode, PWM changes to make the auto breathing effect.

For example: in Current Level mode only, GCC=63, if D7:D0 = 10110101,

I_{OUT} = 20mA × 63/128 × (2^7 +2^5 +2^4 +2^2 +2^0)/256

Table 17-1 10h~18h Color 1 Setting Register of Pattern (OUT1~OUT9)

Bit	D7:D0
Name	COL1_Oy
Default	0000 0000

Table 17-2 20h~28h Color 2 Setting Register of Pattern (OUT1~OUT9)

Bit	D7:D0
Name	COL2_Oy
Default	0000 0000

Table 17-3 30h~38h Color 3 Setting Register of Pattern (OUT1~OUT9)

Bit	D7:D0
Name	COL3_Oy
Default	0000 0000

Color Setting Registers store the color setting for each output in Pattern Mode. Check Pattern Color Setting section for more information about the color setting registers.

When IS31FL3298 operates in Pattern Mode, the value of Color Registers will decide the output current of each output in 256 levels.

The output current may be computed using the Formula (5):

$$I_{OUT} = 20mA \times \frac{GCC}{128} \times \frac{COLx\_Oy}{256} \quad (5)$$

$$COLx_{Oy} = \sum_{n=0}^{7} D[n] \times 2^n \quad (6)$$

Where D[n] stands for the individual bit value, 1 or 0, in location n.

For example: GCC=63, if D7:D0 = 10110101,

I_{OUT} = 20mA× 63/128 × (2^7 +2^5 +2^4 +2^2 +2^0)/256

I_{OUT} is the peak current of the outputs.

Need to write Color Update Register (52h) to update the data.

Table 18 19/29/39h Pattern TS &T1 Setting Register

Bit	D7:D3	D4:D0
Name	T1	TS
Default	0000	0000

The TS & T1 Setting Registers set the TS and T1 time in Pattern Mode. 19h register is used for pattern 1, 29h for pattern 2, similarly 39h for pattern 3.

TS	Pattern Start Time Selection
0000	0.04s
0001	0.16s
0010	0.31s
0011	0.46s
0100	0.61s
0101	0.92s
0110	1.25s
0111	1.92s
1000	2.52s
1001	3.12s
1010	3.72s
1011	5.04s
1100	6.24s
1101	7.44s
1110	8.76s
1111	9.96s

T1	Rise Time Selection
0000	0.04s
0001	0.16s
0010	0.31s
0011	0.46s
0100	0.61s
0101	0.92s
0110	1.25s
0111	1.92s
1000	2.52s
1001	3.12s
1010	3.72s
1011	5.04s
1100	6.24s
1101	7.44s
1110	8.76s
1111	9.96s

Table 19 1A/2A/3Ah Pattern T2 &T3 Setting Register

Bit	D7:D3	D4:D0
Name	T3	T2
Default	0000	0000

The T2 & T3 Setting Registers set the T2 and T3 time in Pattern Mode. 1Ah register is used for pattern 1, 2Ah for pattern 2, similarly 3Ah for pattern 3.

T2 Hold Time Selection

0000	0.04s
0001	0.16s
0010	0.31s
0011	0.46s
0100	0.61s
0101	0.92s
0110	1.25s
0111	1.92s
1000	2.52s
1001	3.12s
1010	3.72s
1011	5.04s
1100	6.24s
1101	7.44s
1110	8.76s
1111	9.96s

T3 Fall Time Selection

0000	0.04s
0001	0.16s
0010	0.31s
0011	0.46s
0100	0.61s
0101	0.92s
0110	1.25s
0111	1.92s
1000	2.52s
1001	3.12s
1010	3.72s
1011	5.04s
1100	6.24s
1101	7.44s
1110	8.76s
1111	9.96s

Table 20 1B/2B/3Bh Pattern TP &T4 Setting Register

Bit	D7:D4	D3:D0
Name	T4	TP
Default	0000	0000

The TP & T4 Setting Registers set the TP and T4 time in Pattern Mode. 1Bh register is used for pattern 1, 2Bh for pattern 2, similarly 3Bh for pattern 3.

TP Time between Pulses

0000	0.04s
0001	0.16s
0010	0.31s
0011	0.46s
0100	0.61s
0101	0.92s
0110	1.25s
0111	1.92s
1000	2.52s
1001	3.12s
1010	3.72s
1011	5.04s
1100	6.24s
1101	7.44s
1110	8.76s
1111	9.96s

T4 Off Time Selection

0000	0.04s
0001	0.16s
0010	0.31s
0011	0.46s
0100	0.61s
0101	0.92s
0110	1.25s
0111	1.92s
1000	2.52s
1001	3.12s
1010	3.72s
1011	5.04s
1100	6.24s
1101	7.44s
1110	8.76s
1111	9.96s

Table 21 1C/2C/3Ch Pattern Color Enable Register

Bit	D7:D3	D2	D1	D0
Name	-	CE3	CE2	CE1
Default	00000	0	0	1

Color Enable Register enables the color function for each color in Pattern Mode. 1Ch register is used for pattern 1, 2Ch for pattern 2, similarly 3Ch for pattern 3.

CEx Color Enable Selection

0 Color x disable

1 Color x enable

Table 22 1D/2D/3Dh Pattern Color Cycle Times Register

Bit	D7:D6	D5:D4	D3:D2	D1:D0
Name	-	CCT3	CCT2	CCT1
Default	00	00	00	00

Pattern Color Cycle Times Register sets Color loop times for each color. 1Dh register is used for pattern 1, 2Dh for pattern 2, similarly 3Dh for pattern 3.

CCTx Color Cycle Times Selection

00 Endless

01 1 time

10 2 times

11 3 times

Table 23-1 1Eh Pattern Register

Bit	D7:D4	D3	D2	D1:D0
Name	MTPLT1	GAM1	-	NXT1
Default	0000	0	0	01

GAM controls the gamma of pattern. MTPLT controls the loop of Pattern.

GAM1 Gamma Selection

0 Gamma=2.4

1 Linearity

MTPLT1 Multi-Pulse Loop Time

0000 endless

0001 1 time

…

1111 15 times

NXT1 Pattern 1 Next

01 Go to Pattern 2 (Only effective in RGB mode)

00/10/11 Just stop

Table 23-2 2Eh Pattern Register

Bit	D7:D4	D3	D2	D1:D0
Name	MTPLT2	GAM2	-	NXT2
Default	0000	0	0	01

GAM controls the gamma of pattern. MTPLT controls the loop of Pattern.

GAM2 Gamma Selection

0 Gamma=2.4

1 Linearity

MTPLT2 Multi-Pulse Loop Time

0000 endless

0001 1 time

…

1111 15 times

NXT2 Pattern 2 Next

01 Go to Pattern 1 (Only effective in RGB mode)

10 Go to Pattern 3 (Only effective in RGB mode)

00/11 Just stop

Table 23-3 3Eh Pattern Register

Bit	D7:D4	D3	D2	D1:D0
Name	MTPLT3	GAM3	-	NXT3
Default	0000	0	0	01

GAM controls the gamma of pattern. MTPLT controls the loop of Pattern.

GAM3 Gamma Selection

0 Gamma=2.4

1 Linearity

MTPLT3 Multi-Pulse Loop Time

0000 endless

0001 1 time

…

1111 15 times

NXT3	Pattern 3 Next
01	Go to Pattern 1 (Only effective in RGB mode)
10	Go to Pattern 2 (Only effective in RGB mode)
00/11	Just stop

Table 24 1F/2F/3Fh Pattern Loop Times Register

Bit	D7	D6:D0
Name	PLTx_H	PLTx_L
Default	0	000 0000

Pattern loop Times register sets the loop time of the pattern. 1Fh register is used for pattern 1, 2Fh for pattern 2, similarly 3Fh for pattern 3.

If PLT_H(D7)=0, PLT_L!=0

Pattern loop times:

$$Looptime = \sum_{n=0}^{6} D[n] \times 2^n \quad (7)$$

If PLT_H(D7)=0, PLT_L=0, endless

If PLT_H(D7)=1, PLT_L!=0

Pattern loop times:

$$Looptime = 16 \times \sum_{n=0}^{6} D[n] \times 2^n \quad (8)$$

If PLT_H(D7)=1, PLT_L=0, endless.

Table 25 40h~51h PWM Register

Reg	41h (43h, 45h)		40h (42h, 44h)
Bit	D7:D4	D3:D0	D7:D0
Name	-	PWM_H	PWM_L
Default	0000	0000	0000 0000

The PWM Registers (40h~51h) modulate LED brightness of each channel.

When IS31FL3298 operates only in PWM & Current Level Mode, each output has 2 bytes to modulate the PWM duty in 4096 steps, in Pattern Mode, the PWM cannot be accessed.

Each dot has 2 bytes to modulate the PWM duty in 4096 steps.

The value of the PWM Registers decide the average current of each LED noted I_{LED}.

I_{LED} computed by Formula (4):

$$I_{LED} = 20mA \times \frac{GCC}{128} \times \frac{CL}{256} \times \frac{PWM}{N} \quad (4)$$

Where I_{OUT} is the peak current of the outputs. I_{LED} is the average current of the outputs.

N=4096:

$$PWM = \sum_{n=0}^{11} D[n] \times 2^n$$

Where D[n] stands for the individual bit value, 1 or 0, in location n.

For example: if PWM_H = 00001001, PWM_L = 10110101, N=4096, GCC=63, CL=255,

I_{LED} = 20mA × 63/128 × (2^{11} +2^8 +2^7 +2^5 +2^4 +2^2 +2^0)/4096

52h Color Update Register

Write “0xC5” to 52h will update the data of 10h~18h/20h~28h/30h~38h.

53h PWM Update Register

Write “0xC5” to 53h will update the data of 40~51h.

54/55/56h Pattern Time Update Register

Write “0xC5” to 54/55/56h will update the data of 19h~1Fh/29h~2Fh/39h~3Fh.

Table 26 58h Open Short Detect Enable Register

Bit	D7	D6	D5	D4	D3:D0
Name	SRE	SDE	ORE	ODE	-
Default	0	0	0	0	0000

ODE enables Open LED detection and stores this open information in LED Open status registers 59h~5Ah.

SDE enables Short LED detection and stores this short information in LED Short status registers 5Ah~5Bh.

The open/short information will continue updating until detection is disabled by writing “0” to ODE/SDE. Writing a “1” to ORE/SRE bit enables reporting of the open/short information on the INT pin. When ORE/SRE is “1”, any detected open/short LED condition on OUT1~OUT9 will cause the INT pin to go logic low.

Note 10: The Open Short LED detection is not available for Current Level Mode. It can be used in PWM Mode or Pattern mode or RGB mode.

ODE	Open Detect Enable
0	Detect disable
1	Detect enable

ORE	Open Report Enable
0	Report disable
1	Report enable

SDE **Short Detect Enable**
0 Detect disable
1 Detect enable

SRE **Short Report Enable**
0 Report disable
1 Report enable

Table 27-1 59h LED Open Status Register 1

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	OP[8]	OP[7]	OP[6]	OP[5]	OP[4]	OP[3]	OP[2]	OP[1]
Default	0	0	0	0	0	0	0	0

Table 27-2 5Ah LED Open Status Register 2

Bit	D7:D5	D4	D3-D1	D0
Name	-	SH[9]	-	OP[9]
Default	000	0	000	0

Open status registers 59h~5Ah are updated when there is an open LED condition and the ODE bit of 58h register was set to "1". Register 59h~5Ah will be cleared upon reading the register.

OPx **Open Information of OUT9:OUT1**
0 No LED open detected
1 LED open detected

Table 27-3 5Bh LED Short Status Register 1

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	SH[8]	SH[7]	SH[6]	SH[5]	SH[4]	SH[3]	SH[2]	SH[1]
Default	0	0	0	0	0	0	0	0

Short status registers 5Ah~5Bh are updated when there is a short LED condition and the SDE bit of 58h register was set to "1". Register 5Ah~5Bh will be cleared upon reading the register.

SHx **Short Information of OUT9:OUT1**
0 No LED short detected
1 LED short detected

6Fh Reset Register

Once user writes "0xC5" to the Reset Register, IS31FL3298 will reset all registers to their default value. On initial power-up, the IS31FL3298 registers are reset to their default values for a blank display.

TYPICAL APPLICATION INFORMATION

GENERAL DESCRIPTION

IS31FL3298 is a 9-channel fun LED driver with auto breathing mode. It has Pattern Mode and Current Level Mode for RGB lighting effects.

CURRENT SETTING

The maximum output current is 20mA. When LCB =”1”, the Iout will become half. The Global Current Control register GCC can be used to set a lower current. The default GCC is 0x3F, the default Iout is 10mA. The 8-bit CL registers (10h~18h) control the individual currents for each of the outputs.

For example, OUT1, OUT2 and OUT3 drive an RGB LED, OUT1 is Red LED, OUT2 is Green LED and OUT 3 is Blue LED. If GCC and CL bits are the same, then the RGB LED may appear slightly pink, or not so white. The CL bits can be used to adjust the IOUTx current so the RGB LED appears closer to a pure white color. We call this CL bit adjustment by another name: white balance register.

PWM FREQUENCY SELECT

The IS31FL3298 output channels operate with a default 12-bit PWM resolution and the PWM frequency of 220Hz. Because all the OUTx channels are synchronized, the DC power supply will experience large instantaneous current surges when the OUTx channels turn ON. These current surges will generate an AC ripple on the power supply which cause stress to the decoupling capacitors. When the AC ripple is applied to a monolithic ceramic capacitor chip (MLCC) it will expand and contract causing the PCB to flex and generate audible hum in the range of between 20Hz to 20kHz, to avoid this hum, there are many countermeasures, such as selecting the capacitor type and value which will not cause the PCB to flex and contract.

An additional option for avoiding audible hum is to set the IS31FL3298’s output PWM frequency above the audible frequency range. The Shutdown Control Register (01h) can be used to set the switching frequency to 220Hz/440Hz/24KHz. Combination settings of the PFS bits will result in different PWM frequency, select a value higher than 20kHz to avoid the audible frequency range.

PWM CONTROL

The PWM Registers (40h~51h) can modulate LED brightness of each channel with 4096 steps. For example, if the data in PWM_H Register is “0000 0000” and in PWM_L Register is “0000 0100”, then the PWM is 4/4096.

Writing new data continuously to the registers can modulate the brightness of the LEDs to achieve a breathing effect.

CURRENT LEVEL MODE

The Current Level Registers (10h~18h) are active and can modulate LED peak current IOUT of each output with 256 steps independently. For example, if the data in Current Lever Register is “0000 0100”, then the current level is the fourth step, with a current level of 4/256.

In Current Level Mode, user doesn’t need to turn on the CEx of 1Ch, a new value must be written to the Current Level registers to change the output current. Writing new data continuously to the registers can modulate the brightness of the LEDs to achieve breathing, blinking, or any other effects that the user defines.

In Current Level Mode, the output current (OUT1~OUT9) is configured by the Current Level Register (10h~18h).

PWM MODE

PWM Mode is the combination of PWM and Current Level. In this mode, the Current Level Registers (10h~18h) adjust the peak current (I_{OUT}) of the outputs, the PWM Registers (40h~51h) adjust the duty cycle of the output current, the finial result is the output average current I_{LED}.

Table 28 Register of PWM & Current Level Mode

Mode	Register	OUT1	OUT2	OUT3
PWM & Current Level	PWM_H	41h	43h	45h
	PWM_L	40h	42h	44h
	CL	10h	11h	12h
	Register	OUT4	OUT5	OUT6
	PWM_H	47h	49h	4Bh
	PWM_L	46h	48h	4Ah
	CL	13h	14h	15h
	Register	OUT7	OUT8	OUT9
	PWM_H	4Dh	4Fh	51h
	PWM_L	4Ch	4Eh	50h
	CL	16h	17h	18h

RGB MODE

By setting the RGB bits of the Operating Configure Register 1 (04h) to “1”, the IS31FL3298 will operate in RGB mode. In this mode 9 channels (3 groups RGB) can be modulated breathing cycle independently by TS~TP (Figure 11). Setting different TS~T4 can achieve RGB breathing with auto color changing. OUT1~OUT9 running in Pattern 1 to Pattern 3. The maximum intensity of each RGB can be adjusted independently by the Color Setting Registers (10h~18h/20h~28h/30h~38h) (Table 29).

Note 11: If IS31FL3298 operates in the RGB mode and then enters into the sleep mode, the SLE bit needs to set as “0”, that the IS31FL3298 will wake up and disable the sleep mode.

Table 29 Color Register of RGB Mode

Pattern Mode	Color Enable	OUT1	OUT2	…	OUT9
Pattern 1	CE1(1Ch)	10h	11h	…	18h
	CE2(1Ch)	20h	21h	…	28h
	CE3(1Ch)	30h	31h	…	38h
Pattern 2	CE1(2Ch)	10h	11h	…	18h
	CE2(2Ch)	20h	21h	…	28h
	CE3(2Ch)	30h	31h	…	38h
Pattern 3	CE1(3Ch)	10h	11h	…	18h
	CE2(3Ch)	20h	21h	…	28h
	CE3(3Ch)	30h	31h	…	38h

PATTERN MODE

By setting the MOD1~MOD9 bits of the Operating Configure Register (04h/05h/06h) to “01”, the corresponding output will operate in Pattern Mode. In Pattern Mode, the timing characteristics for output current - current rising (T1), holding (T2), falling (T3) and off time (TS, TP, T4) (Figure 10), can be adjusted individually so that each output can independently maintain a pre-established pattern achieving mixing color breathing or a single-color breathing without requiring any additional interface activity, thus saving valuable system resources. OUT1~OUT3 running in Pattern 1, OUT4~OUT6 running in Pattern 2, and OUT7~OUT9 running in Pattern 3.

PATTERN COLOR SETTING

In Pattern Mode, the LED color is defined by COLx_Oy (x, y= 1, 2, 3) bits in Color Setting Registers (10h~18h/20h~28h/30h~38h). There are 3 RGB current combinations to generate 3 pre-defined colors for display. More than one of the 3 pre-defined colors can be chosen by setting CEx bits in Color Enable Register (1Ch/2Ch/3Ch). When CEx is set, the color x is allowed to be displayed in current pattern.

In Pattern Mode, the output current (OUT1~OUT9) is configured by the Color Setting Register of Pattern as Table 30.

Table 30 Color Register of Pattern Mode

Pattern Mode	Color Enable	OUT1	OUT2	OUT3
Pattern 1	CE1(1Ch)	10h	11h	12h
	CE2(1Ch)	20h	21h	22h
	CE3(1Ch)	30h	31h	32h
Pattern Mode	Color Enable	OUT4	OUT5	OUT6
Pattern 2	CE1(2Ch)	13h	14h	15h
	CE2(2Ch)	23h	24h	25h
	CE3(2Ch)	33h	34h	35h
Pattern Mode	Color Enable	OUT7	OUT8	OUT9
Pattern 3	CE1(3Ch)	16h	17h	18h
	CE2(3Ch)	26h	27h	28h
	CE3(3Ch)	36h	37h	38h

PATTERN TIME SETTING

User should configure the related pattern time setting registers according to actual timing requirements via I2C interface before starting pattern. The pattern time includes TS, T1~T4 and TP. And the pattern has three continue lighting cycle as Color 1~Color 3. Please check the LED OPERATING MODE section for more about the time setting.

OPEN/SHORT DETECT FUNCTION

IS31FL3298 has open and short detect bit for each LED. By setting the ODE/SDE bit of Open/short Detect Enable Register 58h from “0” to “1”, the LED Open/Short Register will store the open/short information immediately the MCU can get the open/short information by reading the 59h~5Ah and 5Ah~5Bh. The open/short information will continue updating until detection is disabled by writing “0” to ODE/SDE. When the INTO bit is “01” and VINT bit is “1” in the Output Enable Register (03h), writing a “1” to ORE/SRE bit enables reporting of the open/short information on the INT pin. When ORE/SRE is “1”, any detected open/short LED condition on OUT1~OUT9 will cause the INT pin to go logic low.

The Open Short LED detection is not available for Current Level Mode. It can be used in PWM Mode or Pattern mode or RGB mode.

GAMMA CORRECTION

In order to perform a better visual LED breathing effect, the device integrates gamma correction to the Pattern Mode. The gamma correction causes the change in intensity to appear more linear to the human eye.

Gamma correction, also known as gamma compression or encoding, is used to encode linear luminance to match the non-linear characteristics of display. Since the IS31FL3298 can modulate the brightness of the LEDs with 256 steps, a gamma correction function can be applied when computing each subsequent LED intensity setting such that the changes in brightness matches the human eye's brightness curve.

The IS31FL3298 provides three gamma corrections which can be set by GAM bits of Pattern Registers (1Eh/2Eh/3Eh) for each pattern. The gamma correction is shown as below.

BREATHING MARK FUNCTION

In RGB mode or pattern mode, by setting the INTO bit to “00” and VINT bit to “1” in the Output Enable Register (03h), the breathing mark function is enabled. INT is an output pin. The breathing mark function is useful as a signal to notify the MCU when and where the pattern or color is running.

Note 12: When only one color is enabled in Pattern Color Enable Register (1C/2C/3Ch = 0x01 or 0x02 or 0x04), the TMP bit can set as “00” and “1x”.

After selecting the PAMF (Pattern Mark Function) and CMF (Color Mark Function),

When you choose start of T2 (TMP= 00): At the start time T2, INT will induce a falling edge and hold logic low, at the end of time period T2, INT will induce a rising edge.

When you choose start of TP (TMP= 01): At the start time TP, INT will induce a falling edge and hold logic low, at the end of time period TP, INT will induce a rising edge.

When you choose start of T4 (TMP= 1x): At the start time T4, INT will induce a falling edge and hold logic low, at the end of time period T4, INT will induce a rising edge.

The VINT bit of 03h sets the pull up of the INT pin, when VINT= “0”, the INT is open drain and it needs external pull up resistor.

When VINT= “1”, the INT is pulled to internal VCC by 100kΩ.

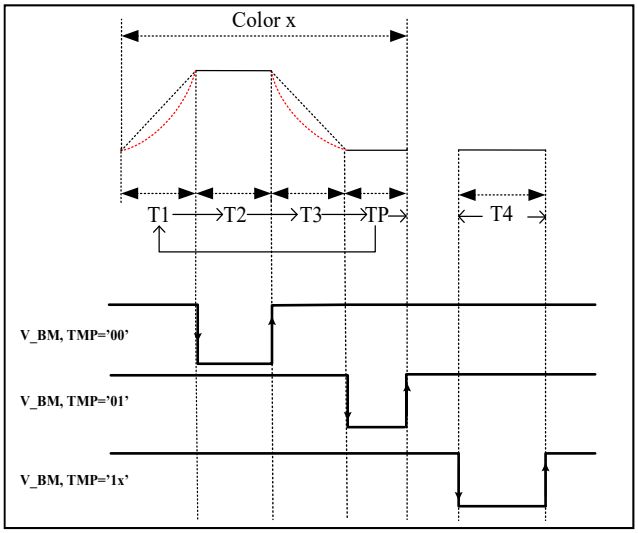


Figure 8 Breathing Mark Function

SHUTDOWN MODE

Shutdown mode can either be used as a means of reducing power consumption or generating a flashing display (repeatedly entering and leaving shutdown mode). During shutdown mode all registers retain their data.

Software Shutdown

By setting SSD bit of the Shutdown Register (01h) to “0”, the IS31FL3298 will operate in software shutdown mode, wherein it will consume only 0.5μA (Typ.) current. When the IS31FL3298 is in software shutdown mode, all current sources are switched off.

Hardware Shutdown

The chip enters hardware shutdown mode when the SDB pin is pulled low, wherein they consume only 0.5μA (Typ.) current. When set SDB high, the rising edge will reset the I2C module, but the register information retains.

LED OPERATING MODE

The IS31FL3298 has three operating modes which can be chosen by the MODx bits of Operating Configure Register (04h/05h/06h).

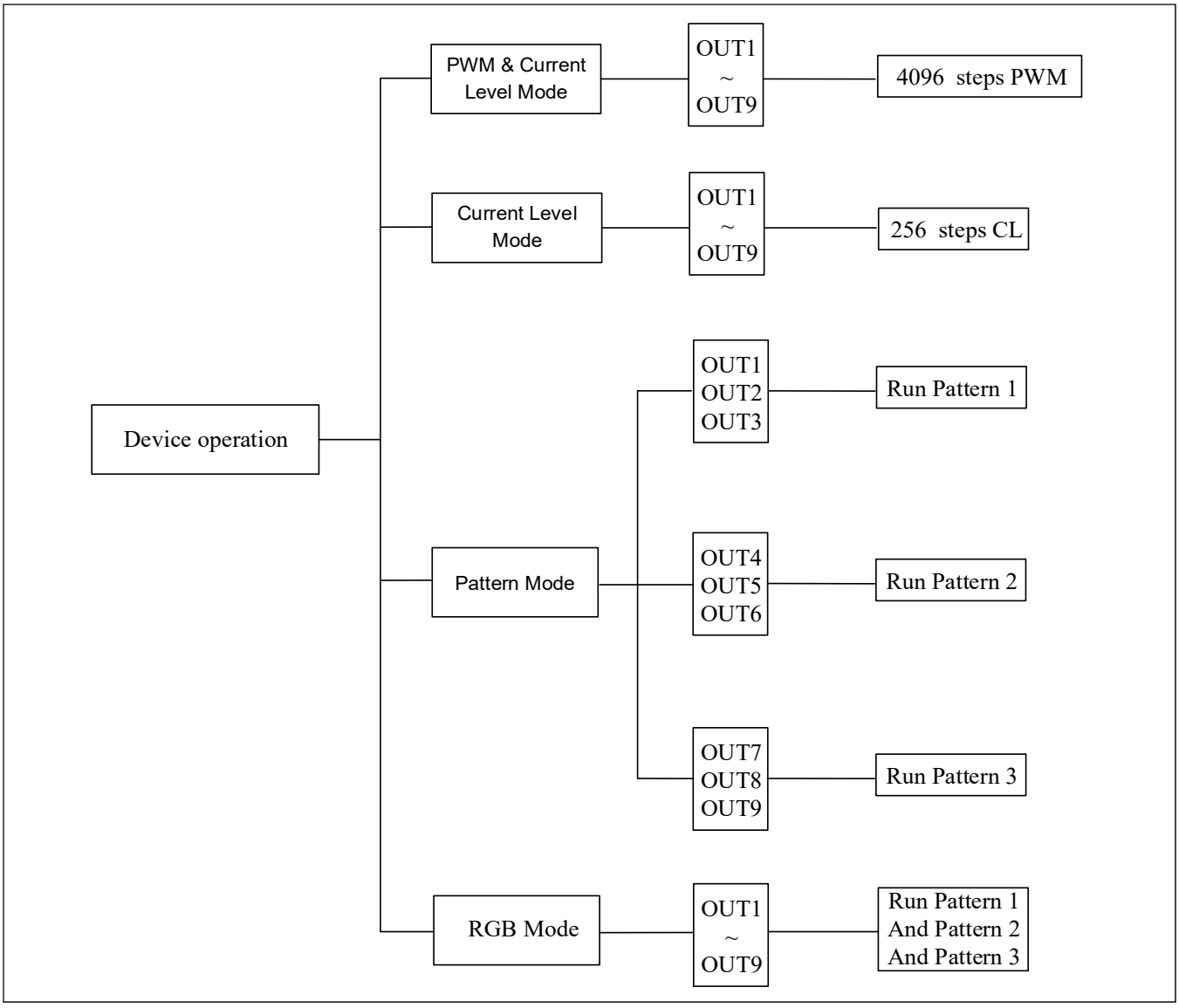


Figure 9 Operating Mode Map

Pattern Mode

If MODx=01 (Pattern Mode), OUT1~OUT3 can operate in Pattern Mode only and run the pattern 1, OUT4~OUT6 run the pattern 2, OUT7~OUT9 run the pattern 3.

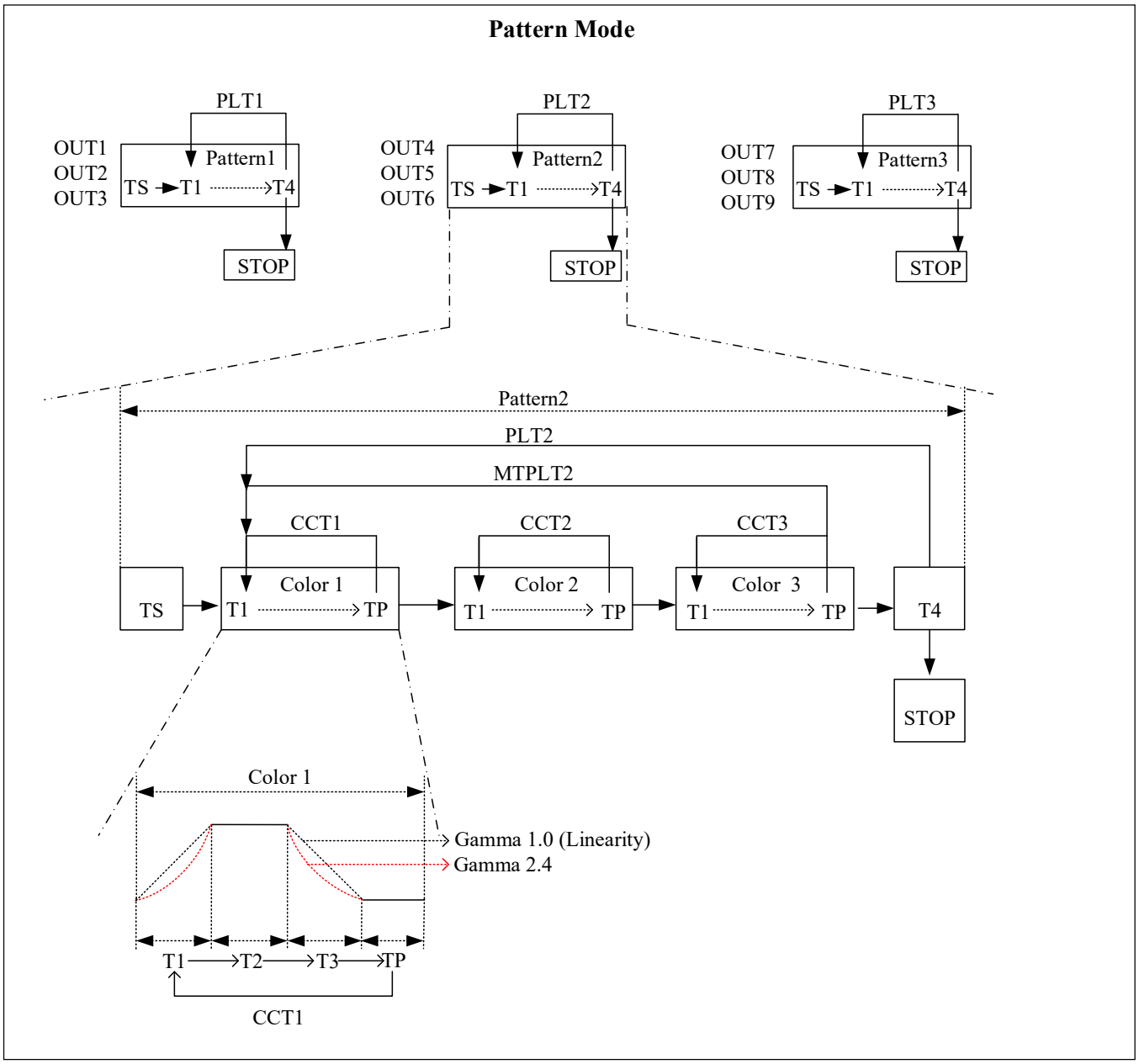


Figure 10 Pattern Mode

RGB Mode

If RGB=1 (RGB Mode), OUT1~OUT9 can operate in Pattern Mode only and run pattern 1, pattern 2 and pattern 3.

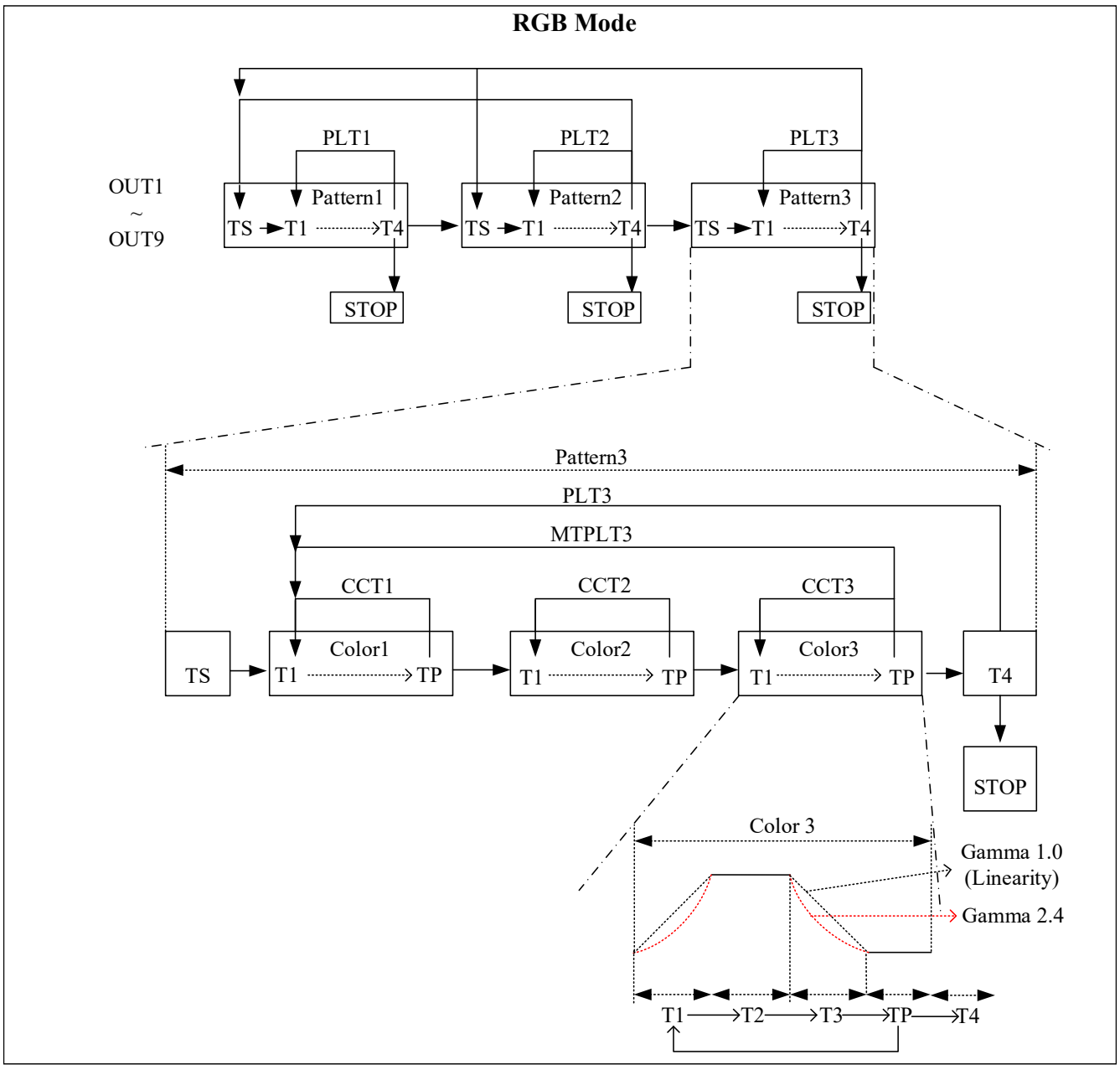


Figure 11 RGB Mode

CLASSIFICATION REFLOW PROFILES

Profile Feature	Pb-Free Assembly
Preheat & Soak Temperature min (Tsmin) Temperature max (Tsmax) Time (Tsmin to Tsmax) (ts)	150°C 200°C 60-120 seconds
Average ramp-up rate (Tsmax to Tp)	3°C/second max.
Liquidous temperature (TL) Time at liquidous (tL)	217°C 60-150 seconds
Peak package body temperature (Tp)*	Max 260°C
Time (tp)** within 5°C of the specified classification temperature (Tc)	Max 30 seconds
Average ramp-down rate (Tp to Tsmax)	6°C/second max.
Time 25°C to peak temperature	8 minutes max.

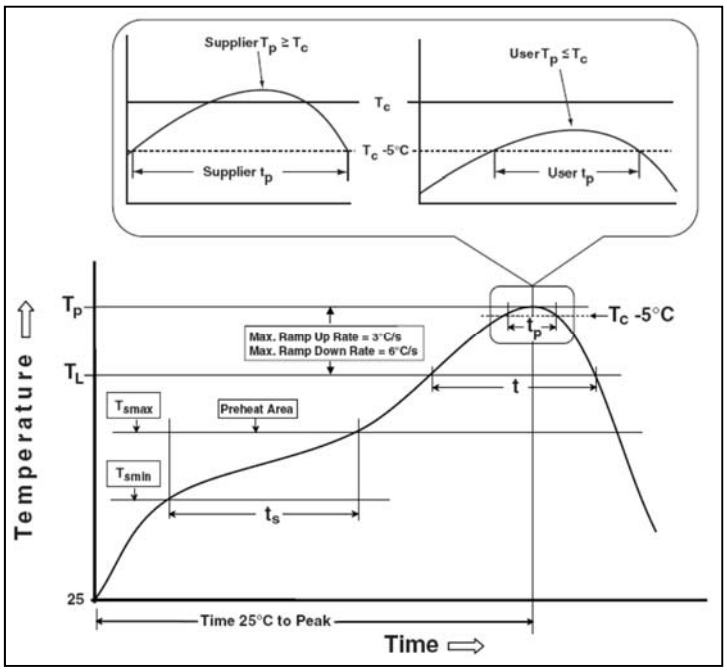
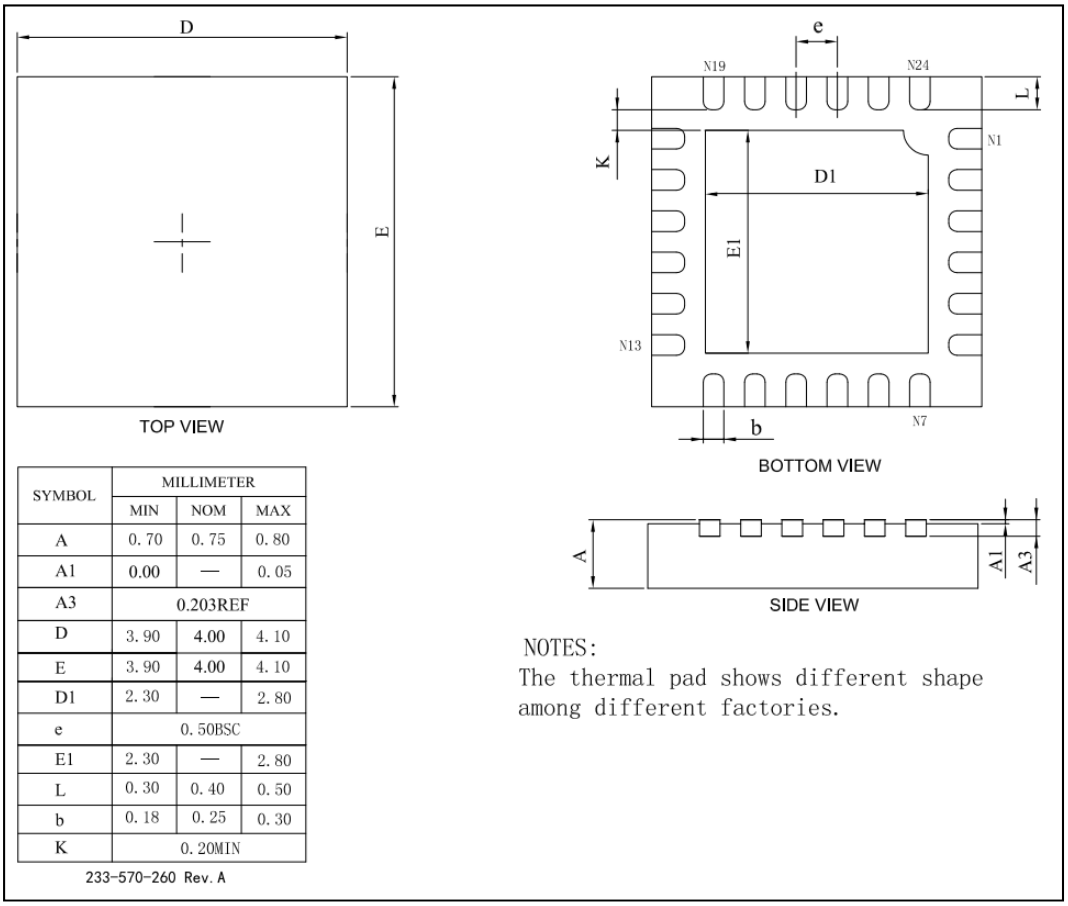


Figure 12 Classification Profile

PACKAGE INFORMATION

QFN-24



SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	0.70	0.75	0.80
A1	0.00	—	0.05
A3	0.203REF		
D	3.90	4.00	4.10
E	3.90	4.00	4.10
D1	2.30	—	2.80
e	0.50BSC		
E1	2.30	—	2.80
L	0.30	0.40	0.50
b	0.18	0.25	0.30
K	0.20MIN		

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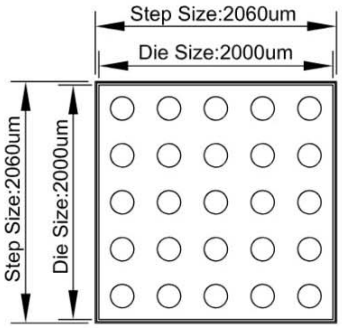
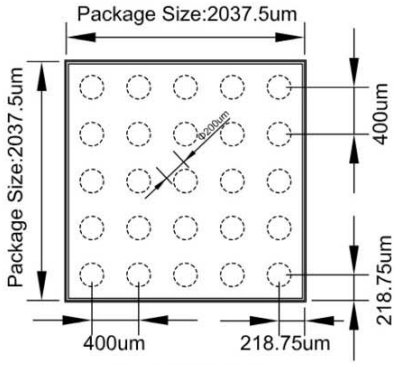
NOTES:
The thermal pad shows different shape among different factories.

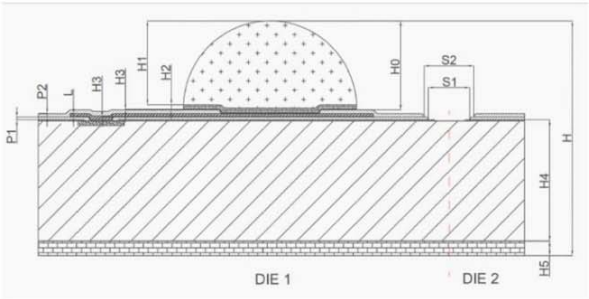
WLCSP-25



TOP VIEW(BALL SIDE)



BOTTOM VIEW



CROSS SECTION

SYMBOL	ITEM	DATA(UM)
H0	BALL HEIGHT	63±6.3
H1	SNAG HEIGHT	55
H2	CU UBM THICKNESS	8
H3	TI/CU SEED LAYER THICKNESS	1000Å/4000Å
H4	SI THICKNESS	323±10
H5	DRY FILM THICKNESS	25±3
P1	PI 1 THICKNESS	7±2
P2	PI 2 THICKNESS	7±2
L	RDL THICKNESS	7±2
S1	PI1 OPENING ON SL AREA	80*80
S2	PI2 OPENING ON SL AREA	90*90
H	PACKAGE HEIGHT	425±23.3

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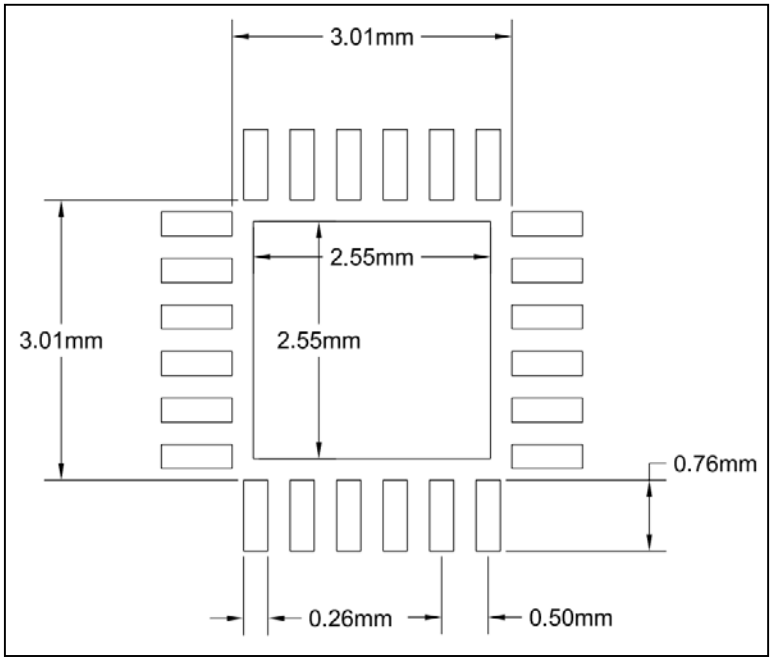
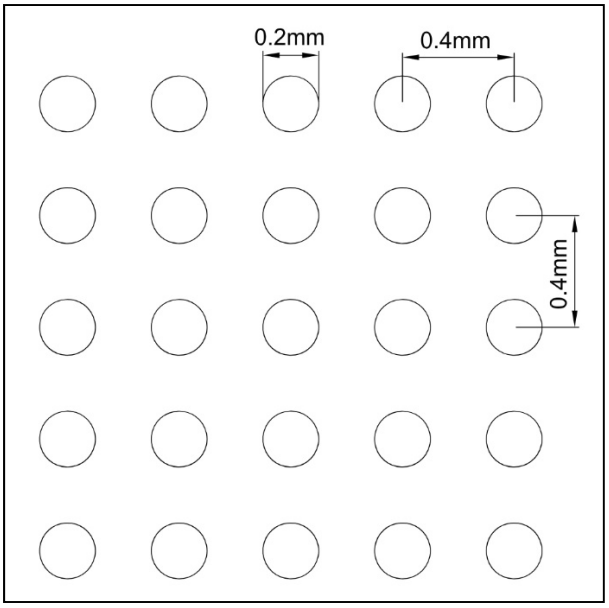
RECOMMENDED LAND PATTERN

QFN-24



WLCSP-25



Note:

1. Land pattern complies to IPC-7351.
2. All dimensions in MM.
3. This document (including dimensions, notes & specs) is a recommendation based on typical circuit board manufacturing parameters. Since land pattern design depends on many factors unknown (eg. User's board manufacturing specs), user must determine suitability for use.

REVISION HISTORY

Revision	Detail Information	Date
0A	Initial release	2023.09.08
A	Released to mass production	2024.01.22
B	Add WLCSP-25 package and add note 8 for Table 11 and note 9 for Table 15	2024.04.28
C	Updated Part No for WLCSP-25 Package	2024.05.17