IS31FL3751

9×8 MATRIX LED DRIVER

April 2021

GENERAL DESCRIPTION

The IS31FL3751 is a general purpose 9×8 LED Matrix programmed via 1MHz I2C compatible interface. Each LED can be dimmed individually with 12-bit PWM data and each LED can be dimmed with 4-bit DC scaling (Color Calibration) data which allowing 4096 steps of linear PWM dimming and 16 steps of DC current level adjustment.

Additionally each LED open and short state can be detected, IS31FL3751 store the open or short information in Open-Short Registers. The Open-Short Registers allowing MCU to read out via I2C compatible interface. Inform MCU whether there are LEDs open or short and the locations of open or short LEDs.

The IS31FL3751 operates from 2.7V to 5.5V and features a very low operational current.

IS31FL3751 is available in QFN-20 (4mm×4mm) package. It operates from 2.7V to 5.5V over the temperature range of -40°C to +125°C.

FEATURES

- Supply voltage range: 2.7V to 5.5V
- Support 9×8 matrix configurations
- Ultra-low operational current 550μA (Typ.), 700μA (Max.)
- Accurate color rendition
  - 2-bit global current adjustment (1/4~4/4)
  - 4-bit current adjust for each dot (1/16~16/16)
  - 12-bit/8-bit PWM for each dot
- programmable patterns (256 gamma corrected auto dimming)
- 1MHz I2C-compatible interface
- Individual open and short detect function
- Synchronization for multi-device application
- 180 degree phase delay operation to reduce power noise
- Spread spectrum
- 4% (Max.) at 20mA bit to bit matching
- 4% (Max.) at 20mA device to device matching
- De-ghost
- QFN-20 (4mm×4mm) package

APPLICATIONS

- Hand-held devices for LED display
- Wireless gaming device (Mouse, Mouse MAT etc.)
- IOT device (AI speaker etc.)

TYPICAL APPLICATION CIRCUIT

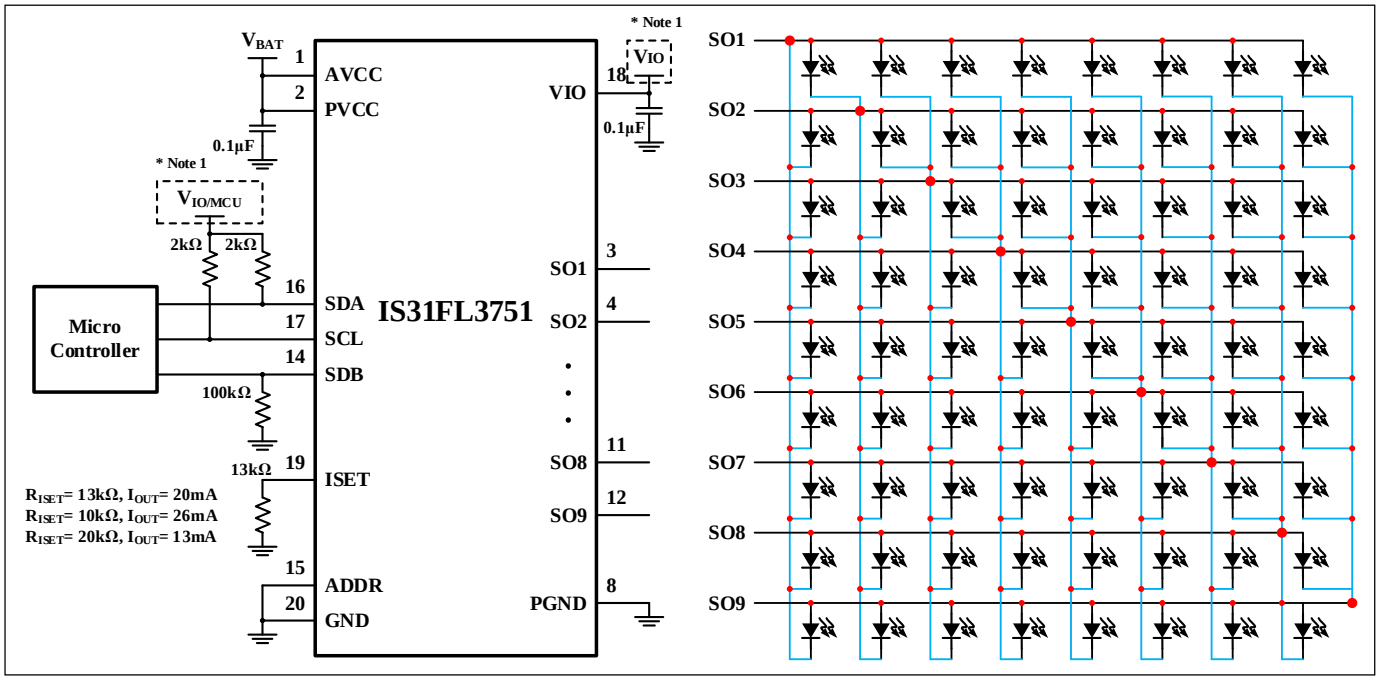


Figure 1 Typical Application Circuit: 72 Mono Color LEDs

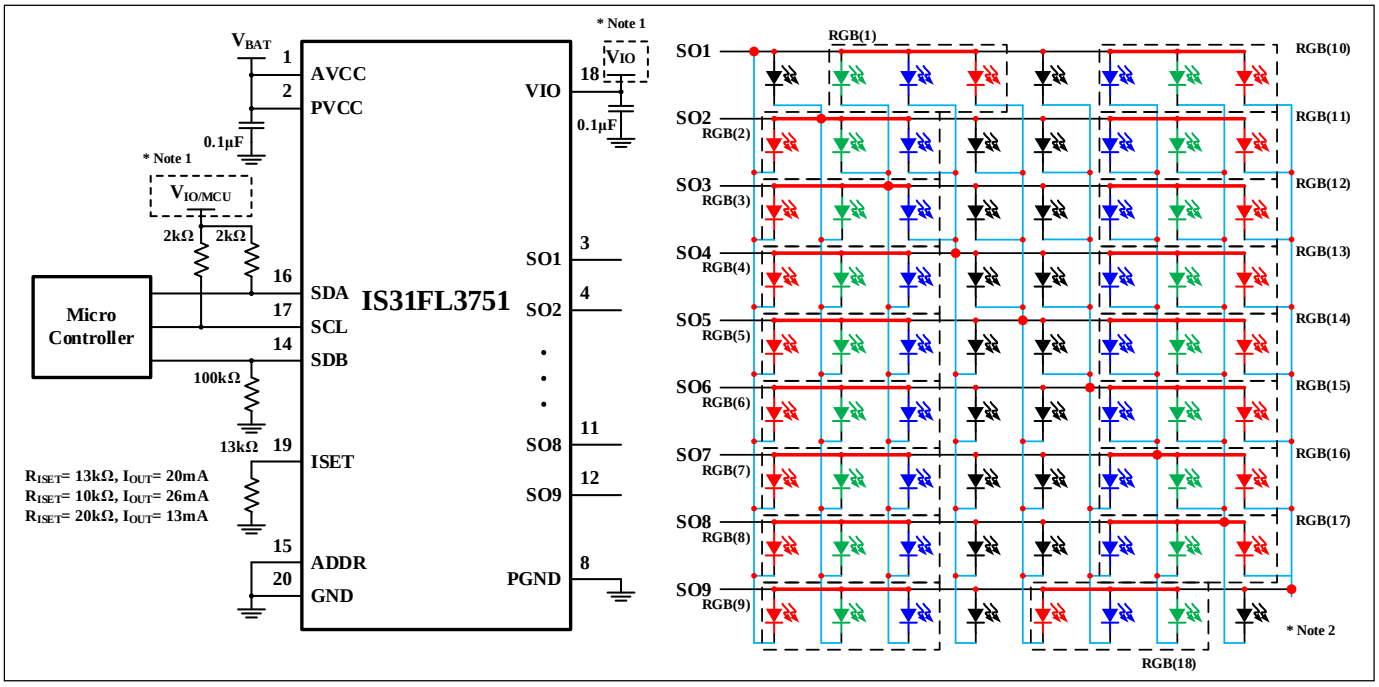
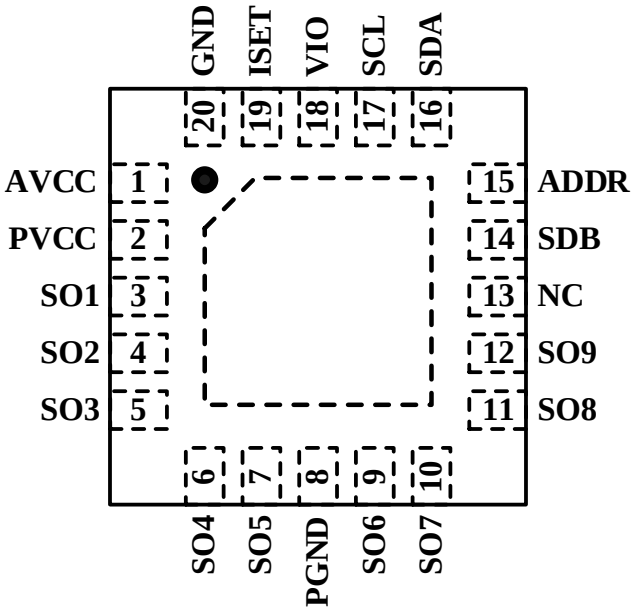


Figure 2 Typical Application Circuit: 18 RGB LEDs

Note 1: The V_{IH} of I2C bus should be same as VIO pin. VIO pin need to connect to a reference voltage and usually it is same as the VCC of MCU. If VCC of MCU is 1.8V, V_{IO}=1.8V, if V_{CC} of MCU is 5V, V_{IO}=5V.

Note 2: The black position can be white/blue/green LED, whose forward voltage is not much lower than blue and green LED.

PIN CONFIGURATION

Package	Pin Configuration (Top View)
QFN-20	

PIN DESCRIPTION

No.	Pin	Description
1	AVCC	Power for current source SW and analog.
2	PVCC	Power supply.
3~7, 9~12	SO1~SO9	Current sink/Power SW.
8	PGND	Power ground.
13	NC	NC.
14	SDB	Shutdown pin.
15	ADDR	I2C address setting pin
16	SDA	I2C compatible serial data.
17	SCL	I2C compatible serial clock.
18	VIO	VIH reference for SDA, SCL SDB and AD pin.
19	ISET	Output current set pin
20	GND	Ground.
	Thermal Pad	Connect to GND.

ORDERING INFORMATION

Industrial Range: -40°C to +125°C

Order Part No.	Package	QTY/Reel
IS31FL3751-QFLS4-TR	QFN-20, Lead-free	2500

ABSOLUTE MAXIMUM RATINGS

Supply voltage, V_{CC}	-0.3V ~+6.0V
Voltage at any input pin	-0.3V ~ V_{CC}+0.3V
Maximum junction temperature, T_{JMAX}	+150°C
Storage temperature range, T_{STG}	-65°C ~+150°C
Operating temperature range, T_A=T_J	-40°C ~ +125°C
Package thermal resistance, junction to ambient (4 layer standard test PCB based on JESD 51-2A), θ_{JA}	50.2°C/W
ESD (HBM) ESD (CDM)	±8kV ±750V

Note 3: Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other condition beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

The following specifications apply for V_{CC}= 3.6V, T_A= 25°C, unless otherwise noted.

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
V_{CC}	Supply voltage		2.7		5.5	V
I_{CC}	Quiescent power supply current	V_{SDB}= V_{CC}, all LEDs off, 9×8 mode, OSC=8MHz, R_{ISET}=13kΩ (I_{OUT}=20mA), 12-bit PWM mode, GCC= "00", SL= 15, PWM= 0		0.55	0.7	mA
		V_{SDB}= V_{CC}, all LEDs off, 1×8 mode, OSC=1MHz, R_{ISET}=13kΩ (I_{OUT}=20mA), 12-bit PWM mode, GCC= "00", SL= 15, PWM= 0		0.27	0.35	mA
I_{SD}	Shutdown current	V_{SDB}= 0V		0.5	1	μA
		V_{SDB}= V_{CC}, Configuration Register written "0000 0000		0.5	1	
I_{OUT}	Peak sink current of SOx	V_{SDB}= V_{CC}, all LEDs off, 9×8 mode, OSC= 8MHz, R_{ISET}= 8.2kΩ (I_{OUT}= 31mA), 12-bit PWM mode, GCC= "00", SL= 15, PWM= 0xFFF		31		mA
		V_{SDB}= V_{CC}, all LEDs off, 9×8 mode, OSC=8MHz, R_{ISET}=13kΩ (I_{OUT}= 20mA), 12-bit PWM mode, GCC= "00", SL= 15, PWM= 0xFFF	18.8	20	21.2	mA
ΔI_{MAT}	Sink current between channels	I_{OUT}= 20mA	-4		4	%
ΔI_{ACC}	Sink current Between device to device	I_{OUT}= 20mA	-4		4	%
I_{LED}	Average current on each LED I_{LED}= $I_{OUT(PEAK)}$/Duty (Duty =1/9.18)	V_{SDB}= V_{CC}, all LEDs off, 9×8 mode, OSC=8MHz, R_{ISET}=13kΩ (I_{OUT}= 20mA), 12-bit PWM mode, GCC= "00", SL= 15, PWM= 0xFFF		2.18		mA
V_{HR}	Output current headroom voltage of SOx	I_{SWITCH}= 160mA		250	350	mV
	Constant sink current headroom voltage of SOx	I_{OUT}= 20mA		250	400	

ELECTRICAL CHARACTERISTICS (CONTINUE)

The following specifications apply for V_{CC}= 3.6V, T_A= 25°C, unless otherwise noted.

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
t_{SCAN}	Period of scanning	PFS= “000” (8MHz), 12-bit PWM mode	430	460	480	μs
t_{NOL1}	Non-overlap blanking time during scan, the SOx are all off during this time	PFS= “000” (8MHz), 12-bit PWM mode	7	9	11	μs
t_{NOL2}	Total delay time from SO2 to SO9 (Note 5)	PFS= “000” (8MHz), 12-bit PWM mode (Note 4)		0.337		μs
V_{OD}	OUTx pin open detect threshold	V_{CC}= 3.6V, I_{OUT}≥ 1mA, PWM> 6%, measured at SOx	0.21			V
V_{SD}	LED short detect threshold	V_{CC}= 3.6V, I_{OUT}≥1mA, PWM>6%, measured at (V_{CC}-V_{OUTx})			1.2	V
Logic Electrical Characteristics (VIO, SDA, SCL, SDB, AD)						
V_{IO}	VIH reference for SDA, SCL SDB and AD pin	V_{CC}= 2.7V~5.5V, f_{SCL}≤ 400kHz	1.6		V_{CC}	V
		V_{CC}= 2.7V~5.5V, f_{SCL}≤ 1MHz	1.8		V_{CC}	
V_{IL}	Logic “0” input voltage	V_{CC}= 2.7V~5.5V, V_{IO}= 1.6~1.8V	GND		0.1V_{IO}	V
		V_{CC}= 2.7V~5.5V, V_{IO}≥ 1.8V	GND		0.2V_{IO}	
V_{IH}	Logic “1” input voltage	V_{CC}= 2.7V~5.5V, V_{IO}= 1.6~1.8V	0.9V_{IO}		V_{IO}	V
		V_{CC}= 2.7V~5.5V, V_{IO}≥ 1.8V	0.8V_{IO}		V_{IO}	
V_{HYS}	Input Schmitt trigger hysteresis		0.5			V
I_{IL}	Logic “0” input current	V_{INPUT}= 0V (Note 4)		5		nA
I_{IH}	Logic “1” input current	V_{INPUT} = V_{CC} (Note 4)		5		nA

DIGITAL INPUT I2C SWITCHING CHARACTERISTICS (NOTE 4)

Symbol	Parameter	Fast Mode			Fast Mode Plus			Units
		Min.	Typ.	Max.	Min.	Typ.	Max.	
f_{SCL}	Serial-clock frequency	-		400	-		1000	kHz
t_{BUF}	Bus free time between a STOP and a START condition	1.3		-	0.5		-	μs
$t_{HD, STA}$	Hold time (repeated) START condition	0.6		-	0.26		-	μs
$t_{SU, STA}$	Repeated START condition setup time	0.6		-	0.26		-	μs
$t_{SU, STO}$	STOP condition setup time	0.6		-	0.26		-	μs
$t_{HD, DAT}$	Data hold time	-		-	-		-	μs
$t_{SU, DAT}$	Data setup time	100		-	50		-	ns
t_{LOW}	SCL clock low period	1.3		-	0.5		-	μs
t_{HIGH}	SCL clock high period	0.7		-	0.26		-	μs
t_R	Rise time of both SDA and SCL signals, receiving	-		300	-		120	ns
t_F	Fall time of both SDA and SCL signals, receiving	-		300	-		120	ns

Note 4: Guaranteed by design.

Note 5: When matrix size is 9x8, only one of SOx will work as power source, and others work as constant current sinks. t_{NOL2} is the delay time of those 8 current sinks. For example, when SO1 is power source, SO2 and SO3 will turn on immediately, SO4 and SO5 will turn on follow the time of $t_{NOL2}/3$, about 0.112μs, SO6 and SO7 will delay another 0.112us, SO8 and SO9 will delay another 0.112us, total delay time from SO2 to SO9 is t_{NOL2}.

DETAILED DESCRIPTION

I2C INTERFACE

The IS31FL3751 uses a serial bus, which conforms to the I2C protocol, to control the chip's functions with two wires: SCL and SDA. The IS31FL3751 has a 7-bit slave address (A7:A1), followed by the R/W bit, A0. Set A0 to "0" for a write command and set A0 to "1" for a read command. The value of bits A1 and A2 are decided by the connection of the ADDR pin. The complete slave address is:

Table 1 Slave Address

Bit	A7:A3	A2:A1	A0
Value	10111	ADDR	0

ADDR connected to GND, ADDR = 00;

ADDR connected to VCC, ADDR = 11;

ADDR connected to SCL, ADDR = 01;

ADDR connected to SDA, ADDR = 10;

The SCL line is uni-directional. The SDA line is bi-directional (open-drain) with a pull-up resistor (typically 2kΩ). The maximum clock frequency specified by the I2C standard is 1MHz. In this discussion, the master is the microcontroller and the slave is the IS31FL3751.

The timing diagram for the I2C is shown in Figure 3. The SDA is latched in on the stable high level of the SCL. When there is no interface activity, the SDA line should be held high.

The "START" signal is generated by lowering the SDA signal while the SCL signal is high. The start signal will alert all devices attached to the I2C bus to check the incoming address against their own chip address.

The 8-bit chip address is sent next, most significant bit first. Each address bit must be stable while the SCL level is high.

After the last bit of the chip address is sent, the master checks for the IS31FL3751's acknowledge. The master releases the SDA line high (through a pull-up resistor). Then the master sends an SCL pulse. If the IS31FL3751 has received the address correctly, then it holds the SDA line low during the SCL pulse. If the SDA line is not low, then the master should send a "STOP" signal (discussed later) and abort the transfer.

Following acknowledge of IS31FL3751, the register address byte is sent, most significant bit first. IS31FL3751 must generate another acknowledge indicating that the register address has been received.

Then 8-bit of data byte are sent next, most significant bit first. Each data bit should be valid while the SCL level is stable high. After the data byte is sent, the IS31FL3751 must generate another acknowledge to indicate that the data was received.

The "STOP" signal ends the transfer. To signal "STOP", the SDA signal goes high while the SCL signal is high.

ADDRESS AUTO INCREMENT

To write multiple bytes of data into IS31FL3751, load the address of the data register that the first data byte is intended for. During the IS31FL3751 acknowledge of receiving the data byte, the internal address pointer will increment by one. The next data byte sent to IS31FL3751 will be placed in the new address, and so on. The auto increment of the address will continue as long as data continues to be written to IS31FL3751 (Figure 6).

READING OPERATION

Most of the registers can be read.

To read the registers, after I2C start condition, the bus master must send the IS31FL3751 device address with the R/$\overline{W}$ bit set to "0", followed by the register address, which determines which register is accessed. Then restart I2C, the bus master should send the IS31FL3751 device address with the R/$\overline{W}$ bit set to "1". Data from the register defined by the command byte is then sent from the IS31FL3751 to the master (Figure 7).

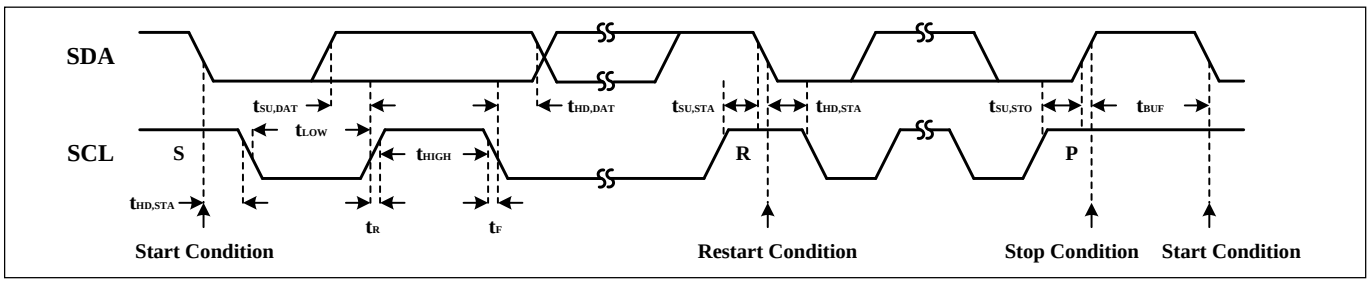


Figure 3 I2C Interface Timing

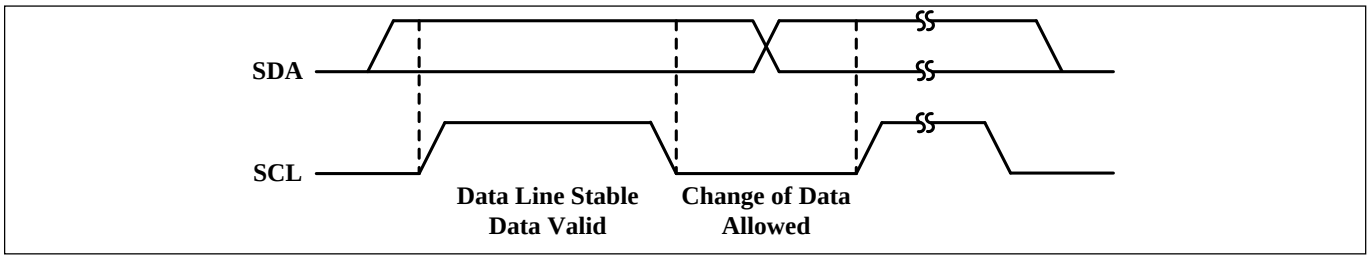


Figure 4 I2C Bit Transfer

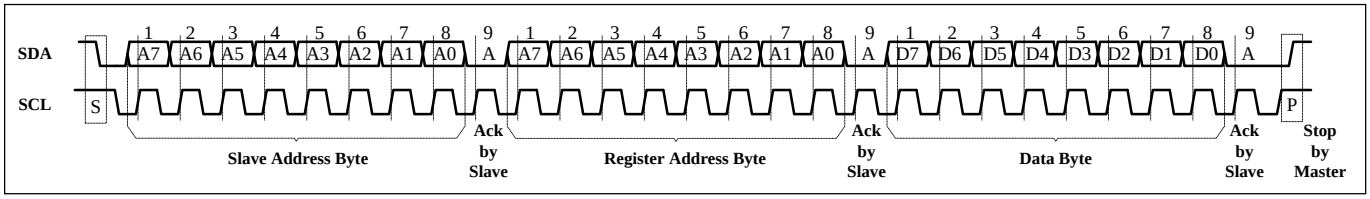


Figure 5 I2C Writing to IS31FL3751 (Typical)

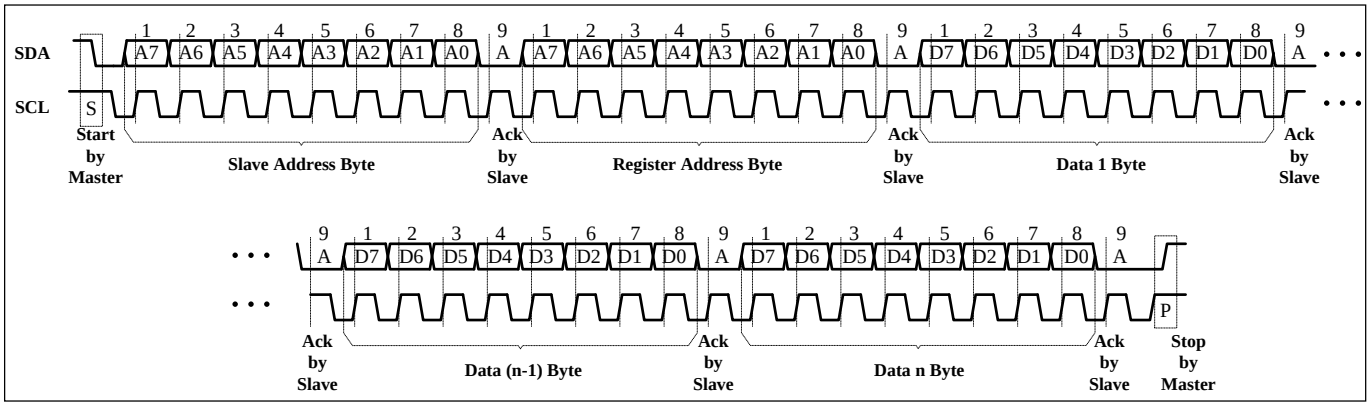


Figure 6 I2C Writing to IS31FL3751 (Automatic Address Increment)

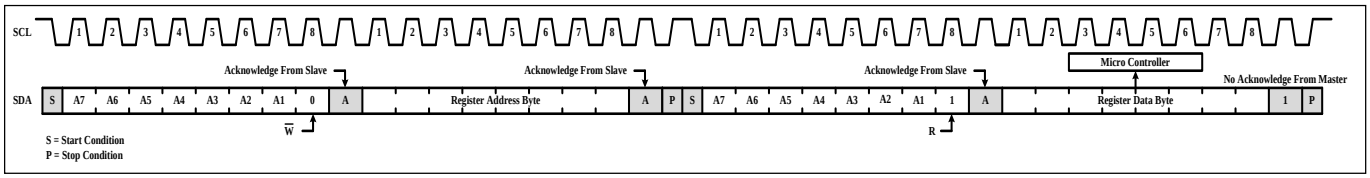


Figure 7 I2C Reading from IS31FL3751

Table 2 Register Definition

Address	Name	Function	Table	R/W	Default
00h~8Fh	PWM Register	Enable/Disable & PWM for each LED	3	W	0000 0000
90h~B3h	Scaling Register	Set Scaling for each LED	5	W	0000 0000
B4h~BCh	ABME Register	Set ABM enable for each LED	7	W	0000 0000
C0h	Configuration Register	Configure the operation mode	8	R/W	0000 0000
C1h	Global Current Control Register	Set the global current	9	R/W	0000 0000
C2h	PWM frequency	Set PWM frequency	10	R/W	0000 0000
C3h	Pull Down/Up Resistor Selection Register	Set the pull down voltage	11	R/W	0000 0000
C4h~C8h	ABM Mode Registers	ABM mode	12~15	R/W	0000 0000
C9h	Spread Spectrum Register	Spread spectrum function enable	16	R/W	0000 0000
CAh~D2h	Open short register	Store the OS information	17	R	0000 0000
EFh	Reset Register	Reset all register to POR state	-	W	0000 0000

Table 3 00h~8Fh PWM Register

	SO1	SO2	SO3	SO4	SO5	SO6	SO7	SO8	SO9
SO1	-	00h~01h	02h~03h	04h~05h	06h~07h	08h~09h	0Ah~0Bh	0Ch~0Dh	0Eh~0Fh
SO2	10h~11h	-	12h~13h	14h~15h	16h~17h	18h~19h	1Ah~1Bh	1Ch~1Dh	1Eh~1Fh
SO3	20h~21h	22h~23h	-	24h~25h	26h~27h	28h~29h	2Ah~2Bh	2Ch~2Dh	2Eh~2Fh
SO4	30h~31h	32h~33h	34h~35h	-	36h~37h	38h~39h	3Ah~3Bh	3Ch~3Dh	3Eh~3Fh
SO5	40h~41h	42h~43h	44h~45h	46h~47h	-	48h~49h	4Ah~4Bh	4Ch~4Dh	4Eh~4Fh
SO6	50h~51h	52h~53h	54h~55h	56h~57h	58h~59h	-	5Ah~5Bh	5Ch~5Dh	5Eh~5Fh
SO7	60h~61h	62h~63h	64h~65h	66h~67h	68h~69h	6Ah~6Bh	-	6Ch~6Dh	6Eh~6Fh
SO8	70h~71h	72h~73h	74h~75h	76h~77h	78h~79h	7Ah~7Bh	7Ch~7Dh	-	7Eh~7Fh
SO9	80h~81h	82h~83h	84h~85h	86h~87h	88h~89h	8Ah~8Bh	8Ch~8Dh	8Eh~8Fh	-

Table 4 00h~8Fh PWM Register

Reg	01h (03h, 05h…)			00h (02h, 04h…)
Bit	D7:D5	D4	D3:D0	D7:D0
Name	-	ENB	PWM_H	PWM_L
Default	000	0	0000	0000 0000

Each dot has a byte to modulate the PWM duty in 4096 or 256 steps.

ENB Dot shutdown bit
0 Normal operation
1 This dot shutdown

PWM_H High bits of PWM Register
PWM_L Low bits of PWM Register

The value of the PWM Registers decides the average current of each LED noted I_{LED}.

I_{LED} computed by Formula (1):

$$I_{LED} = \frac{PWM}{4096} \times I_{OUT(PEAK)} \times Duty \quad \text{(1, 12-bit mode)}$$

$$I_{LED} = \frac{PWM}{256} \times I_{OUT(PEAK)} \times Duty \quad \text{(1, 8-bit mode)}$$

$$PWM = \sum_{n=0}^{11} D[n] \cdot 2^n \quad \text{(1, 12-bit mode)}$$

$$PWM = \sum_{n=0}^{7} D[n] \cdot 2^n \quad \text{(1, 8-bit mode)}$$

Where Duty is the duty cycle of SOx, see SCANING TIMING section for more information.

$$Duty = \frac{460\mu s}{(460+9+0.337)\mu s} \times \frac{1}{9} = \frac{1}{9.18} \quad \text{(2, SWS=1/9)}$$

$$Duty = \frac{460\mu s}{(460+9+0.337)\mu s} \times \frac{1}{8} = \frac{1}{8.16} \quad \text{(2, SWS=1/8)}$$

$$Duty = \frac{460\mu s}{(460+9+0.337)\mu s} \times \frac{1}{7} = \frac{1}{7.14} \quad \text{(2, SWS=1/7)}$$

…

I_{OUT} is the output current of SOx (x=1~9),

$$I_{OUT(PEAK)} = \frac{260}{R_{ISET}} \times GCC \times \frac{SL+1}{16} \quad (3)$$

GCC is the Global Current Control register (C1h, 1/4~4/4) value, SL is the Scaling Register value as Table 5 and R_{ISET} is the external resistor of ISET pin. D[n] stands for the individual bit value, 1 or 0, in location n.

For example: if PWM register D11:D0= “1000 1011 0101” (0x8B5, 2229), SWS= 1/9, R_{ISET}= 13kΩ, GCC= “00”, SL= “1111”:

$$I_{LED} = \frac{260}{13k\Omega} \times \frac{4}{4} \times \frac{15+1}{16} \times \frac{1}{9.18} \times \frac{2229}{4096}$$

Table 5 90h~B3h SL Register

	SO1	SO2	SO3	SO4	SO5	SO6	SO7	SO8	SO9
SO1	-	90L(Note 5)	90H(Note 5)	91L	91H	92L	92H	93L	93H
SO2	94L	-	94H	95L	95H	96L	96H	97L	97H
SO3	98L	98H	-	99L	99H	9AL	9AH	9BL	9BH
SO4	9CL	9CH	9DL	-	9DH	9EL	9EH	9FL	9FH
SO5	A0L	A0H	A1L	A1H	-	A2L	A2H	A3L	A3H
SO6	A4L	A4H	A5L	A5H	A6L	-	A6H	A7L	A7H
SO7	A8L	A8H	A9L	A9H	AAL	AAH	-	ABL	ABH
SO8	ACL	ACH	ADL	ADH	AEL	AEH	AFL	-	AFH
SO9	B0L	B0H	B1L	B1H	B2L	B2H	B3L	B3H	-

Note 5: 90H means high nibble of 90h byte, 90L means low nibble of 90h byte.

Table 6 90h~B3h Scaling Register

Bit	D7:D4	D3:D0
Name	SLH	SLL
Default	0000	0000

Scaling Register (SLx) control the DC output current of each dot. Each dot has a byte to modulate the scaling in 16 steps.

SLx

0000 SL=0, 1/16 DC current
0001 SL=1, 2/16 DC current
0010 SL=2, 3/16 DC current
….

1111 SL=15, 16/16 DC current

The value of the Scaling Register decides the peak current of each LED noted $I_{OUT(PEAK)}$.

$I_{OUT(PEAK)}$ computed by Formula (3):

$$I_{OUT(PEAK)} = \frac{260}{R_{ISET}} \times GCC \times \frac{SL+1}{16} \quad (3)$$

I_{OUT} is the output current of SOx (x=1~9), GCC is the Global Current Control Register (C1h) value and R_{ISET} is the external resistor of ISET pin.

For example: if R_{ISET}=13kΩ, GCC= “00”, SL= “1111”:

$$I_{OUT(PEAK)} = \frac{260}{13k\Omega} \times \frac{4}{4} \times \frac{15+1}{16} = 20mA$$

Table 7 B4h~BCh ABME Register (Auto Breath Mode Enable)

	SO1	SO2	SO3	SO4	SO5	SO6	SO7	SO8	SO9
SO1	-	B4_LSB	B4	B4	B4	B4	B4	B4	B4_MSB
SO2	B5_LSB	-	B5	B5	B5	B5	B5	B5	B5_MSB
SO3	B6_LSB	B6	-	B6	B6	B6	B6	B6	B6_MSB
SO4	B7_LSB	B7	B7	-	B7	B7	B7	B7	B7_MSB
SO5	B8_LSB	B8	B8	B8	-	B8	B8	B8	B8_MSB
SO6	B9_LSB	B9	B9	B9	B9	-	B9	B9	B9_MSB
SO7	BA_LSB	BA	BA	BA	BA	BA	-	BA	BA_MSB
SO8	BB_LSB	BB	BB	BB	BB	BB	BB	-	BB_MSB
SO9	BC_LSB	BC	BC	BC	BC	BC	BC	BC_MSB	-

The Auto Breath Mode Register sets operating mode of each dot. When ABME is set to "1", the LED will work at auto breath mode.

ABME Auto Breath Mode enable bit
0 Disable ABM (default)
1 Enable ABM

Table 8 C0h Configuration Register

Bit	D7:D4	D3	D2:D1	D0
Name	SWS	ABM_EN	OSDE	SSD
Default	0000	0	00	0

The Configuration Register sets operating mode of IS31FL3751.

SWS control the duty cycle of the SOx, default mode is "0000", 1/9.

When OSDE set to "01", open detection will be trigger once, the user could trigger open detection again by set OSDE from "00" to "01".

When OSDE set "10", short detection will be trigger once, the user could trigger short detection again by set OSDE from "00" to "10".

ABM_EN is the ABM mode enable for all the LEDs, for each LED's ABM mode, need to set B4h~BCh to enable.

When SSD is "0", IS31FL3751 works in software shutdown mode and to normal operate the SSD bit should set to "1".

SWS SWx Setting
0000 9x8, SWS=1/9
0001 8x7, SWS=1/8, SO9 no-active
0010 7x6, SWS=1/7, SO8~SO9 no-active
0011 6x5, SWS=1/6, SO7~SO9 no-active
0100 5x4, SWS=1/5, SO6~SO9 no-active
1000 1x8, SWS=1/1, SO2~SO9 ch as sink only
Others Not allowed

OSDE Open Short Detection Enable
00 Disable open/short detection
01/11 Enable open detection
10 Enable short detection

ABM_EN ABM mode enable
0 ABM mode disable
1 ABM mode enable

SSD Software Shutdown Control
0 Software shutdown
1 Normal operation

Table 9 C1h Global Current Control Register

Bit	D7:D2	D1:D0
Name	-	GCC
Default	000000	00

The Global Current Control Register modulates all LEDs DC current which is noted as $I_{OUT(PEAK)}$ in 4 steps.

GCC Global current control
00 GCC=4/4
01 GCC=3/4
10 GCC=2/4
11 GCC=1/4

Table 10 C2h PWM Frequency Register

Bit	D7	D6	D5:D4	D3	D2:D0
Name	PHC	-	-	PWMR	PFS
Default	0	0	00	0	000

The Configuration Register sets the PWM frequency of IS31FL3751, PWM resolution and PHC (Phase delay choice) function.

The PFS bits selects a fixed oscillator frequency, PWMR sets the PWM resolution of IS31FL3751. When PWMR is set to "0", it is 12-bit PWM resolution, when

PWMR is set to “1”, it is 8-bit PWM resolution mode. Auto Breath mode (ABM mode) operates at 12-bit PWM mode, so it is not allowed to enable ABM mode in 9-bit PWM mode.

PFS	PWM frequency
000	8MHz OSC (Default, PWM frequency is 1.95kHz (12-bit) or 31kHz (8-bit))
001	4MHz OSC (8MHz divider, PWM frequency is 0.92kHz (12-bit) or 16kHz (8-bit))
010	2MHz OSC (8MHz divider, PWM frequency is 0.46kHz (12-bit, not recommend) or 8kHz (8-bit))
011	1MHz OSC (8MHz divider, PWM frequency is 0.22kHz (12-bit, not recommend) or 4kHz (8-bit))
100	16MHz OSC (PWM frequency is 4kHz (12-bit) or 62kHz (8-bit))
101	24MHz OSC (PWM frequency is 8kHz (12-bit) or 124kHz (8-bit))
110	1MHz OSC (PWM frequency is 0.46kHz (12-bit, not recommend) or 8kHz (8-bit))
111	2MHz OSC (PWM frequency is 0.22kHz (12-bit, not recommend) or 4kHz (8-bit))

PWMR	PWM Resolution
0	12 bit mode (default)
1	8-bit mode (not allowed when ABM_EN bit is enabled)

PHC	Phase Delay choice
0	Disable Phase Delay (default)
1	Enable Phase Delay

Table 11 C3h Pull Down/Up Resistor Selection Register

Bit	D7:D6	D5	D4	D3	D3:D0
Name	-	PP	PEN	-	PV
Default	00	0	0	0	000

Pull Down/Up Resistor Selection Register Set pull down/up resistor or pull strength for SOx.

PEN	Pull EN
0	Disable
1	Enable

PP	Pull period
0	only in non-overlap time
1	All the time

PV	Pull voltage
000	Pull to PVCC-0.8V
001	Pull to PVCC-1.0V
010	Pull to PVCC-1.2V
011	Pull to PVCC-1.4V
100	Pull to PVCC-1.6V
101	Pull to PVCC-2.0V
110	Pull to PVCC-2.4V
111	Pull to PVCC-2.8V

Table 12 C4h Auto Breath Control Register 1 of ABM

Bit	D7	D6:D4	D3:D0
Name	-	T1	T2
Default	0	000	0000

Auto Breath Control Register 1 set the T1&T2 time in Auto Breath Mode.

T1	T1 Setting
000	0.21s
001	0.42s
010	0.84s
011	1.68s
100	3.36s
101	6.72s
110	13.44s
111	26.88s

T2	T2 Setting
0000	0s
0001	0.21s
0010	0.42s
0011	0.84s
0100	1.68s
0101	3.36s
0110	6.72s
0111	13.44s
1000	26.88s
Others	Unavailable

Table 13 C5h Auto Breath Control Register 2 of ABM

Bit	D7	D6:D4	D3:D0
Name	-	T3	T4
Default	0	000	0000

Auto Breath Control Register 2 set the T3&T4 time in Auto Breath Mode.

T3	T3 Setting
000	0.21s
001	0.42s
010	0.84s
011	1.68s
100	3.36s
101	6.72s

110 13.44s
111 26.88s

T4 T4 Setting
0000 0s
0001 0.21s
0010 0.42s
0011 0.84s
0100 1.68s
0101 3.36s
0110 6.72s
0111 13.44s
1000 26.88s
1001 53.76s
1010 107.52s
Others Unavailable

Table 14 C6h Auto Breath Control Register 3 of ABM-x

Bit	D7:D6	D5:D4	D3:D0
Name	LE	LB	LTA
Default	00	00	0000

Total loop times= LTA ×256 + LTB (defined in next register).

For example, if LTA=2, LTB=100, the total loop times is 256×2+100= 612 times.

For the counting of breathing times, do follow Figure 8 to enable the Auto Breath Mode.

If the loop start from T4,

T4->T1->T2->T3(1)->T4->T1->T2->T3(2)->T4->T1->... and so on.

If the loop not start from T4,

Tx->T3(1) ->T4->T1->T2->T3(2)->T4-> T1->... and so on.

If the loop ends at off state (End of T3), the LED will be off state at last. If the loop ends at on state (End of T1), the LED will run an extra T4&T1, which are not included in loop.

LB Loop Beginning Time
00 Loop begin from T1
01 Loop begin from T2
10 Loop begin from T3
11 Loop begin from T4

LE Loop End Time
00 Loop end at off state (End of T3)
01 Loop end at on state (End of T1)

LTA 8-11 Bits of Loop Times
0000 Endless loop
0001 1
0010 2
… …
1111 15

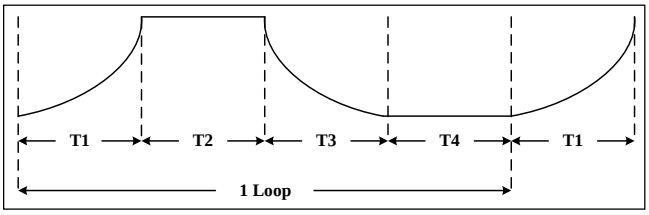


Figure 8 Auto Breathing Function

Table 15 C7h Auto Breath Control Register 4 of ABM

Bit	D7:D0
Name	LTB
Default	0000 0000

Total loop times= LTA ×256 + LTB.

For example, if LTA=2, LTB=100, the total loop times is 256×2+100= 612 times.

LTB 0-7 Bits Of Loop Times
0000 0000 Endless loop
0000 0001 1
0000 0010 2
… …
1111 1111 255

C8h Time Update Register (C4h~C5h)

The data sent to the time registers (C4h~C5h) will be stored in temporary registers. A write operation of "0000 0000" data to the Time Update Register is required to update the registers. Please follow Figure 8 to enable the Auto Breath mode and update the time parameters.

Table 16 C9h Spread Spectrum Register

Bit	D7:D5	D4	D3:D0
Name	-	SSP	-
Default	000	0	00

When SSP enable, the spread spectrum function will be enabled.

It is not recommended to enable SSP function when OSC frequency is or lower than 4MHz (PFS= "001", "010", "011", "110" or "111").

SSP Spread Spectrum Function Enable
0 Disable
1 Enable

Table 17 CA~D2h Open short Register

	SO1	SO2	SO3	SO4	SO5	SO6	SO7	SO8	SO9
SO1	-	CAH_LSB	CAH	CAH	CAH	CAH	CAH	CAH	CAH_MSB
SO2	CBH_LSB	-	CBH	CBH	CBH	CBH	CBH	CBH	CBH_MSB
SO3	CCH_LSB	CCH	-	CCH	CCH	CCH	CCH	CCH	CCH_MSB
SO4	CDH_LSB	CDH	CDH	-	CDH	CDH	CDH	CDH	CDH_MSB
SO5	CEH_LSB	CEH	CEH	CEH	-	CEH	CEH	CEH	CEH_MSB
SO6	CFH_LSB	CFH	CFH	CFH	CFH	-	CFH	CFH	CFH_MSB
SO7	D0H_LSB	D0H	D0H	D0H	D0H	D0H	-	D0H	D0H_MSB
SO8	D1H_LSB	D1H	D1H	D1H	D1H	D1H	D1H	-	D1H_MSB
SO9	D2H_LSB	D2H	D2H	D2H	D2H	D2H	D2H	D2H_MSB	-

Table 18 CA~D2h Open short Register

Bit	D7:D0
Name	OPEN/SHORT
Default	0000 0000

OPEN/SHORT function, can be enabled by configuration register, if enable Open function, read result is open information, if enable short, read result is short information.

When OSDE (D0h) is set to “01”, open detection will be trigger once, and the open information will be stored at CAh~D2h.

When OSDE (D0h) set to “10”, short detection will be trigger once, and the short information will be stored at CAh~D2h.

EFh Reset Register

Once user writes the Reset Register with 0xAE, IS31FL3751 will reset all the IS31FL3751 registers to their default value. On initial power-up, the IS31FL3751 registers are reset to their default values for a blank display.

APPLICATION INFORMATION

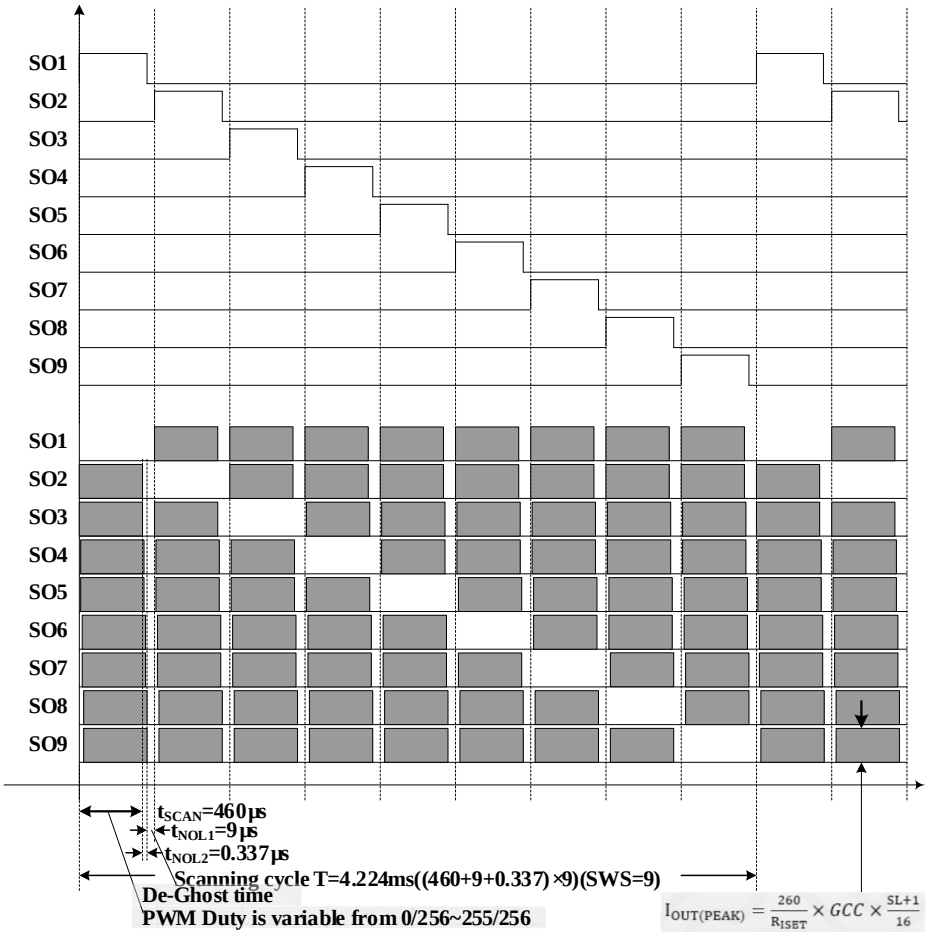


Figure 9 Scanning Timing

SCANING TIMING

As shown in Figure above, the SO1~SO9 work as power source and turned on by serial, LED is driven within the SOx (x=1~9) on time (SOx, x=1~9 is source and it is high when LED on), including the non-overlap blanking time during scan, the duty cycle of SOx (active high, x=1~11) is:

$$Duty = \frac{460\mu s}{(460+9+0.337)\mu s} \times \frac{1}{9} = \frac{1}{9.18} \quad (2,\ SWS=1/9)$$

Where 460μs is t_{SCAN}, the period of scanning and 9μs is t_{NOL1}, the non-overlap time and 0.337μs is the SOx delay time.

PWM CONTROL

The brightness of 72 LEDs can be modulated with 4096 (12-bit PWM mode) or 256 (8-bit PWM mode) steps by PWM Register. For example, in 8-bit PWM mode, if the data in PWM Register is “0000 0100”, then the PWM is the fourth step.

Writing new data continuously to the registers can modulate the brightness of the LEDs to achieve a breathing effect.

EXTERNAL RESISTOR (R_{ISET})

The average output current of each LED can be adjusted by the external resistor, R_{ISET}, as described in Formula (3).

$$I_{OUT(PEAK)} = \frac{260}{R_{ISET}} \times GCC \times \frac{SL+1}{16} \quad (3)$$

$$I_{LED} = \frac{PWM}{4096} \times I_{OUT(PEAK)} \times Duty \quad (1,\ 12\text{-bit mode})$$

$$I_{LED} = \frac{PWM}{256} \times I_{OUT(PEAK)} \times Duty \quad (1,\ 8\text{-bit mode})$$

$$PWM = \sum_{n=0}^{11} D[n] \cdot 2^n \quad (1,\ 12\text{-bit mode})$$

$$PWM = \sum_{n=0}^{7} D[n] \cdot 2^n \quad (1,\ 8\text{-bit mode})$$

Where PWM is PWM Register (00h~8Fh) data showing in Table 4, and GCC is Global Current Control Register (C1h) data showing Table 9.

For example: if in 12-bit PWM mode, PWM register D11:D0= “1000 1011 0101” (0x8B5, 2229), SWS=1/9, R_{ISET}=13kΩ, GCC= “00”, SL= “1111”:

$$I_{LED} = \frac{260}{13k\Omega} \times \frac{4}{4} \times \frac{15+1}{16} \times \frac{1}{9.18} \times \frac{2229}{4096}$$

The recommended minimum value of R_{ISET} is 8.2kΩ.

LED CURRENT (I_{LED})

The LED average current can be set by 3 factors:

1. R_{ISET}, resistant which is connected ISET pin and GND. R_{ISET} set all LED DC current value.

2. Global Current Control Register (C1h). This register control global current, set all LED DC current by 4 steps. Details refer to Table 9.

$$I_{OUT(PEAK)} = \frac{260}{R_{ISET}} \times GCC \times \frac{SL+1}{16} \quad (3)$$

3. Scaling Register (90h~B3h). These registers control peak current for each LED dot, set each LED DC current by 16 steps. Details refer to table 6.

4. PWM Registers (00h~8Fh), every LED has an own PWM register. PWM Registers set individual LED current by 256 or 4096 steps. Details refer to table 4.

OPERATING MODE

IS31FL3751 has 2 operating modes, PWM Mode and Auto Breath Mode (ABM mode).

PWM MODE

When ABM_EN (C0h) bit is disabled, the IS31FL3751 operates in PWM Mode. Set the PWMR bit of PWM Frequency Register (C2h) to choose 8-bit PWM mode or 12-bit PWM mode, and set the PFS bits of PWM Frequency Register (C2h) to choose PWM frequency.

AUTO BREATH MODE

When ABM_EN bit (C0h) is enabled, the IS31FL3751 operates in Auto Breath Mode (ABM mode).

Each LED need to enable its ABME bit first in B4h~BCh before ABM_EN bit is enabled, So PWM control mode and auto breath mode can coexist in the matrix.

ABM mode can only work when PWMR is set to 12-bit PWM mode (PWMR of C2h).

BREATHING FUNCTION SETTING

When IS31FL3751 ABM mode is enabled, breath function is available. By setting the ABM_EN bit of the Configuration Register (C0h) to “1”, breath function enables. When set the ABM_EN bit to “0”, breath function disables.

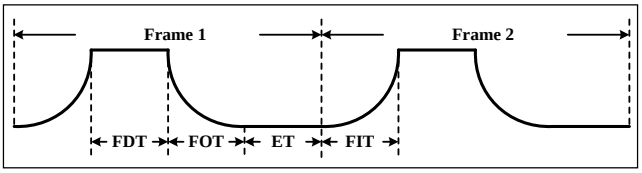


Figure 10 Breathing Function

SHUTDOWN MODE

Shutdown mode can be used as a means of reducing power consumption. During shutdown mode all registers retain their data.

Software Shutdown

By setting SSD bit of the Shutdown Register (C0h) to “0”, the IS31FL3751 will operate in Software Shutdown mode. When the IS31FL3751 is in Software Shutdown mode, all current sources are switched off, so that the matrix is blanked. All registers can be written when the SDB pin is pulled high. Typical current consume is 0.5μA.

Registers Reset

When SDB pin is pulled low, all registers won’t be reset. During SDB pin pulled high, Registers are reset to default once V_{CC} drop below 1.75V (Typ.). SDB pin hold in low voltage state (Hardware Shutdown), all analog circuits are shutdown. The Function Register still can be reset in case of Hardware Shutdown when V_{CC} drops below 0.1V.

Hardware Shutdown

The chip enters Hardware Shutdown when the SDB pin is pulled low. All analog circuits are disabled during Hardware Shutdown, typical current consume is 0.5μA.

The chip enters Hardware Enable when the SDB pin is pulled high. During Hardware Shutdown state Registers can be written.

If V_{CC} has risk drop below 1.75V but above 0.1V during SDB pulled low, please re-initialize all Function Registers before SDB pulled high.

POWER DISSIPATION

The power dissipation of the IS31FL3751 can calculate as below:

$$P_{3751} = I_{PVCC} \times PV_{CC} + I_{CC} \times V_{CC}(AV_{CC}) - I_{PVCC} \times V_{F(AVR)} \quad (4)$$

$$\approx I_{PVCC} \times PV_{CC} - I_{PVCC} \times V_{F(AVR)}$$

$$= I_{PVCC} \times \left(PV_{CC} - V_{F(AVR)}\right)$$

Where IPV_{CC} is the current of PV_{CC} and $V_{F(AVR)}$ is the average forward of all the LED.

For example, if R_{ISET}= 20kΩ, GCC= 255, PWM= 255, PV_{CC}= 5V, $V_{F(AVR)}$= 3.4V@34mA, then the I_{PVCC}= (34mA×8×9/10.5)×2= 466.29mA.

P_{3751}= 466.29mA×(5V-3.4V)= 0.746W

When operating the chip at high ambient temperatures, or when driving maximum load current, care must be taken to avoid exceeding the package power dissipation limits. The maximum power dissipation can be calculated using the following Formula (5):

$$P_{D(MAX)} = \frac{125°C - 25°C}{\theta_{JA}} \qquad (5)$$

So,

$$P_{D(MAX)} = \frac{125°C - 25°C}{50.2°C/W} \approx 2W$$

Figure 11, shows the power derating of the IS31FL3751 on a JEDEC boards (in accordance with JESD 51-5 and JESD 51-7) standing in still air.

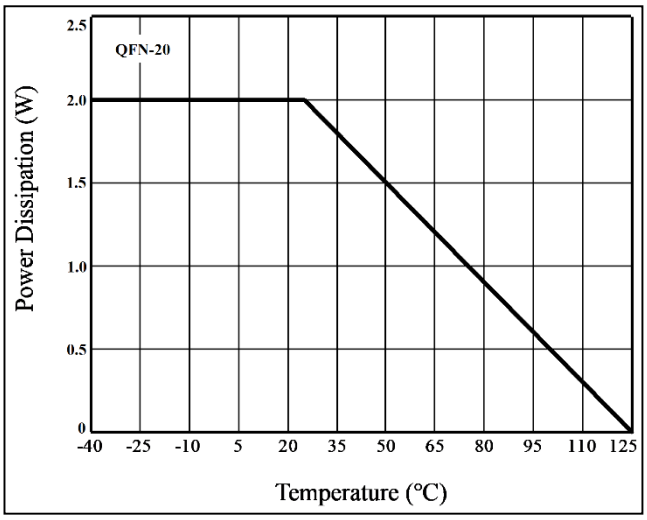


Figure 11 Dissipation Curve

CLASSIFICATION REFLOW PROFILES

Profile Feature	Pb-Free Assembly
Preheat & Soak Temperature min (Tsmin) Temperature max (Tsmax) Time (Tsmin to Tsmax) (ts)	150°C 200°C 60-120 seconds
Average ramp-up rate (Tsmax to Tp)	3°C/second max.
Liquidous temperature (TL) Time at liquidous (tL)	217°C 60-150 seconds
Peak package body temperature (Tp)*	Max 260°C
Time (tp)** within 5°C of the specified classification temperature (Tc)	Max 30 seconds
Average ramp-down rate (Tp to Tsmax)	6°C/second max.
Time 25°C to peak temperature	8 minutes max.

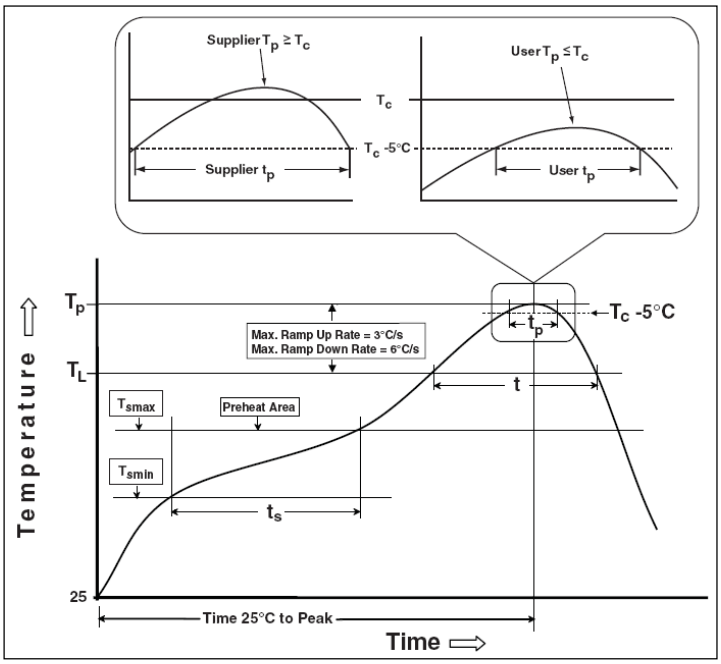
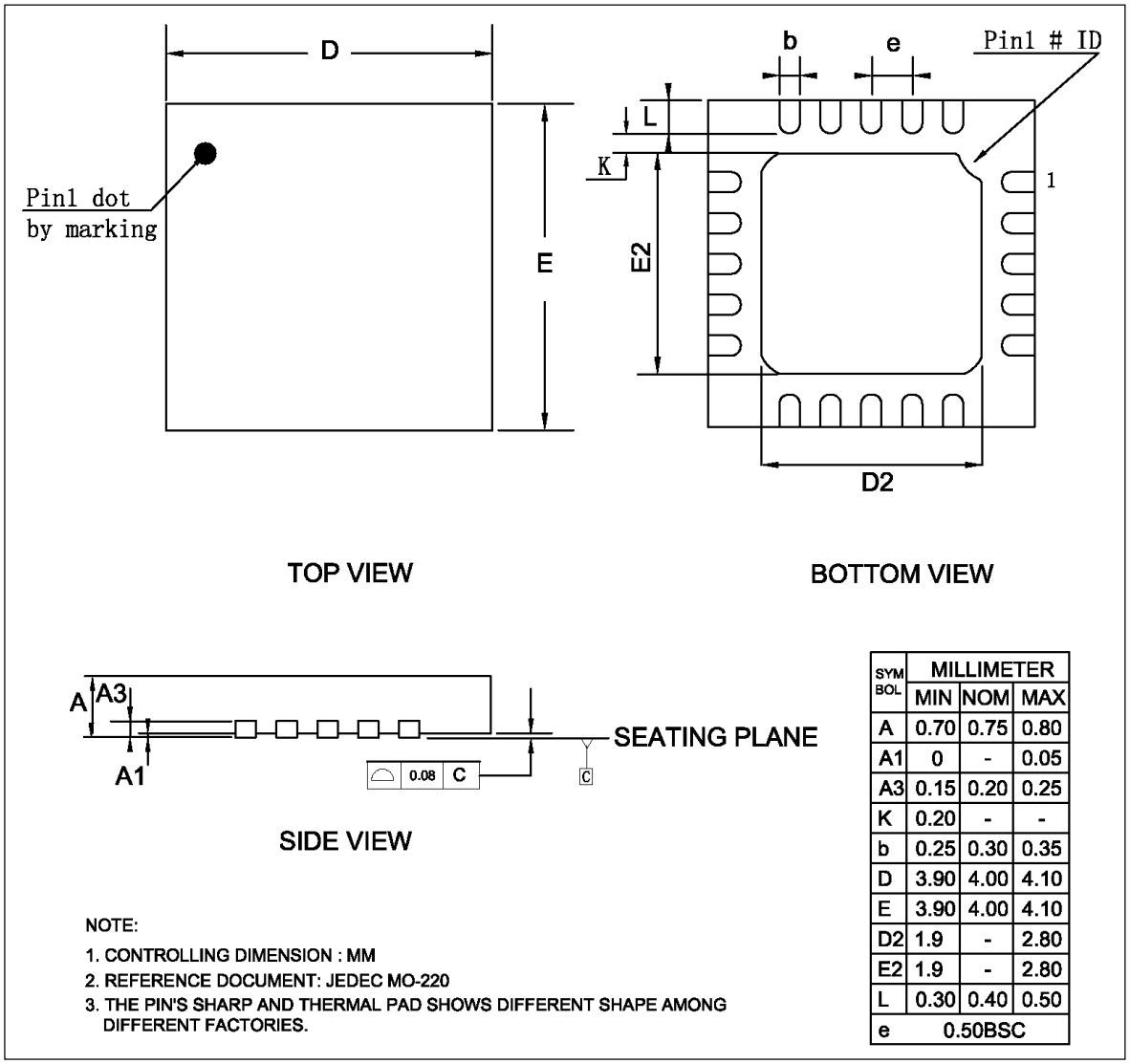


Figure 12 Classification Profile

PACKAGE INFORMATION

QFN-20



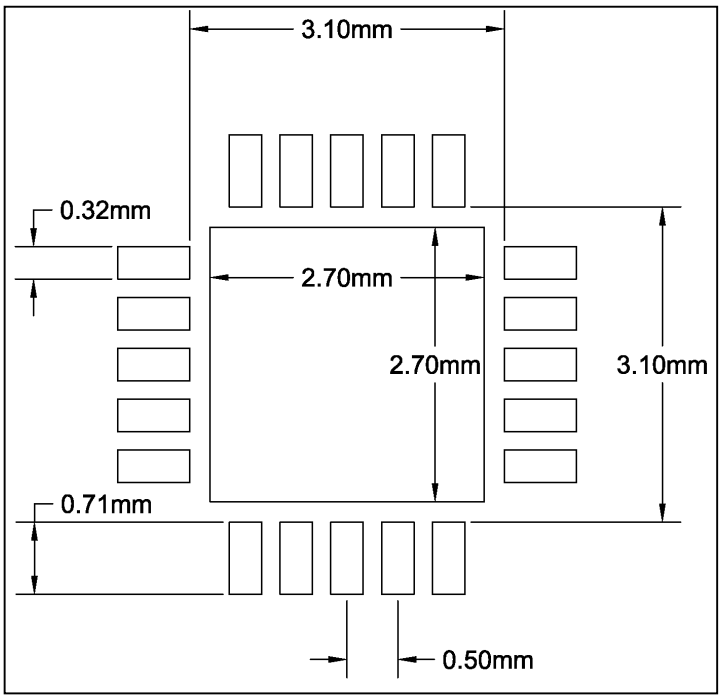
SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	0.70	0.75	0.80
A1	0	-	0.05
A3	0.15	0.20	0.25
K	0.20	-	-
b	0.25	0.30	0.35
D	3.90	4.00	4.10
E	3.90	4.00	4.10
D2	1.9	-	2.80
E2	1.9	-	2.80
L	0.30	0.40	0.50
e	0.50BSC		

NOTE:

1. CONTROLLING DIMENSION : MM
2. REFERENCE DOCUMENT: JEDEC MO-220
3. THE PIN'S SHARP AND THERMAL PAD SHOWS DIFFERENT SHAPE AMONG DIFFERENT FACTORIES.

RECOMMENDED LAND PATTERN

QFN-20



Note:

1. Land pattern complies to IPC-7351.
2. All dimensions in MM.
3. This document (including dimensions, notes & specs) is a recommendation based on typical circuit board manufacturing parameters. Since land pattern design depends on many factors unknown (eg. User's board manufacturing specs), user must determine suitability for use.

REVISION HISTORY

Revision	Detail Information	Date
A	Initial release	2021.03.15