IS31FL3763

18×12 DOTS MATRIX LED DRIVER

February 2024

GENERAL DESCRIPTION

The IS31FL3763 is a general purpose 18 × n (n=2~12) LED Matrix programmed via 1MHz I2C or 12MHz SPI compatible interface. Each LED can be dimmed individually with 12-bit/8+4-bit/8-bit/6+2-bit PWM data and each color sink can have 8-bit DC scaling data which allow 256 steps of linear PWM dimming and each color sink has 256 steps of DC current adjustable level and precision for smooth LED brightness control. The maximum output current of each channel is designed to be 40mA, which can be adjusted by 8-bit x1 global control register.

Additionally, each LED open and short state can be detected, IS31FL3763 stores the open or short information in Open-Short Registers. The Open-Short Registers allow MCU to read out via I2C/SPI compatible interface. Inform MCU whether there are LEDs open or short and the locations of open or short LEDs. Proprietary algorithms are used in IS31FL3763 to minimize power bus noise caused by passive components on the power bus such as MLCC decoupling capacitor. All registers can be programmed via SPI (up to 12MHz) bus or I2C (1MHz) bus.

The IS31FL3763 operates from 3V to 5.5V and features a very low shutdown and operational current.

IS31FL3763 is available in QFN-40 (5mm×5mm) package. It operates from 3V to 5.5V over the temperature range of -40°C to +125°C.

FEATURES

- Supply voltage range: 3.0V to 5.5V
- Support 18 (CS)× n (n=2~12) matrix configuration
- Individual 12-bit/8+4-bit/8-bit /6+2-bit PWM control steps
- Constant-current output range: 40mA
- 24kHz scan frame rate (@6+2-bit PWM)
- Ultra-low I_{CC} when frame rate is about 375Hz (280μA, 6+2-bit mode, $I_{OUT(PEAK)}$=2.9mA)
- Each color sink (CSy) 8-bit DC current steps
- Global 256 steps current setting
- 1MHz I2C-compatible interface & 12MHz SPI interface
- State lookup registers
- Random switching sequencing to mitigate power ripple, EMI, and audible noise
- For matrix scanning operation
  - Built-in de-ghosting circuit
  - Reduced inactive LED reverse bias to improve LED reliability
- LED open/short detection accessible to I2C/SPI
- Group phase shift (180-degree) to reduce audible noise and power ripple
- Support spread spectrum operation for PWM clock to reduce EMI
- Software shutdown mode
- Operating temperature: -40°C to 125°C
- QFN-40 (5mm×5mm) package
- RoHS & Halogen-Free Compliance
- TSCA Compliance

APPLICATIONS

- RGB keyboard
- LED display for hand-held devices

TYPICAL APPLICATION CIRCUIT

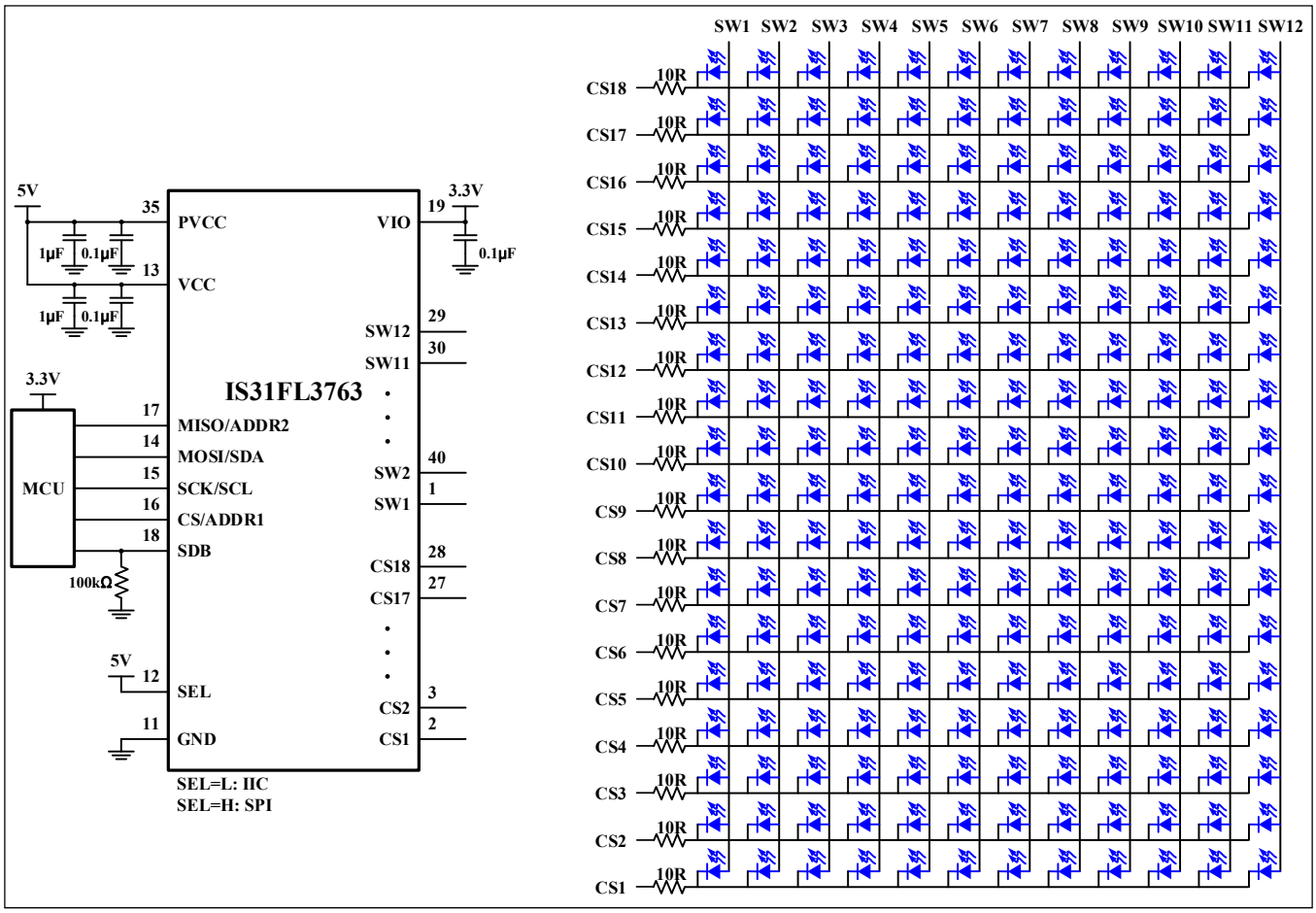


Figure 1 Typical Application Circuit (18×12, LED)

Note 1: The V_{IH} of I2C bus should be not higher than V_{CC}. And if VIH is lower than 3.0V, it is recommended add a level shift circuit to avoid extra shutdown current.

Note 2: These optional resistors are for offloading the thermal dissipation ($P=I^2R$) away from the IS31FL3763, for mono red/yellow/orange LED, if $PV_{CC}=V_{CC}=3.3V$, don't need these resistors.

TYPICAL APPLICATION CIRCUIT (CONTINUED)

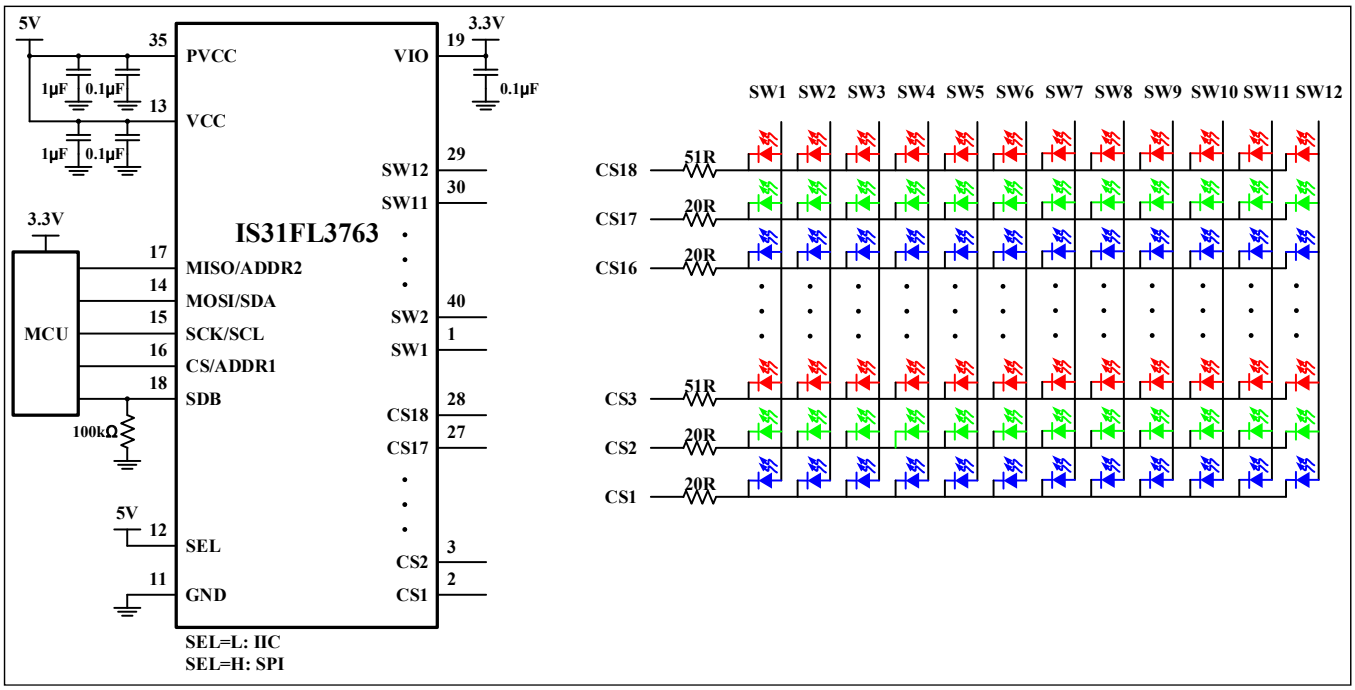
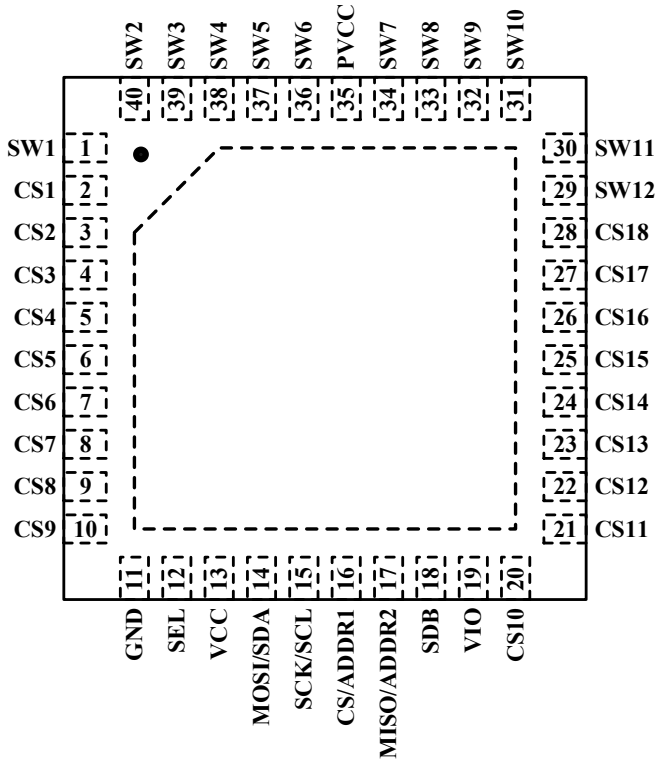


Figure 2 Typical Application Circuit (18×12, RGB)

Note 3: These optional resistors are for offloading the thermal dissipation ($P=I^2R$) away from the IS31FL3763, for red LED, it is recommended to use about 30Ω more than blue/green LED, to offload extra voltage due to lower forward voltage of red LED.

PIN CONFIGURATION

Package	Pin Configuration (Top View)
QFN-40	

PIN DESCRIPTION

No.	Pin	Description
1	SW1	Power SW.
2~10	CS1~CS9	Current sink pin for LED matrix.
11	GND	Power GND and analog GND.
12	SEL	SEL=L: I2C, SEL=H: SPI.
13	VCC	Analog and digital circuits.
14	MOSI/SDA	SPI serial input data or I2C serial data.
15	SCK/SCL	SPI serial clock or I2C serial clock.
16	CS/ADDR1	CS of SPI or I2C address setting pin1.
17	MISO/ADDR2	SPI serial output data or I2C address setting pin2.
18	SDB	Shutdown pin.
19	VIO	Power for communication block.
20~28	CS10~CS18	Current sink pin for LED matrix.
29~34	SW7~SW12	Power SW.
35	PVCC	Power for current source SW.
36~40	SW2~SW6	Power SW.
	Thermal Pad	Connect to GND.

ORDERING INFORMATION

Industrial Range: -40°C to +125°C

Order Part No.	Package	QTY/Reel
IS31FL3763-QFLS4-TR	QFN-40, Lead-free	2500

ABSOLUTE MAXIMUM RATINGS

Supply voltage, V_{CC}	-0.3V ~+6.0V
Voltage at any input pin	-0.3V ~ V_{CC}+0.3V
Maximum junction temperature, T_{JMAX}	+150°C
Storage temperature range, T_{STG}	-65°C ~+150°C
Operating temperature range, T_A=T_J	-40°C ~ +125°C
Package thermal resistance, junction to ambient (4-layer standard test PCB based on JESD 51-2A), θ_{JA}	31.5°C/W
ESD (HBM) ESD (CDM)	±3kV ±750kV

Note 4: Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other condition beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

The following specifications apply for V_{CC} = 5V, T_A = 25°C, unless otherwise noted.

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
V_{CC}	Supply voltage		3		5.5	V
I_{CC}	Quiescent power supply current	V_{SDB}=V_{CC}= PV_{CC}=5V, I_{OUT}=40mA, all LEDs off with PWM=0x00, SRS= 6kHz@8bit mode		2.1	2.4	mA
		V_{SDB}=V_{CC}=PV_{CC}=5V, I_{OUT}=2.9mA (GCC= 0x13), SCM= "10", all LEDs off with PWM=0x00, SRS=400Hz@12bit mode		1.6	1.8	
		V_{SDB}=V_{CC}=PV_{CC}=5V, I_{OUT}=2.9mA (GCC= 0x13), SCM= "10", all LEDs off with PWM=0x00, SRS=375Hz@8bit mode		0.31	0.36	
		V_{SDB}=V_{CC}=PV_{CC}=5V, I_{OUT}=2.9mA (GCC= 0x13), SCM = "10", all LEDs off with PWM=0x00, SRS=750Hz@6+2-bit mode		0.28	0.32	
I_{SD}	Shutdown current	V_{SDB}=0V		0.6	1	μA
		V_{SDB}= V_{CC}=PV_{CC}, Configuration Register written "0000 0000		0.6	1	
I_{OUT}	Maximum constant current of CSy	PWM= 0xFFF, GCC=0xFF, V_{OUT}= 0.8V, SL=0xFF@12bit Mode	37.2	40	42.8	mA
ΔI_{MAT}	Sink current between channels	I_{OUT}= 40mA (Note 5)	-5		5	%
ΔI_{ACC}	Sink current Between device to device	I_{OUT}= 40mA (Note 6)	-7		7	%
I_{LED}	Average current on each LED I_{LED} = $I_{OUT(PEAK)}$/Duty(1/13.5)	V_{SDB}=V_{CC}=PV_{CC}=5V, SRS=400Hz@12-bit Mode, PWM=0xFFF, SL=0xFF, GCC=0xFF		2.96		mA
V_{HR}	Current switch headroom voltage SWx	V_{SDB}=V_{CC}=PV_{CC}=5V, I_{SW}=720mA, GCC=0xFF, SL=0xFF		450	650	mV
	Current sink headroom voltage CSy	V_{SDB}=V_{CC}=PV_{CC}=5V, I_{CS}=40mA, GCC=0xFF, SL=0xFF		420	600	

ELECTRICAL CHARACTERISTICS (CONTINUE)

The following specifications apply for V_{CC} = 5V, T_A = 25°C.

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
t_{SCAN}	SWx on time of scanning	V_{SDB}=V_{CC}=PV_{CC}=5V, 6+2-bit mode@24kHz	3.3	3.6	3.9	μs
		V_{SDB}=V_{CC}=PV_{CC}=5V, 12-bit mode@400Hz	186	201	217	
t_{NOL1}	Non-overlap blanking time during scan, the SWx and CSy are all off during this time	V_{SDB}=V_{CC}=PV_{CC}=5V, SRS= “000”		0.45		μs
t_{NOL2}	Delay total time for CS1 to CS 18, during this time, the SWx is on but CSy is not all turned on (Note 7)	V_{SDB}=V_{CC}=PV_{CC}=5V		24		ns
V_O	Open threshold	V_{CC}= 5V, I_{OUT}≥ 1mA, measured at CSy	50	100	200	mV
V_S	short threshold	V_{CC}= 5V, I_{OUT}≥ 1mA, measured at (V_{CC}-V_{CSy})		V_{CC}-1	V_{CC}-0.5	V
Logic Electrical Characteristics (SCK, MISO, MOSI, CS, SDB)						
V_{IL}	Logic “0” input voltage	V_{CC}=3V~5.5V, V_{IO}=1.7V~V_{CC}			0.2V_{IO}	V
V_{IH}	Logic “1” input voltage	V_{CC}=3V~5.5V, V_{IO}=1.7V~V_{CC}	0.8V_{IO}			V
V_{OH}	H level MISO pin output voltage	I_{OH}= -8mA, V_{IO}=3.3V	V_{IO}-0.4V		V_{IO}	V
V_{OL}	L level MISO pin output voltage	I_{OL}= 8mA, V_{IO}=3.3V	0		0.4	V
V_{HYS}	Input Schmitt trigger hysteresis	V_{CC}=3.6V, V_{IO}=3.3V		0.2		V
V_{OL-SDA}	Low-level output voltage of SDA	I_{LOAD}=5mA			0.4	V
I_{IL}	Logic “0” input current	SDB=L, V_{INPUT}= L (Note 7)		5		nA
I_{IH}	Logic “1” input current	SDB=L, V_{INPUT}= H (Note 7)		5		nA

DIGITAL INPUT SPI SWITCHING CHARACTERISTICS (NOTE 7)

Symbol	Parameter	Min.	Typ.	Max.	Units
f_C	Clock frequency	-		12	MHz
t_{SLCH}	CS active set-up time	34			ns
t_{SHCH}	CS not active set-up time	17			ns
t_{SHSL}	CS detect time	167			ns
t_{CHSH}	CS active hold time	34			ns
t_{CHSL}	CS not active hold time	17			ns
t_{CH}	Clock high time	34			ns
t_{CL}	Clock low time	34			ns
t_{CLCH}	Clock rise time			9	ns
t_{CHCL}	Clock fall time			9	ns
t_{DVCH}	Data in set-up time	7			ns
t_{CHDX}	Data in hold time	9			ns
t_{SHQZ}	Output disable time			34	ns
t_{CLQV}	Clock low to output valid			39	ns
t_{CLQX}	Output hold time	0			ns
t_{QLQH}	Output rise time			17	ns
t_{QLQH}	Output fall time			17	ns

Note 5: I_{OUT} mismatch (bit to bit) $\triangle I_{MAT}$ is calculated:

$$\Delta I_{MAT} = \pm\left(\frac{I_{OUT(MAX)} - I_{OUT(MIN)}}{\left(\frac{I_{OUT0}+I_{OUT1}+\ldots+I_{OUT18}}{18} \times 2\right)}\right) \times 100\%$$

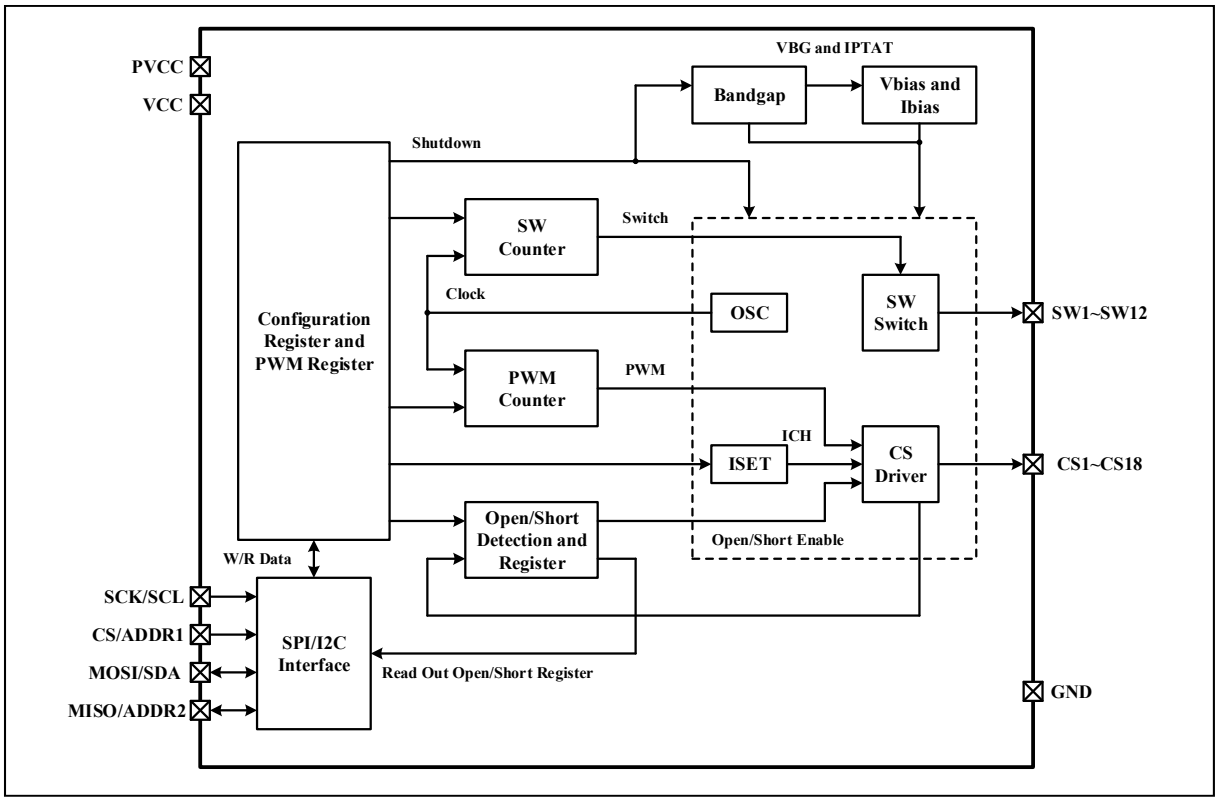
Note 6: I_{OUT} accuracy (device to device) $\triangle I_{ACC}$ is calculated:

$$\Delta I_{ACC} = \pm MAX\left(\frac{I_{OUT(MIN)} - I_{OUT(IDEAL)}}{I_{OUT(IDEAL)}}\right) \times 100\%$$

Where $I_{OUT(IDEAL)}$= 40mA.

Note 7: Guaranteed by design.

FUNCTIONAL BLOCK DIAGRAM



DETAILED DESCRIPTION

I2C INTERFACE

IS31FL3763 uses a serial bus, which conforms to the I2C protocol, to control the chip's functions with two wires: SCL and SDA. The IS31FL3763 has a 7-bit slave address (A7:A1), followed by the R/W bit, A0. Set A0 to "0" for a write command and set A0 to "1" for a read command. The value of bits A1 and A2 are decided by the connection of the ADDRx pin.

Table 1 Slave Address:

ADDR2	ADDR1	A7:A5	A4:A3	A2:A1	A0
GND	GND	110	00	00	0/1
GND	SCL		00	01	
GND	SDA		00	10	
GND	VCC		00	11	
SCL	GND		01	00	
SCL	SCL		01	01	
SCL	SDA		01	10	
SCL	VCC		01	11	
SDA	GND		10	00	
SDA	SCL		10	01	
SDA	SDA		10	10	
SDA	VCC		10	11	
VCC	GND		11	00	
VCC	SCL		11	01	
VCC	SDA		11	10	
VCC	VCC		11	11	

ADDR1/2 connected to GND, (A2:A1)/(A4:A3)=00;
ADDR1/2 connected to VCC, (A2:A1)/(A4:A3)=11;
ADDR1/2 connected to SCL, (A2:A1)/(A4:A3)=01;
ADDR1/2 connected to SDA, (A2:A1)/(A4:A3)=10;

The SCL line is uni directional. The SDA line is bi-directional (open drain) with a pull-up resistor (typically 400kHz I2C with 4.7kΩ, 1MHz I2C with 2kΩ). The maximum clock frequency specified by the I2C standard is 1MHz. In this discussion, the master is the microcontroller, and the slave is the IS31FL3763.

The timing diagram for the I2C is shown in Figure 3. The SDA is latched in on the stable high level of the SCL. When there is no interface activity, the SDA line should be held high.

The "START" signal is generated by lowering the SDA signal while the SCL signal is high. The start signal will alert all devices attached to the I2C bus to check the incoming address against their own chip address.

The 8-bit chip address is sent next, most significant bit first. Each address bit must be stable while the SCL level is high.

After the last bit of the chip address is sent, the master checks for the IS31FL3763's acknowledge. The master releases the SDA line high (through a pull-up resistor). Then the master sends an SCL pulse. If the IS31FL3763 has received the address correctly, then it holds the SDA line low during the SCL pulse. If the SDA line is not low, then the master should send a "STOP" signal (discussed later) and abort the transfer.

Following acknowledge of IS31FL3763, the register address byte is sent, most significant bit first. IS31FL3763 must generate another acknowledge indicating that the register address has been received.

Then 8-bit of data byte are sent next, most significant bit first. Each data bit should be valid while the SCL level is stable high. After the data byte is sent, the IS31FL3763 must generate another acknowledge to indicate that the data was received.

The "STOP" signal ends the transfer. To signal "STOP", the SDA signal goes high while the SCL signal is high.

ADDRESS AUTO INCREMENT

To write multiple bytes of data into IS31FL3763, load the address of the data register that the first data byte is intended for. During the IS31FL3763 acknowledge of receiving the data byte, the internal address pointer will increment by one. The next data byte sent to IS31FL3763 will be placed in the new address, and so on. The auto increment of the address will continue if data continues to be written to IS31FL3763 (Figure 6).

READING OPERATION

Most of the registers can be read.

To read the registers, after I2C start condition, the bus master must send the IS31FL3763 device address with the R/$\overline{W}$ bit set to "0", followed by the register address which determines which register is accessed. Then restart I2C, the bus master should send the IS31FL3763 device address with the R/$\overline{W}$ bit set to "1". Data from the register defined by the command byte is then sent from the IS31FL3763 to the master (Figure 7).

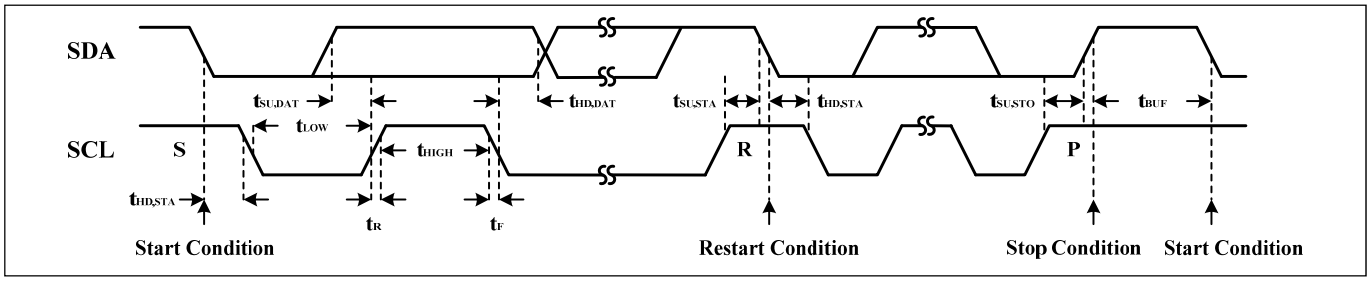


Figure 3 I2C Interface Timing

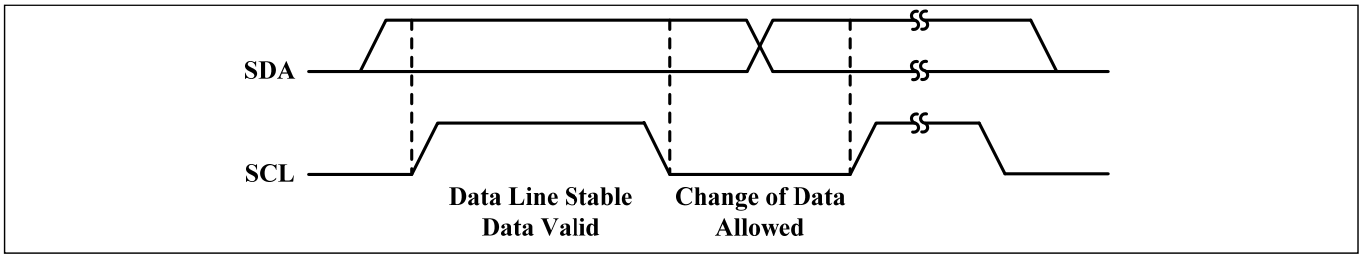


Figure 4 I2C Bit Transfer

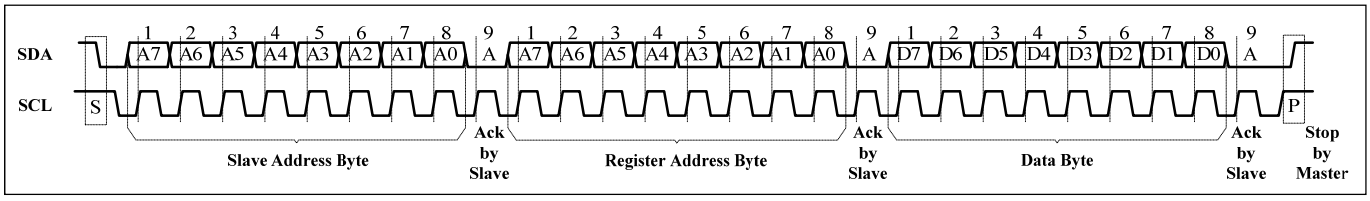


Figure 5 I2C Writing to IS31FL3763 (Typical)

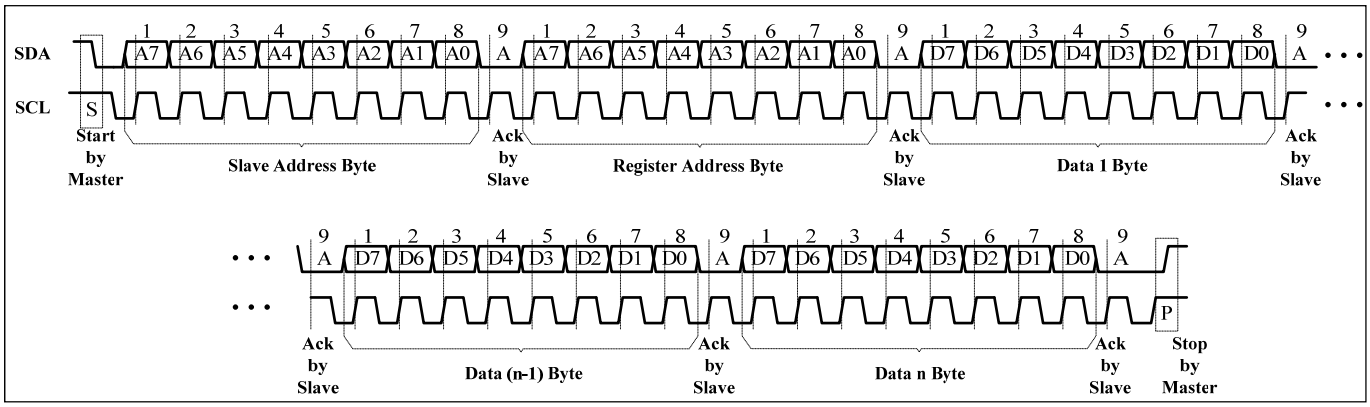


Figure 6 I2C Writing to IS31FL3763 (Automatic Address Increment)

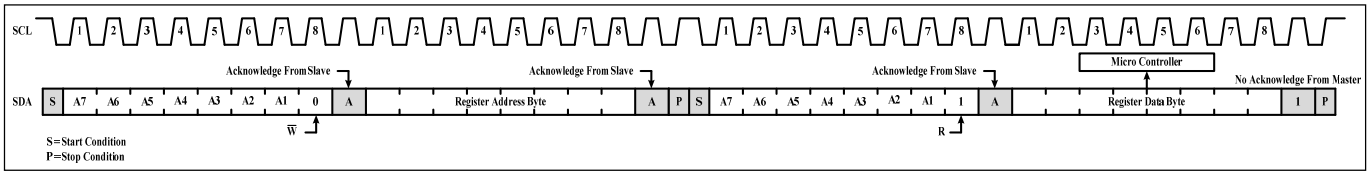


Figure 7 I2C Reading from IS31FL3763

SPI INTERFACE

IS31FL3763 uses a SPI protocol to control the chip's function with four wires: CS, SCK, MOSI and MISO. SPI transfer starts form CS pin from high to low controlled by Master (Microcontroller), and IS31FL3763 latches data when clock rising.

SPI data format is 8-bit length. The first command byte composite of 1-bit R/W bit, 3-bit chip ID bit and 4-bit page bit. The command byte must be sent first and is followed by register address byte then the register data. If the R/W bit is "0", it will be written operation and Master (Micro-controller) can write the register data into the register.

The maximum SCK frequency supported in IS31FL3763 is 12MHz.

Table 2 SPI Command Byte

Name	R/W	ID bit	Page No.
Bit	D7	D6:D4	D3:D0
Value	0: Write 1: Read	110	0x00: Point to Page 0 0x01: Point to Page 1

ADDRESS AUTO INCREMENT

To write multiple bytes of data into IS31FL3763, load the address of the data register that the first data byte is intended for. During the 8th rising edge of receiving the data byte, the internal address pointer will increment by one. The next data byte sent to IS31FL3763 will be placed in the new address, and so on. The auto increment of the address will continue if data continues to be written to IS31FL3763 (Figure 11).

READING OPERATION

Page 0~Page 1 registers can be read by SPI.

To read the registers of Page 0 thru Page 1, The D7 of the Command Byte need to be set to "1" and select the page number. If read one register, as shown in Figure 12, read the MISO data after sending the command byte and register address. If read more registers, as shown in Figure 13, the register address will auto increase during the 8th rising edge of receiving the last bit of the previous register data.

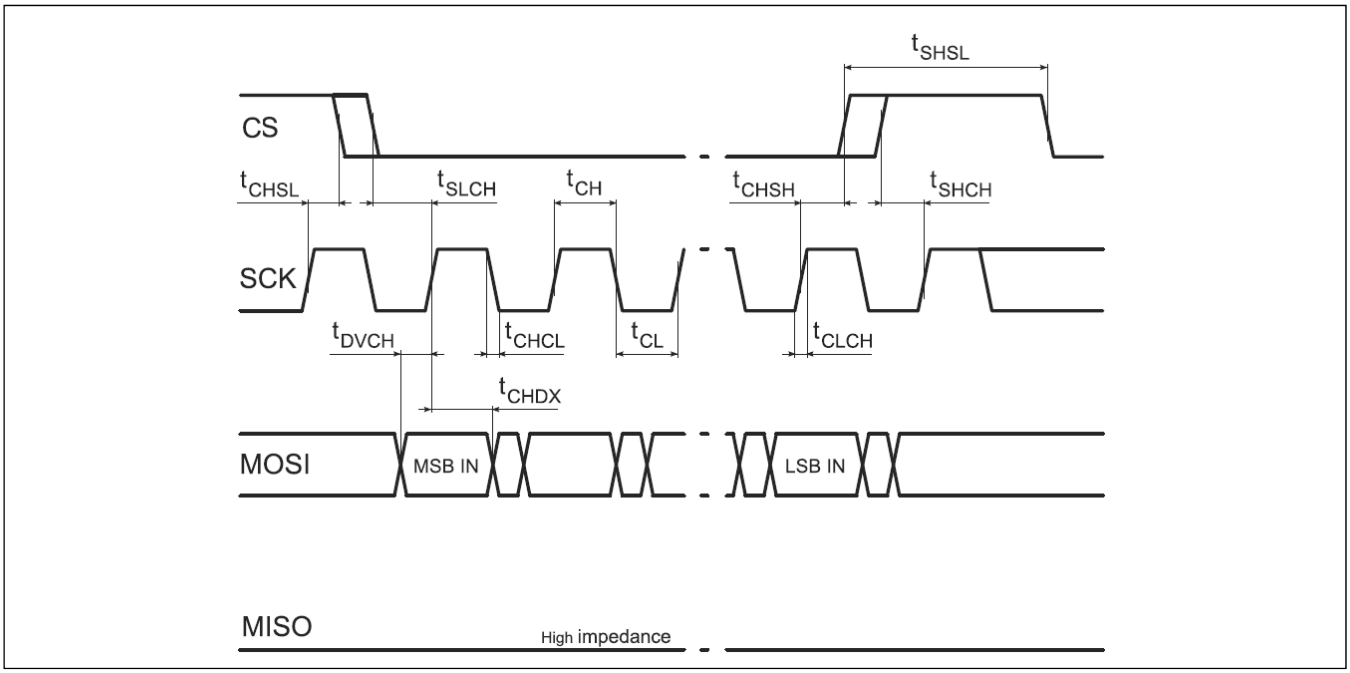


Figure 8 SPI Input Timing

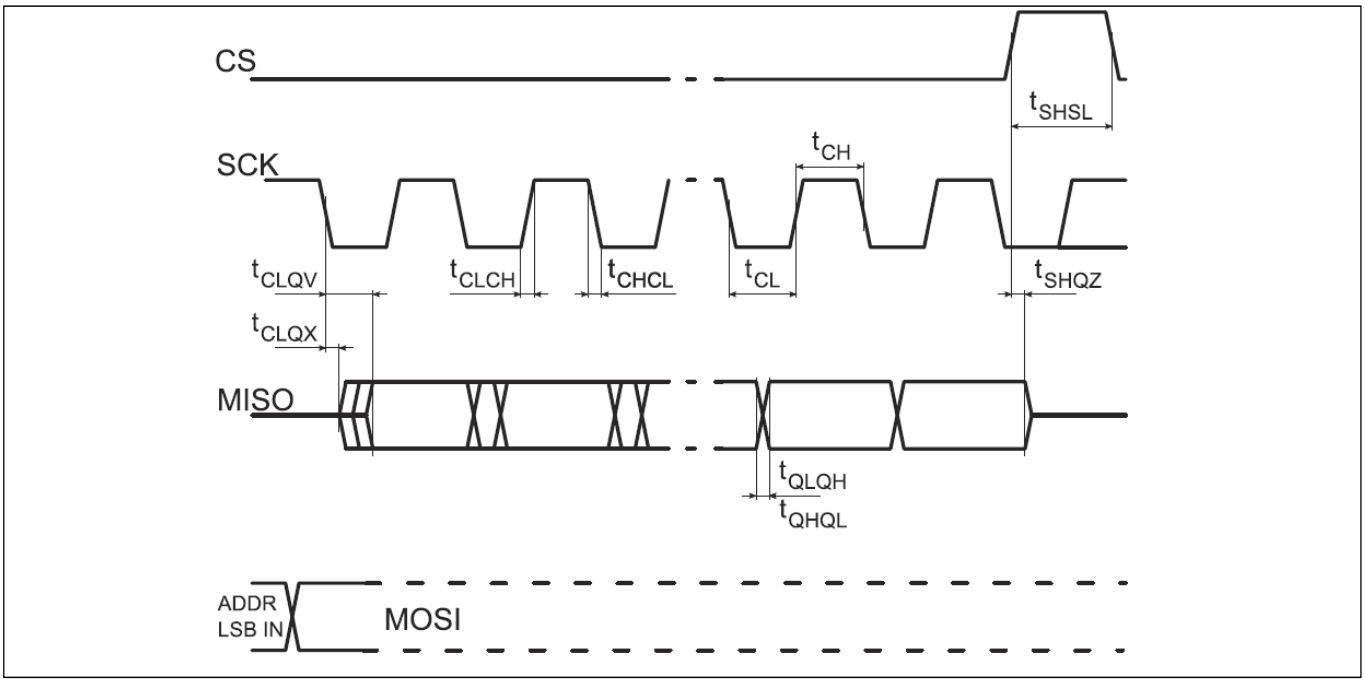


Figure 9 SPI Input Timing

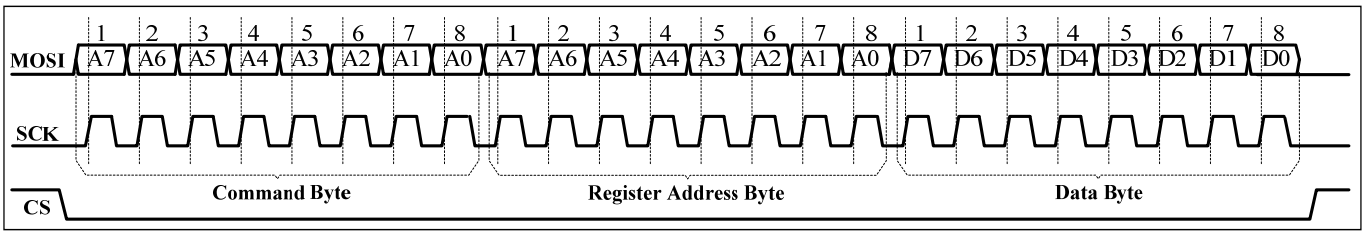


Figure 10 SPI writing to IS31FL3763 (Typical)

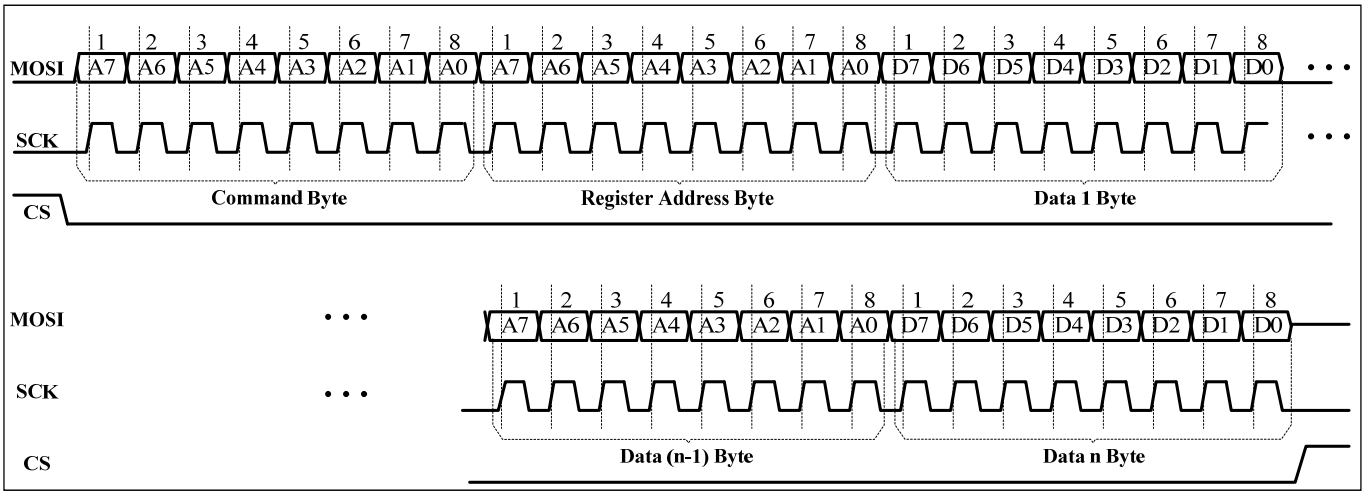


Figure 11 SPI writing to IS31FL3763 (Automatic address increment)

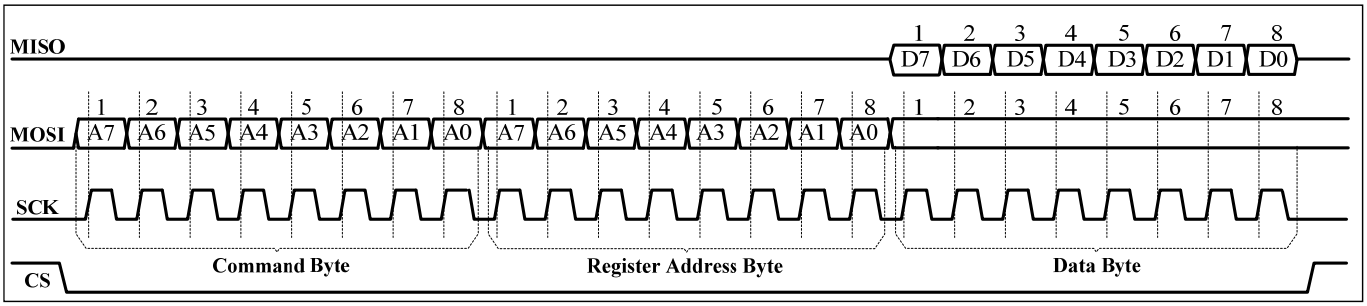


Figure 12 SPI Reading From IS31FL3763 (Typical)

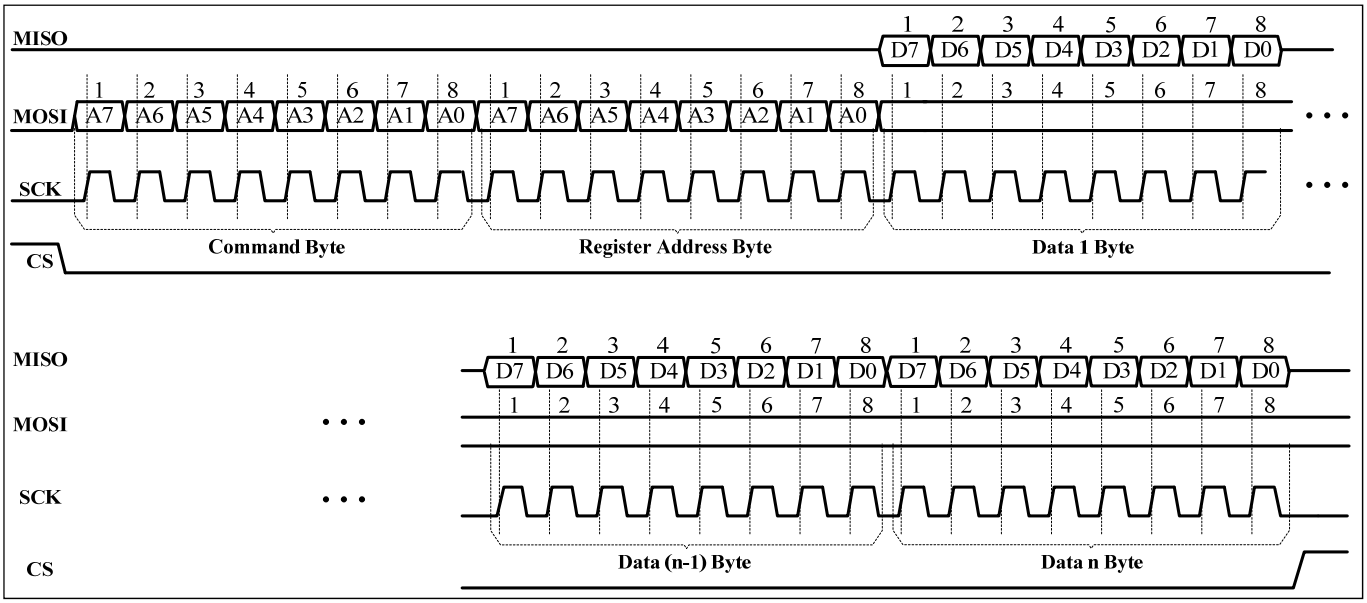


Figure 13 SPI Reading From IS31FL3763 (Automatic Address Increment)

Register Definition-1

Address	Name	Function	Table	R/W	Default
FEh	Command Register	Available Page 0 to Page 1 Registers	3	W	xxxx xxxx
FFh	Command Register Write lock	To lock/unlock Command Register	4	R/W	0000 0000

REGISTER CONTROL WITH I2C

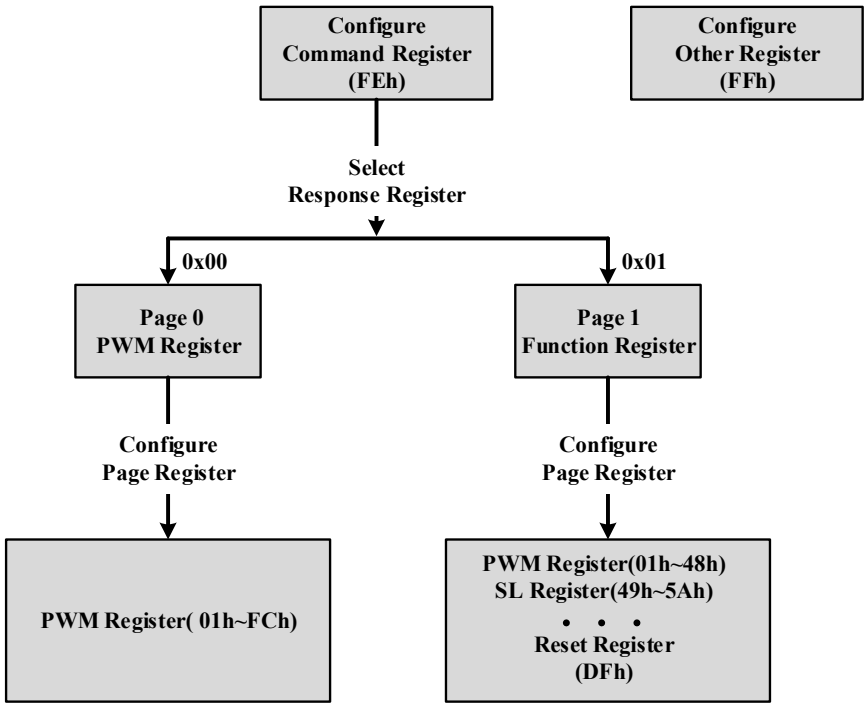


Table 3 FEh Command Register (Write Only)

Data	Function
0000 0000	Point to Page 0 (PG0, LED PWM Register is available)
0000 0001	Point to Page 1 (PG1, Function Register is available)

Note: FFh is locked when power up, need to unlock this register before write command to it. See Table 4 for detail.

The Command Register should be configured first after writing in the slave address to choose the available register. Then write data in the choosing register. Power up default state is “0000 0000”.

For example, when write “0000 0001” in the Command Register (FEh), the data which writing after will be stored in Function Register is available (Page1).

Table 4 FFh Command Register Write Lock (Read/Write)

Bit	D7:D0
Name	CRWL
Default	0000 0000

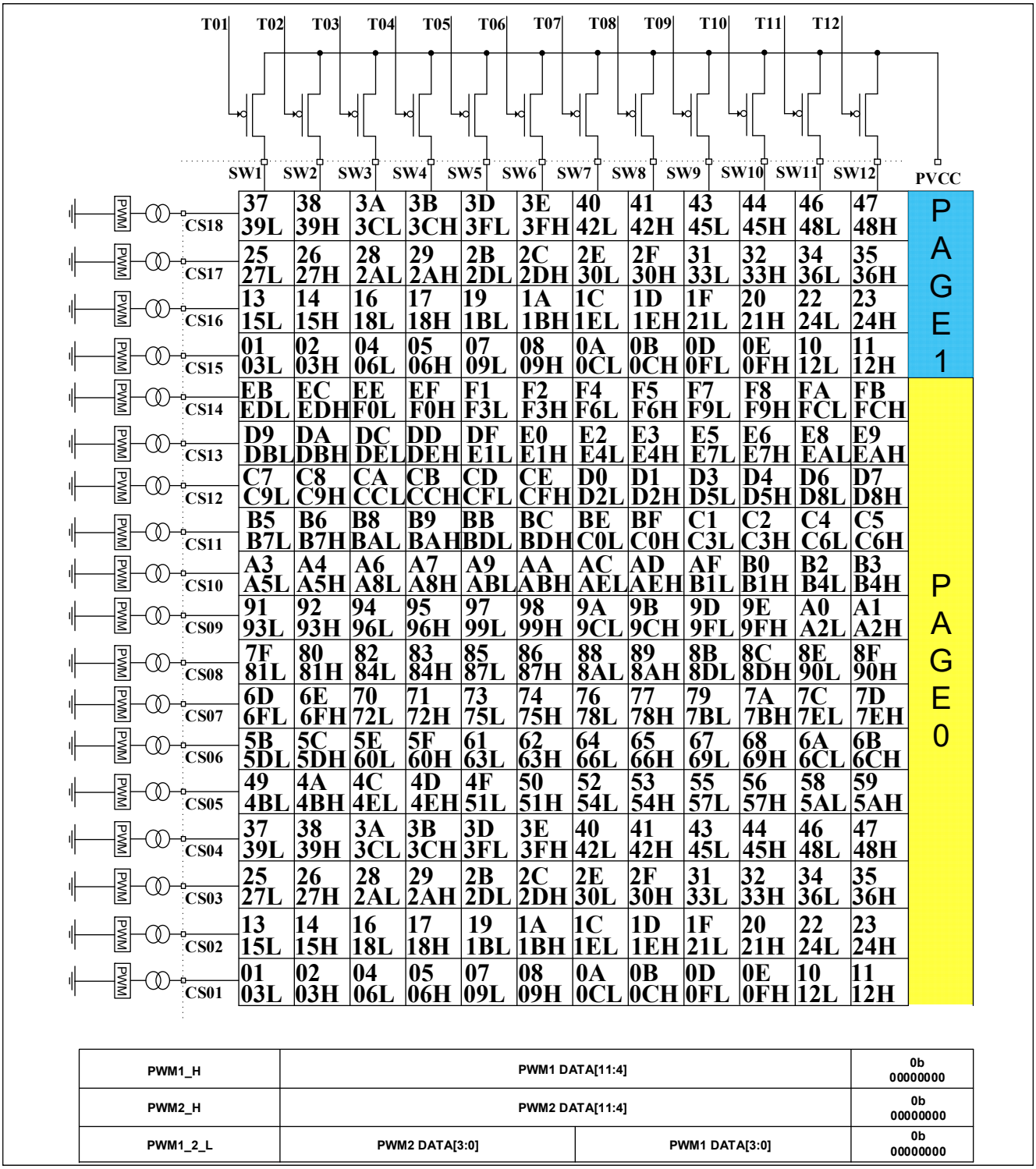
To select the PG0~PG1, need to unlock this register first, with the purpose of avoiding misoperation of this register. When FFh is written with 0xC5, FEh is allowed to modify once, after the FEh is modified the FFh will reset to be 0x00 at once.

CRWL Command Register Write Lock
0x00 FEh write disable
0xC5 FEh write enable once

Register Definition-2

Address	Name	Function	Table	R/W	Default
Page 0, I2C: FE=0x00, SPI page No.=0x00					
01h~FCh	PWM Register	Set PWM for each LED	5	R/W	0000 0000
Page 1, I2C: FE=0x01, SPI page No.=0x01					
01h~48h	PWM Register	Set PWM for each LED	5	R/W	0000 0000
49h~5Ah	SL Register	Set Current for each CS channel	6	R/W	0000 0000
60h	Configuration Register	Configure the operation mode	7	R/W	0000 0000
61h	Global Current Control Register	Set the global current	8	R/W	0000 0000
62h	Pull Down/Up Resistor Selection Register	Set the pull-down resistor for SWx and pull-up resistor for CSy	9	R/W	0000 0000
63h	SRS/Random Enable Register	Set SW random enable and scan rate setting	10	R/W	0000 0000
64h	Spread Spectrum Register	Spread spectrum function enable	11	R/W	0000 0000
65h	Open Short Enable Register	Enable open/short detect	12	R/W	0000 0000
66h~68h	Open Short Register	Read open/short LED dot data	13	R	0000 0000
91h	CS Pull Up Ability Register	Set the CS pull up ability in t_{NOL1} time	14	W	0000 0000
DFh	Reset Register	Reset all register to default value	-	W	0000 0000
FDh	PWM update register	Update PWM register	-	W	0000 0000

PWM Register



PWM1_H	PWM1 DATA[11:4]		0b 00000000
PWM2_H	PWM2 DATA[11:4]		0b 00000000
PWM1_2_L	PWM2 DATA[3:0]	PWM1 DATA[3:0]	0b 00000000

Figure 14 PWM Register

Table 5-1 Page 0 01h ~ FCh PWM Register
Table 5-2 Page 1 01h ~ 48h PWM Register

Page 0 SW1-CS1

Bit	01h: D7:D0		03h: D3:D0
Name	PWM_H	PWM_H	PWM_L
Default	0000	0000	0000

Page 0 SW2-CS1

Bit	02h: D7:D0		03h: D7:D4
Name	PWM_H	PWM_H	PWM_L
Default	0000	0000	0000

Page 0 SW1-CS3

Bit	04h: D7:D0		06h: D3:D0
Name	PWM_H	PWM_H	PWM_L
Default	0000	0000	0000

Page 0 SW2-CS4

Bit	05h: D7:D0		06h: D7:D4
Name	PWM_H	PWM_H	PWM_L
Default	0000	0000	0000

Page 1 SW12-CS18

Bit	47h: D7:D0		48h: D7:D4
Name	PWM_H	PWM_H	PWM_L
Default	0000	0000	0000

Each dot has a byte + a nibble to modulate the PWM duty in 256 or 4096 steps.

The high 8 bit and the low 4 bits mapping between PWM registers as Figure 14.

The value of the PWM Registers decides the average current of each LED noted I_{LED}.

I_{LED} computed by Formula (1):

8bit mode

$$I_{LED} = \frac{PWM}{256} \times I_{OUT(PEAK)} \times Duty \quad (1)$$

$$PWM = \sum_{n=0}^{7} D[n] \cdot 2^n$$

12bit mode

$$I_{LED} = \frac{PWM}{4096} \times I_{OUT(PEAK)} \times Duty \quad (1)$$

$$PWM = \sum_{n=0}^{11} D[n] \cdot 2^n$$

Where Duty is the duty cycle of SWx, see SCANING TIMING section for more information.

$$Duty = \frac{3.6\mu s}{(3.6\mu s + 0.45\mu s)} \times \frac{1}{12} \quad (2)$$

Where 3.6μs is t_{SCAN}, the period of scanning and 0.45μs is t_{NOL1}, the non-overlap time.

I_{OUT} is the output current of CSy (y=1~18),

$$I_{OUT(PEAK)} = 40.32 \times \frac{GCC}{256} \times \frac{SL}{256} \quad (3)$$

GCC is the Global Current Control register, SL is the Scaling Register value as Table 6.D[n] stands for the individual bit value, 1 or 0, in location n.

For example: in 8-bit mode, if D7:D0=1011 0101 (0xB5, 181), GCC=1111 1111, SL=1111 1111:

$$I_{LED} = 40.32 \times \frac{GCC}{256} \times \frac{SL}{256} \times Duty \times \frac{PWM}{256} \quad (1)$$

Table 6 Page 1 49h ~ 5Ah Scaling Register

Bit	D7:D0
Name	SL
Default	0000 0000

Note 8: When LED off by set SL = 0x00, there also should be set GCC = 0x00 or PWM = 0x00.

Scaling register controls the DC output current of each CS. Each CS has a byte to modulate the scaling in 256 steps.

The value of the Scaling Register decides the peak current of each LED noted $I_{OUT(PEAK)}$.

$I_{OUT(PEAK)}$ computed by Formula (3):

$$I_{OUT(PEAK)} = 40.32 \times \frac{GCC}{256} \times \frac{SL}{256} \quad (3)$$

$$SL = \sum_{n=0}^{7} D[n] \cdot 2^n$$

I_{OUT} is the output current of CSy (y=1~18), GCC is the Global Current Control Register (PG1, 61h) value. D[n] stands for the individual bit value, 1 or 0, in location n.

For example: if GCC=1111 1111, SL=0111 1111:

$$SL = \sum_{n=0}^{7} D[n] \cdot 2^n = 127$$

$$I_{OUT} = 40.32 \times \frac{255}{256} \times \frac{127}{256} = 19.92mA$$

$$I_{LED} = 19.92mA \times \frac{1}{13.5} \times \frac{PWM}{256} \quad (1)$$

Table 7 Page 1 60h Configuration Register

Bit	D7:D4	D3	D2:D1	D0
Name	SWS	-	PWMM	SSD
Default	0000	0	00	0

The Configuration Register sets operating mode of IS31FL3763.

When SSD is “0”, IS31FL3763 works in software shutdown mode and to normal operate the SSD bit should set to “1”.

PWMM choose the PWM Mode. For example, when PWMM = “10” PWM Mode is 8+4-bit.

SWS control the duty cycle of the SW, default mode is 1/12.For example, when SWS = “0010”, the duty cycle is 1/10.

SSD Software Shutdown Control
0 Software shutdown
1 Normal operation

PWMM PWM mode
00 6+2-bit
01 8-bit
10 8+4-bit
11 12-bit

SWS SWx Setting
0000 SW1~SW12, 1/12
0001 SW1~SW11, 1/11, SW12 no active
0010 SW1~SW10, 1/10, SW11~SW12 no active
0011 SW1~SW9, 1/9, SW10~SW12 no active
0100 SW1~SW8, 1/8, SW9~SW12 no active
0101 SW1~SW7, 1/7, SW8~SW12 no active
0101 SW1~SW6, 1/6, SW7~SW12 no active
0111 SW1~SW5, 1/5, SW6~SW12 no active
1000 SW1~SW4, 1/4, SW5~SW12 no active
1001 SW1~SW3, 1/3, SW4~SW12 no active
1010 SW1~SW2, 1/2, SW3~SW12 no active
1011 SW1&2~SW11&SW12, 1/6, 2 SW as one to reduce RDSON of SW
Work as SW 1-6
Reserve for 18x6
1100 SW1&2~SW9&SW10, 1/5, 2 SW as one to reduce RDSON of SW
Work as SW 1-5
Reserve for 18x5
1101 SW1&2&3~SW10&SW11&SW12, 1/4, 3 SW as one to reduce RDSON of SW
Work as SW 1-4
Reserve for 18x4
1110 SW1&2&3&4~W9&SW10&SW11&SW12, 1/3, 4 SW as one to reduce RDSON of SW
Work as SW 1-3
Reserve for 18x3
1111 &SW1-6~&SW7-12, 1/2, 6 SW as one to reduce RDSON of SW
Work as SW 1-2
Reserve for 18x2

Table 8 Page1 61h Global Current Control Register

Bit	D7:D0
Name	GCC
Default	0000 0000

The Global Current Control Register modulates all CSy (x=1~18) DC current which is noted as I_{OUT} in 256 steps.

I_{OUT} is computed by the Formula (3):

$$I_{OUT(PEAK)} = 40.32 \times \frac{GCC}{256} \times \frac{SL}{256} \quad (3)$$

$$GCC = \sum_{n=0}^{7} D[n] \cdot 2^n$$

Where D[n] stands for the individual bit value, 1 or 0, in location n.

Table 9 Page1 62h Pull Down/Up Resistor Selection Register

Bit	D7	D6:D4	D3	D2:D0
Name	PHC	SWPDR	-	CSPUR
Default	0	000	0	000

PHC control 180-degree phase enable or disable. When PHC= “1”, the 180-degree phase is enabled, and the phase difference between CS is about 180-degree.

SWPDR control SWx pull down to setting voltage when SWx closed. For example, if SWPDR = “100”, that SWx will pull down to setting voltage is 2.0V when SWx closed.

CSPUR control CSy pull up to setting voltage when CSy closed. For example, if CSPUR= “101”, that CSy will pull up to setting voltage is PV_{CC}-1.6V when CSy closed.

Please check De-Ghost Function section for more information in Application Information.

PHC Phase choice
0 0-degree phase
1 180-degree phase

SWPDR SWx Pull down Selection Bit
000 floating
001 3.2V
010 2.8V
011 2.4V
100 2.0V
101 1.6V
110 1.2V
111 GND

CSPUV CSy Pull up Selection Bit
000 floating
001 PV_{CC}-3.2V
010 PV_{CC}-2.8V
011 PV_{CC}-2.4V
100 PV_{CC}-2.0V
101 PV_{CC}-1.6V
110 PV_{CC}-1.2V
111 PV_{CC}

Table 10 Page1 63h SRS/Random Enable Register

Bit	D7	D6	D5:D4	D3	D2:D0
Name	RME	-	SCM	-	SRS
Default	0	0	00		000

RME control SW Random of scan enable bit. If RME= "1", the SW Random of scan is enable. That is SW scan frequency will by random.

SCM is small current mode enable bit. If SCM = "10", the I_{CC} will become more smaller when I_{CC} current small.

If SCM= "01", the SL will become smaller a half when I_{OUT} current small.

SRS control scan rate frequency setting bits. For example, if PWM Mode is 6+2-bit and SRS= "010", that the Scan rate frequency is 6kHz.

RME Random mode enable
0 Disable
1 Enable
Only affective when n=12 or 8;

SCM Small current mode
00 Disable
01 SL/2
10 Disable output OP & Make ICC smaller
11 all enable

SRS Scan rate frequency setting
000 24kHz for 6+2-bit mode
6kHz for 8-bit mode
6kHz for 8+4-bit mode
400+Hz for 12-bit mode

001 12kHz for 6+2-bit mode
3kHz for 8-bit mode
3kHz for 8+4-bit mode
200Hz for 12-bit mode

010 6kHz for 6+2-bit mode
1.5kHz for 8-bit mode
1.5kHz for 8+4-bit mode

011 3kHz for 6+2-bit mode
750Hz for 8-bit mode

100 1.5kHz for 6+2-bit mode
375Hz for 8-bit mode

101 750Hz for 6+2-bit mode
188Hz for 8-bit mode
188Hz for 8+4-bit mode

110 375Hz for 6+2-bit mode

Table 11 Page1 64h Spread Spectrum Register

Bit	D7:D6	D4	D3:D2	D1:D0
Name	-	SSP	RNG	CLT
Default	000	0	00	00

When SSP enable, the spread spectrum function will be enabled and the RNG & CLT bits will adjust the range and cycle time of spread spectrum function.

Only SRS = 000,001,010 or 011 have effect, where SRS is scan rate frequency setting bits.

SSP Spread spectrum function enable
0 Disable
1 Enable

RNG Spread spectrum range
00 ±10%
01 ±15%

CLT Spread spectrum cycle time
00 4.0ms
01 2.2ms
10 1.5ms
11 1.1ms

Table 12 Page1 65h Open Short Enable Register

Bit	D7:D6	D5:D4	D3:D0
Name	O/S	-	OS of SW
Default	00	00	0000

(Page1, 65h) register stores the open and short detect information of LED string. When O/S is "00", open and short detect is disable, if O/S is "10", open detect enable, if O/S is "11", short detect enable.

OS of SW bits choose where SW to detect open or short. For example, when OS of SW= "0010", that select SW3 to detect open or short.

Please check Open/Short detect function section for more information in Application Information.

O/S Select open or short
0X Disable
10 Open (Note 9)
11 Short

OS of SW Select which SW to detect
0000 SW1
0001 SW2
0010 SW3
0011 SW4
…
1010 SW11
1011 SW12

Table13-1 Page 1 66h Open Short Register

Bit	D7:D6	D5:D0
Name	-	CS06:CS01
Default	00	00 0000

Table 13-2 Page 1 67h Open Short Register

Bit	D7:D6	D5:D0
Name	-	CS12:CS07
Default	00	00 0000

Table 13-3 Page 1 68h Open Short Register

Bit	D7:D6	D5:D0
Name	-	CS18:CS13
Default	00	00 0000

After setting 65h, 66~68h can be read for the open or short information of each LED dot.

DFh Reset Register

Once user writes the Reset Register with 0xAE, IS31FL3763 will reset all the IS31FL3763 registers to their default value. On initial power-up, the IS31FL3763 registers are reset to their default values for a blank display.

FDh Update Register

When SDB= “H” and SSD= “1”, a write of “0000 0000” to FDh is to update the PWM Register (Page 0, 01h~FCh & Page 1 01h~48h) values.

APPLICATION INFORMATION

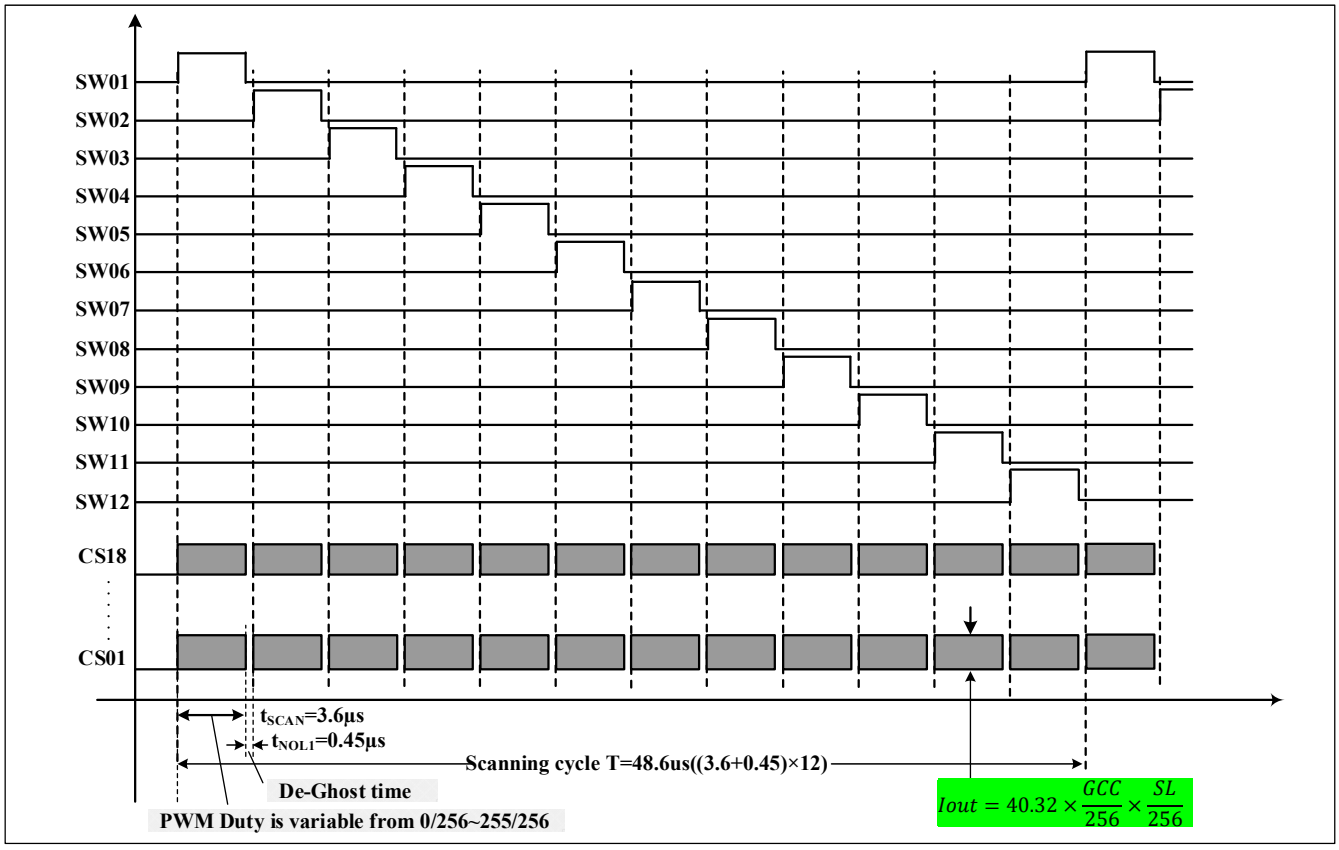


Figure 15 Scanning Timing

SCANING TIMING

As shown in Figure 15 above, the SW1~SW12 is turned on by serial, LED is driven 12 by 12 within the SWx (x=1~12) on time (SWx, x=1~12 is source and it is high when LED on), including the non-overlap blanking time during scan, the duty cycle of SWx (active high, x=1~12) is:

$$Duty = \frac{3.6\mu s}{(3.6\mu s+0.45\mu s)} \times \frac{1}{12} = \frac{1}{13.5} \qquad (2)$$

Where 3.6μs is t_{SCAN}, the period of scanning and 0.45μs is t_{NOL1}.

PWM CONTROL

After setting the I_{OUT} and GCC, the brightness of each LEDs (LED average current (I_{LED})) can be modulated with 256 steps by PWM Register, as described in Formula (1).

$$I_{LED} = \frac{PWM}{256} \times I_{OUT\,(PEAK)} \times Duty \qquad (1)$$

Where PWM is PWM Registers (PG0, 00h~FCh /PG1, 00h~48h) data showing in Table 5.

For example, if PWM= 255, and GCC= 255, Scaling= 255, then

$$I_{OUT(PEAK)} = 40.32 \times \frac{255}{256} \times \frac{255}{256} = 40mA$$

$$I_{LED} = 40mA \times \frac{1}{13.5} \times \frac{PWM}{256}$$

Writing new data continuously to the registers can modulate the brightness of the LEDs to achieve a breathing effect.

GAMMA CORRECTION

To perform a better visual LED breathing effect, we recommend using a gamma corrected PWM value to set the LED intensity. This results in a reduced number of steps for the LED intensity setting but causes the change in intensity to appear more linear to the human eye.

Gamma correction, also known as gamma compression or encoding, is used to encode linear luminance to match the non-linear characteristics of display. Since the IS31FL3763 can modulate the brightness of the LEDs with 256 steps, a gamma correction function can be applied when computing each subsequent LED intensity setting such that the change in brightness matches the human eye's brightness curve.

Table 14 32 Gamma Steps with 256 PWM Steps

C(0)	C(1)	C(2)	C(3)	C(4)	C(5)	C(6)	C(7)
0	1	2	4	6	10	13	18
C(8)	C(9)	C(10)	C(11)	C(12)	C(13)	C(14)	C(15)
22	28	33	39	46	53	61	69
C(16)	C(17)	C(18)	C(19)	C(20)	C(21)	C(22)	C(23)
78	86	96	106	116	126	138	149
C(24)	C(25)	C(26)	C(27)	C(28)	C(29)	C(30)	C(31)
161	173	186	199	212	226	240	255

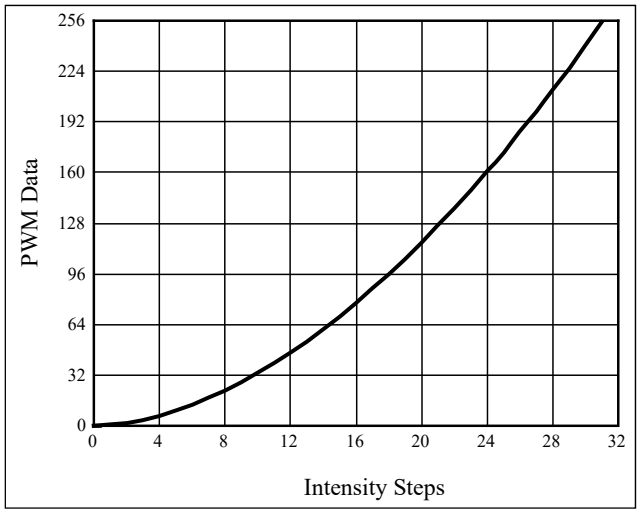


Figure 16 Gamma Correction (32 Steps)

Choosing more gamma steps provides for a more continuous looking breathing effect. This is useful for very long breathing cycles. The recommended configuration is defined by the breath cycle T. When T=1s, choose 32 gamma steps, when T=2s, choose 64 gamma steps. The user must decide the final number of gamma steps not only by the LED itself, but also based on the visual performance of the finished product.

Table 15 64 Gamma Steps with 256 PWM Steps

C(0)	C(1)	C(2)	C(3)	C(4)	C(5)	C(6)	C(7)
0	1	2	3	4	5	6	7
C(8)	C(9)	C(10)	C(11)	C(12)	C(13)	C(14)	C(15)
8	10	12	14	16	18	20	22
C(16)	C(17)	C(18)	C(19)	C(20)	C(21)	C(22)	C(23)
24	26	29	32	35	38	41	44
C(24)	C(25)	C(26)	C(27)	C(28)	C(29)	C(30)	C(31)
47	50	53	57	61	65	69	73
C(32)	C(33)	C(34)	C(35)	C(36)	C(37)	C(38)	C(39)
77	81	85	89	94	99	104	109
C(40)	C(41)	C(42)	C(43)	C(44)	C(45)	C(46)	C(47)
114	119	124	129	134	140	146	152
C(48)	C(49)	C(50)	C(51)	C(52)	C(53)	C(54)	C(55)
158	164	170	176	182	188	195	202
C(56)	C(57)	C(58)	C(59)	C(60)	C(61)	C(62)	C(63)
209	216	223	230	237	244	251	255

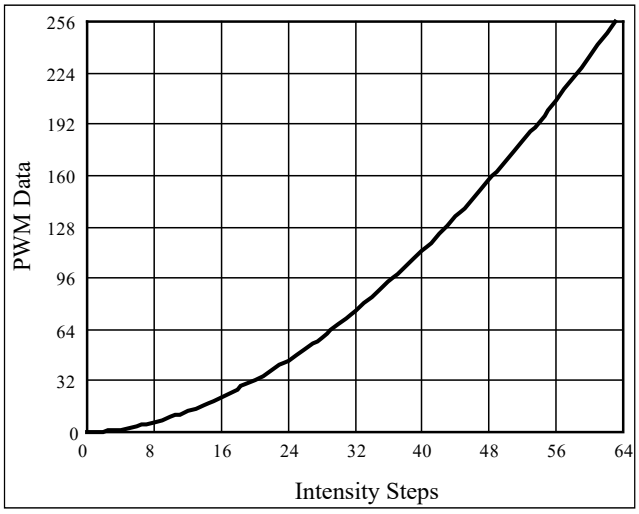


Figure 17 Gamma Correction (64 Steps)

Note: The data of 32 gamma steps is the standard value and the data of 64 gamma steps is the recommended value.

OPERATING MODE

IS31FL3763 can only operate in PWM Mode. The brightness of each LED can be modulated with 256 steps by PWM registers. For example, if the data in PWM Register is “0000 0100”, then the PWM is the fourth step.

Writing new data continuously to the registers can modulate the brightness of the LEDs to achieve a breathing effect.

OPEN/SHORT DETECT FUNCTION

IS31FL3763 has open and short detect bit for each LED.

By setting the O/S bits of the Configuration Register (PG1, 65h) from “00” to “10” or “11” the LED Open/short Register will start to store the open/short information and after at least 2 scanning cycles and the MCU can get the open/short information by reading the 66h~68h, for those dots are turned off via LED Scaling Registers (PG1, 49h~5Ah), the open/short data will not get refreshed when setting the O/S bit of the Configuration Register.

To get the correct open and short information, two configurations need to set before setting the O/S bits:

1 0x0F≤ GCC≤ 0x40
2 62h= 0x00

Where GCC is the Global Current Control Register (PG1, 61h) and 62h is the Pull Down/UP Resistor Selection Register and set to 0x00 is to disable the SWx pull-down and CSy pull-up function.

Th Open circuit or short circuit detection only needs to be enabled once to obtain the LED open circuit or short circuit data in real time.

Note 9: When open detect is enable, if PWM ≠ 0 and SL = 0, there should be set GCC = 0.

DE-GHOST FUNCTION

The “ghost” term is used to describe the behavior of an LED that should be OFF but instead glows dimly when another LED is turned ON. A ghosting effect typically can occur when multiplexing LEDs. In matrix architecture any parasitic capacitance found in the constant-current outputs or the PCB traces to the LEDs may provide sufficient current to dimly light an LED to create a ghosting effect.

To prevent this LED ghost effect, the IS31FL3763 has integrated Pull down resistors for each SWx (x=1~12) and pull up resistors for each CSy (y=1~18). Select the right SWx Pull down resistor (PG1, 62h) and CSy Pull up resistor (PG1, 62h) which eliminates the ghost LED for a particular matrix layout configuration.

Typically, selecting the SWx Pull down to 3.2V，CS Pull up to PV_{CC}-3.2V will be sufficient to eliminate the LED ghost phenomenon.

The SWx Pull down resistors and CSy Pull up resistors are active only when the CSy/SWx output working the OFF state and therefore no power is lost through these resistors.

SHUTDOWN MODE

Shutdown mode can be used as a means of reducing power consumption. During shutdown mode all registers retain their data.

Software Shutdown

By setting SSD bit of the Configuration Register (PG1, 60h) to “0”, the IS31FL3763 will operate in software shutdown mode. When the IS31FL3763 is in software shutdown, all current sources are switched off, so that the matrix is blanked. All registers can be operated. Typical current consume is 0.6μA.

Hardware Shutdown

The chip enters hardware shutdown when the SDB pin is pulled low. All analog circuits are disabled during hardware shutdown, typical the current consume is 0.6μA.

The chip releases hardware shutdown when the SDB pin is pulled high. During hardware shutdown state Function Register can be operated.

If V_{CC} has risk drop below 1.75V but above 0.1V during SDB pulled low, please re-initialize all Function Registers before SDB pulled high.

LAYOUT

Because of the chip consumes lots of power. Please consider below factors when layout the PCB.

1. The V_{CC} (PVCC, AVCC) capacitors need to close to the chip and the ground side should well connected to the GND of the chip.

2. The thermal pad should connect to ground pins and the PCB should have the thermal pad too, usually this pad should have 16 or 25 via thru the PCB to other side’s ground area to help radiate the heat. About the thermal pad size, please refer to the land pattern of each package.

3. The CSy pins maximum current is 40mA, and the SWx pins maximum current is larger, the width of the trace, SWx should have wider trace then CSy.

6+2-bit PWM Mode

When PWMM of the Control Register (address 60h) is 1, 6+2-bit PWM Mode is enabled. Then the final output PWM frequency is 6-bit, resolution is 8-bit. This is achieved through 6-bit PWM modulation and 2-bit dither control. For 2-bit dither, according to the 4-dither timing, each of the 4 PWM groups can add one PWM_H or no PWM_H.

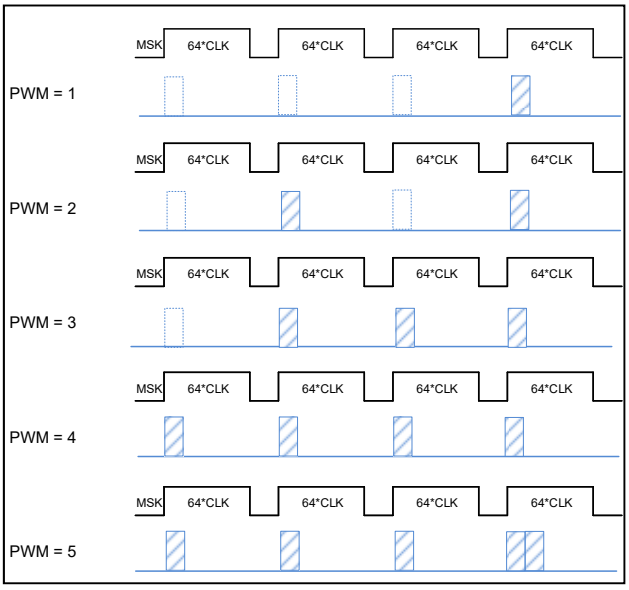


Figure 18 PWMM= “00”, 6+2-bit PWM Mode Enable

8+4-bit PWM Mode

When PWMM of the Control Register (address 60h) is 1, 8+4-bit PWM Mode is enabled. Then the final output PWM frequency is 8-bit, resolution is 12-bit. This is achieved through 8-bit PWM modulation and 4-bit dither control. For 4-bit dither, according to the 16-dither timing, each of the 16 PWM groups can add one PWM_x or no PWM_x (Where x = H or L).

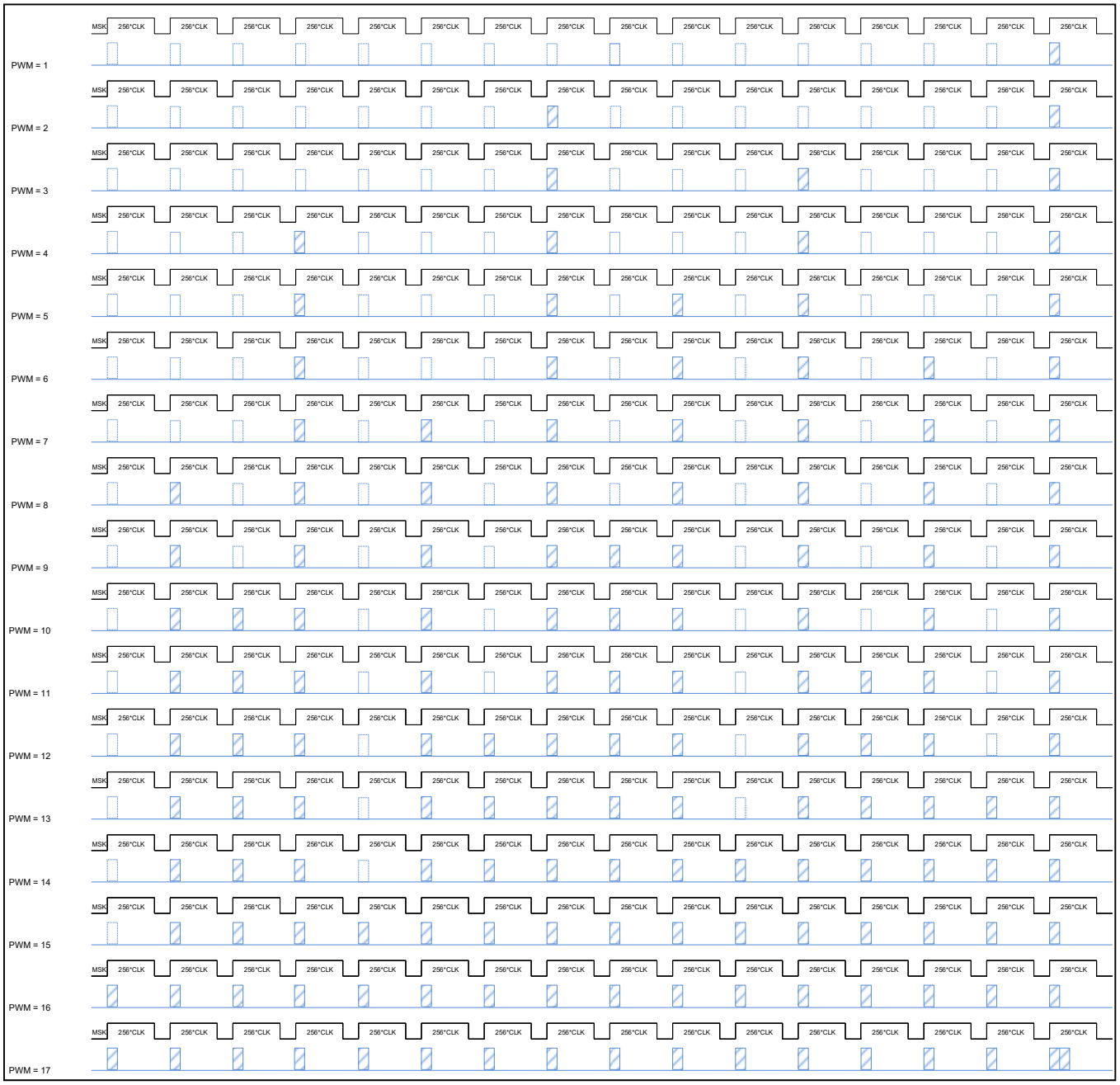


Figure 19 PWMM= “10”, 8+4-bit PWM Mode Enable

CLASSIFICATION REFLOW PROFILES

Profile Feature	Pb-Free Assembly
Preheat & Soak Temperature min (Tsmin) Temperature max (Tsmax) Time (Tsmin to Tsmax) (ts)	150°C 200°C 60-120 seconds
Average ramp-up rate (Tsmax to Tp)	3°C/second max.
Liquidous temperature (TL) Time at liquidous (tL)	217°C 60-150 seconds
Peak package body temperature (Tp)*	Max 260°C
Time (tp)** within 5°C of the specified classification temperature (Tc)	Max 30 seconds
Average ramp-down rate (Tp to Tsmax)	6°C/second max.
Time 25°C to peak temperature	8 minutes max.

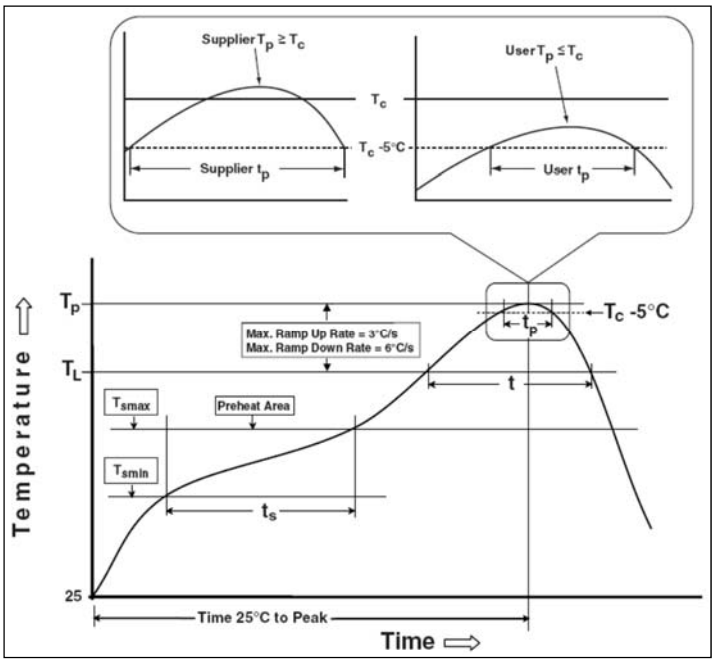
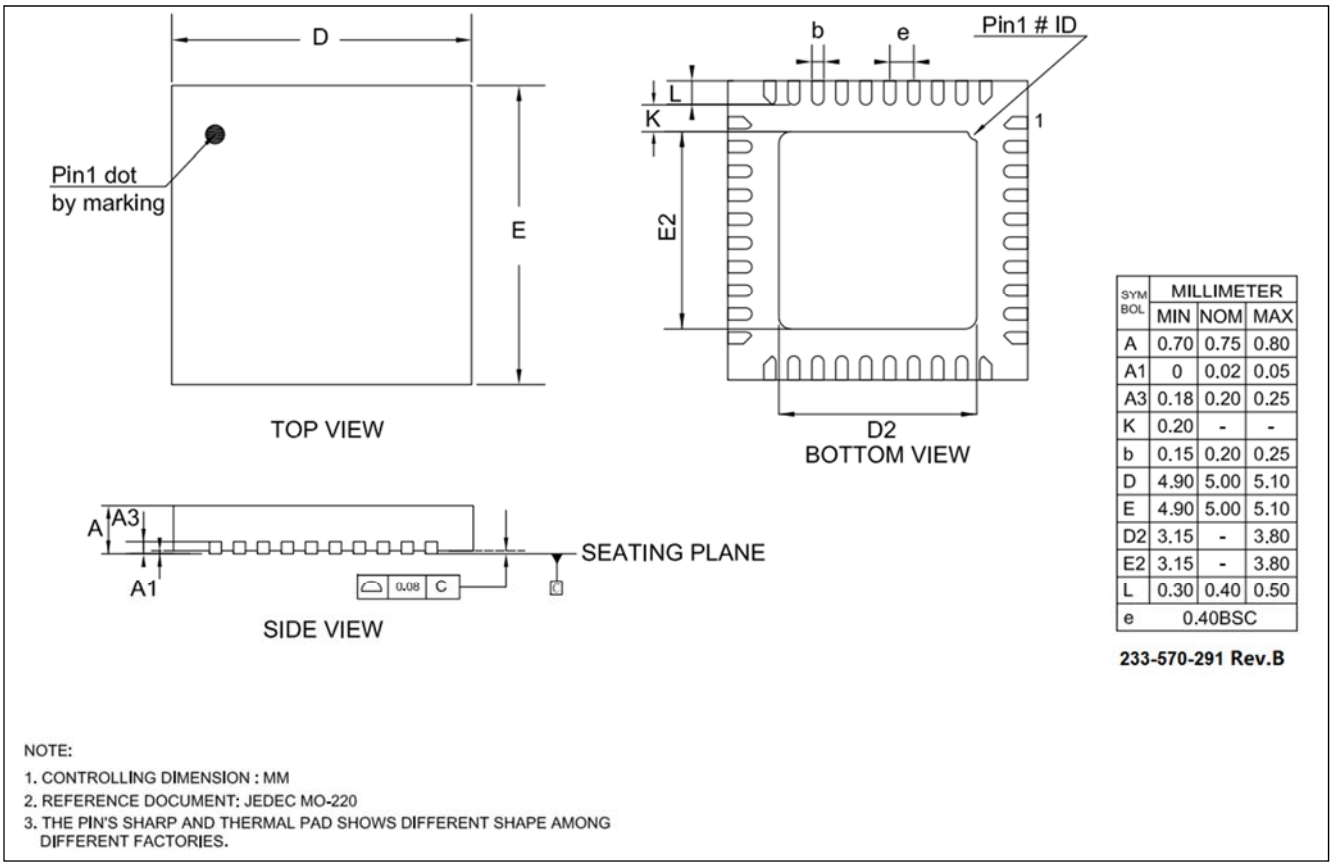


Figure 20 Classification Profile

PACKAGE INFORMATION

QFN-40



SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	0.70	0.75	0.80
A1	0	0.02	0.05
A3	0.18	0.20	0.25
K	0.20	-	-
b	0.15	0.20	0.25
D	4.90	5.00	5.10
E	4.90	5.00	5.10
D2	3.15	-	3.80
E2	3.15	-	3.80
L	0.30	0.40	0.50
e	0.40BSC		

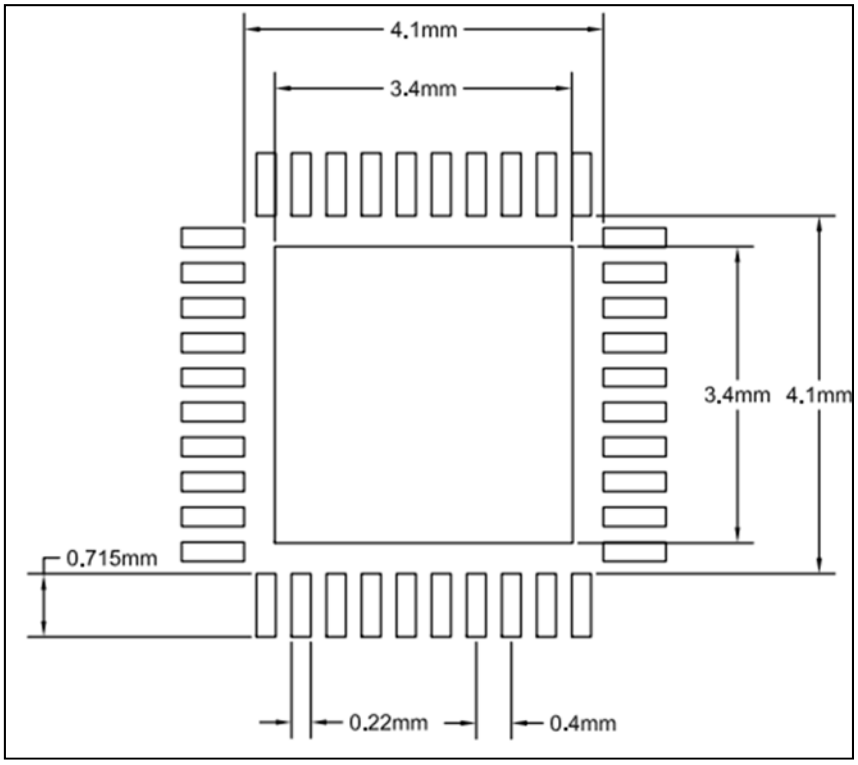
233-570-291 Rev.B

NOTE:

1. CONTROLLING DIMENSION : MM
2. REFERENCE DOCUMENT: JEDEC MO-220
3. THE PIN'S SHARP AND THERMAL PAD SHOWS DIFFERENT SHAPE AMONG DIFFERENT FACTORIES.

RECOMMENDED LAND PATTERN

QFN-40



Note:

1. Land pattern complies to IPC-7351.
2. All dimensions in MM.
3. This document (including dimensions, notes & specs) is a recommendation based on typical circuit board manufacturing parameters. Since land pattern design depends on many factors unknown (eg. user's board manufacturing specs), user must determine suitability for use.

REVISION HISTORY

Revision	Detail Information	Date
0A	Initial Release	2023.09.01
A	1.Increase Note 9 to this section describes how to configure the Open check 2.Increase 91h CS Pull Up Ability Register 3.Delete SYNC introduction of EC table 4.Increase V_{OL-SDA} of EC table 5.Modify scan number from 1~12 to 2~12. 6.Modify open/short detection introduce of Feature 7. Update EC table data 8. Increase Note8 about introduce when SL = 0, meanwhile need set GCC or PWM is 0	2024.01.24