IS31FL3766

18×6 DOTS MATRIX LED DRIVER

April 2024

GENERAL DESCRIPTION

The IS31FL3766 is a general purpose 18 × 6 (n=1~6) LED Matrix programmed via 1MHz I2C compatible interface. Each LED can be dimmed individually with 12-bit/8+4-bit/8-bit/6+2-bit PWM data and each color sink can have 8-bit DC scaling data which allowing 256 steps of linear PWM dimming and each color sink has 256 steps of DC current adjustable level and precision for smooth LED brightness control. The maximum output current of each channel is designed to be 40mA, which can be adjusted by 8-bit global control register.

Additionally, each LED open and short state can be detected, IS31FL3766 stores the open or short information in Open-Short Registers. The Open-Short Registers allow MCU to read out via I2C compatible interface. Inform MCU whether there are LEDs open or short and the locations of open or short LEDs. Proprietary algorithms are used in IS31FL3766 to minimize power bus noise caused by passive components on the power bus such as MLCC decoupling capacitor. All registers can be programmed via I2C (1MHz) bus.

The IS31FL3766 operates from 3V to 5.5V and features a very low shutdown and operational current.

IS31FL3766 is available in QFN-32 (4mm×4mm) package. It operates from 3V to 5.5V over the temperature range of -40°C to +125°C.

FEATURES

- Supply voltage range: 3.0V to 5.5V
- Support 18 (CS)× n (n=1~6) matrix configuration
- Individual 12-bit/8+4-bit/8-bit /6+2-bit PWM control steps
- Constant-current output range: 40mA
- 288kHz PWM Frequency (@6+2-bit PWM)
- Ultra-low I_{CC} when PWM frequency is 4.5kHz (280μA, 6+2-bit mode, $I_{OUT(PEAK)}$=2.9mA)
- Each color sink (CSy) 8-bit DC current steps
- Global 256 steps current setting
- 1MHz I2C-compatible interface
- State lookup registers
- Random switching sequencing to mitigate power ripple, EMI, and audible noise
- For matrix scanning operation
  - Built-in de-ghosting circuit
  - Reduced inactive LED reverse bias to improve LED reliability
- LED open/short detection accessible to I2C
- Group phase shift (180-degree) to reduce audible noise and power ripple
- Support spread spectrum operation for PWM clock to reduce EMI
- Software shutdown mode
- Operating temperature: -40°C to 125°C
- QFN-32 (4mm×4mm) package
- RoHS & Halogen-Free Compliance
- TSCA Compliance

APPLICATIONS

- RGB keyboard
- LED display for hand-held devices

TYPICAL APPLICATION CIRCUIT

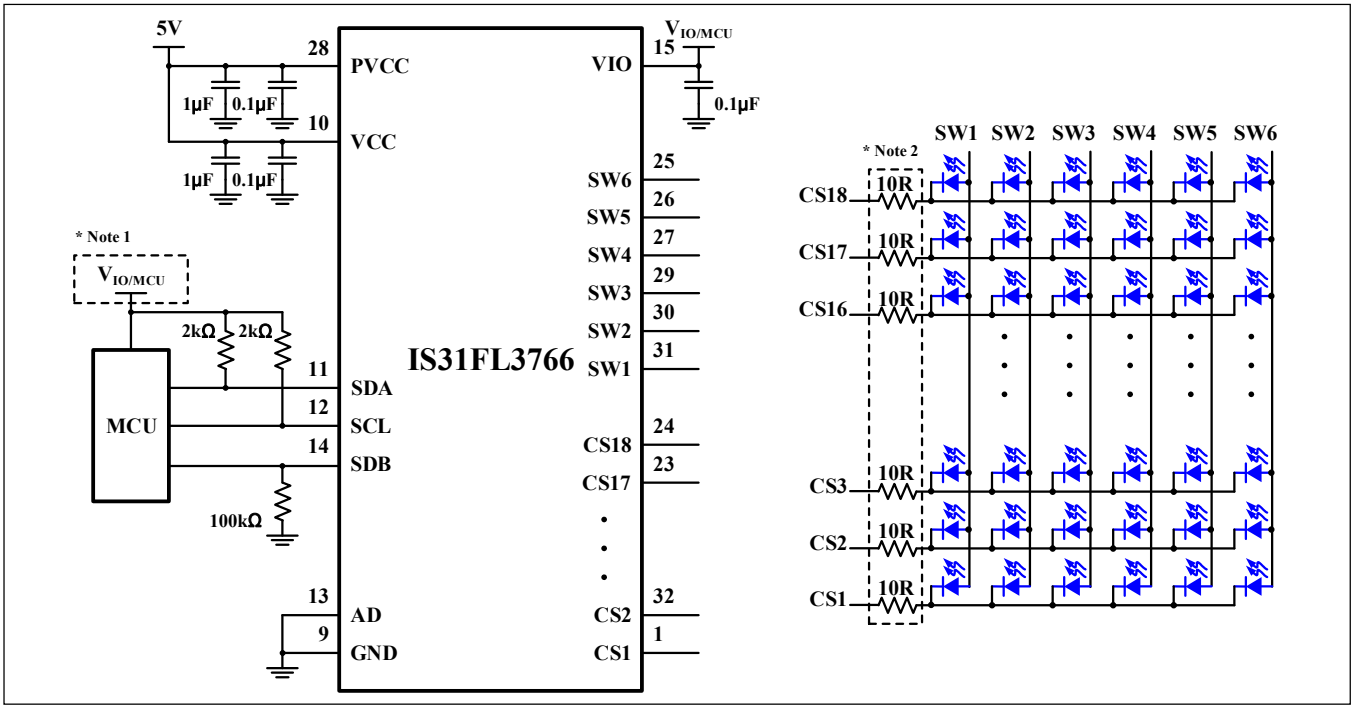


Figure 1 Typical Application Circuit (18×6, LED)

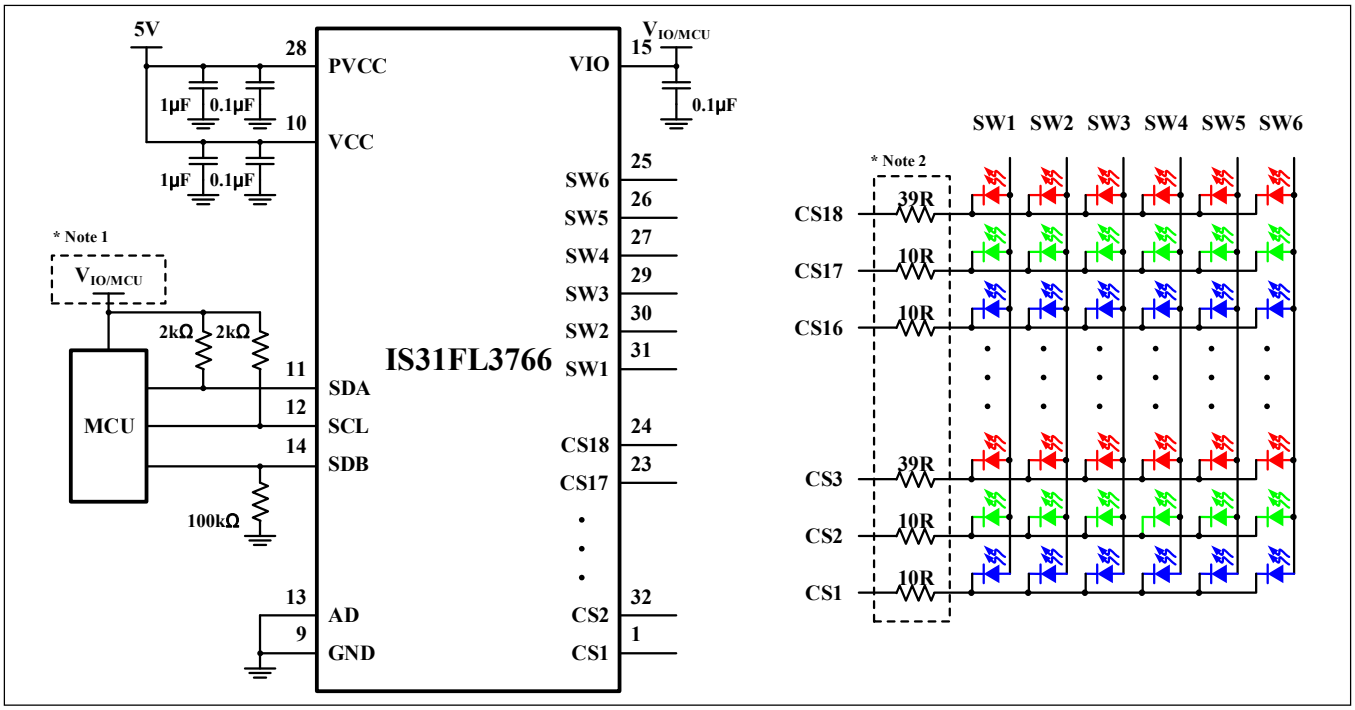
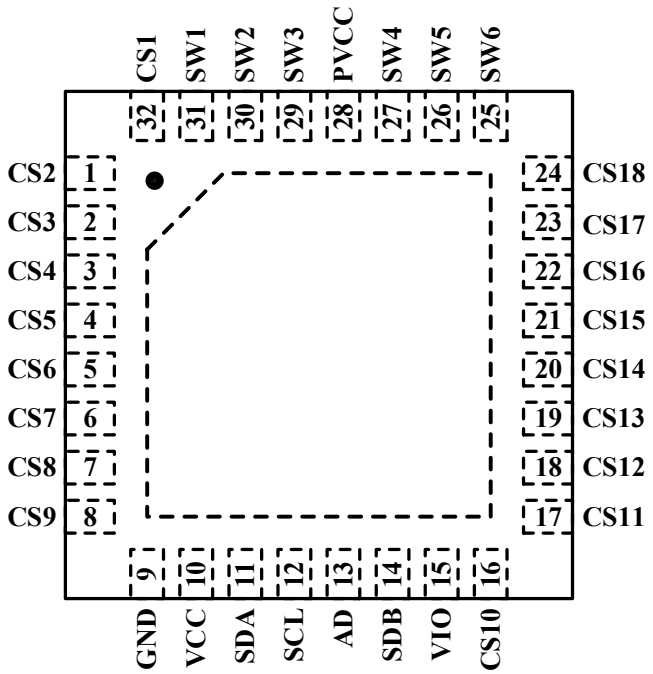


Figure 2 Typical Application Circuit (18×6, RGB)

Note 1: The V_{IH} of I2C bus should be not higher than V_{CC}. And if V_{IH} is lower than 3.0V, it is recommended add a level shift circuit to avoid extra shutdown current.

Note 2: These optional resistors are for offloading the thermal dissipation ($P=I^2R$) away from the IS31FL3766, it is determined by PV_{CC}, I_{OUT} (current of CSy), V_F of LED, V_{CS} of CSy headroom voltage, V_{SW} of SWx headroom voltage. $R_{LED}= (PV_{CC}-V_{SW}-V_F-V_{CS})/I_{OUT}$. It is optional or 10Ω recommended for white/blue/green LEDs, 39Ω recommended for red/yellow/orange LEDs when PV_{CC}=5V and single LED application.

PIN CONFIGURATION

Package	Pin Configuration (Top View)
QFN-32	

PIN DESCRIPTION

No.	Pin	Description
1~8,16~24,32	CS1~CS18	Current sink pin for LED matrix.
9	GND	Power GND and analog GND.
10	VCC	Analog and digital circuits.
11	SDA	I2C serial data.
14	SDB	Shutdown pin.
13	AD	AD of I2C.
12	SCL	I2C serial clock.
15	VIO	Power for communication block.
25~27,29~31	SW1~SW6	Power SW.
28	PVCC	Power for current source SW.
	Thermal Pad	Connect to GND.

ORDERING INFORMATION

Industrial Range: -40°C to +125°C

Order Part No.	Package	QTY/Reel
IS31FL3766-QFLS4-TR	QFN-32, Lead-free	2500

ABSOLUTE MAXIMUM RATINGS

Supply voltage, V_{CC}	-0.3V ~+6.0V
Voltage at any input pin	-0.3V ~ V_{CC}+0.3V
Maximum junction temperature, T_{JMAX}	+150°C
Storage temperature range, T_{STG}	-65°C ~+150°C
Operating temperature range, T_A=T_J	-40°C ~ +125°C
Package thermal resistance, junction to ambient (4-layer standard test PCB based on JESD 51-2A), θ_{JA}	50.5°C/W
ESD (HBM) ESD (CDM)	±3kV ±750kV

Note 3: Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other condition beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

The following specifications apply for V_{CC} = 5V, T_A = 25°C, unless otherwise noted.

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
V_{CC}	Supply voltage		3		5.5	V
I_{CC}	Quiescent power supply current	V_{SDB}=V_{CC}= PV_{CC}=5V, I_{OUT}=40mA, all LEDs off with PWM=0x00, PFS = 72kHz@8bit mode		2.2	2.6	mA
		V_{SDB}=V_{CC}=PV_{CC}=5V, I_{OUT}=2.9mA (GCC= 0x13), SCM= "10", all LEDs off with PWM=0x00, PFS = 4.8kHz@12bit mode		1.7	2	
		V_{SDB}=V_{CC}=PV_{CC}=5V, I_{OUT}=2.9mA (GCC= 0x13), SCM= "10", all LEDs off with PWM=0x00, PFS = 4.5kHz@8bit mode		0.31	0.36	
		V_{SDB}=V_{CC}=PV_{CC}=5V, I_{OUT}=2.9mA (GCC= 0x13), SCM = "10", all LEDs off with PWM=0x00, PFS = 9kHz@6+2-bit mode		0.28	0.32	
I_{SD}	Shutdown current	V_{SDB}=0V		0.6	1	μA
		V_{SDB}= V_{CC}=PV_{CC}, Configuration Register written "0000 0000		0.6	1	
I_{OUT}	Maximum constant current of CSy	GCC=0xFF, SL=0xFF@12bit Mode	37.2	40	42.8	mA
ΔI_{MAT}	Sink current between channels	I_{OUT}= 40mA (Note 4)	-5		5	%
ΔI_{ACC}	Sink current Between device to device	I_{OUT}= 40mA (Note 5)	-7		7	%
I_{LED}	Average current on each LED I_{LED} =$I_{OUT(PEAK)}$/Duty(1/6.75)	V_{SDB}=V_{CC}=PV_{CC}=5V, PFS = 4.8kHz@12-bit Mode, PWM=0xFFF, SL=0xFF, GCC=0xFF		5.92		mA
V_{HR}	Current switch headroom voltage SWx	V_{SDB}=V_{CC}=PV_{CC}=5V, I_{SW}=720mA, GCC=0xFF, SL=0xFF		450	600	mV
	Current sink headroom voltage CSy	V_{SDB}=V_{CC}=PV_{CC}=5V, I_{CS}=40mA, GCC=0xFF, SL=0xFF		420	600	

ELECTRICAL CHARACTERISTICS (CONTINUE)

The following specifications apply for V_{CC} = 5V, T_A = 25°C, unless otherwise noted.

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
t_{SCAN}	SWx on time of scanning	V_{SDB}=V_{CC}=PV_{CC}=5V, 6+2-bit mode@48kHz	3.15	3.5	3.9	μs
		V_{SDB}=V_{CC}=PV_{CC}=5V, 12-bit mode@800Hz	180	196	217	
t_{NOL1}	Non-overlap blanking time during scan, the SWx and CSy are all off during this time	V_{SDB}=V_{CC}=PV_{CC}=5V, SRS= “000”		0.45		μs
t_{NOL2}	Delay total time for CS1 to CS 18, during this time, the SWx is on but CSy is not all turned on	V_{SDB}=V_{CC}=PV_{CC}=5V		24		ns
V_O	Open threshold	V_{CC}= 5V, I_{OUT}≥ 1mA, measured at CSy	50	100	200	V
V_S	short threshold	V_{CC}= 5V, I_{OUT}≥ 1mA, measured at (V_{CC}-V_{CSy})		V_{CC}-1	V_{CC}-0.5	V
Logic Electrical Characteristics (SCL, SDA, AD, SDB)						
V_{IL}	Logic “0” input voltage	V_{CC}=3V~5.5V, V_{IO}=1.7V~V_{CC}			0.2V_{IO}	V
V_{IH}	Logic “1” input voltage	V_{CC}=3V~5.5V, V_{IO}=1.7V~V_{CC}	0.8V_{IO}			V
V_{HYS}	Input Schmitt trigger hysteresis	V_{CC}=3.6V, V_{IO}=3.3V		0.2		V
V_{OL-SDA}	Low-level output voltage of SDA	I_{LOAD}=5mA			0.4	V
I_{IL}	Logic “0” input current	SDB=L, V_{INPUT}= L (Note 6)		5		nA
I_{IH}	Logic “1” input current	SDB=L, V_{INPUT}= H (Note 6)		5		nA

DIGITAL INPUT SWITCHING CHARACTERISTICS (NOTE 6)

Symbol	Parameter	Fast Mode			Fast Mode Plus			Units
		Min.	Typ.	Max.	Min.	Typ.	Max.	
f_{SCL}	Serial-clock frequency	-		400	-		1000	kHz
t_{BUF}	Bus free time between a STOP and a START condition	1.3		-	0.5		-	μs
$t_{HD, STA}$	Hold time (repeated) START condition	0.6		-	0.26		-	μs
$t_{SU, STA}$	Repeated START condition setup time	0.6		-	0.26		-	μs
$t_{SU, STO}$	STOP condition setup time	0.6		-	0.26		-	μs
$t_{HD, DAT}$	Data hold time	-		-	-		-	μs
$t_{SU, DAT}$	Data setup time	100		-	50		-	ns
t_{LOW}	SCL clock low period	1.3		-	0.5		-	μs
t_{HIGH}	SCL clock high period	0.7		-	0.26		-	μs
t_R	Rise time of both SDA and SCL signals, receiving	-		300	-		120	ns
t_F	Fall time of both SDA and SCL signals, receiving	-		300	-		120	ns

Note 4: I_{OUT} mismatch (bit to bit) $\triangle I_{MAT}$ is calculated:

$$\Delta I_{MAT} = \pm\left(\frac{I_{OUT(MAX)} - I_{OUT(MIN)}}{\left(\frac{I_{OUT0}+I_{OUT1}+\ldots+I_{OUT18}}{18} \times 2\right)}\right) \times 100\%$$

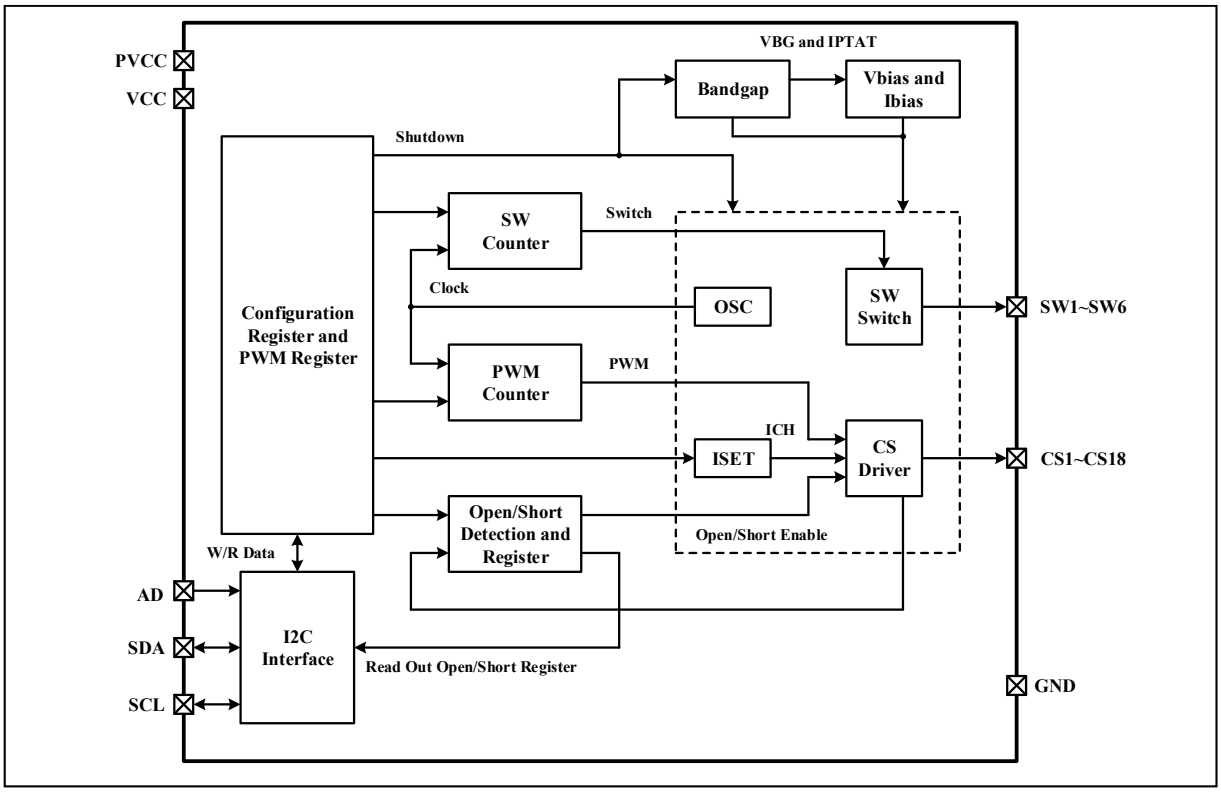
Note 5: I_{OUT} accuracy (device to device) $\triangle I_{ACC}$ is calculated:

$$\Delta I_{ACC} = \pm MAX\left(\frac{I_{OUT(MIN)} - I_{OUT(IDEAL)}}{I_{OUT(IDEAL)}}\right) \times 100\%$$

Where $I_{OUT(IDEAL)}$= 40mA.

Note 6: Guaranteed by design.

FUNCTIONAL BLOCK DIAGRAM



DETAILED DESCRIPTION

I2C INTERFACE

IS31FL3766 uses a serial bus, which conforms to the I2C protocol, to control the chip's functions with two wires: SCL and SDA. The IS31FL3766 has a 7-bit slave address (A7:A1), followed by the R/W bit, A0. Set A0 to "0" for a write command and set A0 to "1" for a read command. The value of bits A4 : A2 are decided by the connection of the AD pin.

Table 1 Slave Address:

AD	A7:A5	A4:A1	A0
GND	110	0000	0/1
SCL		0101	
SDA		1010	
VCC		1111	

AD connected to GND, (A4: A1)=0000;
AD connected to SCL, (A4: A1)=0101;
AD connected to SDA, (A4: A1)=1010;
AD connected to VCC, (A4: A1)=1111;

The SCL line is uni directional. The SDA line is bi-directional (open drain) with a pull-up resistor (typically 400kHz I2C with 4.7kΩ, 1MHz I2C with 2kΩ). The maximum clock frequency specified by the I2C standard is 1MHz. In this discussion, the master is the microcontroller, and the slave is the IS31FL3766.

The timing diagram for the I2C is shown in Figure 3. The SDA is latched in on the stable high level of the SCL. When there is no interface activity, the SDA line should be held high.

The "START" signal is generated by lowering the SDA signal while the SCL signal is high. The start signal will alert all devices attached to the I2C bus to check the incoming address against their own chip address.

The 8-bit chip address is sent next, most significant bit first. Each address bit must be stable while the SCL level is high.

After the last bit of the chip address is sent, the master checks for the IS31FL3766's acknowledge. The master releases the SDA line high (through a pull-up resistor). Then the master sends an SCL pulse. If the IS31FL3766 has received the address correctly, then it holds the SDA line low during the SCL pulse. If the SDA line is not low, then the master should send a "STOP" signal (discussed later) and abort the transfer.

Following acknowledge of IS31FL3766, the register address byte is sent, most significant bit first. IS31FL3766 must generate another acknowledge indicating that the register address has been received.

Then 8-bit of data byte are sent next, most significant bit first. Each data bit should be valid while the SCL level is stable high. After the data byte is sent, the IS31FL3766 must generate another acknowledge to indicate that the data was received.

The "STOP" signal ends the transfer. To signal "STOP", the SDA signal goes high while the SCL signal is high.

ADDRESS AUTO INCREMENT

To write multiple bytes of data into IS31FL3766, load the address of the data register that the first data byte is intended for. During the IS31FL3766 acknowledge of receiving the data byte, the internal address pointer will increment by one. The next data byte sent to IS31FL3766 will be placed in the new address, and so on. The auto increment of the address will continue if data continues to be written to IS31FL3766 (Figure 6).

READING OPERATION

Most of the registers can be read.

To read the registers, after I2C start condition, the bus master must send the IS31FL3766 device address with the R/$\overline{W}$ bit set to "0", followed by the register address which determines which register is accessed. Then restart I2C, the bus master should send the IS31FL3766 device address with the R/$\overline{W}$ bit set to "1". Data from the register defined by the command byte is then sent from the IS31FL3766 to the master (Figure 7).

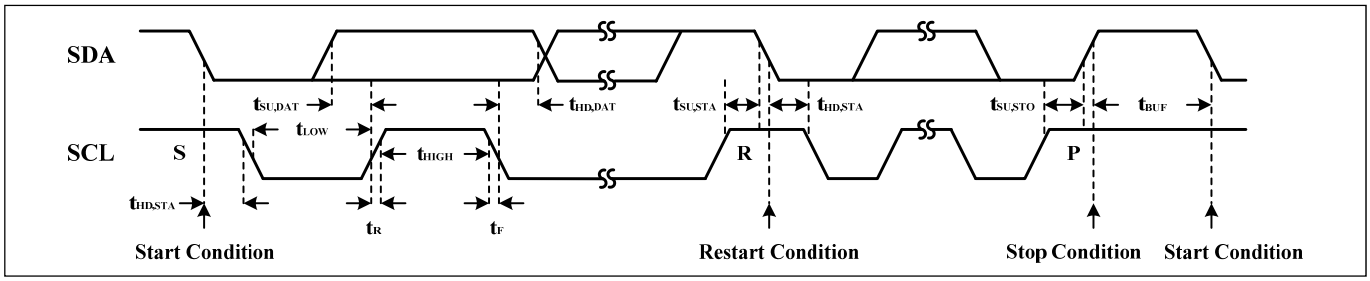


Figure 3 I2C Interface Timing

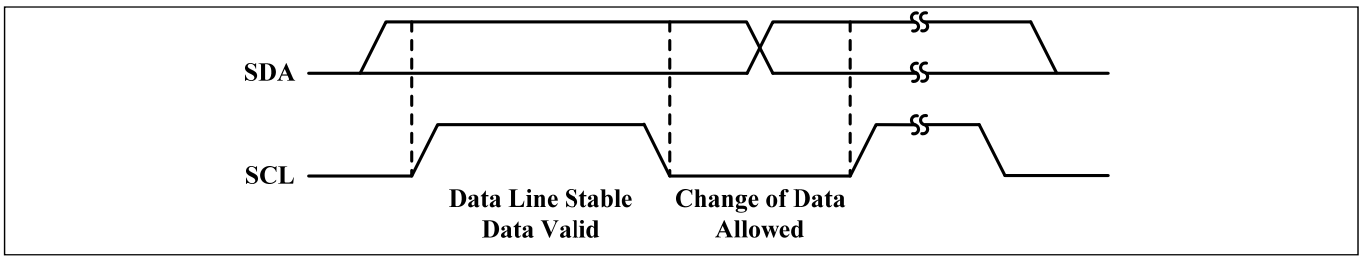


Figure 4 I2C Bit Transfer

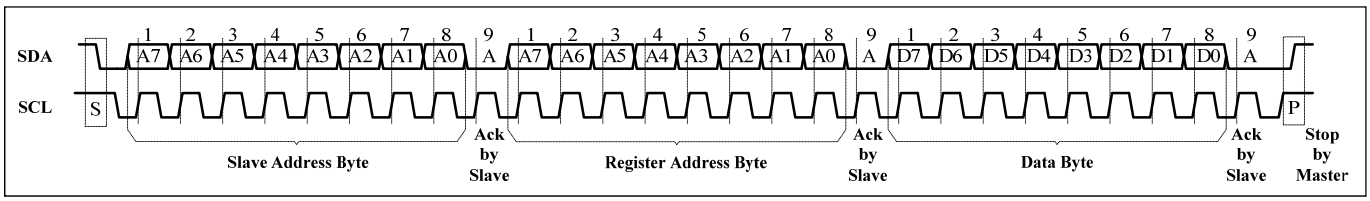


Figure 5 I2C Writing to IS31FL3766 (Typical)

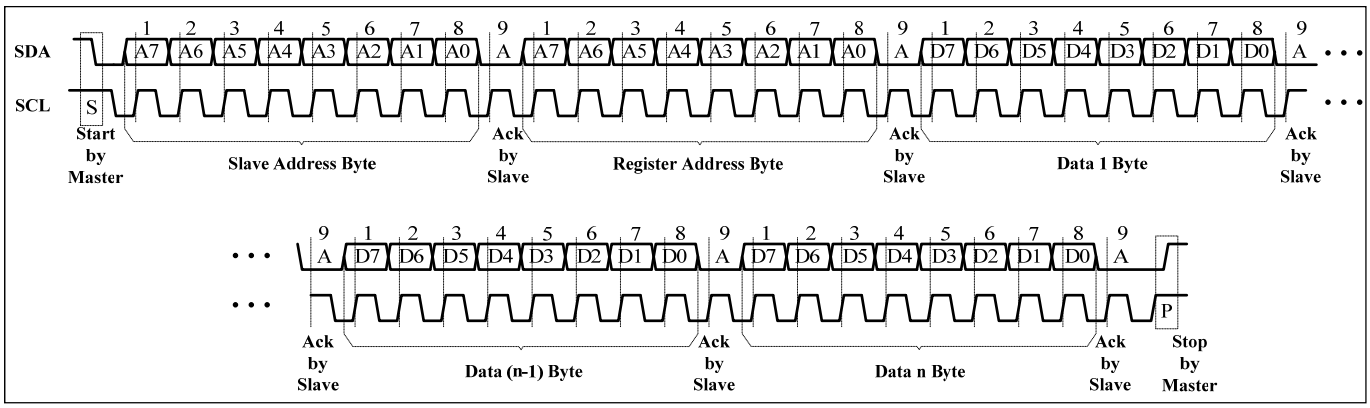


Figure 6 I2C Writing to IS31FL3766 (Automatic Address Increment)

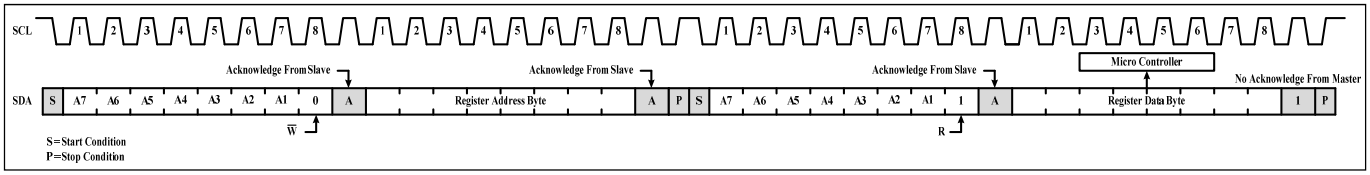


Figure 7 I2C Reading from IS31FL3766

Register Definition-1

Address	Name	Function	Table	R/W	Default
FEh	Command Register	Available Page 0 to Page 1 Registers	3	W	0000 0000
FFh	Command Register Write lock	To lock/unlock Command Register	4	R/W	0000 0000

REGISTER CONTROL WITH I2C

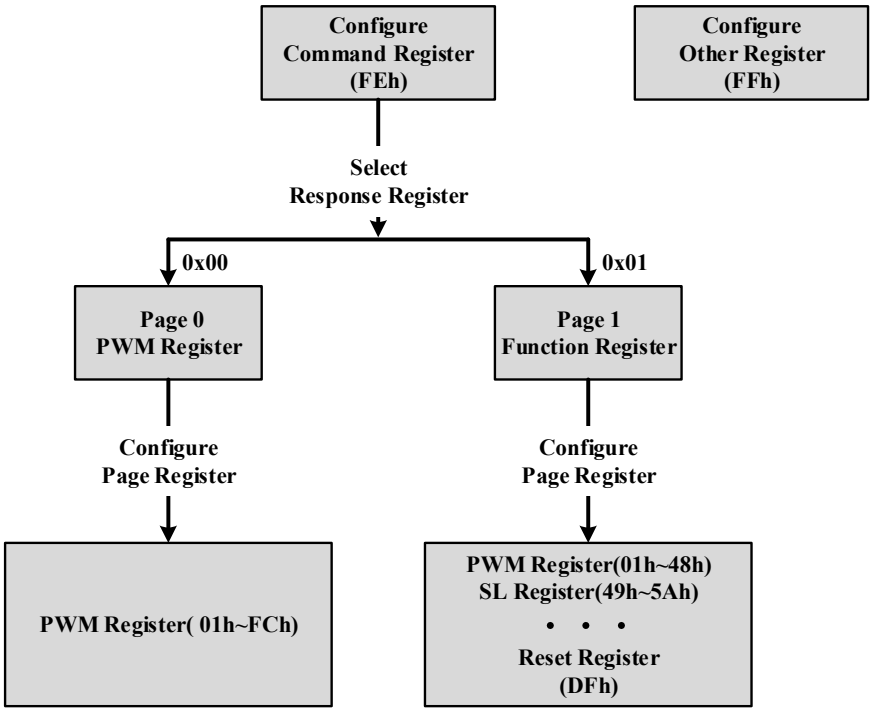


Table 2 FEh Command Register (Write Only)

Data	Function
0000 0000	Point to Page 0 (PG0, LED PWM Register is available)
0000 0001	Point to Page 1 (PG1, Function Register is available)

Note 7: FFh is locked when power up, need to unlock this register before write command to it. See Table 3 for detail.

The Command Register should be configured first after writing in the slave address to choose the available register. Then write data in the choosing register. Power up default state is "0000 0000".

For example, when write "0000 0001" in the Command Register (FEh), the data which writing after will be stored in Function Register is available (Page1).

Table 3 FFh Command Register Write Lock (Read/Write)

Bit	D7:D0
Name	CRWL
Default	0000 0000

To select the PG0~PG1, need to unlock this register first, with the purpose to avoid misoperation of this register. When FFh is written with 0xC5, FEh is allowed to modify once, after the FEh is modified the FFh will reset to be 0x00 at once.

CRWL Command Register Write Lock
0x00 FEh write disable
0xC5 FEh write enable once

Register Definition-2

Address	Name	Function	Table	R/W	Default
Page 0: FEh = 0x00					
01h~F3h	PWM Register	Set PWM for each LED	4	R/W	0000 0000
Page 1: FEh = 0x01					
01h~3Fh	PWM Register	Set PWM for each LED	4	R/W	0000 0000
49h~5Ah	SL Register	Set Current for each CS channel	5	R/W	0000 0000
60h	Configuration Register	Configure the operation mode	6	R/W	0000 0000
61h	Global Current Control Register	Set the global current	7	R/W	0000 0000
62h	Pull Down/Up Resistor Selection Register	Set the pull-down resistor for SWx and pull-up resistor for CSy	8	R/W	0000 0000
63h	PFS /Random Enable Register	Set SW random enable and PWM frequency setting	9	R/W	0000 0000
64h	Spread Spectrum Register	Spread spectrum function enable	10	R/W	0000 0000
65h	Open Short Enable Register	Enable open/short detect	11	R/W	0000 0000
66h~68h	Open Short Register	Read open/short LED dot data	12	R	0000 0000
DFh	Reset Register	Reset all register to default value	-	W	0000 0000
FDh	PWM update register	Update PWM register	-	W	0000 0000

PWM Register

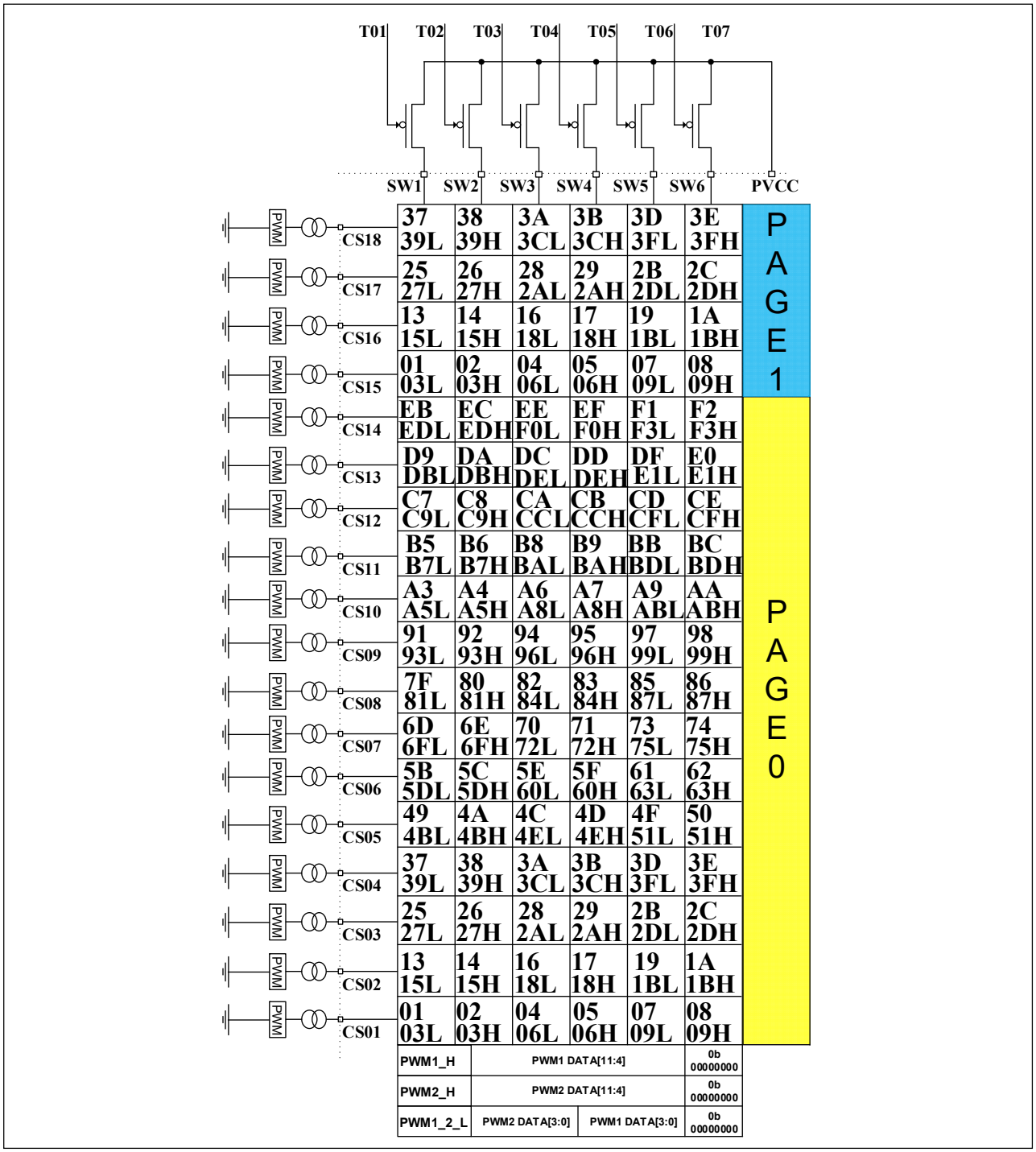


Figure 8 PWM Register

Table 4-1 Page 0 01h ~ F3h PWM Register
Table 4-2 Page 1 01h ~ 3Fh PWM Register

Page 0 SW1-CS1

Bit	01h: D7:D0		03h: D3:D0
Name	PWM_H	PWM_H	PWM_L
Default	0000	0000	0000

Page 0 SW2-CS1

Bit	02h: D7:D0		03h: D7:D4
Name	PWM_H	PWM_H	PWM_L
Default	0000	0000	0000

Page 0 SW1-CS3

Bit	04h: D7:D0		06h: D3:D0
Name	PWM_H	PWM_H	PWM_L
Default	0000	0000	0000

Page 0 SW2-CS4

Bit	05h: D7:D0		06h: D7:D4
Name	PWM_H	PWM_H	PWM_L
Default	0000	0000	0000

Page 1 SW6-CS18

Bit	3Eh: D7:D0		3Fh: D7:D4
Name	PWM_H	PWM_H	PWM_L
Default	0000	0000	0000

Each dot has a byte + a nibble to modulate the PWM duty in 256 or 4096 steps.

The high 8 bit and the low 4 bits mapping between PWM registers as Figure 8.

The value of the PWM Registers decides the average current of each LED noted I_{LED}.

I_{LED} computed by Formula (1):

8bit mode

$$I_{LED} = \frac{PWM}{256} \times I_{OUT(PEAK)} \times Duty \quad (1)$$

$$PWM = \sum_{n=0}^{7} D[n] \cdot 2^n$$

12bit mode

$$I_{LED} = \frac{PWM}{4096} \times I_{OUT(PEAK)} \times Duty \quad (1)$$

$$PWM = \sum_{n=0}^{11} D[n] \cdot 2^n$$

Where Duty is the duty cycle of SWx, see SCANING TIMING section for more information.

$$Duty = \frac{3.6\mu s}{(3.6\mu s + 0.45\mu s)} \times \frac{1}{6} \quad (2)$$

Where 3.6μs is t_{SCAN}, the period of scanning and 0.3μs is t_{NOL1}, the non-overlap time.

I_{OUT} is the output current of CSy (y=1~18),

$$I_{OUT(PEAK)} = 40.32 \times \frac{GCC}{256} \times \frac{SL}{256} \quad (3)$$

GCC is the Global Current Control register, SL is the Scaling Register value as Table 9.D[n] stands for the individual bit value, 1 or 0, in location n.

For example: in 8-bit mode, if D7:D0=1011 0101 (0xB5, 181), GCC=1111 1111, SL=1111 1111:

$$I_{LED} = 40.32 \times \frac{GCC}{256} \times \frac{SL}{256} \times Duty \times \frac{PWM}{256} \quad (1)$$

Table 5 Page 1 49h ~ 5Ah Scaling Register

Bit	D7:D0
Name	SL
Default	0000 0000

Note 8: When LED off by set SL = 0x00, there also should be set GCC = 0x00 or PWM = 0x00.

Scaling register control the DC output current of each CS. Each CS has a byte to modulate the scaling in 256 steps.

The value of the Scaling Register decides the peak current of each LED noted $I_{OUT(PEAK)}$.

$I_{OUT(PEAK)}$ computed by Formula (3):

$$I_{OUT(PEAK)} = 40.32 \times \frac{GCC}{256} \times \frac{SL}{256} \quad (3)$$

$$SL = \sum_{n=0}^{7} D[n] \cdot 2^n$$

I_{OUT} is the output current of CSy (y=1~18), GCC is the Global Current Control Register (PG1, 61h) value. D[n] stands for the individual bit value, 1 or 0, in location n.

For example: if GCC=1111 1111, SL=0111 1111:

$$SL = \sum_{n=0}^{7} D[n] \cdot 2^n = 127$$

$$I_{OUT} = 40.32 \times \frac{255}{256} \times \frac{127}{256} = 19.92mA$$

$$I_{LED} = 19.92mA \times \frac{1}{6.75} \times \frac{PWM}{256} \quad (1)$$

Table 6 Page 1 60h Configuration Register

Bit	D7:D4	D3	D2:D1	D0
Name	SWS	-	PWMM	SSD
Default	0000	0	00	0

The Configuration Register sets operating mode of IS31FL3766.

When SSD is “0”, IS31FL3766 works in software shutdown mode and to normal operate the SSD bit should set to “1”.

SWS control the duty cycle of the SW, default mode is 1/12. Need to configure to 1/6 or below options for normal operation.

SSD	Software Shutdown Control
0	Software shutdown
1	Normal operation

PWMM	PWM mode
00	6+2-bit
01	8-bit
10	8+4-bit
11	12-bit

SWS	SWx Setting
1011	SW1~SW6, 1/6
1100	SW1~SW5, 1-5
1110	SW1&2~SW5&6, 1/3
1111	&SW1-3~&SW4-6, 1/2

Table 7 Page1 61h Global Current Control Register

Bit	D7:D0
Name	GCC
Default	0000 0000

The Global Current Control Register modulates all CSy (x=1~18) DC current which is noted as I_{OUT} in 256 steps.

I_{OUT} is computed by the Formula (3):

$$I_{OUT(PEAK)} = 40.32 \times \frac{GCC}{256} \times \frac{SL}{256} \quad (3)$$

$$GCC = \sum_{n=0}^{7} D[n] \cdot 2^n$$

Where D[n] stands for the individual bit value, 1 or 0, in location n.

Table 8 Page1 62h Pull Down/Up Resistor Selection Register

Bit	D7	D6:D4	D3	D2:D0
Name	PHC	SWPDR	-	CSPUR
Default	0	000	0	000

PHC control 180-degree phase enable or disable. When PHC= “1”, the 180-degree phase is enabled, and the phase difference between CS is about 180-degree.

SWPDR control SWx pull down to setting voltage when SWx closed. For example, if SWPDR= “100”, that SWx will pull down to setting voltage is 2.0V when SWx closed.

CSPUR control CSy pull up to setting voltage when CSy closed. For example, if CSPUR= “101”, that CSy will pull up to setting voltage is PV_{CC}-1.6V when CSy closed.

Please check De-Ghost Function section for more information in Application Information.

PHC	Phase choice
0	0-degree phase
1	180-degree phase

SWPDR	SWx Pull down Selection Bit
000	floating
001	3.2V
010	2.8V
011	2.4V
100	2.0V
101	1.6V
110	1.2V
111	GND

CSPUV	CSy Pull up Selection Bit
000	floating
001	PV_{CC}-3.2V
010	PV_{CC}-2.8V
011	PV_{CC}-2.4V
100	PV_{CC}-2.0V
101	PV_{CC}-1.6V
110	PV_{CC}-1.2V
111	PV_{CC}

Table 9 Page1 63h SRS/Random Enable Register

Bit	D7	D6	D5:D4	D3	D2:D0
Name	-	-	SCM	-	SRS
Default	0	0	00		000

SCM is small current mode enable bit. If SCM = “10”, the I_{CC} will become more smaller when I_{CC} current small. If SCM = “01”, the SL will become smaller a half when IOUT current small.

PFS control PWM frequency setting bits. For example, if PWM Mode is 6+2-bit and PFS = “010”, that the PWM frequency is 72kHz and the scan frequency is 1/6 namely SWS = “1011” is 12kHz.

SCM	Small current mode
00	Disable
01	SL/2
10	Disable output OP&Make ICC smaller
11	all enable

PFS	PWM frequency setting
000	288kHz for 6+2-bit mode (Scan frequency is 48kHz) 72kHz for 8-bit mode 72kHz for 8+4-bit mode 4.8kHz for 12-bit mode
001	144kHz for 6+2-bit mode 36kHz for 8-bit mode 36kHz for 8+4-bit mode 2.4kHz for 12-bit mode
010	72kHz for 6+2-bit mode 18kHz for 8-bit mode 18kHz for 8+4-bit mode
011	36kHz for 6+2-bit mode

	9kHz for 8-bit mode
100	18kHz for 6+2-bit mode
	4.5kHz for 8-bit mode
101	9kHz for 6+2-bit mode
	2.25kHz for 8-bit mode
	2.25kHz for 8+4-bit mode
110	4.5kHz for 6+2-bit mode

Table 10 Page1 64h Spread Spectrum Register

Bit	D7:D6	D4	D3:D2	D1:D0
Name	-	SSP	RNG	CLT
Default	000	0	00	00

When SSP enable, the spread spectrum function will be enabled and the RNG & CLT bits will adjust the range and cycle time of spread spectrum function.

Only >=2.5MHz have effect.

SSP Spread spectrum function enable

0	Disable
1	Enable

RNG Spread spectrum range

00	±10%
01	±15%

CLT Spread spectrum cycle time

00	4.0ms
01	2.2ms
10	1.5ms
11	1.1ms

Table 11 Page1 65h Open Short Enable Register

Bit	D7:D6	D5:D4	D3:D0
Name	O/S	-	OS of SW
Default	00	00	0000

(Page 1, 65h) register stores the open and short detect information of LED string. When O/S is “00”, open and short detect is disable, if O/S is “10”, open detect enable, if O/S is “11”, short detect enable.

OS of SW bits choose where SW to detect open or short. For example, when OS of SW = “0010”, that select SW3 to detect open or short.

Please check Open/Short detect function section for more information in Application Information.

O/S Select open or short

0x	Disable
10	Open(Note 10)
11	Short

OS of SW Select which SW to detect

0000	SW1
0001	SW2
0010	SW3
0011	SW4
0100	SW5
0101	SW6

Table12-1 Page1 66h Open Short Register

Bit	D7:D6	D5:D0
Name	-	CS06:CS01
Default	00	00 0000

Table 12-2 Page1 67h Open Short Register

Bit	D7:D6	D5:D0
Name	-	CS12:CS07
Default	00	00 0000

Table 12-3 Page1 68h Open Short Register

Bit	D7:D6	D5:D0
Name	-	CS18:CS13
Default	00	00 0000

After setting 65h, 66~68h can be read for the open or short information of each LED dot.

DFh Reset Register

Once user writes the Reset Register with 0xAE, IS31FL3766 will reset all the IS31FL3766 registers to their default value. On initial power-up, the IS31FL3766 registers are reset to their default values for a blank display.

FDh Update Register

When SDB= “H” and SSD= “1”, a written of “0000 0000” to FDh is to update the PWM Registers (Page 0, 01h~FCh & Page 1 01h~48h) values.

APPLICATION INFORMATION

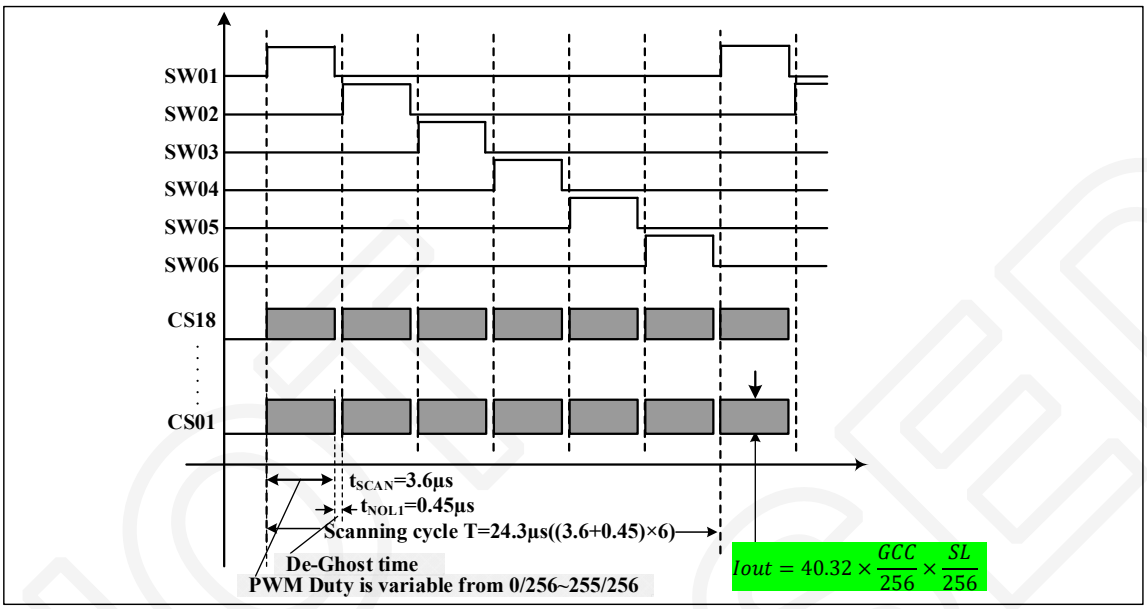


Figure 9 Scanning Timing

SCANING TIMING

As shown in Figure 9 above, the SW1~SW6 is turned on by serial, LED is driven 6 by 6 within the SWx (x=1~6) on time (SWx, x=1~6 is source and it is high when LED on), including the non-overlap blanking time during scan, the duty cycle of SWx (active high, x=1~6) is:

$$Duty = \frac{3.6\mu s}{(3.6\mu s+0.45\mu s)} \times \frac{1}{6} = \frac{1}{6.75} \qquad (2)$$

Where 3.6μs is t_{SCAN}, the period of scanning and 0.45μs is t_{NOL1}.

And the scan frequency is 1/n of PWM frequency, where n is SW scan number that can be choose by SWS of 60h register and the number of select range as 1, 2, 3 … 6. For example, when n = 6, namely SWS = 1011, and the PWM frequency is 288kHz, the scan frequency is 1/6 of PWM frequency is 48kHz.; or when n = 5, the scan frequency is 1/5 of PWM frequency is 57.6kHz…

PWM CONTROL

After setting the I_{OUT} and GCC, the brightness of each LEDs (LED average current (I_{LED})) can be modulated with 256 steps by PWM Register, as described in Formula (1).

$$I_{LED} = \frac{PWM}{256} \times I_{OUT\,(PEAK)} \times Duty \qquad (1)$$

Where PWM is PWM Registers (PG0, 00h~FCh /PG1, 00h~48h) data showing in Table 7.

For example, if PWM= 255, and GCC= 255, Scaling= 255, then

$$I_{OUT(PEAK)} = 40.32 \times \frac{255}{256} \times \frac{255}{256} = 40mA$$

$$I_{LED} = 40mA \times \frac{1}{6.75} \times \frac{PWM}{256}$$

Writing new data continuously to the registers can modulate the brightness of the LEDs to achieve a breathing effect.

GAMMA CORRECTION

To perform a better visual LED breathing effect, we recommend using a gamma corrected PWM value to set the LED intensity. This results in a reduced number of steps for the LED intensity setting but causes the change in intensity to appear more linear to the human eye.

Gamma correction, also known as gamma compression or encoding, is used to encode linear luminance to match the non-linear characteristics of display. Since the IS31FL3766 can modulate the brightness of the LEDs with 256 steps, a gamma correction function can be applied when computing each subsequent LED intensity setting such that the change in brightness matches the human eye's brightness curve.

Table 14 32 Gamma Steps with 256 PWM Steps

C(0)	C(1)	C(2)	C(3)	C(4)	C(5)	C(6)	C(7)
0	1	2	4	6	10	13	18
C(8)	C(9)	C(10)	C(11)	C(12)	C(13)	C(14)	C(15)
22	28	33	39	46	53	61	69
C(16)	C(17)	C(18)	C(19)	C(20)	C(21)	C(22)	C(23)
78	86	96	106	116	126	138	149
C(24)	C(25)	C(26)	C(27)	C(28)	C(29)	C(30)	C(31)
161	173	186	199	212	226	240	255

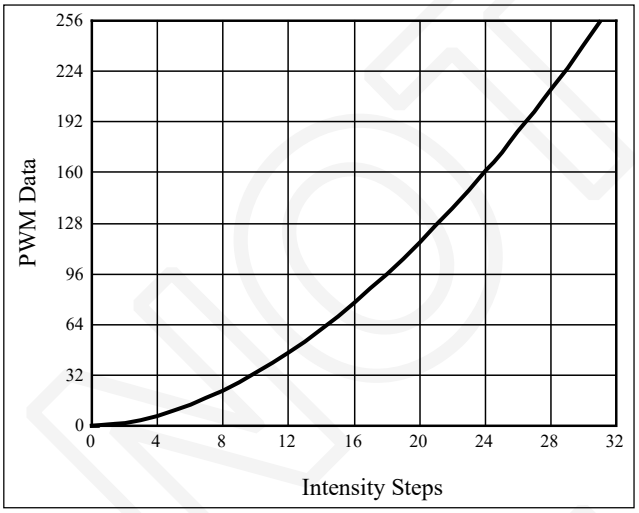


Figure 10 Gamma Correction (32 Steps)

Choosing more gamma steps provides for a more continuous looking breathing effect. This is useful for very long breathing cycles. The recommended configuration is defined by the breath cycle T. When T=1s, choose 32 gamma steps, when T=2s, choose 64 gamma steps. The user must decide the final number of gamma steps not only by the LED itself, but also based on the visual performance of the finished product.

Table 15 64 Gamma Steps with 256 PWM Steps

C(0)	C(1)	C(2)	C(3)	C(4)	C(5)	C(6)	C(7)
0	1	2	3	4	5	6	7
C(8)	C(9)	C(10)	C(11)	C(12)	C(13)	C(14)	C(15)
8	10	12	14	16	18	20	22
C(16)	C(17)	C(18)	C(19)	C(20)	C(21)	C(22)	C(23)
24	26	29	32	35	38	41	44
C(24)	C(25)	C(26)	C(27)	C(28)	C(29)	C(30)	C(31)
47	50	53	57	61	65	69	73
C(32)	C(33)	C(34)	C(35)	C(36)	C(37)	C(38)	C(39)
77	81	85	89	94	99	104	109
C(40)	C(41)	C(42)	C(43)	C(44)	C(45)	C(46)	C(47)
114	119	124	129	134	140	146	152
C(48)	C(49)	C(50)	C(51)	C(52)	C(53)	C(54)	C(55)
158	164	170	176	182	188	195	202
C(56)	C(57)	C(58)	C(59)	C(60)	C(61)	C(62)	C(63)
209	216	223	230	237	244	251	255

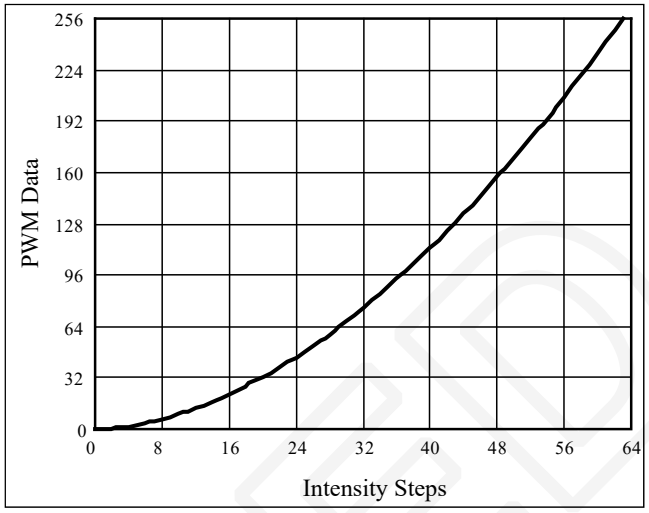


Figure 11 Gamma Correction (64 Steps)

Note 9: The data of 32 gamma steps is the standard value and the data of 64 gamma steps is the recommended value.

OPERATING MODE

IS31FL3766 can only operate in PWM Mode. The brightness of each LED can be modulated with 256 steps by PWM registers. For example, if the data in PWM Register is “0000 0100”, then the PWM is the fourth step.

Writing new data continuously to the registers can modulate the brightness of the LEDs to achieve a breathing effect.

OPEN/SHORT DETECT FUNCTION

IS31FL3766 has open and short detect bit for each LED.

By setting the O/S bits of the Configuration Register (PG1, 65h) from “00” to “10” or “11” the LED Open/short Register will start to store the open/short information and after at least 2 scanning cycles and the MCU can get the open/short information by reading the 66h~68h, for those dots are turned off via LED Scaling Registers (PG1,49h~5Ah), the open/short data will not get refreshed when setting the O/S bit of the Configuration Register.

To get the correct open and short information, two configurations need to set before setting the O/S bits:

1 0x0F≤ GCC≤ 0x40
2 62h= 0x00

Where GCC is the Global Current Control Register (PG1, 61h) and 62h is the Pull Down/UP Resistor Selection Register and set to 0x00 is to disable the SWx pull-down and CSy pull-up function.

Th Open circuit or short circuit detection only needs to be enabled once to obtain the LED open circuit or short circuit data in real time

Note 10: When open detect is enable, if PWM ≠ 0 and SL = 0, there should be set GCC = 0.

DE-GHOST FUNCTION

The “ghost” term is used to describe the behavior of an LED that should be OFF but instead glows dimly when another LED is turned ON. A ghosting effect typically can occur when multiplexing LEDs. In matrix architecture any parasitic capacitance found in the constant-current outputs or the PCB traces to the LEDs may provide sufficient current to dimly light an LED to create a ghosting effect.

To prevent this LED ghost effect, the IS31FL3766 has integrated Pull down resistors for each SWx (x=1~6) and pull up resistors for each CSy (y=1~18). Select the right SWx Pull down resistor (PG1, 62h) and CSy Pull up resistor (PG1, 62h) which eliminates the ghost LED for a particular matrix layout configuration.

Typically, selecting the SWx Pull down to 3.2V，CS Pull up to PVCC-3.2V will be sufficient to eliminate the LED ghost phenomenon.

The SWx Pull down resistors and CSy Pull up resistors are active only when the CSy/SWx output working the OFF state and therefore no power is lost through these resistors.

SHUTDOWN MODE

Shutdown mode can be used as a means of reducing power consumption. During shutdown mode all registers retain their data.

Software Shutdown

By setting SSD bit of the Configuration Register (PG1, 60h) to “0”, the IS31FL3766 will operate in software shutdown mode. When the IS31FL3766 is in software shutdown, all current sources are switched off, so that the matrix is blanked. All registers can be operated. Typical current consume is 0.6μA.

Hardware Shutdown

The chip enters hardware shutdown when the SDB pin is pulled low. All analog circuits are disabled during hardware shutdown, typical the current consume is 0.6μA.

The chip releases hardware shutdown when the SDB pin is pulled high. During hardware shutdown state Function Register can be operated.

If V_{CC} has risk drop below 1.75V but above 0.1V during SDB pulled low, please re-initialize all Function Registers before SDB pulled high.

LAYOUT

Because of the chip consumes lots of power. Please consider below factors when layout the PCB.

1. The V_{CC} (PVCC, AVCC) capacitors need to close to the chip and the ground side should well connected to the GND of the chip.

2. The thermal pad should connect to ground pins and the PCB should have the thermal pad too, usually this pad should have 16 or 25 via thru the PCB to other side’s ground area to help radiate the heat. About the thermal pad size, please refer to the land pattern of each package.

3. The CSy pins maximum current is 40mA, and the SWx pins maximum current is larger, the width of the trace, SWx should have wider trace then CSy.

6+2-Bit PWM MODE

When PWMM of the Control Register (address 60h) is 1, 6+2-bit PWM Mode is enabled. Then the final output PWM frequency is 6-bit, resolution is 8-bit. This is achieved through 6-bit PWM modulation and 2-bit dither control. For 2-bit dither, according to the 4-dither timing, each of the 4 PWM groups can add one PWM_H or no PWM_H.

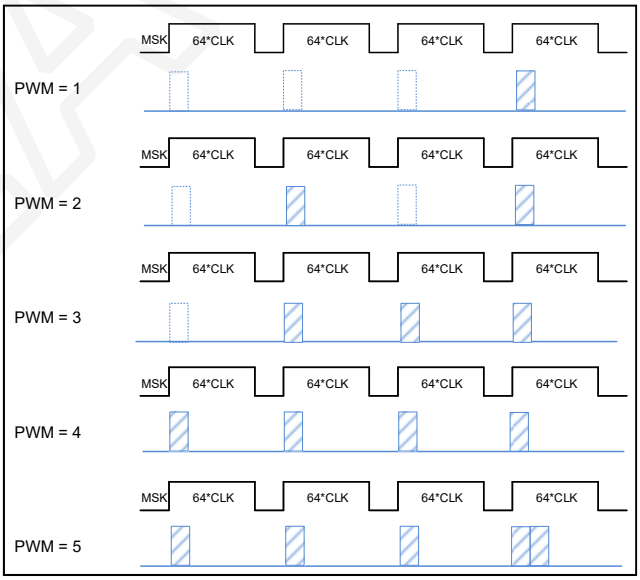


Figure 12 PWMM= “00”, 6+2-bit PWM Mode Enable

8+4-Bit PWM MODE

When PWMM of the Control Register (address 60h) is 1, 8+4-bit PWM Mode is enabled. Then the final output PWM frequency is 8-bit, resolution is 12-bit. This is achieved through 8-bit PWM modulation and 4-bit dither control. For 4-bit dither, according to the 16-dither timing, each of the 16 PWM groups can add one PWM_x or no PWM_x (Where x = H or L).

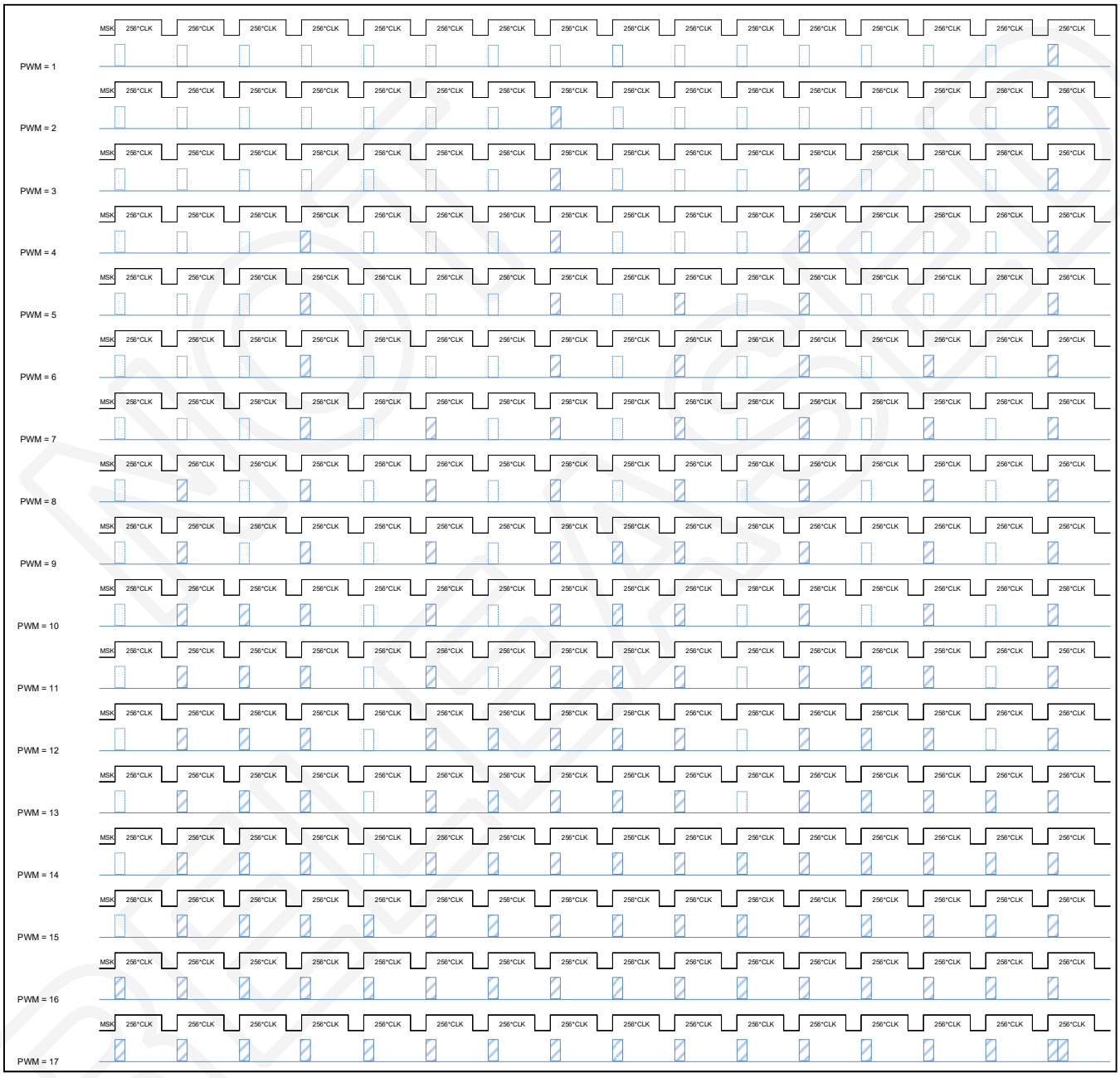


Figure 13 PWMM= “10”, 8+4-bit PWM Mode Enable

CLASSIFICATION REFLOW PROFILES

Profile Feature	Pb-Free Assembly
Preheat & Soak Temperature min (Tsmin) Temperature max (Tsmax) Time (Tsmin to Tsmax) (ts)	150°C 200°C 60-120 seconds
Average ramp-up rate (Tsmax to Tp)	3°C/second max.
Liquidous temperature (TL) Time at liquidous (tL)	217°C 60-150 seconds
Peak package body temperature (Tp)*	Max 260°C
Time (tp)** within 5°C of the specified classification temperature (Tc)	Max 30 seconds
Average ramp-down rate (Tp to Tsmax)	6°C/second max.
Time 25°C to peak temperature	8 minutes max.

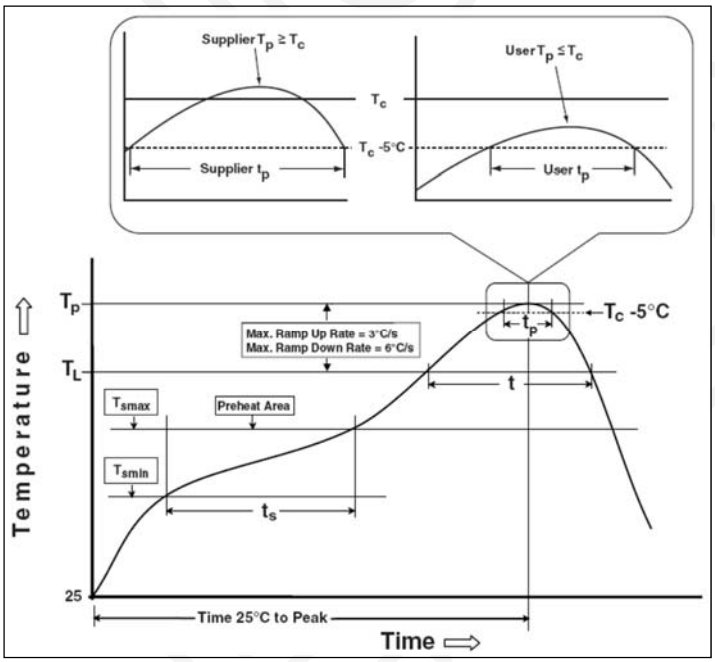
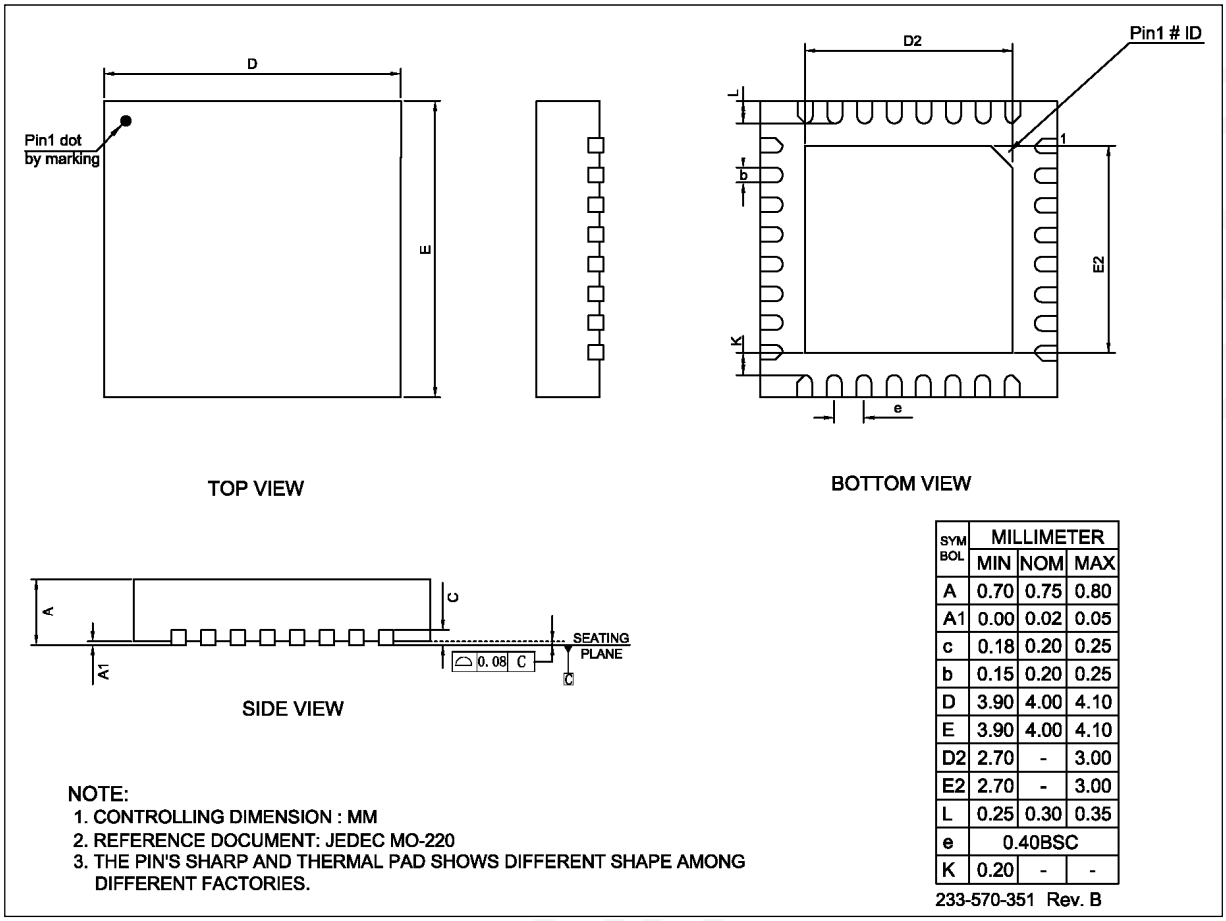


Figure 14 Classification Profile

PACKAGE INFORMATION

QFN-32



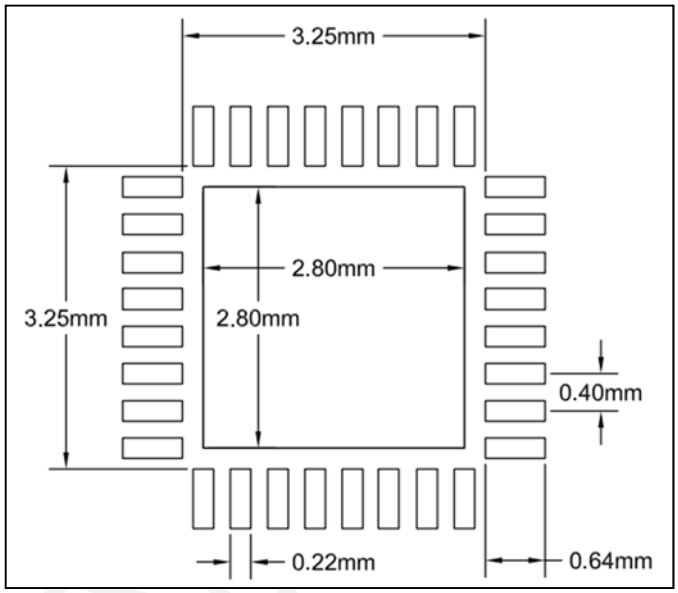
SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	0.70	0.75	0.80
A1	0.00	0.02	0.05
c	0.18	0.20	0.25
b	0.15	0.20	0.25
D	3.90	4.00	4.10
E	3.90	4.00	4.10
D2	2.70	-	3.00
E2	2.70	-	3.00
L	0.25	0.30	0.35
e	0.40BSC		
K	0.20	-	-

233-570-351 Rev. B

NOTE:
1. CONTROLLING DIMENSION : MM
2. REFERENCE DOCUMENT: JEDEC MO-220
3. THE PIN'S SHARP AND THERMAL PAD SHOWS DIFFERENT SHAPE AMONG DIFFERENT FACTORIES.

RECOMMENDED LAND PATTERN

QFN-32



Note:

1. Land pattern complies to IPC-7351.
2. All dimensions in MM.
3. This document (including dimensions, notes & specs) is a recommendation based on typical circuit board manufacturing parameters. Since land pattern design depends on many factors unknown (eg. user's board manufacturing specs), user must determine suitability for use.

REVISION HISTORY

Revision	Detail Information	Date
0A	Initial Release	2023.09.01
A	1. Update EC table 2. Release to Mass-Production	2024.03.18