TRIAC Dimmable AC/DC LED Driver with Active PFC

March 2013
Preliminary

GENERAL DESCRIPTION

The Flicker-Free™ IS31LT3935 is a single stage current-mode LED driver optimized for high power factor and compatibility with all TRIAC dimmers. The PFC architecture enables excellent power factor over a wide range of operating line and load conditions, even with the simplest of inductor-based driver topologies, thereby reducing system cost and size while maximizing efficiency.

The IS31LT3935 LED controller features patent pending AccuDim™ flicker-free dimming technology that mimics the characteristics of an incandescent light bulb. It presents a dynamic impedance to the dimmer and integrates an active bleed circuit for true dimming performance across all dimmers.

The device is available in a tiny 10 lead DFN-EP (3mm × 3mm) package. It operates over the temperature range of -40°C to +85°C.

TYPICAL APPLICATIONS

- Dimmable Retrofit LED Lamps/Luminaries up to 30W
- Industrial and Commercial Lighting
- Offline LED Driver Modules and Bricks

FEATURES

- Smooth 0-100% Flicker-free Dimming Range
- Compatibility with all TRIAC Dimmers (Digital, Leading and Trailing-edge)
- Near- unity PFC without External PFC Circuitry
- Spread- Spectrum Switching for Reduced EMI
- Low 500µA Quiescent Current
- Protections:
  - Soft Start
  - Under- -voltage, (Over-voltage) Lockout
  - Thermal Shutdown)

DIMMING PERFORMANCE

- Power Factor = 0.99 at 13W output
- Power Factor = 0.91 at 1W output
- Efficiency: 87% from 120Vrms to 39Vdc at full power
- Efficiency: 85% from 120Vrms to 23Vdc at full power
- Efficiency: >82% down to 2W output
- 0~100% Light Output and anything in between
- No flicker over Full Dimming Range

TYPICAL APPLICATION CIRCUIT

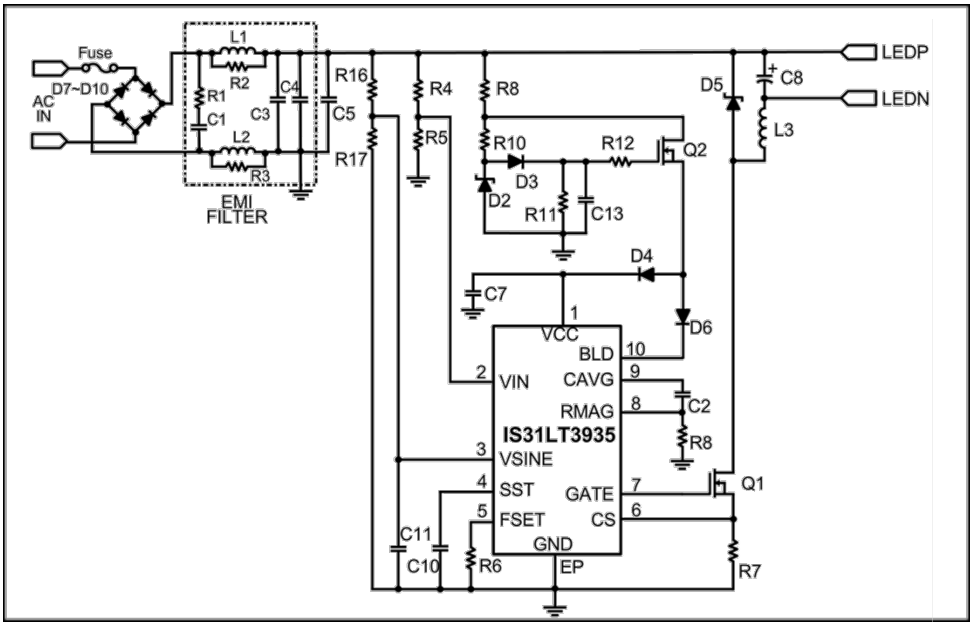
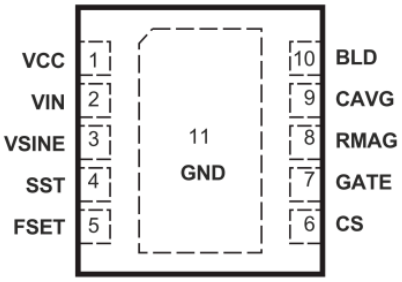


Figure 1 Typical Application Schematic

PIN CONFIGURATION

Package	Top View
DFN-10 3x3 (Exposed Pad)	 10-LEAD (3mm x 3mm) PLASTIC DFN EXPOSED PAD (PIN 11) IS GND, MUST BE SOLDERED TO PCB

PIN DESCRIPTION – (PINOUT IS SUBJECT TO CHANGE BASED)

Pin #	Name	Type	Description
1	VCC	Power	Input power supply pin for the IC
2	VIN	Input	Scaled line input voltage. Used to control the TRIAC bias circuit block.
3	VSINE	I/O	Scaled line input voltage. Used to shape the inductor current to match line input voltage.
4	SST	Input	Soft-start input. Connect a capacitor between this pin and GND to control startup delay time
5	FSET	I/O	Frequency select pin. Connect a resistor between this pin and GND to set the base operating frequency of the IC.
6	CS	Input	Inductor current sense input pin.
7	GATE	Output	Gate drive output. Connect to the gate of the power NMOS.
8	RMAG	Input	Bleeder current set pin. Connect a resistor between this pin and GND to set the magnitude of the bleeder current for the TRIAC based dimmer.
9	CAVG	Input	Bleeder circuit averaging capacitor. Connect a capacitor between this pin and RMAG to control the bleeder current average function.
10	BLD	Input	Bleeder current path. Connect this pin to the output of the linear regulator via a diode to provide bleeder current for the TRIAC dimmer.
11 *Note1	GND	Power	Ground connection. Connect the exposed pad to GND to provide the power return for the IC supply.

*Note 1: Exposed pad (Pin 11) is GND, must be soldered to GND for the IC to operate.

ORDERING INFORMATION

INDUSTRIAL RANGE: -40°C TO +85°C

Order Part No.	Package	QTY/Reel
IS31LT3935-DLS2-TR	DFN10 (3x3)	2500

ABSOLUTE MAXIMUM RATINGS (*NOTE 2)

VCC, VIN, CS, BLD voltage to GND	-0.3V to 7.0V
VSINE, SST, CAVG, RMAG voltage to GND	-0.3V to 2.7V
FSET voltage to GND	-0.3V to 1.0V
GATE Output Current	50mA (RMS)
GATE Output Voltage	-0.3V to (VCC+0.3V)
ESD Susceptibility:	
HBM	2kV
MM	200V
Junction Temperature	150°C
Storage Temperature	-65°C to 150°C
Lead Temperature (Soldering, 10sec)	260°C

***Note 2:**

1. Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other condition beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

T_A = 25°C, VCC=5.5V, unless otherwise specified. Minimum and maximum limits are guaranteed through test, by design, or by statistical correlation.

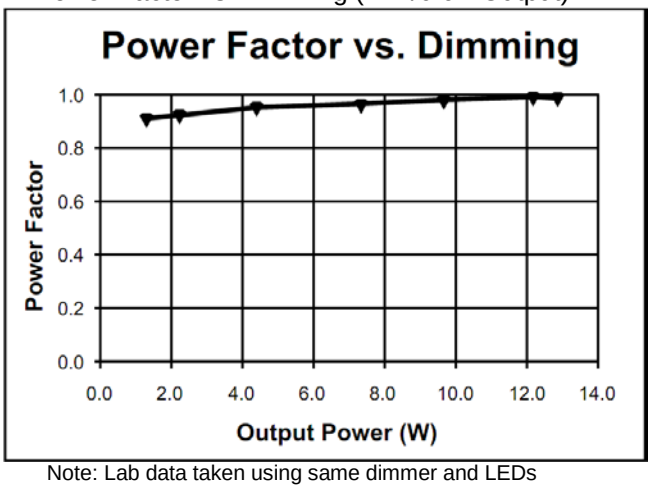
Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
VCC	Supply voltage		3.0		6.0	V
I_{VCC}	Operating Supply Current			500		µA
UVLO	Under-voltage lockout	VCC rising		2.3	2.5	V
		VCC falling	1.8	2.1		
GATE Driver						
tr_{GATE}	Gate driver output rise time	Cload = 1nF (note 2)		20		ns
tf_{GATE}	Gate driver output fall time	Cload = 1nF (note 2)		20		ns
$I_{GATEsrc}$	GATE driver peak current	V_{GATE} = 5V		1		A
$I_{GATEsnk}$	GATE driver peak current	V_{GATE} = 0V		1		A
Voltage and Temperature Reference						
V_{FSET}	Voltage on FSET pin			0.6		V
T_{max}	Over-temperature shutdown threshold			165		°C
T_{hyst}	Over-temperature hysteresis			25		°C
Error Amplifier						
A	Open-loop gain			1000		V/V
gm	Transconductance			0.1		mmho
V_{VSINE}	Maximum voltage on VSINE pin	No external voltage overdrive			1.5	V
		With external voltage overdrive			2.0	
Oscillator						
fOSC	Frequency	R_{FSET} = 180kΩ		105		kHz
tmin	Minimum on-time			100		Ns
Bleed Circuitry						
V_{RMAG}	RMAG voltage	R_{RMAG} = 10kΩ; V_{VIN}= 0V		1.0		V
V_{CAVG}	CAVG voltage			0.3		V
I_{BLD}	BLD current			100		mA
Softstart and Sensing						
I_{SST}	SST pin output current			-8		µA
I_{CS}	CS pin input current				10	nA
V_{VIN}	VIN input voltage range		0		2.5	V

NOTES:

1. Stresses beyond those listed under absolute maximum ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under recommended operating conditions is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
2. All parts are production tested at T_A = 25°C. Other temperature limits are guaranteed by design
3. Guaranteed by design

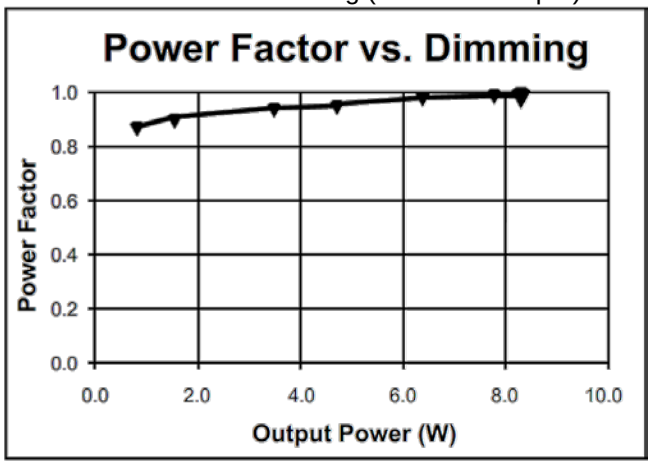
TYPICAL PERFORMANCE CHARACTERISTICS

Power Factor vs. Dimming (22V/0.6A Output)



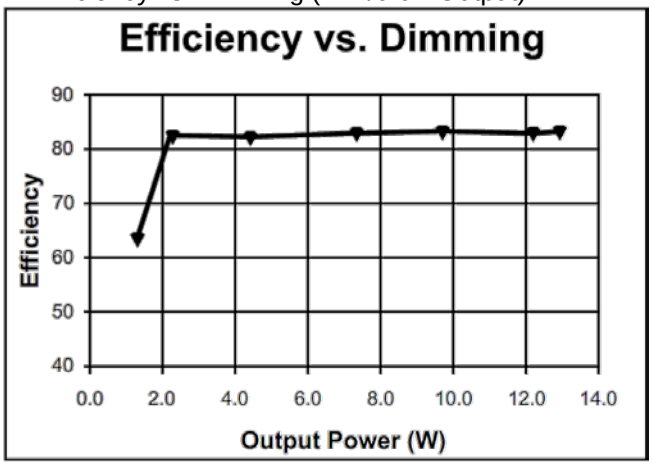
Note: Lab data taken using same dimmer and LEDs

Power Factor vs. Dimming (28V/0.3A Output)



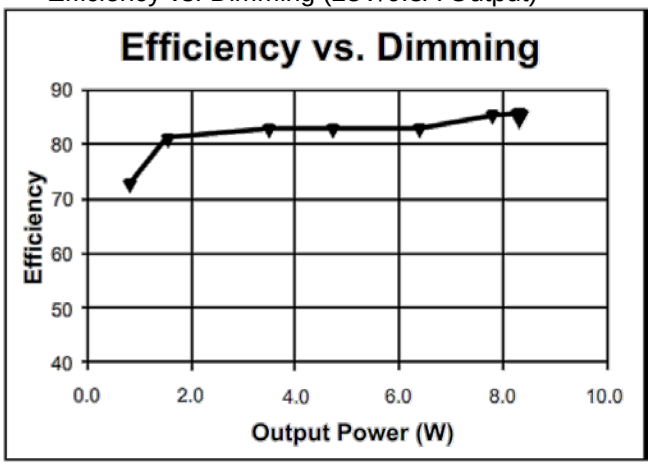
Note: Lab data taken using same dimmer and LEDs

Efficiency vs. Dimming (22V/0.6A Output)



Note: Lab data taken using same dimmer and LEDs
Efficiency is from 120Vrms input to 22Vdc output

Efficiency vs. Dimming (28V/0.3A Output)



Note: Lab data taken using same dimmer and LEDs
Efficiency is from 120Vrms input to 28Vdc output

Functional Block Diagram

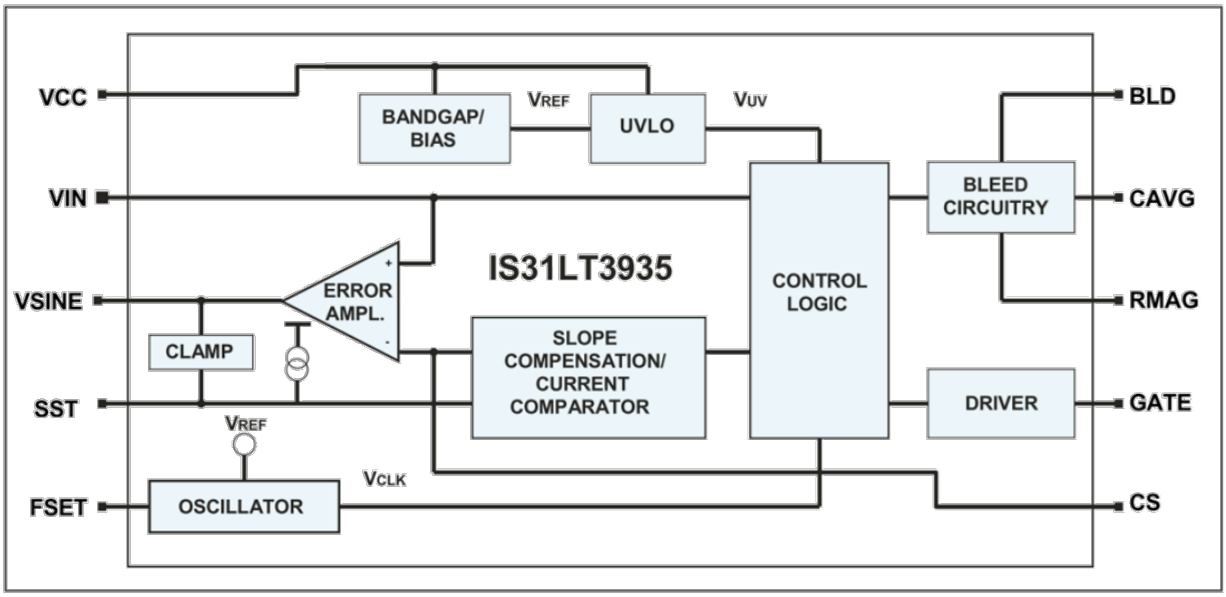


Figure 2 Typical Application Schematic

FUNCTIONAL DESCRIPTION

The IS31LT3935 is a high performance off-line AC/DC LED controller for dimmable LED retrofit lamps and luminaries using patent pending dimming technology to eliminate visible light flicker. It can work with all types of wall dimmers including leading-edge and trailing-edge dimmers. The controller can also work when no dimmer is connected.

The IS31LT3935 uses primary-feedback technology to remove the need for secondary feedback circuitry while achieving excellent line and load regulation. It eliminates the need for external loop compensation components while maintaining stable overall operating conditions. Pulse-by-pulse waveform analysis allows for accurate LED current regulations. On every clock cycle, the oscillator sends a pulse of minimum on- time to the control logic. Nominal switching frequency is determined by the value of the resistor attached between FSET and ground, with approximately 10% variation due to spread-spectrum modulation. Provided there is no fault condition (UV or OT or OC high), the driver will switch the GATE high. GATE will stay high until V_{CS} ~= V_{VSINE}/10, and will switch low once that condition is met, or the over current comparator switches.

The proprietary bleed circuitry provides current such that TRIAC based dimmers properly switch and more sophisticated electronic dimmers maintain proper functionality even in their standby state.

DETAILED DESCRIPTION

The IS31LT3935 is a AC/DC, current mode LED driver controller which incorporates PFC and supports TRIAC dimming. The device features a simple, single stage topology for minimal BOM cost. IS31LT3935 can be configured as either a flyback or a buck controller for use in either isolated or non-isolated applications. The IS31LT3935 features ISSI's FlickerFree™ technology, and includes a proprietary bleeder circuit which supports virtually all existing TRIAC based dimmers.

The device operates in a constant frequency mode which is easily programmed via a single external resistor. IS31LT3935 automatically dithers the operating frequency resulting in a spreading of the EMI spectrum, and effectively reducing the EMI produced by the circuit. Furthermore, a soft start feature is included to limit the surge current which can be produced when the power is initially applied to the circuit.

Startup Circuit

The IS31LT3935 derives its supply voltage from an external linear regulator stage which also doubles as the bleeder path for the TRIAC bias circuitry. Assuming all of the capacitors are initially discharged, when the power is first applied to the circuit, the zener diode, D2, generates a 12V reference voltage which is fed to the GATE of Q2. This voltage causes Q2 to begin to conduct current to the capacitor on VCC, C7, which begins to charge up. Once the voltage on the VCC pin exceeds the UVLO, VCC rising, threshold, the device begins to operate, and the soft start sequence will commence.

During operation, the startup circuit performs the dual duty of keeping the VCC capacitor charged as well as providing any additional bleeder current that the TRIAC wall dimmer (if used) requires. It is recommended that the VCC capacitor, C7, be 10uF or greater to maintain adequate supply voltage during normal circuit operation. The operating current for VCC consists of two main components, the quiescent supply current and the gate charge provided to the extern power NMOS. The external MOSFET gate charge, QG, can be found on the datasheet for that device. Knowing the switching frequency of the converter, f_{SWITCH} and the operating supply current of the IS31LT3935 can be approximated by:

$$I_{CC} = 0.5mA + Q_G * f_{SWITCH}$$

Power Factor Correction

Power factor correction is implemented in the IS31LT3935 by sensing the input waveform at the *VSINE* pin. This sensed voltage is internally divided by 10 and used to control the peak current in the inductor. Using a simple voltage divider circuit causes V_{VSINE} to follow the line voltage, and thus draw the average current through the inductor in a nearly sinusoidal manner. This action causes the current to be drawn proportionally and in-phase with the line voltage, thus correcting the power factor to nearly 1.

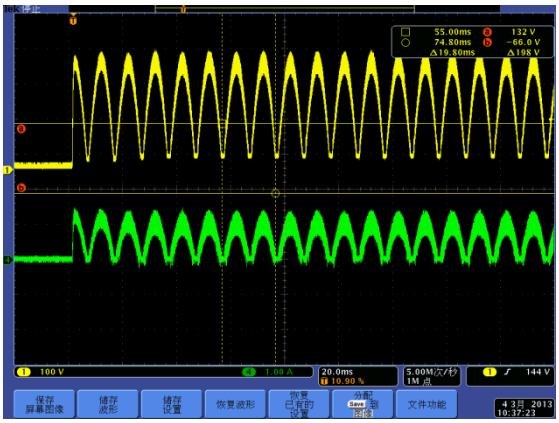


Figure 3 :Power Factor Correction

Power Circuit Operation

IS31LT3935 may be configured as either a buck or a flyback controller, however the general circuit action controlling the gate of the external power NMOS is the same regardless of the external configuration. After startup, the gate of the external NMOS is driven high, turning on the switch. This completes a current path from the power supply to GND through the inductor. Thus, the current in the inductor will begin to increase, as will the voltage across the current sense resistor, R7. The voltage across the current sense resistor is continuously compared with the threshold voltage as provided by the *VSINE* pin, and once this threshold voltage is achieved, the gate of the external NMOS is switched low, effectively turning off the switch. Since the inductor current is non-zero at this time, the inductor voltage immediately reverses allowing current to continue flowing through the LED load.
NOTE: The detail of this action differs between flyback and buck configurations, but from the perspective of the primary inductor, it is basically the same.

Since IS31LT3935 is a constant-frequency architecture, the time from the start of one switching cycle to the next switching cycle remains constant (neglecting the spread spectrum effect for now). Thus, the switch will remain off until the oscillator period has expired, at which time the switch will again turn on.

Soft Start

IS31LT3935 contains a programmable soft start circuit which is designed to limit the inrush current to the circuit at the time that power is first applied. A single capacitor connected between the SST pin and ground is used to set the timing of the soft start feature. At initial power on,

after VCC has increased above the UVLO threshold, an internal, 8µA current source is enabled to begin charging the SST capacitor. The soft-start voltage is compared to the CS voltage threshold provided by the VSINE pin and the lower value of the two voltages is used as the current sense threshold for the inductor. In this way, the peak inductor current will rise slowly over a few input cycles, as controlled by the soft start capacitor value. The peak value of the VSINE pin is internally clamped to 150mV, meaning that once the soft start pin exceeds 150mV, the VSINE pin takes over and the device begins operating normally.

Operating Frequency/Oscillator

IS31LT3935 has an internal oscillator which controls the time period between consecutive rising edges of the gate signal. The internal oscillator's period is easily programmed via a simple, single external resistor from FSET (pin 5) to GND.

The nominal operating frequency of the oscillator is found by:

$$F_{OSC}(kHz) = 18{,}900 / R_{FSET}(k\Omega)$$

Spread Spectrum Operation

As with any switching converter, the switching frequency of the converter can cause spikes in the EMI spectrum and, in some cases cause EMI testing failures. To improve the circuit performance, as well as to ease the design complexity of the EMI filters for the circuit, IS31LT3935 implements a spread spectrum approach which alters the period of the switching frequency each cycle by a pseudo-random amount. The targeted switching frequency will vary randomly by approximately 10%. This spreads the energy of the frequency harmonics by a factor of about 10, greatly improving EMI performance as well as THD.

Linear Regulator

In order to provide the supply voltage (VCC) to the IS31LT3935, which should not exceed 6V, a linear regulator is needed to regulate the line voltage to the appropriate level. For the given example, a zener diode (D2) is used to set a reference voltage level of 9.1V. After a small signal diode drop, the voltage at the gate of the linear regulator FET (Q2) is ~8.8V. After the Vgs drop of the FET and another diode drop, the voltage at VCC ranges from 5.3V to 6V, depending on the dimming level, with 5.3V corresponding to the minimum brightness while 6V corresponds to no dimming at all.

For the linear regulator FET, a BSP125 (600V, 120mA) n-channel FET in a SOT223 package is shown here. Alternatively, a BSS225 (600V, 90mA) n-channel FET in a SOT89 package can be used for lower power levels.

The amount of bypass capacitance for VCC can range from 1x 10uF MLCC capacitor to 2 x 22uF MLCC capacitors.

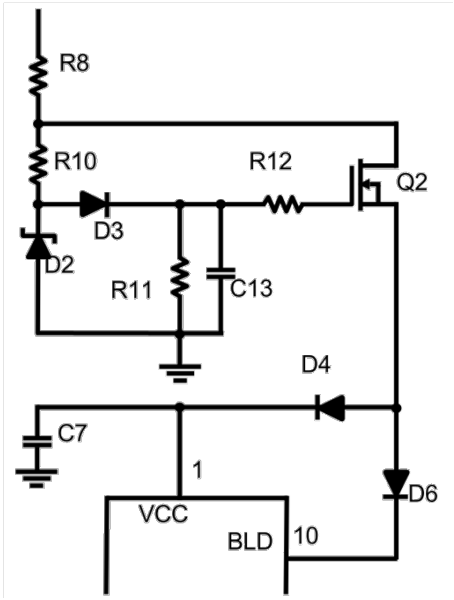


Figure 4 : Linear Regulator

The Power Train

The power-conversion topology used for the power train shown is a high side referred buck regulator. It is an electrically non isolated circuit configuration, but as such, it is the simplest and most inexpensive implementation. Though simple, it still yields excellent performance when using the IS31LT3935 controller chip, which provides good dimming functionality, efficiency and power factor, regardless of topology.

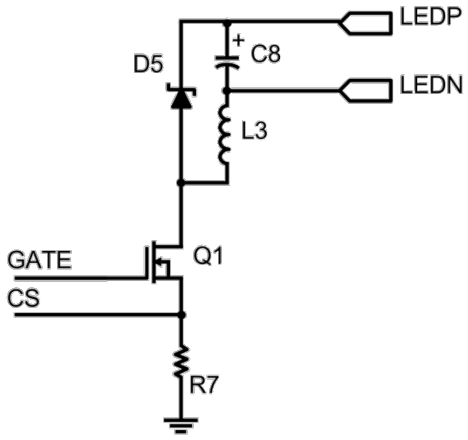


Figure 5: Power Train

The main switching diode (D5) is a C3D04060E (600V, 4A) silicon carbide, Schottky in a TO252 (DPAK) package. Alternatively, a C3D02060E (600V, 2A) diode should also work fine. Silicon carbide diodes are recommended for better efficiency, although less expensive diodes may be employed, at the expense of a few percentage points in efficiency. It is important to insure that the voltage rating is adequate for the application; 400-600V devices typically work fine.

Similarly, a 600V rated n--channel FET has been chosen for the main switching FET. In this example, an IRFRC20 has been chosen. With a Qg(max) of 18nC and Rds(on) of 4.4Ω (specified at a Vgs=10V), it enables reasonable power conversion efficiency, optimizing for both switching and conduction losses. Although FETs with even lower Rds(on) can be used to increase efficiency further, it is very important to select a FET that can support the required drain current (Id) for a 5V gate drive.

For the inductor, the inductance value is chosen in order to achieve a particular ratio of peak-to-peak ripple current relative to the maximum rated DC output current for a given switching frequency. For this application, a ratio of 0.5 is targeted in order to optimize for power losses as well as physical size.

The formula below shows the relationship between inductor ripple current, voltages, switching frequency and inductance:

$$\Delta \mathbf{I} = \frac{(\boldsymbol{Vin} - \boldsymbol{Vout})\mathbf{D}}{\boldsymbol{f} * \boldsymbol{L}}$$

where:
ΔI is the peak-to-peak inductor ripple current
$\mathbf{V_{in}}$ is the input voltage
$\mathbf{V_{out}}$ is the output voltage (or LED voltage in this case)
f is the switching frequency (programmed by R_{FSET})
L is the inductance
D is the duty cycle = $(V_{out}+V_{diode})/(V_{in}+V_{diode})$

It is also important to size the inductor current rating to insure plenty of margin for the peak inductor current before saturation, especially at high operating temperatures. Finally, it is, of course, important to check that the physical size of the inductor fits within the mechanical form factor where it will be located.

For output capacitors, a range of values and capacitor types can be used. At a minimum, four 10uF MLCC capacitors (such as Murata's GRM31CR61H106K - 1206, 50V, 10uF, X5R) are recommended. To smooth out the ripple content in the LED string more, however, more capacitance can be used, up to 1000uF where there seems to be a diminishing return. For a 50V rating, electrolytic capacitors offer more capacitance and are more economical; however ceramic capacitors (MLCCs) offer better long term reliability. A combination of a single 470uF electrolytic capacitor with two 10uF MLCCs is a good, generic starting point. In addition to observing voltage ratings (ideally de-rated for margin in the application), designers should also check ripple current ratings and insure that any self-heating in the capacitors due to ESR, etc., is acceptable.

The final output capacitor configuration depends on the application requirements and can be further optimized depending on items ranging from the types of dimmers supported to 120Hz flicker sensitivity

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CLASSIFICATION REFLOW PROFILES

Profile Feature	Pb-Free Assembly
Preheat & Soak Temperature min (Tsmin) Temperature max (Tsmax) Time (Tsmin to Tsmax) (ts)	150°C 200°C 60-120 seconds
Average ramp-up rate (Tsmax to Tp)	3°C/second max.
Liquidous temperature (TL) Time at liquidous (tL)	217°C 60-150 seconds
Peak package body temperature (Tp)*	Max 260°C
Time (tp)** within 5°C of the specified classification temperature (Tc)	Max 30 seconds
Average ramp-down rate (Tp to Tsmax)	6°C/second max.
Time 25°C to peak temperature	8 minutes max.

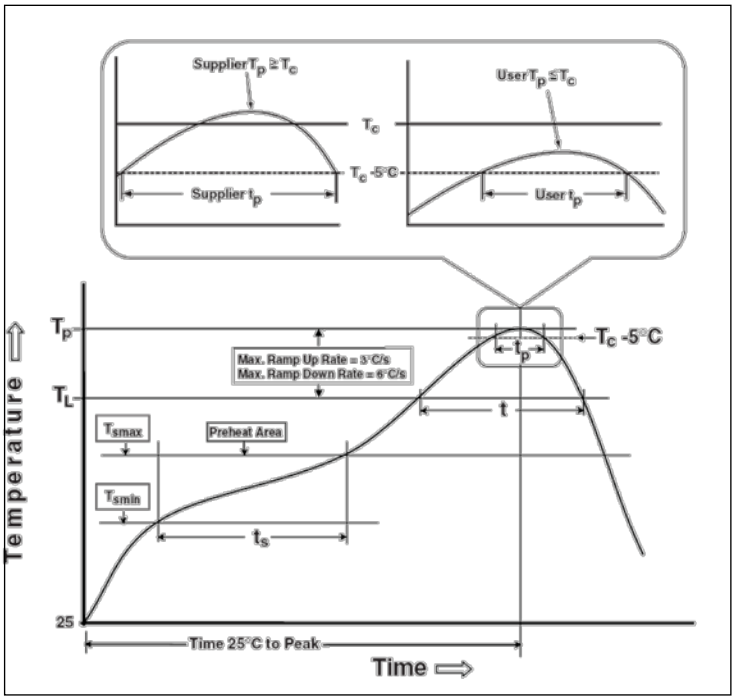
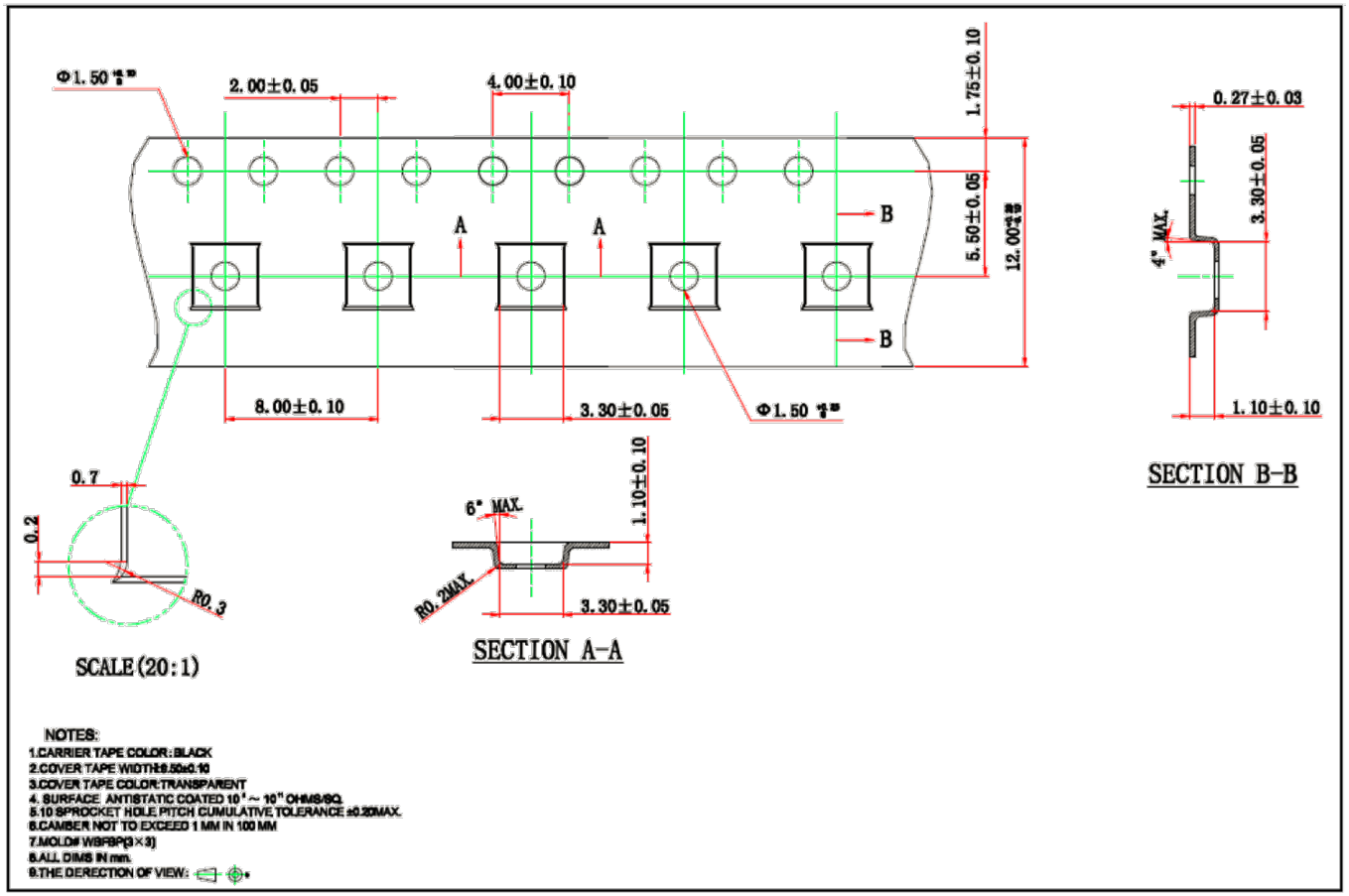


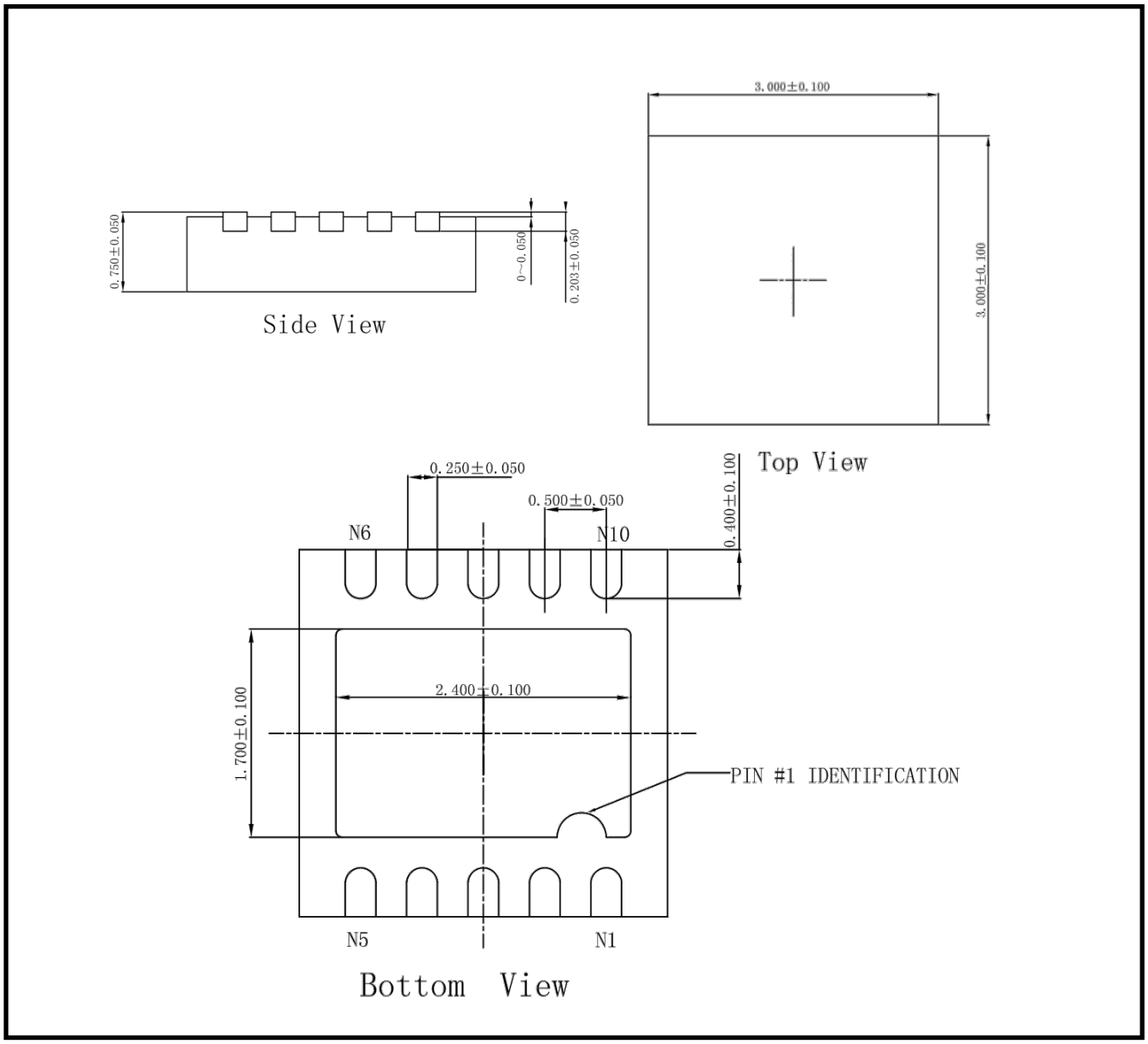
Figure 6 Classification Profile

TAPE AND REEL INFORMATION



PACKAGE OUTLINE DRAWING

10 LEAD THIN DUAL FLAT PACKAGE (DFN) WITH E-PAD



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2. A critical component is any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.