IS32FL3761

33×12 DOTS MATRIX LED DRIVER

Preliminary Information
April 2024

GENERAL DESCRIPTION

The IS32FL3761 is a general purpose 33 × n (n=12~2) LED Matrix programmed via 1MHz I2C or 12MHz SPI compatible interface. Each LED can be dimmed individually with 12-bit/8+4-bit/8-bit/6+2-bit PWM data and each color sink can have 8-bit DC scaling data which allowing 256 steps of linear PWM dimming and each color sink has 256 steps of DC current adjustable level and precision for smooth LED brightness control. The output current of each channel is designed to be 30mA, which can be adjusted by 8-bit global control register and the SL registers. Proprietary algorithms are used in IS32FL3761 to minimize power bus noise caused by passive components on the power bus such as MLCC decoupling capacitor.

Additionally, each LED open and short state can be detected, IS32FL3761 stores the open or short information in Open/Short Registers. The Open/Short Registers can be read out via I2C/SPI compatible interface, inform MCU whether there are LEDs open or short and the locations of open or short LEDs.

The IS32FL3761 operates from 2.7V to 5.5V and features a very low shutdown and operational current.

IS32FL3761 is available in QFN-60 (7mm×7mm) package. It operates from 2.7V to 5.5V over the temperature range of -40°C to +125°C.

FEATURES

- Supply voltage range: 2.7V to 5.5V
- Support 33 × n (n=12~2) matrix configuration
- Individual 12-bit/8+4-bit/8-bit/6+2-bit PWM control steps
- 312kHz PWM Frequency (@6+2-bit PWM)
- Ultra-low I_Q (1.2mA Typ.) when frame rate is 3.8kHz PWM frequency
- Global 256 step current setting
- Each current sink (CSy) 8-bit DC current steps
- 1MHz I2C or 12MHz SPI by SEL pin
- For matrix scanning operation
  - Built-in de-ghosting circuit
  - Reduced inactive LED reverse bias to improve LED reliability
- LED open/short detection accessible to SPI/I2C
- Group phase shift (180 degree) to reduce audible noise and power ripple
- Spread spectrum
- ±6% device to device @I_{OUT}= 30mA
- ±5% bit to bit @I_{OUT}= 30mA
  AEC-Q100 qualification in process with Temperature Grade 1: -40°C to 125°C
- QFN-60 (7mm×7mm) package
- RoHS & Halogen-Free Compliance
- TSCA Compliance

APPLICATIONS

- Mini LED Back Light
- Automotive RGB dynamic atmosphere light
- Automotive Center Information Display
- Automotive Cluster Display

TYPICAL APPLICATION CIRCUIT

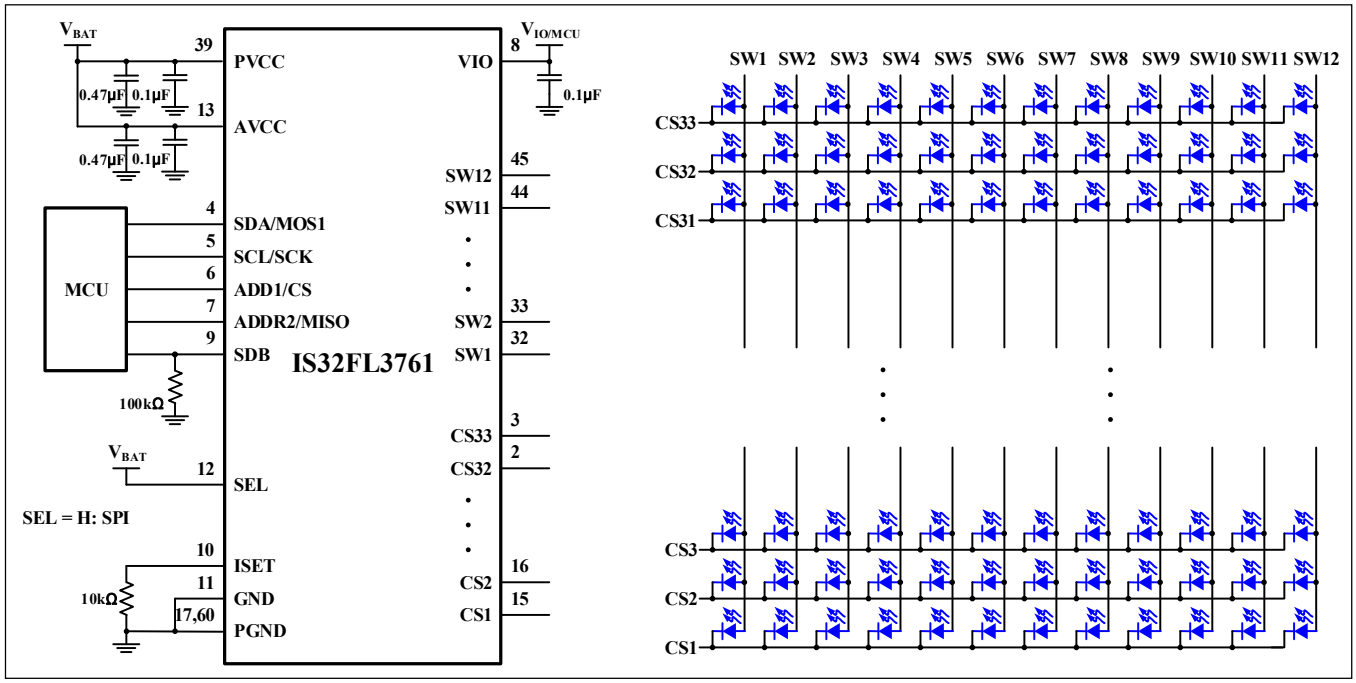


Figure 1 Typical Application Circuit: SPI interface, 33×12 Array

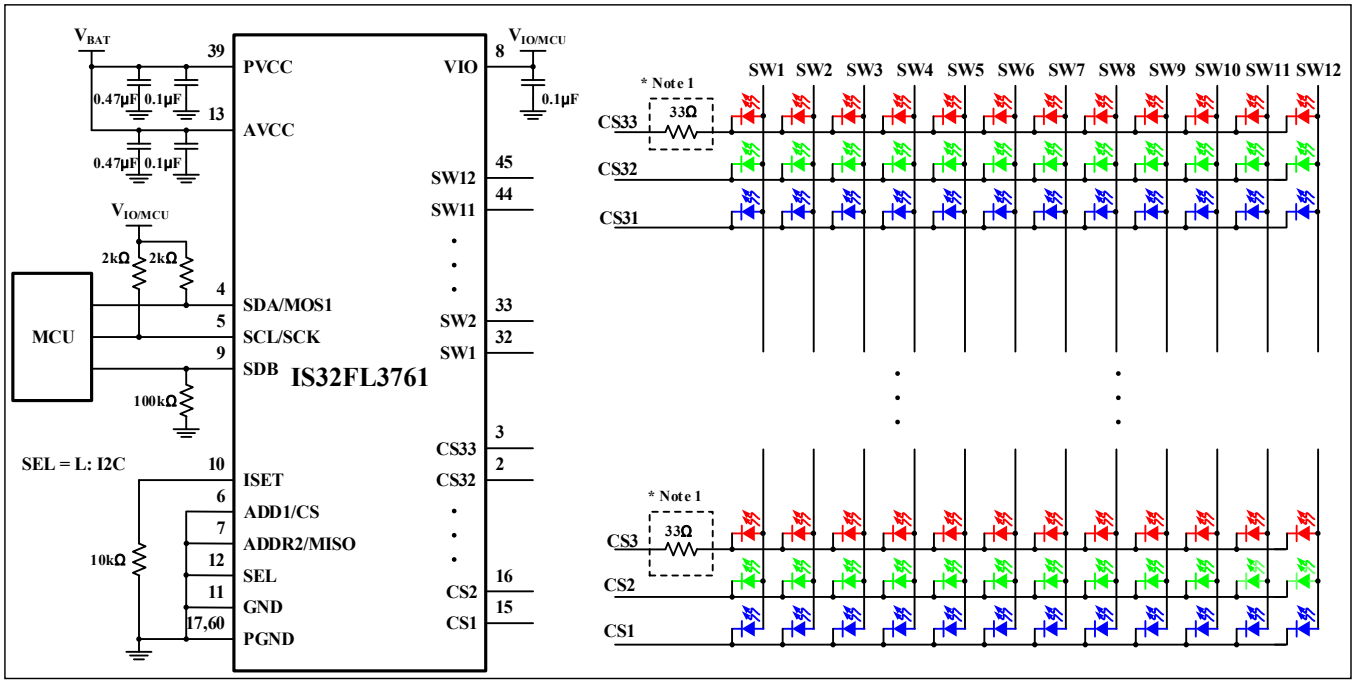
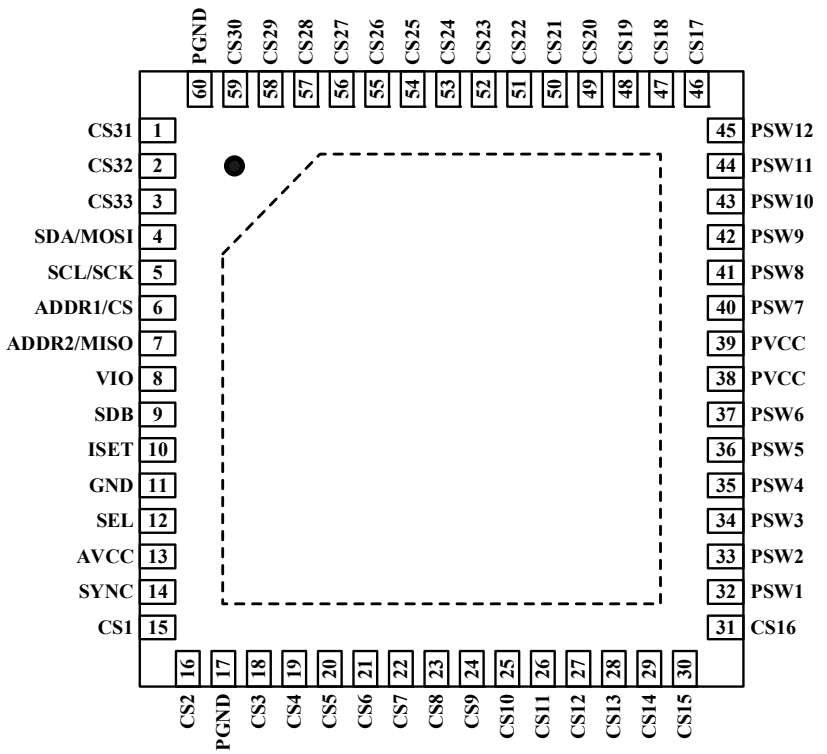


Figure 2 Typical Application Circuit: I2C interface, 11×12 RGB Array

Note 1: These optional resistors are for offloading the thermal dissipation (P= I^2R) away from the IS32FL3761 (values are for V_{LED+}= 5V).

PIN CONFIGURATION

Package	Pin Configuration (Top View)
QFN-60	

PIN DESCRIPTION

No.	Pin	Description
32~37,40~45	PSW1~PSW12	Power SW.
15~16,18~31, 46~59,1~3	CS1~CS33	Current sink pin for LED matrix.
11	GND	Analog GND.
17,60	PGND	Power GND.
13,38~39	AVCC/PVCC	Analog, digital circuits and power VCC.
12	SEL	Select SPI or I2C, SEL=L: I2C, SEL=H: SPI.
8	VIO	Power for communication block.
7	ADDR2/MISO	Address select pin/MISO of SPI.
9	SDB	Shutdown pin.
6	ADDR1/CS	Address select pin/CS of SPI.
5	SCL/SCK	I2C clock/SPI clock.
4	SDA /MOSI	I2C input data/SPI input data.
10	ISET	Set the maximum IOUT current.
14	SYNC	Synchronization.
Thermal Pad		Need to connect to GND.

ORDERING INFORMATION

Industrial Range: -40°C to +125°C

Order Part No.	Package	QTY/Reel
IS32FL3761-QFLCA3-TR	QFN-60, Lead-free	2500

ABSOLUTE MAXIMUM RATINGS

Supply voltage, V_{CC}	-0.3V ~+6.0V
Voltage at any input pin	-0.3V ~ V_{CC}+0.3V
Maximum junction temperature, T_{JMAX}	+150°C
Storage temperature range, T_{STG}	-65°C ~+150°C
Operating temperature range, T_A=T_J	-40°C ~ +125°C
Package thermal resistance, junction to ambient (4-layer standard test PCB based on JESD 51-2A), θ_{JA}	34.5°C/W
Package thermal resistance, junction to thermal PAD (4-layer standard test PCB based on JESD 51-2A), θ_{JP}	3.61°C/W
ESD (HBM) ESD (CDM)	±4kV ±750V

Note 2: Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other condition beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

The following specifications apply for V_{CC}= 5V, T_A= 25°C, unless otherwise noted.

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
V_{CC}	Supply voltage		2.7		5.5	V
I_{CC}	Quiescent power supply current	V_{SDB}= V_{CC}, I_{OUT}= 30mA (R_{ISET}=10kΩ, LFM= "0") GCC=SL= 0xFF, PWM= 0x00 PFS = 312kHz@6+2-bit mode		3.5	4	mA
		V_{SDB}= V_{CC}, R_{ISET}= 10kΩ, GCC= 0xFF, SL= 0x20, PWM= 0x00, PFS = 11.5kHz, LFM= "1" @8-bit mode		1.2	1.4	mA
I_{SD}	Shutdown current	V_{SDB}= 0V		0.6	1	μA
		V_{SDB}= V_{CC}, Configuration Register written "0000 0000		0.6	1	
I_{OUT}	Constant current of CSy	R_{ISET}= 10kΩ, GCC= 0xFF, SL= 0xFF, PWM= 0xFFF,12-bit mode	28.2	30	31.8	mA
ΔI_{MAT}	Output current error between outputs (Note 3)	I_{OUT}= 30mA	-5		5	%
ΔI_{ACC}	Output current error between devices (Note 4)	I_{OUT}= 30mA	-6		6	%
I_{LED}	Average current on each LED I_{LED} = $I_{OUT(PEAK)}$/Duty (1/12.1)	R_{ISET}= 10kΩ, GCC= 0xFF, SL= 0xFF, PWM= 0xFFF,12-bit mode		2.49		mA
V_{HR}	Current switch headroom voltage SWx pin	I_{SWITCH}= 0.8A R_{ISET}= 10kΩ, GCC= 0xFF, SL= 0xFF		350	500	mV
	Current sink headroom voltage CSy pin	I_{SINK}= 30mA, R_{ISET}= 10kΩ, GCC= 0xFF, SL= 0xFF		480	600	
t_{SCAN}	Period of SWx (SWx)	PWM is 6+2-bit mode, Maximum frequency	2.51	2.96	3.4	μs
t_{PERIOD}	SW1~SW12 overall time	PWM is 6+2-bit mode, Maximum frequency	32.6	39.6	45.7	μs

ELECTRICAL CHARACTERISTICS (CONTINUE)

The following specifications apply for V_{CC}= 5V, T_A= 25°C, unless otherwise noted.

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
t_{NOL1}	Non-overlap blanking time during scan, the SWx and CSy are all off during this time	PWM is 6+2-bit mode, Maximum frequency	0.2	0.33	0.4	μs
t_{NOL2}	Delay total time for CS1 to CS 33, during this time, the SWx is on but CSy is not all turned on	PWM is 6+2-bit mode, Maximum frequency (Note 5)		10		ns
t_{NOL2_max}	Delay total time for CS1 to CS 33, during this time, the SWx is on but CSy is not all turned on	PWM is 8-bit mode, PFS= 1.438kHz	7.04	8	9.2	μs
V_{OD}	CSy pin open detect threshold	R_{ISET}= 10kΩ, I_{OUT}≥ 0.1mA, PWM> 50%, measured at CSy	0.08	0.15		V
V_{SD}	LED short detect threshold	R_{ISET}= 10kΩ, I_{OUT}≥ 0.1mA, PWM> 50%, measured at CS (PV_{CC}-V_{CSy})	0.7	0.9		V
T_{SD}	Thermal shutdown	(Note 5)		165		°C
T_{SD_HY}	Thermal shutdown hysteresis	(Note 5)		25		°C
Logic Electrical Characteristics (SCL/SCK, ADDR2/MISO, SDA /MOSI, ADDR1/CS, SDB, SYNC)						
V_{IL}	Logic “0” input voltage	V_{CC}=2.7V~5.5V, V_{IO}=1.6V~2.8V			0.15V_{IO}	V
V_{IL}	Logic “0” input voltage	V_{CC}=2.7V~5.5V, V_{IO}=2.8V~V_{CC}			0.2V_{IO}	V
V_{IH}	Logic “1” input voltage	V_{CC}=2.7V~5.5V, V_{IO}=1.6V~2.8V	0.7V_{IO}			V
V_{IH}	Logic “1” input voltage	V_{CC}=2.7V~5.5V, V_{IO}=2.8V~V_{CC}	0.5V_{IO}			V
V_{OH}	H level MISO pin output voltage	I_{OH}= -8mA, V_{IO}= 1.6V	V_{IO}-0.4V		V_{IO}	V
V_{OL}	L level MISO pin output voltage	I_{OL}= 8mA, V_{IO}= 1.6V	0		0.4	V
I_{IL}	Logic “0” input current	SDB= L, V_{INPUT}= L (Note 5)		5		nA
I_{IH}	Logic “1” input current	SDB= L, V_{INPUT}= H (Note 5)		5		nA

DIGITAL INPUT I2C SWITCHING CHARACTERISTICS (NOTE 5)

Symbol	Parameter	Fast Mode			Fast Mode Plus			Units
		Min.	Typ.	Max.	Min.	Typ.	Max.	
f_{SCL}	Serial-clock frequency	-		400	-		1000	kHz
t_{BUF}	Bus free time between a STOP and a START condition	1.3		-	0.5		-	μs
$t_{HD, STA}$	Hold time (repeated) START condition	0.6		-	0.26		-	μs
$t_{SU, STA}$	Repeated START condition setup time	0.6		-	0.26		-	μs
$t_{SU, STO}$	STOP condition setup time	0.6		-	0.26		-	μs
$t_{HD, DAT}$	Data hold time	-		-	-		-	μs
$t_{SU, DAT}$	Data setup time	100		-	50		-	ns
t_{LOW}	SCL clock low period	1.3		-	0.5		-	μs
t_{HIGH}	SCL clock high period	0.7		-	0.26		-	μs
t_R	Rise time of both SDA and SCL signals, receiving	-		300	-		120	ns
t_F	Fall time of both SDA and SCL signals, receiving	-		300	-		120	ns

DIGITAL INPUT SPI SWITCHING CHARACTERISTICS (NOTE 5)

Symbol	Parameter	Min.	Typ.	Max.	Units
f_C	Clock frequency	-		12	MHz
t_{SLCH}	CS active set-up time	34			ns
t_{SHCH}	CS not active set-up time	17			ns
t_{SHSL}	CS detect time	167			ns
t_{CHSH}	CS active hold time	34			ns
t_{CHSL}	CS not active hold time	17			ns
t_{CH}	Clock high time	34			ns
t_{CL}	Clock low time	34			ns
t_{CLCH}	Clock rise time			9	ns
t_{CHCL}	Clock fall time			9	ns
t_{DVCH}	Data in set-up time	7			ns
t_{CHDX}	Data in hold time	9			ns
t_{SHQZ}	Output disable time			34	ns
t_{CLQV}	Clock low to output valid			39	ns
t_{CLQX}	Output hold time	0			ns
t_{QLQH}	Output rise time			17	ns
t_{QLQH}	Output fall time			17	ns

Note 3: I_{OUT} mismatch (bit to bit) $\triangle I_{MAT}$ is calculated:

$$\Delta I_{MAT} = \pm\left(\frac{I_{OUT(MAX)} - I_{OUT(MIN)}}{\left(\frac{I_{OUT0}+I_{OUT1}+\ldots+I_{OUT32}}{33} \times 2\right)}\right) \times 100\%$$

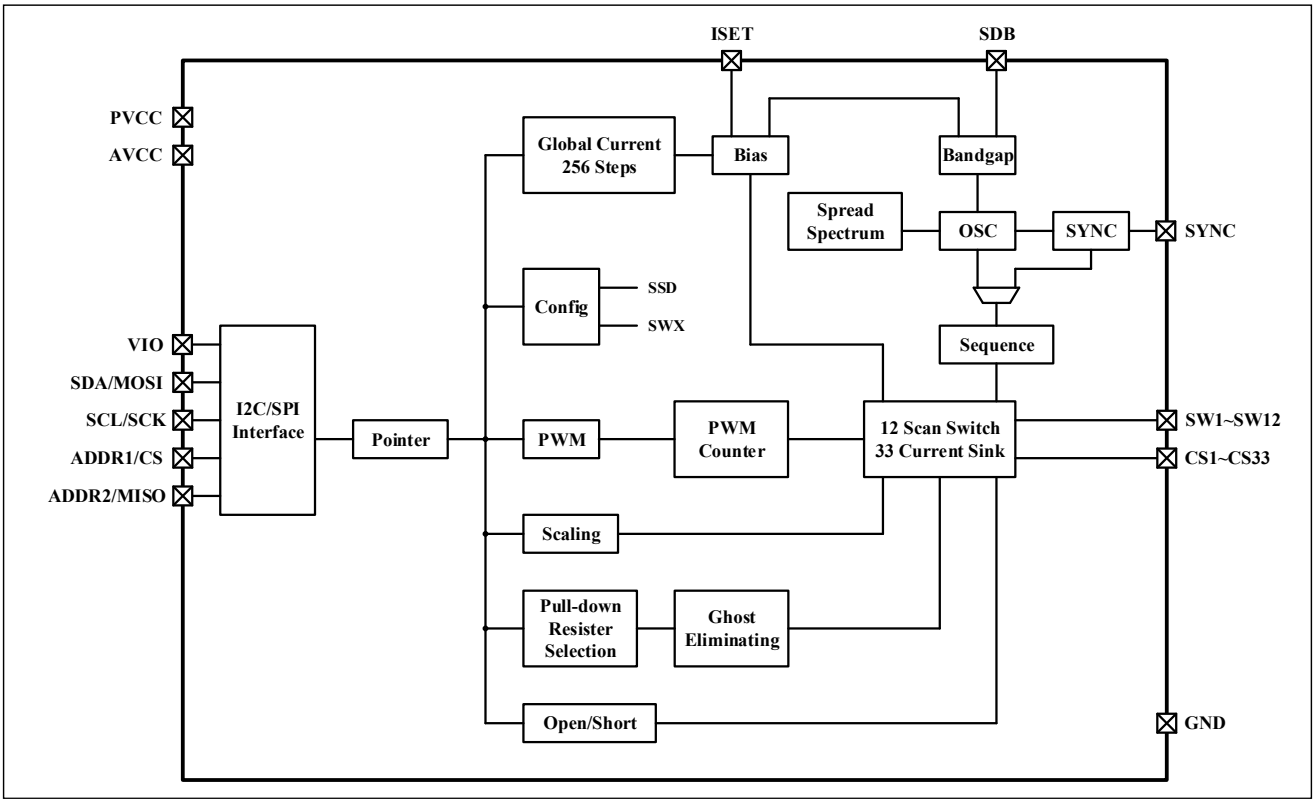
Note 4: I_{OUT} accuracy (device to device) $\triangle I_{ACC}$ is calculated:

$$\Delta I_{ACC} = \pm MAX\left(\frac{I_{OUT(MIN)} - I_{OUT(IDEAL)}}{I_{OUT(IDEAL)}}\right) \times 100\%$$

Where $I_{OUT(IDEAL)}$= 30mA when R_{ISET}= 10kΩ.

Note 5: Guaranteed by design.

FUNCTIONAL BLOCK DIAGRAM



DETAILED DESCRIPTION

I2C INTERFACE

IS32FL3761 uses a serial bus, which conforms to the I2C protocol, to control the chip's functions with two wires: SCL and SDA. The IS32FL3761 has a 7-bit slave address (A7:A1), followed by the R/W bit, A0. Set A0 to "0" for a write command and set A0 to "1" for a read command. The value of bits A1 and A2 are decided by the connection of the ADDRx pin.

Table 1 Slave Address

ADDR2	ADDR1	A7:A5	A4:A3	A2:A1	A0
GND	GND	011	00	00	0/1
GND	SCL		00	01	
GND	SDA		00	10	
GND	VCC		00	11	
SCL	GND		01	00	
SCL	SCL		01	01	
SCL	SDA		01	10	
SCL	VCC		01	11	
SDA	GND		10	00	
SDA	SCL		10	01	
SDA	SDA		10	10	
SDA	VCC		10	11	
VCC	GND		11	00	
VCC	SCL		11	01	
VCC	SDA		11	10	
VCC	VCC		11	11	

ADDR1/2 connected to GND, (A2:A1)/(A4:A3)=00;
ADDR1/2 connected to VCC, (A2:A1)/(A4:A3)=11;
ADDR1/2 connected to SCL, (A2:A1)/(A4:A3)=01;
ADDR1/2 connected to SDA, (A2:A1)/(A4:A3)=10;

The SCL line is uni-directional. The SDA line is bi-directional (open-drain) with a pull-up resistor (typically 400kHz I2C with 4.7kΩ, 1MHz I2C with 2kΩ). The maximum clock frequency specified by the I2C standard is 1MHz. In this discussion, the master is the microcontroller, and the slave is the IS32FL3761.

The timing diagram for the I2C is shown in Figure 3. The SDA is latched in on the stable high level of the SCL. When there is no interface activity, the SDA line should be held high.

The "START" signal is generated by lowering the SDA signal while the SCL signal is high. The start signal will alert all devices attached to the I2C bus to check the incoming address against their own chip address.

The 8-bit chip address is sent next, most significant bit first. Each address bit must be stable while the SCL level is high.

After the last bit of the chip address is sent, the master checks for the IS32FL3761's acknowledge. The master releases the SDA line high (through a pull-up resistor). Then the master sends an SCL pulse. If the IS32FL3761 has received the address correctly, then it holds the SDA line low during the SCL pulse. If the SDA line is not low, then the master should send a "STOP" signal (discussed later) and abort the transfer.

Following acknowledge of IS32FL3761, the register address byte is sent, most significant bit first. IS32FL3761 must generate another acknowledge indicating that the register address has been received.

Then 8-bit of data byte are sent next, most significant bit first. Each data bit should be valid while the SCL level is stable high. After the data byte is sent, the IS32FL3761 must generate another acknowledge to indicate that the data was received.

The "STOP" signal ends the transfer. To signal "STOP", the SDA signal goes high while the SCL signal is high.

ADDRESS AUTO INCREMENT

To write multiple bytes of data into IS32FL3761, load the address of the data register that the first data byte is intended for. During the IS32FL3761 acknowledge of receiving the data byte, the internal address pointer will increment by one. The next data byte sent to IS32FL3761 will be placed in the new address, and so on. The auto increment of the address will continue as long as data continues to be written to IS32FL3761 (Figure 6).

READING OPERATION

Most of the registers can be read.

To read the registers, after I2C start condition, the bus master must send the IS32FL3761 device address with the R/$\overline{W}$ bit set to "0", followed by the register address which determines which register is accessed. Then restart I2C, the bus master should send the IS32FL3761 device address with the R/$\overline{W}$ bit set to "1". Data from the register defined by the command byte is then sent from IS32FL3761 to the master (Figure 7).

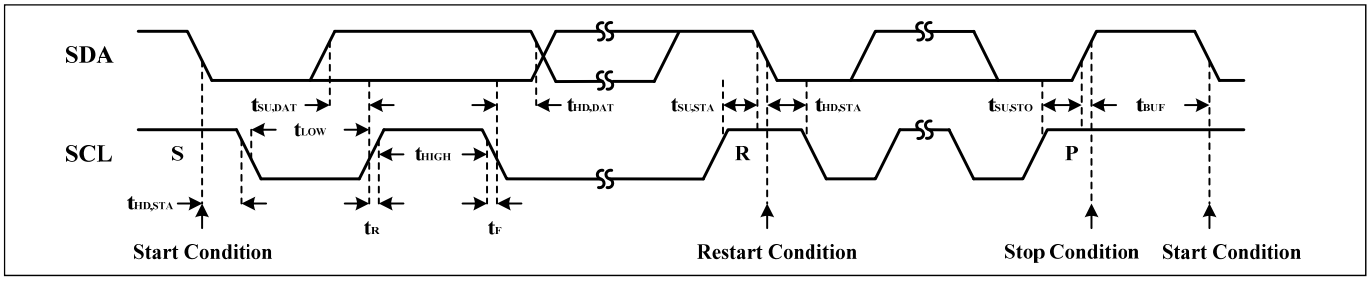


Figure 3 I2C Interface Timing

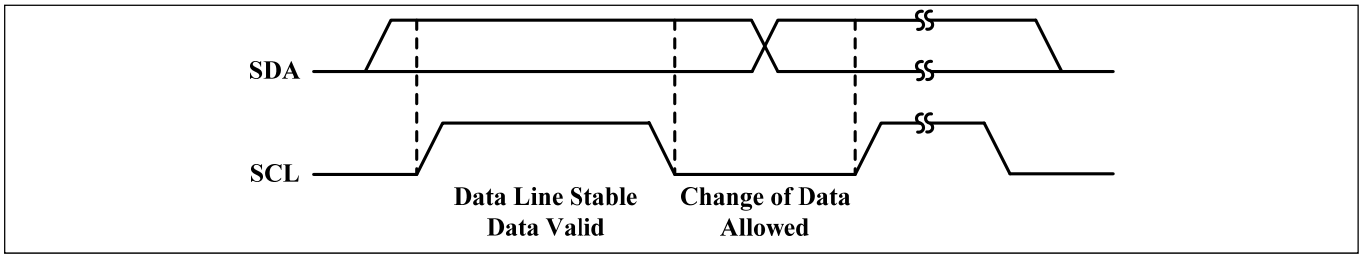


Figure 4 I2C Bit Transfer

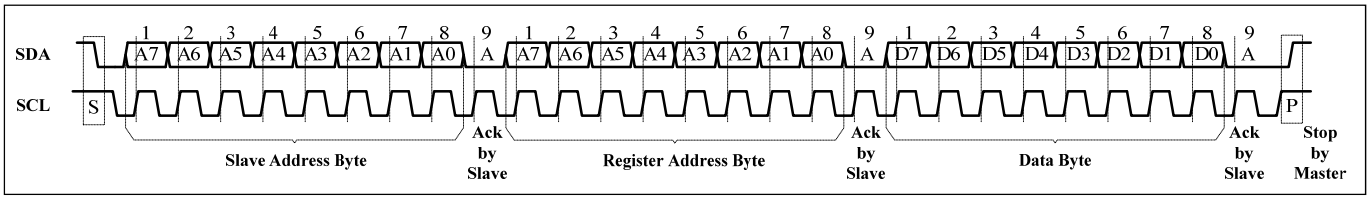


Figure 5 I2C Writing to IS32FL3761 (Typical)

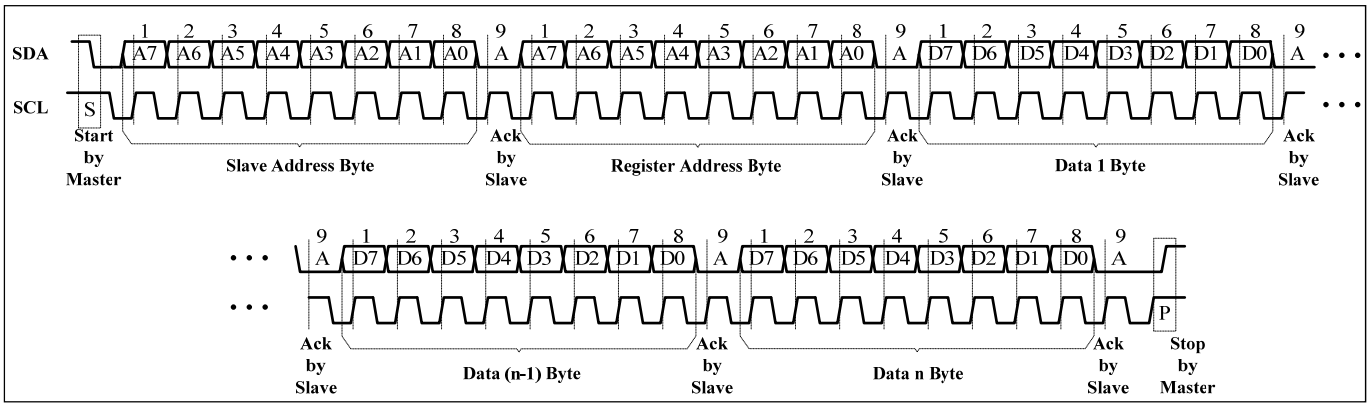


Figure 6 I2C Writing to IS32FL3761 (Automatic Address Increment)

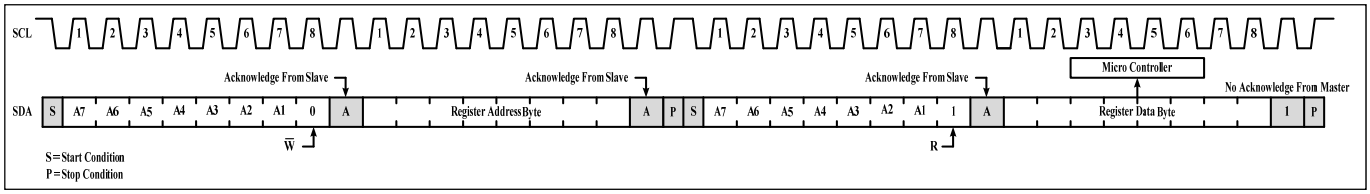


Figure 7 I2C Reading from IS32FL3761

SPI INTERFACE

IS32FL3761 uses a SPI protocol to control the chip's function with four wires: CS, SCK, MOSI and MISO. SPI transfer starts form CS pin from high to low controlled by Master (Microcontroller), and IS32FL3761 latches data when clock rising.

SPI data format is 8-bit length. The first command byte composite of 1-bit R/W bit, 3-bit chip ID bit and 4-bit page bit. The command byte must be sent first, and is followed by register address byte then the register data. If the R/W bit is "0", it will be written operation and Master (Micro-controller) can write the register data into the register.

The maximum SCK frequency supported in IS32FL3761 is 12MHz.

Table 2 SPI Command Byte

Name	R/W	ID bit	Page No.
Bit	D7	D6:D4	D3:D0
Value	0: Write 1: Read	011	0x00: Point to Page 0 0x01: Point to Page 1 0x02: Point to Page 2

ADDRESS AUTO INCREMENT

To write multiple bytes of data into IS32FL3761, load the address of the data register that the first data byte is intended for. During the 8th rising edge of receiving the data byte, the internal address pointer will increment by one. The next data byte sent to IS32FL3761 will be placed in the new address, and so on. The auto increment of the address will continue as long as data continues to be written to IS32FL3761 (Figure 11).

READING OPERATION

Page 0~Page 2 registers can be read by SPI.

To read the registers of Page 0 thru Page 1, The D7 of the Command Byte need to be set to "1" and select the page number. If read one register, as shown in Figure 8, read the MISO data after sending the command byte and register address. If read more registers, as shown in Figure 13, the register address will auto increase during the 8th rising edge of receiving the last bit of the previous register data.

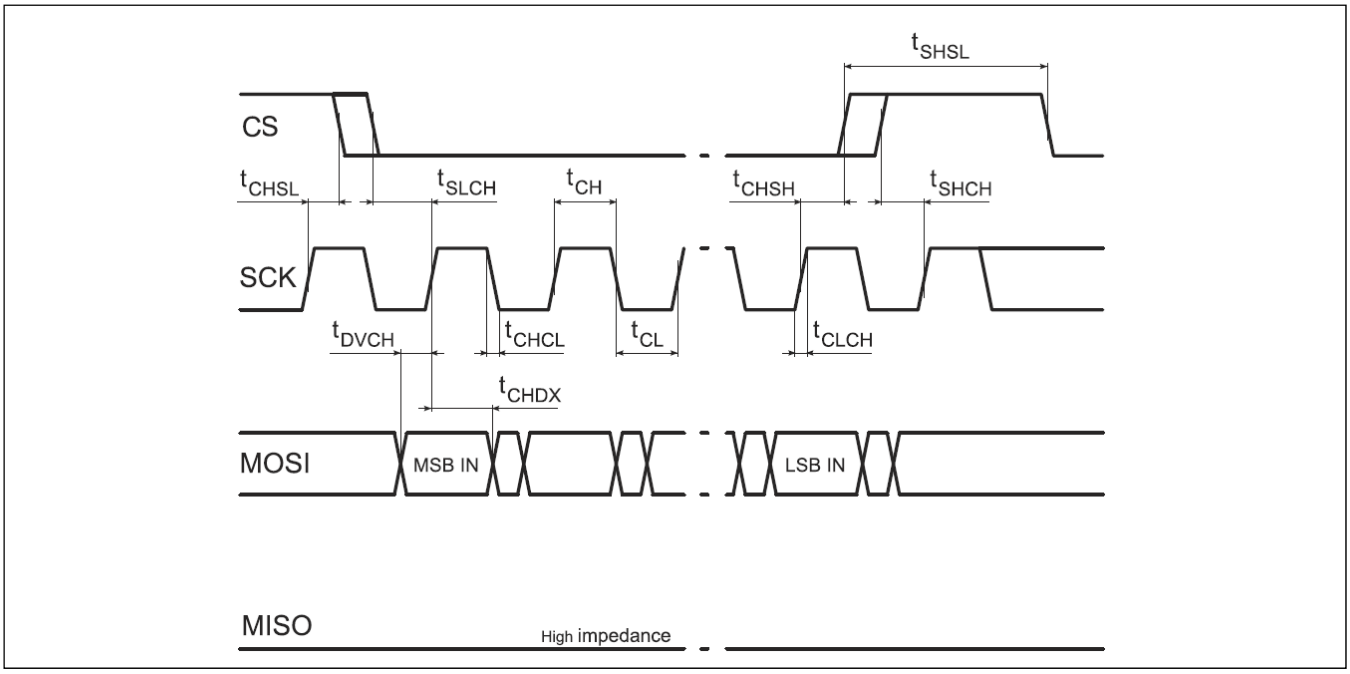


Figure 8 SPI Input Timing

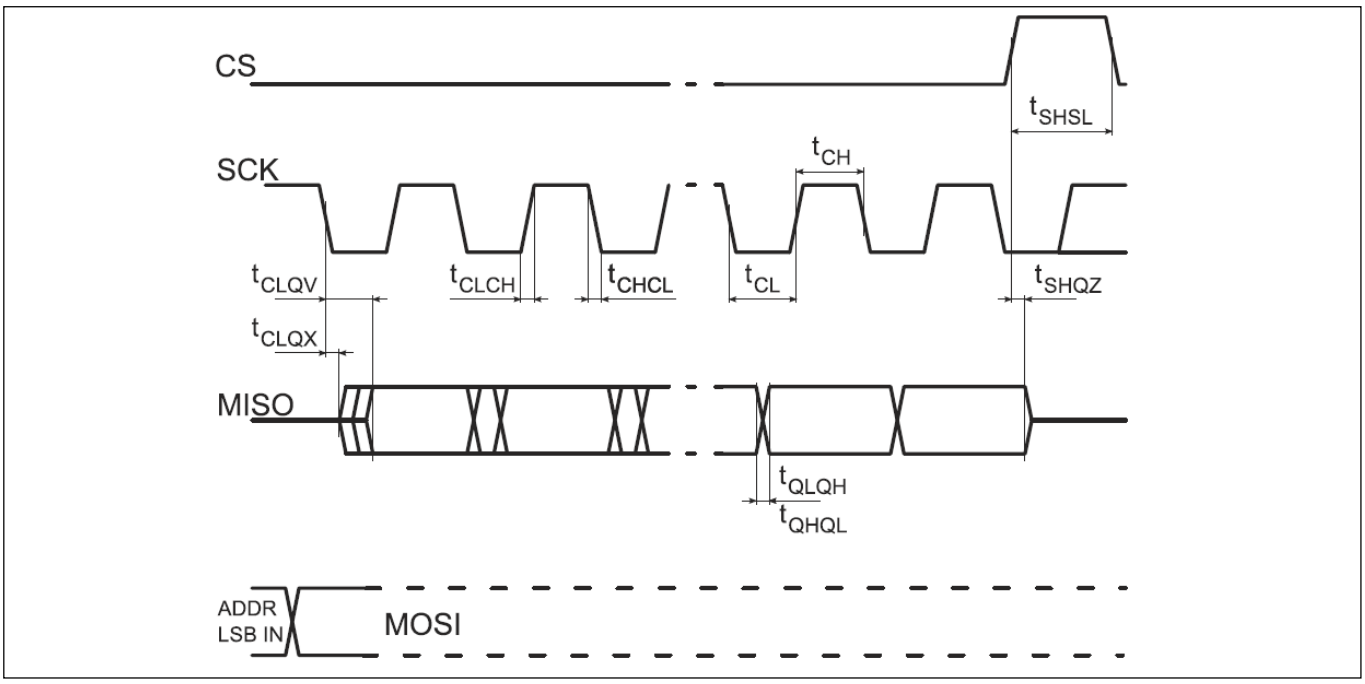


Figure 9 SPI Input Timing

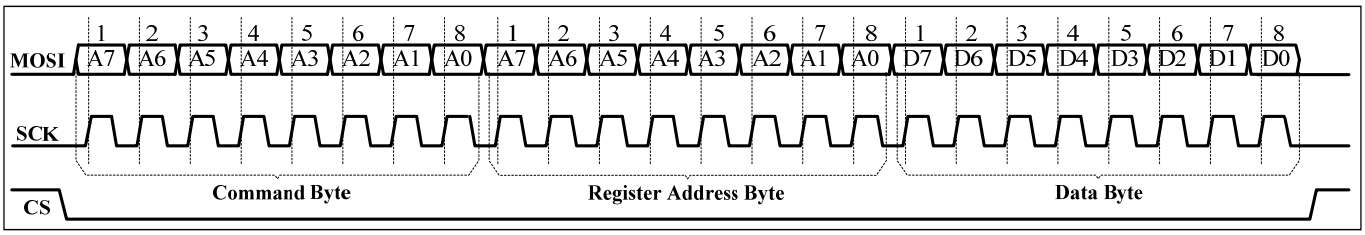


Figure 10 SPI writing to IS32FL3761 (Typical)

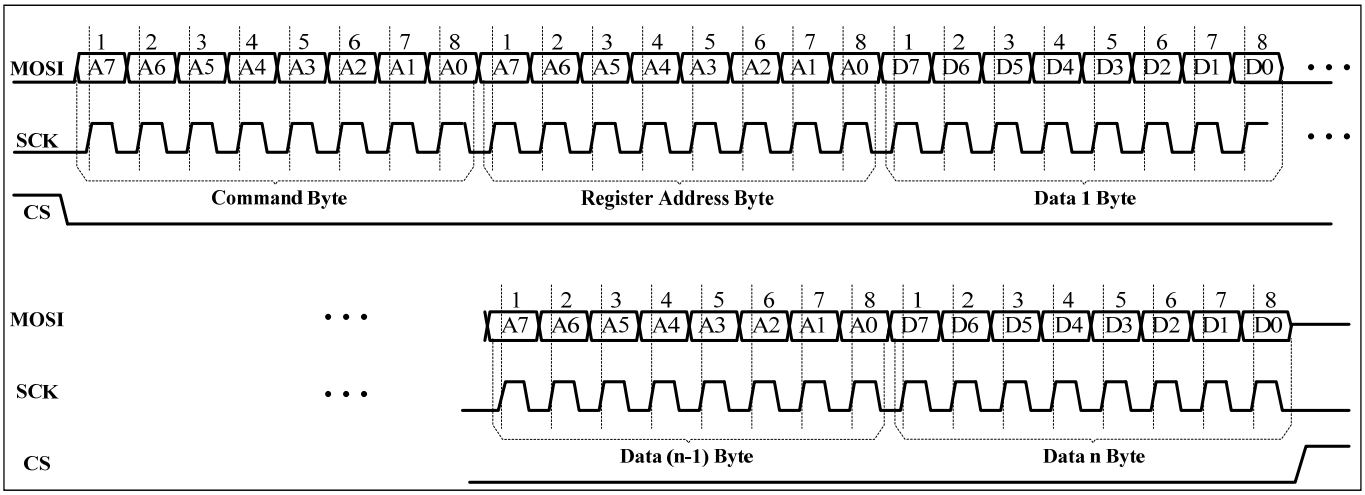


Figure 11 SPI writing to IS32FL3761 (Automatic address increment)

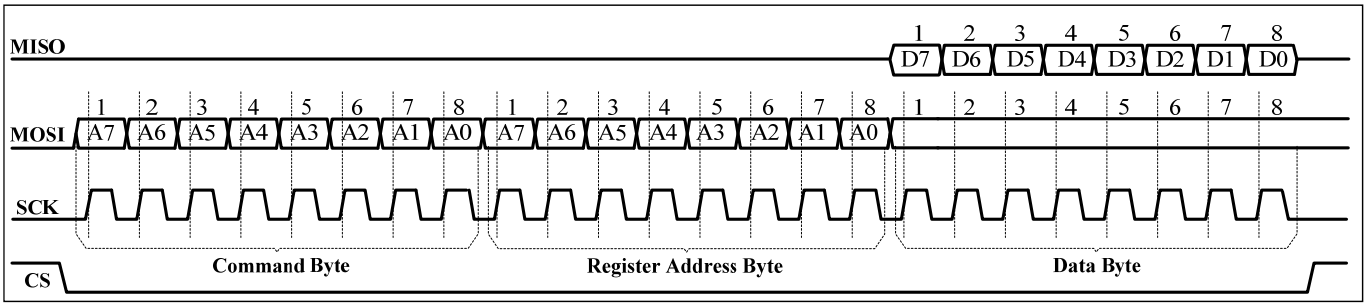


Figure 12 SPI Reading From IS32FL3761 (Typical)

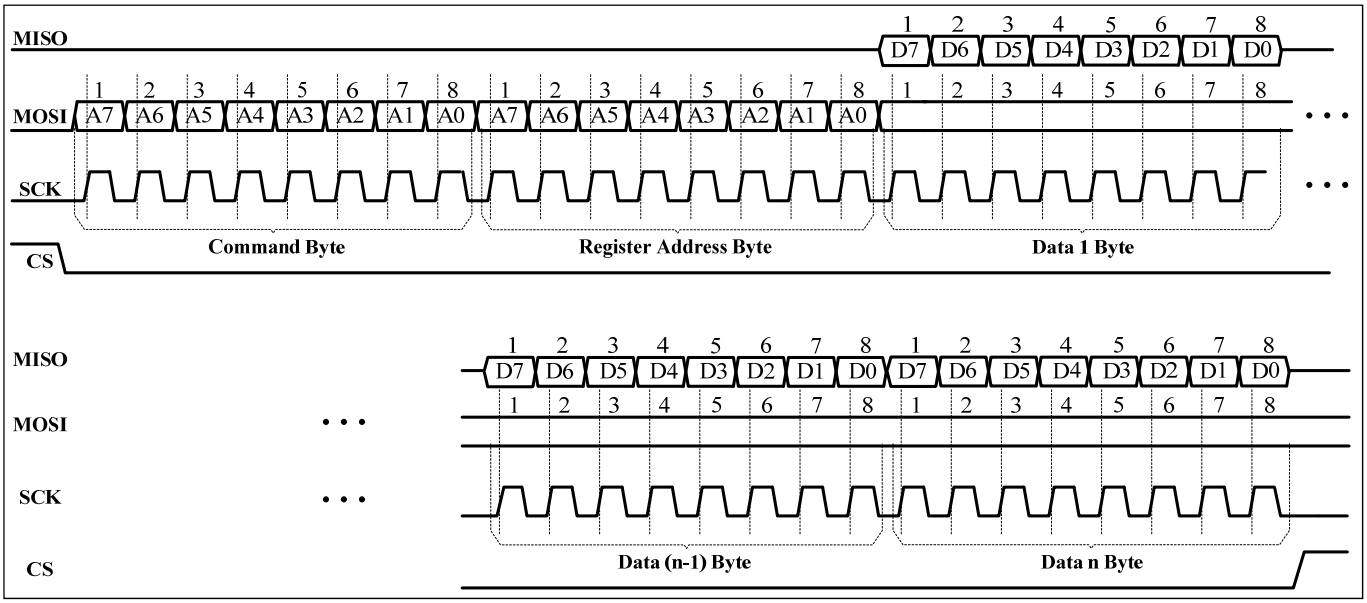


Figure 13 SPI Reading From IS32FL3761 (Automatic Address Increment)

REGISTER DEFINITIONS

Table 3 Command Register Definition

Address	Name	Function	Table	R/W	Default
FDh	PWM update register	Update PWM register	-	W	0000 0000
FEh	Command Register	Available Page 0 to Page 2 Registers	4	W	0000 0010
FFh	Command Register Write Lock	To unlock Command Register	-	W	0000 0000

Note 6: For SPI mode only, the command already include the page information and it does not need to unlock the command register.

FDh Update Register

When SDB= “H” and SSD= “1”, a write of “0000 0000” to FDh is to update the PWM Register (Page 0, 01h~FCh & Page 1 01h~FCh & Page 2 01h~5Ah) values.

REGISTER PAGE CONTROL

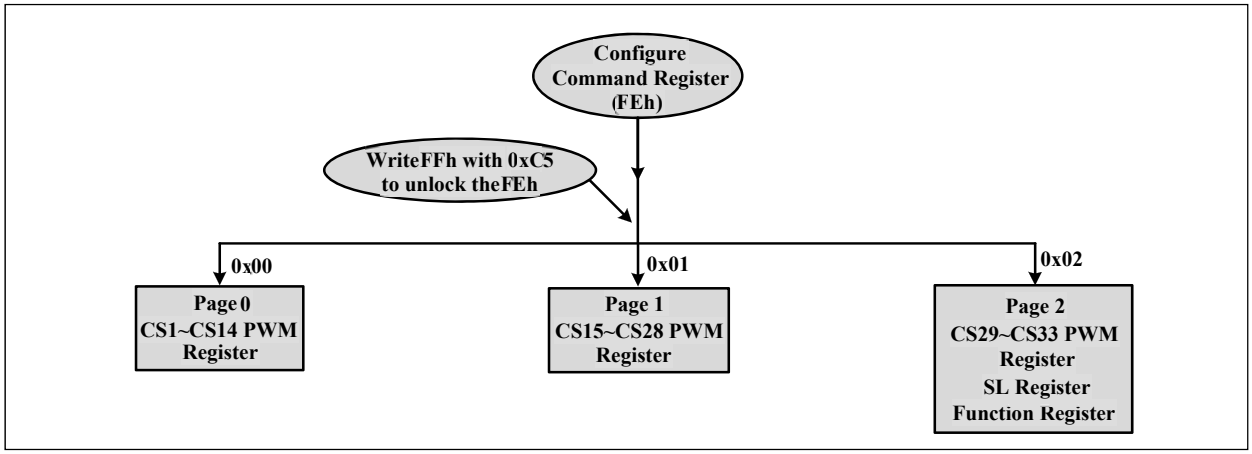


Figure 14 Register Pages (For I2C Mode Only)

Table 4 FEh Command Register

Data	Hex	Function
0000 0000	0x00	Point to Page 0(PG0): PWM (CS1~CS14 PWM Register is available)
0000 0001	0x01	Point to Page 1(PG1): PWM (CS14~CS28 PWM Register is available)
0000 0010	0x02	Point to Page 2(PG2): PWM and Function Register (CS29~CS33 PWM Register is available)
Others	-	Not allowed

Note 7: Register FEh is not in any of above pages, and it can swap the pages at any time, when power up, default page is page 2(FEh=0x02), and all the writing will be stored in page 2, if it is not swapped to other pages. Follow the sequence above in table 4 to swap to a new page:

SPI mode: The SPI command already includes page information, see table 2 for detail information.

For example, when write “0000 0000” (0x00) in the Command Register (FEh), the data written will be stored on page 0, the PWM data of CS1-CS14.

The PWM data needs to be updated with the writing 0x00 to FDh register, FDh does not belong to any page, every time when user writes the FDh, the PWM data will be updated.

FFh Command Register Write Lock Register

To select the PG0~PG2, need to unlock this register first, with the purpose of avoiding misoperation of this register. When FFh is written with 0xC5, FEh is allowed to modify once, after the FEh is modified the FFh will reset to be 0x00 at once.

Table 5 Register Definition

Address	Name	Function	Table	R/W	Default
Page 0 I2C: FEh= 0x00, SPI page No.= 0x00					
01h-FCh	PWM Register	Set PWM for CS1-CS14	6	R/W	0000 0000
Page 1 I2C: FEh= 0x01, SPI page No.= 0x01					
01h-FCh	PWM Register	Set PWM for CS15-CS28	6	R/W	0000 0000
Page 2 I2C: FEh= 0x02, SPI page No.= 0x02					
01h-5Ah	PWM Register	Set PWM for CS29-CS33	6	R/W	0000 0000
5Bh-9Ch	Scaling Register	Set Current for each CS channel	7	R/W	0000 0000
A0h	Configuration register	Configure the operation mode	8	R/W	0000 0000
A1h	Global Current Control Register	Set the global current	9	R/W	0000 0000
A2h	De-ghost Enable/Resister selection Register	Enables De-ghost function and select resisters	10	R/W	0000 0000
A3h	Pull Down/Up Resistor Selection Register	Set the pull-down resistor for SWx and pull up resistor for CSy	11	R/W	0000 0000
A4h	PWM Frequency Register	Selects the PWM frequency and low frequency mode	12	R/W	0000 0000
A5h	Spread spectrum Register	Spread spectrum function enable	13	R/W	0000 0000
A6h	Open/Short Enable Register	Open and short function enable	14	R/W	0000 0000
A7h-ABh	Open and short read registers	Store the open or short information	15~19	R	0000 0000
DFh	Reset register	Reset all register to default value	-	W	0000 0000

PWM Register

		SW1	SW2	SW3	SW4	SW5	SW6	SW7	SW8	SW9	SW10	SW11	SW12
PAGE2	CS33	49 4BL	4A 4BH	4C 4EL	4D 4EH	4F 51L	50 51H	52 54L	53 54H	55 57L	56 57H	58 5AL	59 5AH
	CS32	37 39L	38 39H	3A 3CL	3B 3CH	3D 3FL	3E 3FH	40 42L	41 42H	43 45L	44 45H	46 48L	47 48H
	CS31	25 27L	26 27H	28 2AL	29 2AH	2B 2DL	2C 2DH	2E 30L	2F 30H	31 33L	32 33H	34 36L	35 36H
	CS30	13 15L	14 15H	16 18L	17 18H	19 1BL	1A 1BH	1C 1EL	1D 1EH	1F 21L	20 21H	22 24L	23 24H
	CS29	01 03L	02 03H	04 06L	05 06H	07 09L	08 09H	0A 0CL	0B 0CH	0D 0FL	0E 0FH	10 12L	11 12H
PAGE1	CS28	EB EDL	EC EDH	EE F0L	EF F0H	F1 F3L	F2 F3H	F4 F6L	F5 F6H	F7 F9L	F8 F9H	FA FCL	FB FCH
	CS27	D9 DBL	DA DBH	DC DEL	DD DEH	DF E1L	E0 E1H	E2 E4L	E3 E4H	E5 E7L	E6 E7H	E8 EAL	E9 EAH
	CS26	C7 C9L	C8 C9H	CA CCL	CB CCH	CD CFL	CE CFH	D0 D2L	D1 D2H	D3 D5L	D4 D5H	D6 D8L	D7 D8H
	CS25	B5 B7L	B6 B7H	B8 BAL	B9 BAH	BB BDL	BC BDH	BE C0L	BF C0H	C1 C3L	C2 C3H	C4 C6L	C5 C6H
	CS24	A3 A5L	A4 A5H	A6 A8L	A7 A8H	A9 ABL	AA ABH	AC AEL	AD AEH	AF B1L	B0 B1H	B2 B4L	B3 B4H
	CS23	91 93L	92 93H	94 96L	95 96H	97 99L	98 99H	9A 9CL	9B 9CH	9D 9FL	9E 9FH	A0 A2L	A1 A2H
	CS22	7F 81L	80 81H	82 84L	83 84H	85 87L	86 87H	88 8AL	89 8AH	8B 8DL	8C 8DH	8E 90L	8F 90H
	CS21	6D 6FL	6E 6FH	70 72L	71 72H	73 75L	74 75H	76 78L	77 78H	79 7BL	7A 7BH	7C 7EL	7D 7EH
	CS20	5B 5DL	5C 5DH	5E 60L	5F 60H	61 63L	62 63H	64 66L	65 66H	67 69L	68 69H	6A 6CL	6B 6CH
	CS19	49 4BL	4A 4BH	4C 4EL	4D 4EH	4F 51L	50 51H	52 54L	53 54H	55 57L	56 57H	58 5AL	59 5AH
	CS18	37 39L	38 39H	3A 3CL	3B 3CH	3D 3FL	3E 3FH	40 42L	41 42H	43 45L	44 45H	46 48L	47 48H
	CS17	25 27L	26 27H	28 2AL	29 2AH	2B 2DL	2C 2DH	2E 30L	2F 30H	31 33L	32 33H	34 36L	35 36H
	CS16	13 15L	14 15H	16 18L	17 18H	19 1BL	1A 1BH	1C 1EL	1D 1EH	1F 21L	20 21H	22 24L	23 24H
	CS15	01 03L	02 03H	04 06L	05 06H	07 09L	08 09H	0A 0CL	0B 0CH	0D 0FL	0E 0FH	10 12L	11 12H
PAGE0	CS14	EB EDL	EC EDH	EE F0L	EF F0H	F1 F3L	F2 F3H	F4 F6L	F5 F6H	F7 F9L	F8 F9H	FA FCL	FB FCH
	CS13	D9 DBL	DA DBH	DC DEL	DD DEH	DF E1L	E0 E1H	E2 E4L	E3 E4H	E5 E7L	E6 E7H	E8 EAL	E9 EAH
	CS12	C7 C9L	C8 C9H	CA CCL	CB CCH	CD CFL	CE CFH	D0 D2L	D1 D2H	D3 D5L	D4 D5H	D6 D8L	D7 D8H
	CS11	B5 B7L	B6 B7H	B8 BAL	B9 BAH	BB BDL	BC BDH	BE C0L	BF C0H	C1 C3L	C2 C3H	C4 C6L	C5 C6H
	CS10	A3 A5L	A4 A5H	A6 A8L	A7 A8H	A9 ABL	AA ABH	AC AEL	AD AEH	AF B1L	B0 B1H	B2 B4L	B3 B4H
	CS9	91 93L	92 93H	94 96L	95 96H	97 99L	98 99H	9A 9CL	9B 9CH	9D 9FL	9E 9FH	A0 A2L	A1 A2H
	CS8	7F 81L	80 81H	82 84L	83 84H	85 87L	86 87H	88 8AL	89 8AH	8B 8DL	8C 8DH	8E 90L	8F 90H
	CS7	6D 6FL	6E 6FH	70 72L	71 72H	73 75L	74 75H	76 78L	77 78H	79 7BL	7A 7BH	7C 7EL	7D 7EH
	CS6	5B 5DL	5C 5DH	5E 60L	5F 60H	61 63L	62 63H	64 66L	65 66H	67 69L	68 69H	6A 6CL	6B 6CH
	CS5	49 4BL	4A 4BH	4C 4EL	4D 4EH	4F 51L	50 51H	52 54L	53 54H	55 57L	56 57H	58 5AL	59 5AH
	CS4	37 39L	38 39H	3A 3CL	3B 3CH	3D 3FL	3E 3FH	40 42L	41 42H	43 45L	44 45H	46 48L	47 48H
	CS3	25 27L	26 27H	28 2AL	29 2AH	2B 2DL	2C 2DH	2E 30L	2F 30H	31 33L	32 33H	34 36L	35 36H
	CS2	13 15L	14 15H	16 18L	17 18H	19 1BL	1A 1BH	1C 1EL	1D 1EH	1F 21L	20 21H	22 24L	23 24H
	CS1	01 03L	02 03H	04 06L	05 06H	07 09L	08 09H	0A 0CL	0B 0CH	0D 0FL	0E 0FH	10 12L	11 12H

Figure 15 PWM Register

Table 6 Page 0: 01h ~ FCh PWM Register
Page 1: 01h ~ FCh PWM Register
Page 2: 01h ~ 5Ah PWM Register

Bit	01h D7:D0 03h D3:D0 02h D7:D0 03h D7:D4
Name	PWM
Default	0000 0000

The value of the PWM Registers decides the average current of each LED noted I_{LED}. Please see Figure 15 for more details.

For 6+2-bit and 8-bit mode, I_{LED} is computed as Formula (1).

$$I_{LED} = \frac{PWM}{256} \times I_{OUT(PEAK)} \times Duty \qquad (1)$$

For 12-bit and for 8+4-bit mode, I_{LED} is computed as Formula (2).

$$I_{LED} = \frac{PWM}{4096} \times I_{OUT(PEAK)} \times Duty \qquad (2)$$

$$PWM = \sum_{n=0}^{11} D[n] \cdot 2^n$$

Scaling Register

		SW1	SW2	SW3	SW4	SW5	SW6	SW7	SW8	SW9	SW10	SW11	SW12
PAGE2	CS33	91	92	93	94	95	96	97	98	99	9A	9B	9C
	CS32	85	86	87	88	89	8A	8B	8C	8D	8E	8F	90
	CS31	79	7A	7B	7C	7D	7E	7F	80	81	82	83	84
	CS30	78											
	CS29	77											
	CS28	76											
	CS27	75											
	CS26	74											
	CS25	73											
	CS24	72											
	CS23	71											
	CS22	70											
	CS21	6F											
	CS20	6E											
	CS19	6D											
	CS18	6C											
	CS17	6B											
	CS16	6A											
	CS15	69											
	CS14	68											
	CS13	67											
	CS12	66											
	CS11	65											
	CS10	64											
	CS9	63											
	CS8	62											
	CS7	61											
	CS6	60											
	CS5	5F											
	CS4	5E											
	CS3	5D											
	CS2	5C											
	CS1	5B											

Figure 16 Scaling Register

Where Duty is the duty cycle of SWx, see SCANING TIMING section for more information.

$$Duty = \frac{39.6\mu s}{(39.6\mu s+0.33\mu s+0.01\mu s)} \times \frac{1}{12} = \frac{1}{12.1} \quad (3)$$

Where 39.6μs is t_{SCAN}, the period of scanning and 0.33μs is t_{NOL}, the non-overlap time and 0.01μs is the CSy delay time.

I_{OUT} is the output current of CSy (y=1~33),

$$I_{OUT(PEAK)} = \frac{300}{R_{ISET}} \times \frac{GCC}{256} \times \frac{SL}{256} \quad (4)$$

GCC is the Global Current Control register (PG2, A1h) value, SL is the Scaling Register value as shown in Table 5 and Figure 16. R_{ISET} is the external resistor of ISET pin. D[n] stands for the individual bit value, 1 or 0, in location n.

For example: if D7:D0=1011 0101 (0xB5, 181), GCC=1111 1111, R_{ISET}=10kΩ, SL=1111 1111:

$$I_{LED} = \frac{300}{10k\Omega} \times \frac{GCC}{256} \times \frac{SL}{256} \times Duty \times \frac{PWM}{256} \quad (5)$$

PWM data need to be updated with a writing of FDh register with any value.

Table 7 Page 2 5Bh ~ 9Ch Scaling Register

Bit	D7:D0
Name	SL
Default	0000 0000

Scaling register control the DC output current of each dot. Each dot has a byte to modulate the scaling in 256 steps. For CS1-CS30, all SW channels use the same SL(5B~78h), and for CS31-CS33, each SW channel uses unique SL (79~9Ch).

The value of the Scaling Register decides the peak current of each LED noted $I_{OUT(PEAK)}$.

$I_{OUT(PEAK)}$ computed by Formula (4):

$$I_{OUT(PEAK)} = \frac{300}{R_{ISET}} \times \frac{GCC}{256} \times \frac{SL}{256} \qquad (4)$$

$$SL = \sum_{n=0}^{7} D[n] \cdot 2^n$$

I_{OUT} is the output current of CSy (y=1~33), GCC is the Global Current Control Register (PG2, A1h) value and R_{ISET} is the external resistor of ISET pin. D[n] stands for the individual bit value, 1 or 0, in location n.

For example: if R_{ISET}=10kΩ, GCC=1111 1111, SL=0111 1111:

$$SL = \sum_{n=0}^{7} D[n] \cdot 2^n = 127$$

$$I_{OUT} = \frac{300}{10k\Omega} \times \frac{255}{256} \times \frac{127}{256} = 16.8mA$$

$$I_{LED} = 16.8mA \times \frac{1}{12.1} \times \frac{PWM}{256}$$

Table 8 Page 2 A0h Configuration Register

Bit	D7:D4	D3:D2	D1	D0
Name	SWS	PWMM	-	SSD
Default	0000	00	0	0

The Configuration Register sets operating mode of IS32FL3761.

When SSD is "0", IS32FL3761 works in software shutdown mode and to operate it normally the SSD bit should set to "1". SWS controls the duty cycle of the SW, default mode is 1/12.

SSD	Software Shutdown Control
0	Software shutdown
1	Normal operation

PWMM	PWM Mode
00	6+2-bit
01	8-bit
10	8+4-bit
11	12-bit

SWS	SWx Setting
0000	SW1~SW12, 1/12 (All SWx active)
0001	SW1~SW11, 1/11, SW12(Not active)
0010	SW1~SW10, 1/10, SW11~SW12 (Not active)
0011	SW1~SW9, 1/9, SW10~SW12 (Not active)
0100	SW1~SW8, 1/8, SW9~SW12 (Not active)
0101	SW1~SW7, 1/7, SW8~SW12 (Not active)
0101	SW1~SW6, 1/6, SW7~SW12 (Not active)
0111	SW1~SW5, 1/5, SW6~SW12 (Not active)
1000	SW1~SW4, 1/4, SW5~SW12 (Not active)
1001	SW1~SW3, 1/3, SW4~SW12 (Not active)
1010	SW1~SW2, 1/2, SW3~SW12 (Not active)

Table 9 Page 2 A1h Global Current Control Register

Bit	D7:D0
Name	GCC
Default	0000 0000

The Global Current Control Register modulates all CSy (x=1~33) DC current which is noted as I_{OUT} in 256 steps.

I_{OUT} is computed by the Formula (3):

$$I_{OUT(PEAK)} = \frac{300}{R_{ISET}} \times \frac{GCC}{256} \times \frac{SL}{256} \qquad (4)$$

$$GCC = \sum_{n=0}^{7} D[n] \cdot 2^n$$

Where D[n] stands for the individual bit value, 1 or 0, in location n.

Table 10 Page 2 A2h De-ghost Enable/Resister selection Register

Bit	D7	D6:D4	D3:D2	D1	D0
Name	DGT_EN	-	TIME	SW MODE	CS MODE
Default	0	000	00	0	0

A2h Register enables/disables de-ghost function and select the time as well as resister for the detection.

DGT_EN	De-ghost Enable
0	disable all De-ghost function
1	enable

TIME Time Selection

6+2-bit PWM Mode @V_{CC}= 5V

TIME	PFS= 000	PFS= 001	PFS= 010	PFS= 011~110
00	9 CLK	10 CLK	11 CLK	12 CLK
01	13 CLK	14 CLK	15 CLK	16 CLK
10	7 CLK	8 CLK	9 CLK	10 CLK
11	5 CLK	6 CLK	7 CLK	8 CLK

6+2-bit PWM Mode @V_{CC}= 2.7V

TIME	PFS= 000	PFS= 001	PFS= 010	PFS= 011	PFS= 100~110
00	6 CLK	9 CLK	11CLK	11CLK	12CLK
01	10CLK	13CLK	15CLK	15CLK	16CLK
10	4 CLK	7 CLK	9 CLK	9 CLK	10CLK
11	2 CLK	5 CLK	7 CLK	7 CLK	8 CLK

Other PWM Mode @V_{CC}= 5V

TIME	PFS= 000	PFS= 001	PFS= 010	PFS= 011~110
00	5 CLK	6 CLK	7 CLK	8 CLK
01	13 CLK	14 CLK	15 CLK	16 CLK
10	29 CLK	30 CLK	31 CLK	32 CLK
11	61 CLK	62 CLK	63 CLK	63 CLK

Other PWM Mode @V_{CC}= 2.7V

TIME	PFS= 000	PFS= 001	PFS= 010	PFS= 011	PFS= 100~110
00	2 CLK	5 CLK	7 CLK	7 CLK	8 CLK
01	10CLK	13CLK	15CLK	15CLK	16 CLK
10	26CLK	29CLK	31CLK	31CLK	31 CLK
11	58CLK	61CLK	63CLK	63CLK	63 CLK

Note 8: This CLK refers to the oscillator clock frequency after selecting the PFS and LFM Settings.

SW MOD SW Mode
0 Between SW
1 When SW OFF De-ghost begin

CS MOD CS Mode
0 Between SW
1 When CS OFF De-ghost begin

Table 11 Page 2 A3h Pull Down/Up Resistor Selection Register

Bit	D7	D6:D4	D3	D2:D0
Name	PHC	SWPDR	-	CSPUR
Default	0	000	0	000

A3h Register Set pull down resistor for SWx and pull up resistor for CSy.

Please check DE-GHOST FUNCTION section for more information.

PHC Phase choice
0 0 degree phase delay
1 180 degree phase delay

SWPDR SWx Pull down Resister Selection Bit
000 No pull up
001 2.6V
010 2.2V
011 1.9V
100 1.6V
101 1.2V
110 0.9V
111 GND

CSPUR CSy Pull up Resister Selection Bit
000 No pull up
001 PV_{CC}-2.3V
010 PV_{CC}-2.0V
011 PV_{CC}-1.7V
100 PV_{CC}-1.4V
101 PV_{CC}-1.1V
110 PV_{CC}-0.8V
111 PV_{CC}

Table 12 Page 2 A4h PWM Frequency Register

Bit	D7:D6	D5	D4:D3	D2:D0
Name	-	LFM	-	PFS
Default	00	0	00	000

A4h register sets the PWM frequency as well as it enables low/normal Frequency mode.

LFM is Low frequency mode enable bit. If LFM= “0”, The PWM frequency is set by the PFS bit. If LFM = “1”, The PWM frequency will be one-third of the set for PFS. This helps to reduce ICC when applied at low frequencies.

PFS control PWM frequency setting bits. For example, if PWM Mode is 6+2-bit and PFS = “010”, that the PWM frequency is 78kHz and the scan frequency is 1/12 namely SWS = “0000” is 6.5kHz.

LFM	Low frequency mode
0	Normal (Default)
1	PWM frequency and OSC frequency is slowed by three times

PFS	PWM frequency setting
000	312kHz for 6+2-bit mode (Scan frequency is 26kHz when n=12) 92kHz for 8-bit mode 92kHz for 8+4-bit mode 6kHz for 12-bit mode 24MHz OSC
001	156kHz for 6+2-bit mode 46kHz for 8-bit mode 46kHz for 8+4-bit mode 3kHz for 12-bit mode 12MHz OSC
010	78kHz for 6+2-bit mode 23kHz for 8-bit mode 23kHz for 8+4-bit mode 1.5kHz for 12-bit mode 6MHz OSC
011	39kHz for 6+2-bit mode 11.5kHz for 8-bit mode 11.5kHz for 8+4-bit mode (not allowed when n>6, when PWM=0x01, it is Scan frequency only 60+Hz) 750Hz for 12-bit mode (not allowed when n>6) 3MHz OSC
100	19.5kHz for 6+2-bit mode 5.75kHz for 8-bit mode 5.75kHz for 8+4-bit mode (not allowed when n>3, when PWM=0x01, it is Scan frequency only 30+Hz) 375Hz for 12-bit mode (not allowed when n>3) 1.5MHz OSC
101	9.75kHz for 6+2-bit mode 2.875kHz for 8-bit mode 2.875kHz for 8+4-bit mode (not allowed, when PWM=0x01, it is Scan frequency only 10+Hz) 187.5Hz for 12-bit mode (not allowed) 0.75MHz OSC
110	4.875kHz for 6+2-bit mode 1.438kHz for 8-bit mode 1.438kHz for 8+4-bit mode (not allowed, when PWM=0x01, it is Scan frequency only 7+Hz) 93.75Hz for 12-bit mode (not allowed) 0.375MHz OSC

Table 13 Page 2 A5h Spread Spectrum Register

Bit	D7:D6	D5	D4	D3:D2	D1:D0
Name	SYNCE	-	SSP	SSR	SSCLT
Default	00	0	0	00	00

A5h register enables the spread spectrum function, and its range/cycle time can be selected by the corresponding bits. Writing “11” to the SYNCE function bits is not allowed.

To be configured as a clock slave device and accept an external clock input the slave device’s SYNC bits must be set to “10”.

When SSP enables, the spread spectrum function will be enabled and the SSR & SSCLT bits will adjust the range and cycle time of spread spectrum function. It is recommended that PFS<010 because when using at the low operating frequency it may cause flashing of LED at lower PWM.

SYNCE	SYNC function Enable
0x	Disable SYNC function, 30kΩ pull-low
10	Slave, clock input
11	Not allowed

SSP	Spread spectrum function
0	Disable
1	Enable

SSR	Spread Spectrum Range
00	±5%
10	±20%
11	±25%
01	Not allowed

SSCLT	Spread Spectrum Cycle Time
00	1.8ms
01	1.1ms
10	0.82ms
11	0.66ms

Table 14 Page 2 A6h Open Short Register

Bit	D7:D6	D5:D4	D3:D0
Name	O/S	-	OS of SW
Default	00	00	0000

A6h enables/disables open/short detect information which can be detected by selecting the equivalent SW1~12.

When O/S is “10” or “11”, the Open/short detect enable. If O/S is “10”, Open detect enable and if O/S is “11”, Short detect enable, and the result is stored in A7h~ABh registers.

O/S	Select open or short
0x	Disable
10	Open
11	Short

OS of SW	Select which SW to detect
0000	SW1
0001	SW2
…	
1011	SW12

Note 9: It should be noted that it will not store both open/short detect information at the same time, either it will store open or it will store short information. Open/short information can be read by the A7h~ABh registers.

Table 15 Page 2 A7h Open Short Register

Bit	D7:D0
Name	CS08:CS01
Default	0000 0000

Table 16 Page 2 A8h Open Short Register

Bit	D7:D0
Name	CS16:CS09
Default	0000 0000

Table 17 Page 2 A9h Open Short Register

Bit	D7:D0
Name	CS24:CS17
Default	0000 0000

Table 18 Page 2 AAh Open Short Register

Bit	D7:D0
Name	CS32:CS25
Default	0000 0000

Table 19 Page 2 ABh Open Short Register

Bit	D7:D0
Name	CS33
Default	0000 0000

After setting 0/S of A6h register, A7h~ABh can be read for the open or short information of each LED string. A6h needs to be set to 0x00 before another set to enable open/short test.

When O/S is set to “10”, open detection will be triggered once, and the open information will be stored at A7h~ABh registers. When O/S (A6h) is set to “11”, short detection will be triggered once, and the short information will be stored at A7h~ABh registers.

To get the correct open/short information, several configurations are recommended to set before setting the O/S bits (D7:D6 of A6h).

1. GCCx=0x10, too low or too high GCCx, like GCCx=0x01, may read out incorrect open information.
2. PWM> 50% duty cycle, too low PWM, like PWM=0x01, may read out incorrect open information.

Page 0 DFh Reset Register

Once user writes the Reset Register with 0xAE, IS32FL3761 will reset all the IS32FL3761 registers to their default value. On initial power-up, the IS32FL3761 registers are reset to their default values for a blank display.

APPLICATION INFORMATION

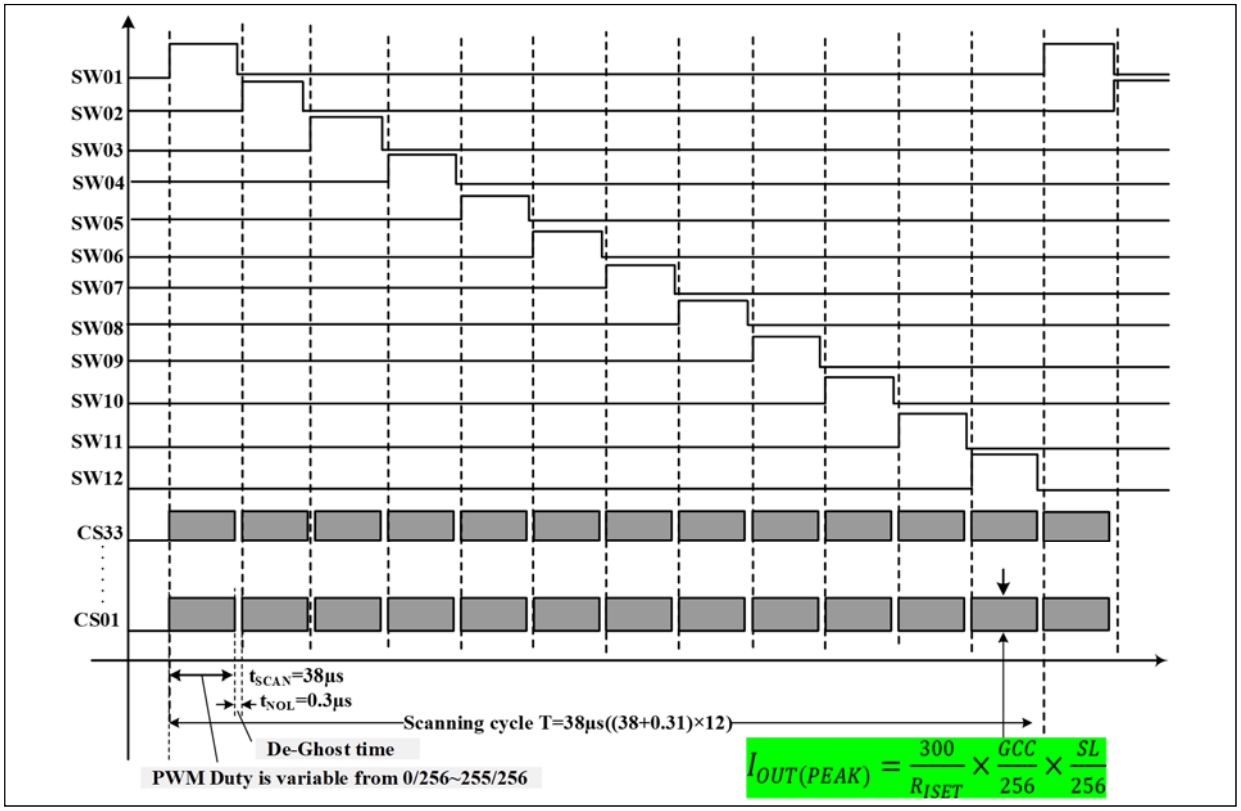


Figure 17 Scanning Timing

SCANING TIMING

As shown in Figure 17 above, the SW1~SW12 is turned on by serial, LED is driven 12 by 12 within the SWx (x=2~12) on time (SWx, x=2~12 is source and it is high when LED on), including the non-overlap blanking time during scan, the duty cycle of SWx (active high, x=2~12) is:

$$Duty = \frac{39.6\mu s}{(39.6\mu s+0.33\mu s+0.01\mu s)} \times \frac{1}{12} = \frac{1}{12.1} \quad (3)$$

Where 39.6μs is t_{SCAN}, the period of scanning and 0.33μs is t_{NOL}, the non-overlap time and 0.1μs is the CSy delay time.

And the scan frequency is 1/n of PWM frequency, where n is SW scan number that can be choose by SWS of Page2 A0h register and the number of select range as 2, 3, 4 … 12. For example, when n = 11, namely SWS = 0001, and the PWM frequency is 312kHz, the scan frequency is 1/11 of PWM frequency is 28.4kHz; or when n = 10, the scan frequency is 1/10 of PWM frequency is 31.2kHz…

PWM CONTROL

After setting the I_{OUT} and GCC, the brightness of each LEDs (LED average current (I_{LED})) can be modulated with 256 or 4096 steps by PWM Register, as described in equation (1). For 6+2-bit and 8-bit mode, ILED is computed as Formula (1).

$$I_{LED} = \frac{PWM}{256} \times I_{OUT(PEAK)} \times Duty \quad (1)$$

For 8+4-bit and 12-bit mode, I_{LED} is computed as Formula (2).

$$I_{LED} = \frac{PWM}{4096} \times I_{OUT(PEAK)} \times Duty \quad (2)$$

GCC is the Global Current Control register (PG2, A1h) value, R_{ISET} is the external resistor of ISET pin. D[n] stands for the individual bit value, 1 or 0, in location n.

For example: if D7:D0=1011 0101 (0xB5, 181), GCC=1111 1111, R_{ISET}=10kΩ:

$$I_{LED} = \frac{300}{10k\Omega} \times \frac{GCC}{256} \times Duty \times \frac{PWM}{256} \quad (5)$$

Writing new data continuously to the registers can modulate the brightness of the LEDs to achieve a breathing effect.

GAMMA CORRECTION

In order to perform a better visual LED breathing effect, we recommend using a gamma corrected PWM value to set the LED intensity. This results in a reduced number of steps for the LED intensity setting but causes the change in intensity to appear more linear to the human eye.

Gamma correction, also known as gamma compression or encoding, is used to encode linear

luminance to match the non-linear characteristics of display. Since the IS32FL3761 can modulate the brightness of the LEDs with 256 or 4096 steps, a gamma correction function can be applied when computing each subsequent LED intensity setting such that the change in brightness matches the human eye's brightness curve.

Table 20 32 Gamma Steps with 256 PWM Steps

C(0)	C(1)	C(2)	C(3)	C(4)	C(5)	C(6)	C(7)
0	1	2	4	6	10	13	18
C(8)	C(9)	C(10)	C(11)	C(12)	C(13)	C(14)	C(15)
22	28	33	39	46	53	61	69
C(16)	C(17)	C(18)	C(19)	C(20)	C(21)	C(22)	C(23)
78	86	96	106	116	126	138	149
C(24)	C(25)	C(26)	C(27)	C(28)	C(29)	C(30)	C(31)
161	173	186	199	212	226	240	255

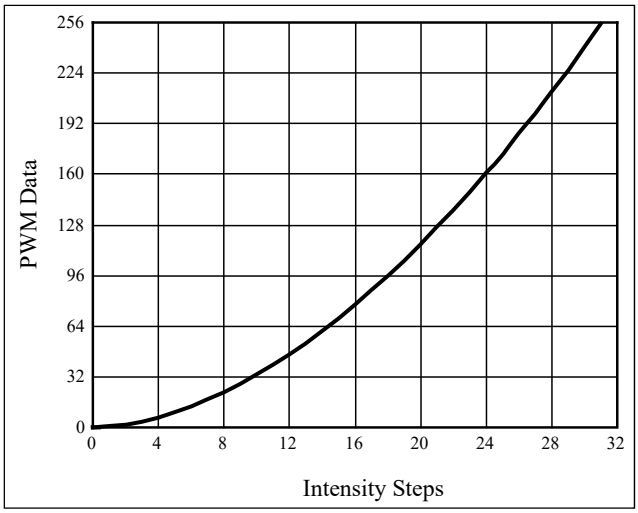


Figure 18 Gamma Correction (32 Steps)

Choosing more gamma steps provides for a more continuous looking breathing effect. This is useful for very long breathing cycles. The recommended configuration is defined by the breath cycle T. When T=1s, choose 32 gamma steps, when T=2s, choose 64 gamma steps. The user must decide the final number of gamma steps not only by the LED itself, but also based on the visual performance of the finished product.

Table 21 64 Gamma Steps with 256 PWM Steps

C(0)	C(1)	C(2)	C(3)	C(4)	C(5)	C(6)	C(7)
0	1	2	3	4	5	6	7
C(8)	C(9)	C(10)	C(11)	C(12)	C(13)	C(14)	C(15)
8	10	12	14	16	18	20	22
C(16)	C(17)	C(18)	C(19)	C(20)	C(21)	C(22)	C(23)
24	26	29	32	35	38	41	44
C(24)	C(25)	C(26)	C(27)	C(28)	C(29)	C(30)	C(31)
47	50	53	57	61	65	69	73
C(32)	C(33)	C(34)	C(35)	C(36)	C(37)	C(38)	C(39)
77	81	85	89	94	99	104	109
C(40)	C(41)	C(42)	C(43)	C(44)	C(45)	C(46)	C(47)
114	119	124	129	134	140	146	152
C(48)	C(49)	C(50)	C(51)	C(52)	C(53)	C(54)	C(55)
158	164	170	176	182	188	195	202
C(56)	C(57)	C(58)	C(59)	C(60)	C(61)	C(62)	C(63)
209	216	223	230	237	244	251	255

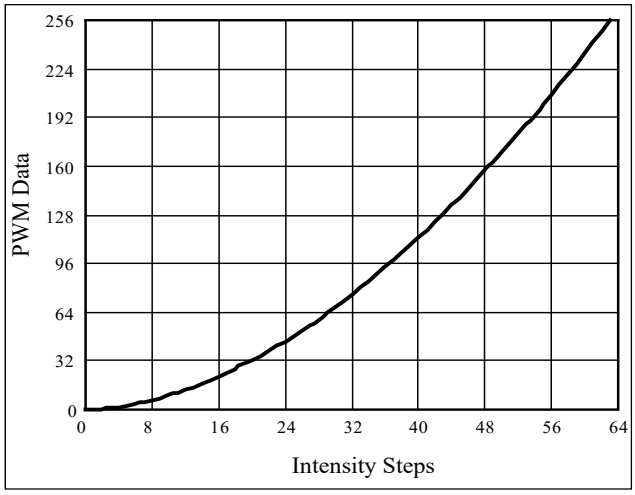


Figure 19 Gamma Correction (64 Steps)

Note 10: The data of 32 gamma steps is the standard value and the data of 64 gamma steps is the recommended value.

OPERATING MODE

IS32FL3761 can only operate in PWM Mode. The brightness of each LED can be modulated with 256 or 4096 steps by PWM registers. For example, if the data in PWM Register is “0000 0100”, then the PWM is the fourth step. Writing new data continuously to the registers can modulate the brightness of the LEDs to achieve a breathing effect.

OPEN SHORT DETECT FUNCTION

IS32FL3761 has an open and short detect bit for each LED.

The open status register stores the open information of LED string. A6h needs to be set to 0x00 before another set to enable open/short test.

When O/S is set to “10”, open detection will be triggered once, and the open information will be stored at A7h~ABh. When O/S (A6h) is set to “11”, short detection will be triggered once, and the short information will be stored at A7h~ABh to get the correct open information, several configurations are recommended to set before setting the O/S bit (D7:D6 of A6h):

1. GCCx=0x10, too low or too high GCCx, like GCCx=0x01, may read out incorrect open information.
2. PWM> 50% duty cycle, too low PWM, like PWM=0x01, may read out incorrect open information.

DE-GHOST FUNCTION

The “ghost” term is used to describe the behavior of an LED that should be OFF but instead glows dimly when another LED is turned ON. A ghosting effect typically can occur when multiplexing LEDs. In matrix architecture any parasitic capacitance found in the constant-current outputs or the PCB traces to the LEDs may provide sufficient current to dimly light an LED to create a ghosting effect.

To prevent this LED ghost effect, the IS32FL3761 has integrated Pull down resistors for each SWx (x=2~12) and pull up resistors for each CSy (y=1~33). Select the right SWx Pull down resistor and CSy Pull up resistor (Page 2, A3h) which eliminates the ghost LED for a particular matrix layout configuration. Typically, selecting the SWx Pull down to 2.6V，CS Pull up to PVCC-2.3V will be sufficient to eliminate the LED ghost phenomenon.

The SWx Pull down resistors and CSy Pull up resistors are active only when the CSy/SWx output is working in the OFF state and therefore no power is lost through these resistors.

INTERFACE RESET

The SPI/I2C will be reset if the SDB pin is pull-high from 0V to logic high, at the operating SDB rising edge.

SHUTDOWN MODE

Shutdown mode can be used as a means of reducing power consumption. During shutdown mode all registers retain their data.

Software Shutdown

By setting SSD bit of the Configuration Register (PG2, A0h) to “0”, the IS32FL3761 will operate in software shutdown mode. When the IS32FL3761 is in software shutdown, all current sources are switched off, so that the matrix is blanked. All registers can be operated. Typical current consumption is 0.6μA.

Hardware Shutdown

The chip enters hardware shutdown when the SDB pin is pulled low. All analog circuits are disabled during hardware shutdown, typical the current consume is 0.6μA.

The chip releases hardware shutdown when the SDB pin is pulled high.

If VCC has a risk drop below 1.75V but above 0.1V during SDB pulled low, please re-initialize all Function Registers before SDB pulled high.

LAYOUT

As described in external resistor (R_{ISET}), the chip consumes lots of power. Please consider below factors when layout the PCB.

1. The V_{CC} (PVCC) capacitors need to be close to the chip and the ground side should be well connected to the GND of the chip.

2. R_{ISET} should be close to the chip and the ground side should connect well to the GND of the chip.

3. The thermal pad should connect to ground pins and the PCB should have the thermal pad too, usually this pad should have 16 or 25 via through the PCB to other side’s ground area to help radiate the heat. About the thermal pad size, please refer to the land pattern of each package.

4. The CSy pins current is 30mA (R_{ISET}=10kΩ).

THERMAL CONSIDERATION

The over temperature of the chip may result in deterioration of the properties of the chip. IS32FL3761 has a thermal pad but the chip could be very hot if the power is very large. So do consider the ground area connects to the GND pins and thermal pad. Other traces should keep away and ensure the ground area below the package is integrated, and the back layer should be connected to the thermal pad thru 9 or 16 vias to be maximized the area size of ground plane.

The package thermal resistance, θ_{JA}, determines the amount of heat that can pass from the silicon die to the surrounding ambient environment. The θ_{JA} is a measure of the temperature rise created by power dissipation and is usually measured in degree Celsius per watt (°C/W).

When operating the chip at high ambient temperatures, or when driving maximum load current, care must be taken to avoid exceeding the package power dissipation limits. The maximum power dissipation can be calculated using the following Formula (6):

$$P_{D(MAX)} = \frac{T_{J(MAX)} - T_A}{\theta_{JA}} \quad (6)$$

So,

$$P_{D(MAX)} = \frac{125°C - 25°C}{34.5°C/W} \approx 2.9W$$

Figure 20 shows the power derating of the IS32FL3761 on a JEDEC boards (in accordance with JESD 51-5 and JESD 51-7) standing in still air.

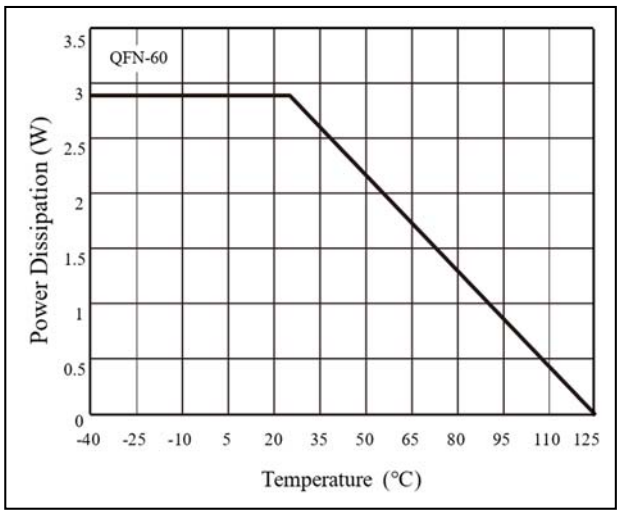


Figure 20 Dissipation Curve

6+2-BIT PWM MODE

When PWMM of the Control Register (PG2, A0h) are “00”, 6+2-bit PWM Mode is enabled. Then the final output PWM frequency is 6-bit, resolution is 8-bit. This is achieved through 6-bit PWM modulation and 2-bit dither control. For 2-bit dither, according to the 4-dither timing, each of the 4 PWM groups can add one PWM_H or no PWM_H.

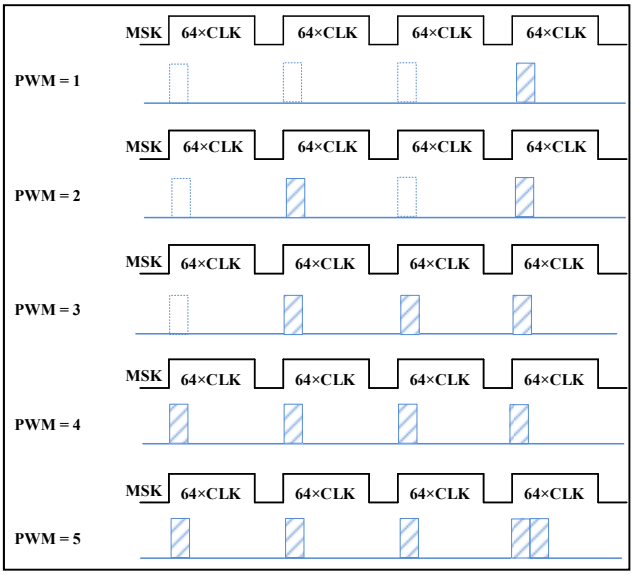


Figure 21 PWMM= “00”, 6+2-bit PWM Mode Enable

8+4-BIT PWM MODE

When PWMM of the Control Register (PG2, A0h) are “10”, 8+4-bit PWM Mode is enabled. Then the final output PWM frequency is 8-bit, resolution is 12-bit. This is achieved through 8-bit PWM modulation and 4-bit dither control. For 4-bit dither, according to the 16-dither timing, each of the 16 PWM groups can add one PWM_x or no PWM_x (Where x= H or L).

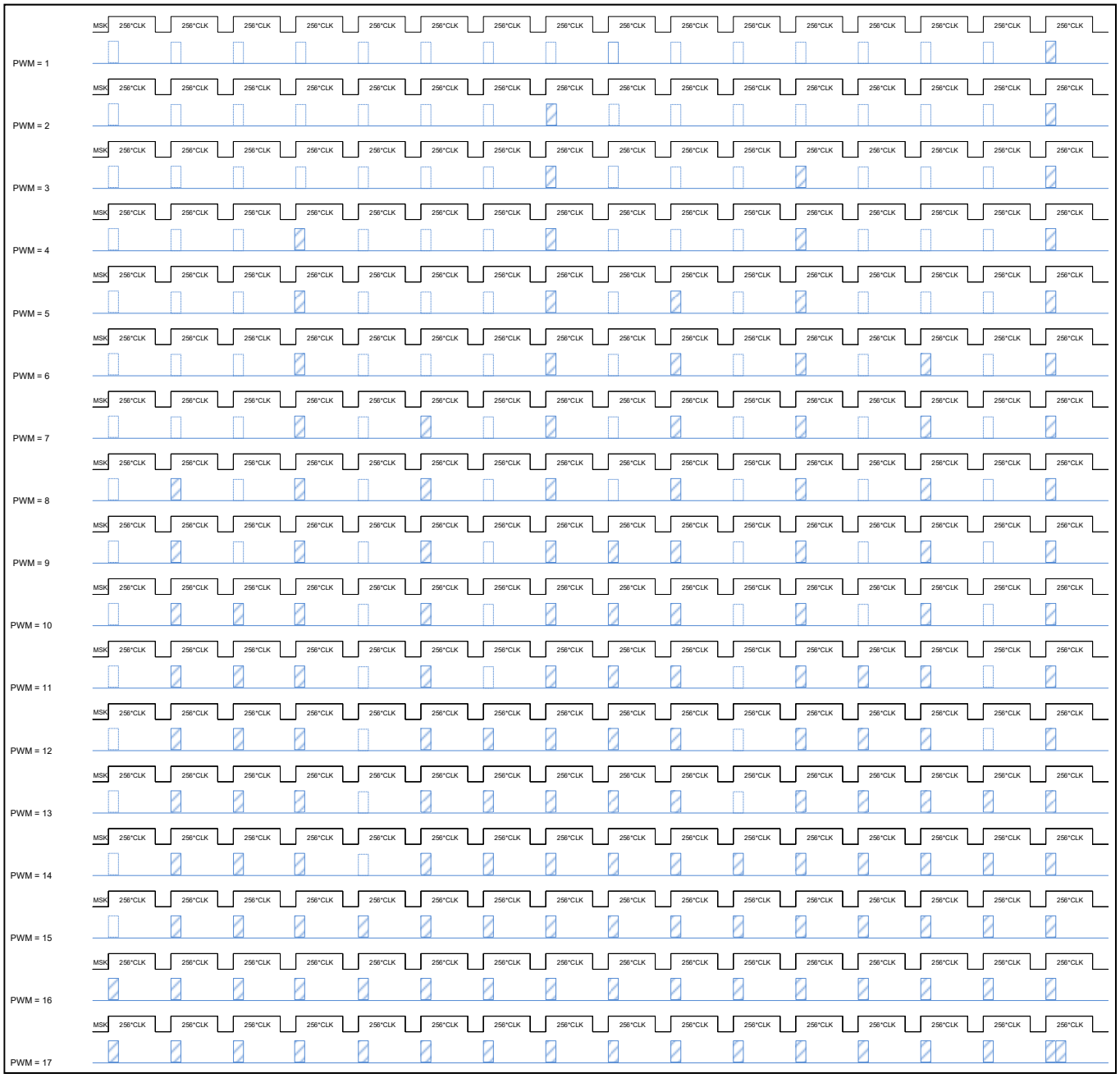


Figure 22 PWMM= “10”, 8+4-bit PWM Mode Enable

CLASSIFICATION REFLOW PROFILES

Profile Feature	Pb-Free Assembly
Preheat & Soak Temperature min (Tsmin) Temperature max (Tsmax) Time (Tsmin to Tsmax) (ts)	150°C 200°C 60-120 seconds
Average ramp-up rate (Tsmax to Tp)	3°C/second max.
Liquidous temperature (TL) Time at liquidous (tL)	217°C 60-150 seconds
Peak package body temperature (Tp)*	Max 260°C
Time (tp)** within 5°C of the specified classification temperature (Tc)	Max 30 seconds
Average ramp-down rate (Tp to Tsmax)	6°C/second max.
Time 25°C to peak temperature	8 minutes max.

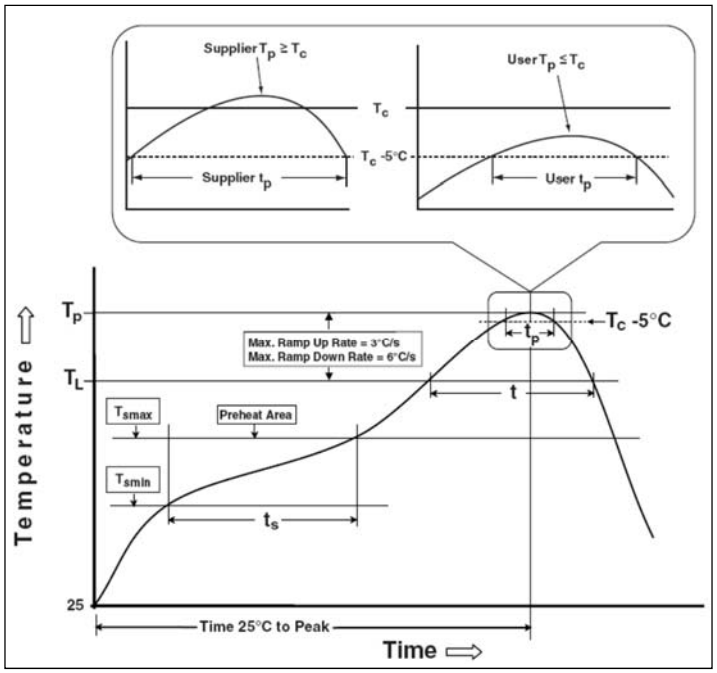
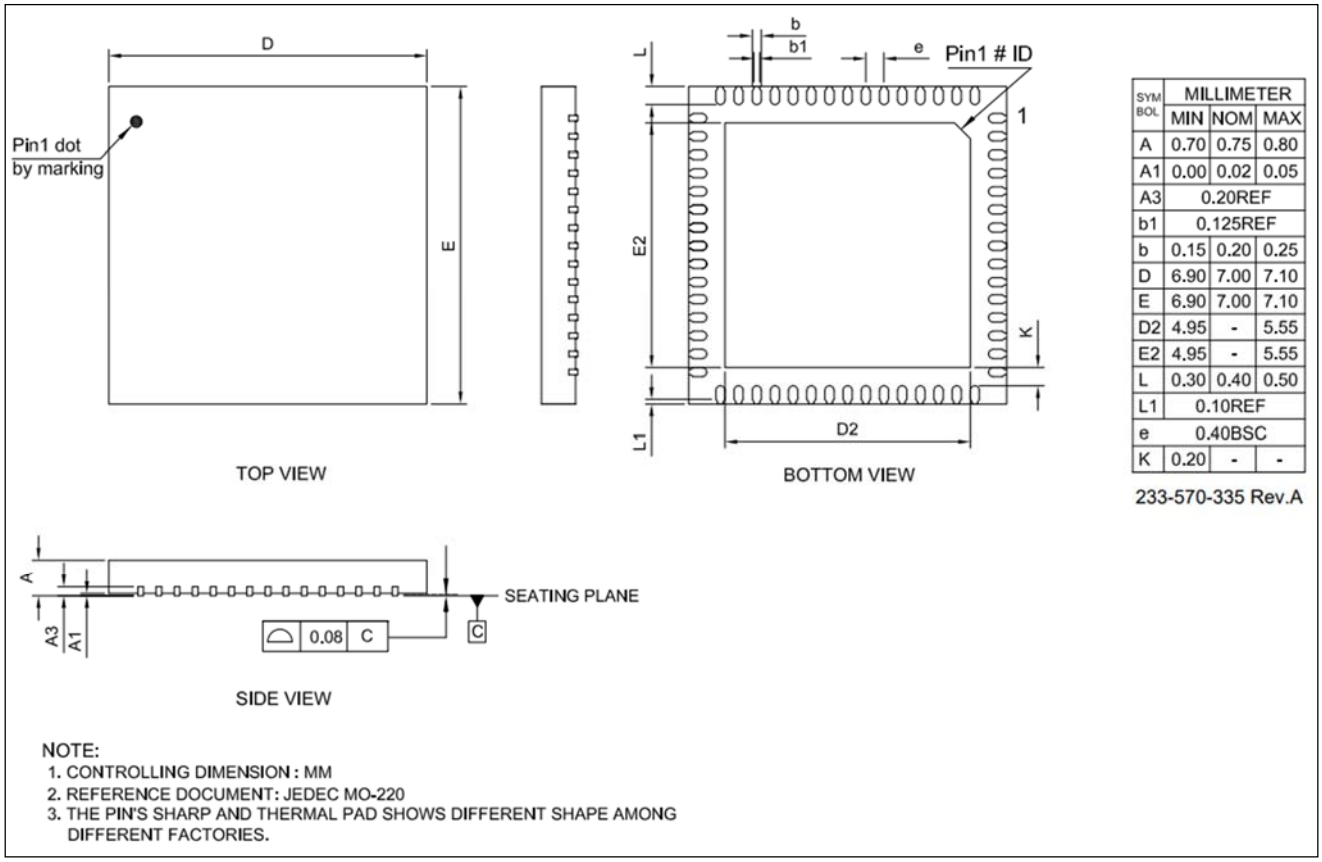


Figure 23 Classification Profile

PACKAGE INFORMATION

QFN-60



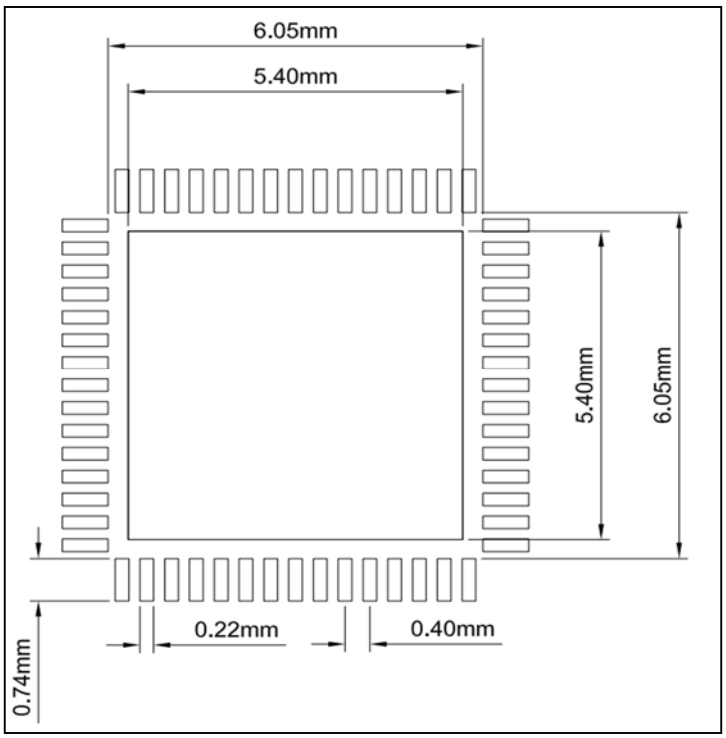
SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	0.70	0.75	0.80
A1	0.00	0.02	0.05
A3		0.20REF	
b1		0.125REF	
b	0.15	0.20	0.25
D	6.90	7.00	7.10
E	6.90	7.00	7.10
D2	4.95	-	5.55
E2	4.95	-	5.55
L	0.30	0.40	0.50
L1		0.10REF	
e		0.40BSC	
K	0.20	-	-

233-570-335 Rev.A

NOTE:
1. CONTROLLING DIMENSION : MM
2. REFERENCE DOCUMENT: JEDEC MO-220
3. THE PIN'S SHARP AND THERMAL PAD SHOWS DIFFERENT SHAPE AMONG DIFFERENT FACTORIES.

RECOMMENDED LAND PATTERN

QFN-60



Note:

1. Land pattern complies to IPC-7351.
2. All dimensions in MM.
3. This document (including dimensions, notes & specs) is a recommendation based on typical circuit board manufacturing parameters. Since land pattern design depends on many factors unknown (eg. User's board manufacturing specs), user must determine suitability for use.

REVISION HISTORY

Revision	Detail Information	Date
0A	Initial release	2024.04.12