IS32LT3131A/B/C

12 CHANNEL LINEAR LED DRIVER WITH UART/CANLITE/SPI INTERFACE

May 2024

1 GENERAL DESCRIPTION

The IS32LT3131A/B/C is a linear LED driver with 12 programmable current sources capable of up to 75mA each. It supports an external thermal shunt resistor that dissipates thermal energy away from the LED driver to minimize thermal stress on the device and maintain a high output current accuracy. There are three bus interface options, UART (IS32LT3131A), CANLITE (IS32LT3131B) or SPI (IS32LT3131C) used for individual output control by a host MCU. A configurable watchdog automatically sets fail-safe modes should the bus interface loose communication.

Each output can individually support 10-bit PWM dimming and 8-bit DC current adjustment. The output channels can be combined to provide a higher current drive capability, up to 900mA.

For added system reliability, the IS32LT3131A/B/C integrates fault detection circuitry for LED string open/short, single LED short, overcurrent, overvoltage and over temperature conditions. The fault condition can be reported by a dedicated fault reporting pin (FAULTB) and the fault details can be read from the Fault Flag Registers. Multiple FAULTB pins can be tied together to disable all IS32LT3131A/B/C devices on the same parallel circuit to satisfy the “One Fail All Fail” requirement.

The IS32LT3131A/B/C is targeted at pixel-controlled automotive lighting market, such as interior and exterior animation light. It is offered in a thermally enhanced eTSSOP-28 package.

2 APPLICATIONS

- Automotive LED Lighting
  - Animation taillight
  - Animation daytime running light
  - Cluster display

3 FEATURES

- Wide input voltage supply from 4.5V to 40V
- Thermal shunt resistor to minimize device thermal stress
- UART interface (IS32LT3131A), CANLITE interface (IS32LT3131B), SPI interface (IS32LT3131C) with Lumibus protocol
  - UART/CANLITE interface compatible with CAN physical layer, 100kbps~1Mbps baud rate
  - SPI supports up to 9MHz
  - CRC to ensure robustness of communication
  - Support up to maximum 16 addressable devices (IS32LT3131A/B)
  - Watchdog timer to support fail-safe mode
- 12 current source channel outputs
  - Up to 75mA per channel set by resistor
  - ±5% device-to-device output current accuracy
  - Channels can be combined for higher current capability with same current accuracy
  - Low headroom voltage of 1.2V (Max.) at 75mA
- Individual PWM dimming for each channel
  - 10-bit PWM duty cycle setting
  - Programmable PWM frequency up to 31.25kHz
  - PWM phase control minimizes inrush current
  - Current slew rate control and spread spectrum to optimize EMI performance
- Individual 8-bit DC current adjustment on each channel
- 32-step global DC current setting
- Functional Safety-Capable
  - Documentation available to aid functional safety system design
- Fault protection with reporting
  - Programmable fail-safe modes
  - LED string open/short detection
  - Single LED short detection
  - Overcurrent (ISET pin shorted)
  - Overvoltage
  - CRC error
  - Programmable over temperature current roll-off
  - Thermal shutdown
  - Programmable fault reporting delay time
  - FAULTB pin for hardware fault reporting, allowing parallel bus connection for “One Fail All Fail” or “One Fail Others On” options
- Operating junction temperature range (-40°C ~ +150°C)
- AEC-Q100 Qualified with Temperature Grade 1: -40°C to 125°C
- RoHS & Halogen-Free Compliance
- TSCA Compliance

4 TYPICAL APPLICATION CIRCUIT

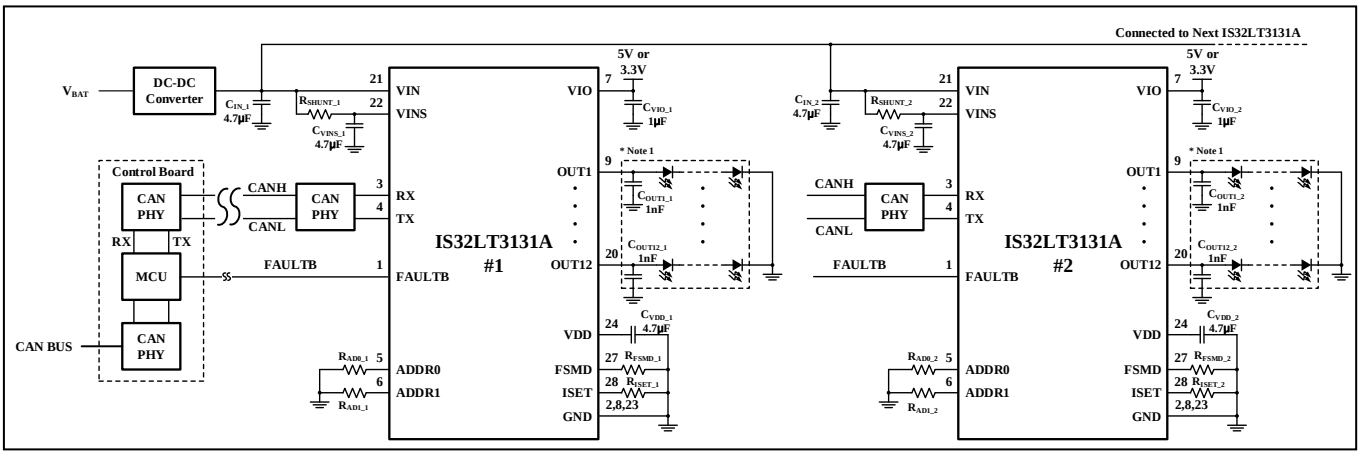


Figure 1 Typical Application Circuit of Multiple IS32LT3131A with External CAN Transceiver for Off-board Long Distance Communication

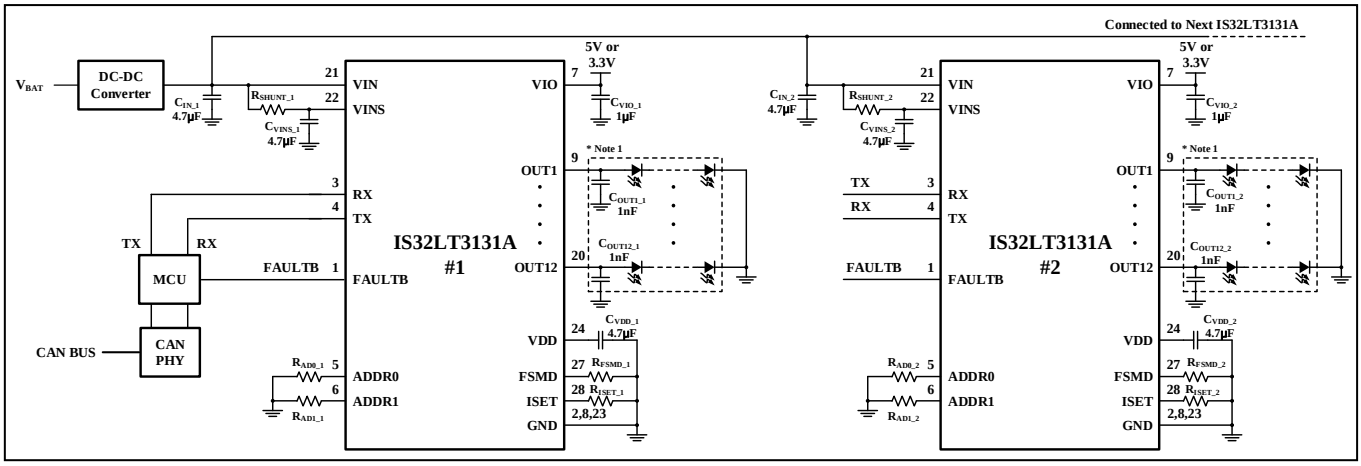


Figure 2 Typical Application Circuit of Multiple IS32LT3131A with UART Interface for On-board Communication

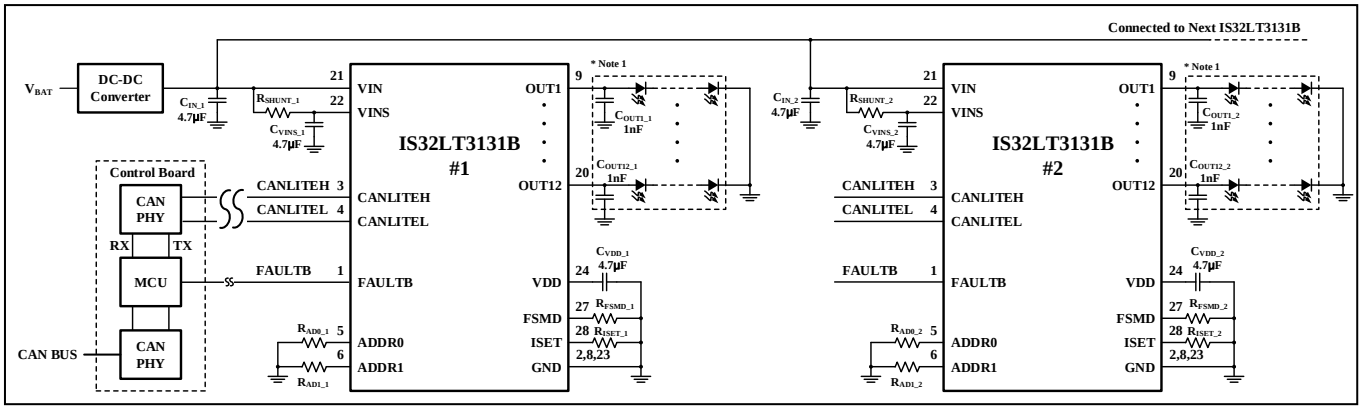


Figure 3 Typical Application Circuit of Several IS32LT3131B with CANLITE Interface for Off-board Long Distance Communication

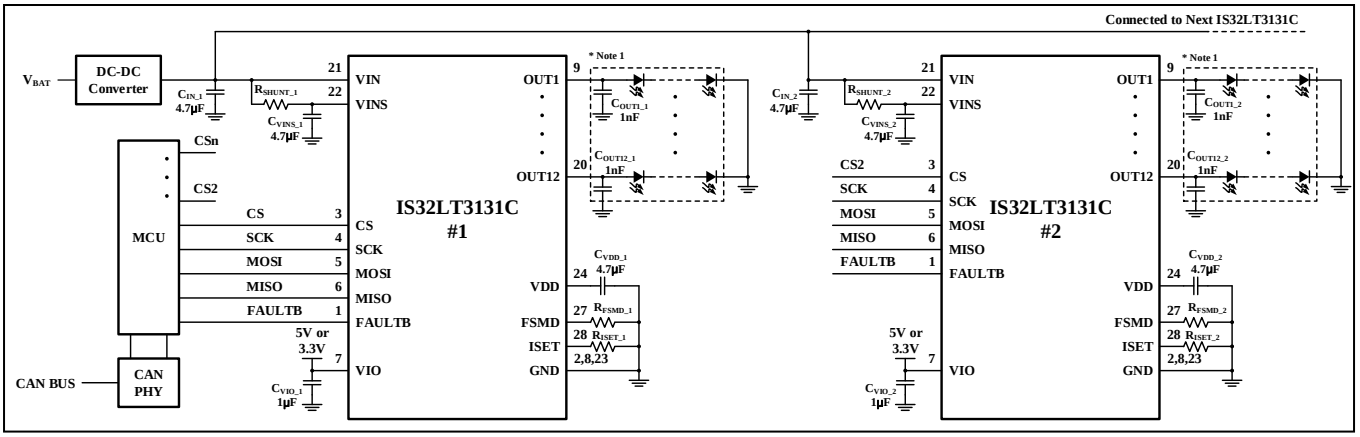
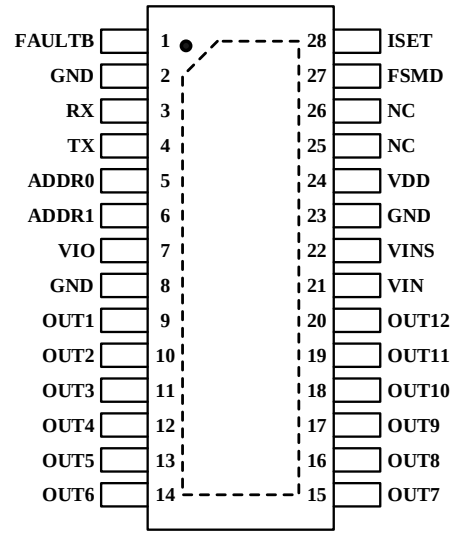
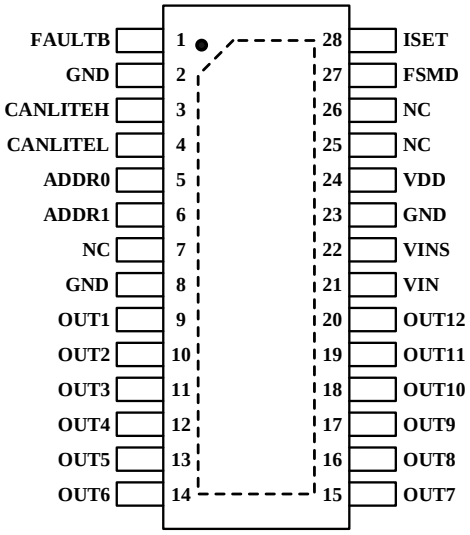
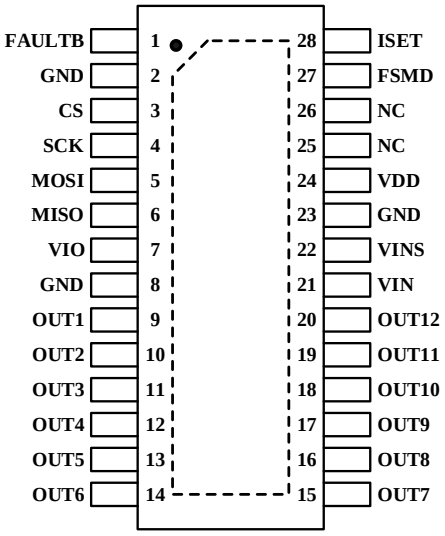


Figure 4 Typical Application Circuit of Several IS32LT3131C with SPI Interface for On-board Communication

Note 1: The capacitors C_{OUT1}~C_{OUT12} are recommended for most applications. These capacitors must be placed as close to the corresponding OUTx pin as possible to optimize the EMI and ESD performance, especially when LEDs are connected to OUTx with long wires. The recommended value is 1nF~10nF.

Note 2: The thermal shunt mechanism (R_{SHUNT}) is optional. When the power supply voltage does not have significant variation, the thermal shunt mechanism can be saved by connecting the VINS pin directly to the VIN pin.

5 PIN CONFIGURATION AND DESCRIPTION

Package	Device	Pin Configuration (Top View)
eTSSOP-28	IS32LT3131A	
	IS32LT3131B	
	IS32LT3131C	

PIN DESCRIPTION

No.	Pin	Description
1	FAULTB	Open drain fault reporting pin. In the “One Fail All Fail” mode, this pin is also an input pin. Pulling this pin low will disable the device outputs.
2, 8, 23	GND	Ground pin.
3 (IS32LT3131A)	RX	UART interface receive data pin.
4 (IS32LT3131A)	TX	UART interface transmit data pin.
3 (IS32LT3131B)	CANLITEH	CANLITE interface high-level pin.
4 (IS32LT3131B)	CANLITEL	CANLITE interface low-level pin.
5, 6 (IS32LT3131A/B)	ADDR0, ADDR1	Address set. Connect a proper valued resistor from this pin to GND to assign the address.
3 (IS32LT3131C)	CS	SPI interface chip select pin.
4 (IS32LT3131C)	SCK	SPI interface clock pin.
5 (IS32LT3131C)	MOSI	SPI interface data input pin.
6 (IS32LT3131C)	MISO	SPI interface data output pin.
7 (IS32LT3131A/C)	VIO	Power supply for MISO or TX output. It requires a 1μF X7R ceramic capacitor from this pin to GND, which must be placed close to this pin.
9~20	OUT1~OUT12	LED output channels.
21	VIN	Power supply input. It requires a ≥4.7μF X7R ceramic capacitor from this pin to GND, which must be placed close to this pin.
22	VINS	Thermal shunt pin. Connect a proper valued power resistor from VIN to this pin to shunt the power dissipation on the device. It needs a ≥4.7μF X7R ceramic capacitor from this pin to GND, which must be placed close to this pin. If the thermal shunt mechanism is not implemented, connect both VIN and VINS pins to the power supply.
24	VDD	5V internal LDO output. Connect a 4.7μF X7R ceramic capacitor from this pin to GND, which must be placed close to this pin.
25, 26 7 (IS32LT3131B)	NC	No connection. Recommend connecting to GND.
27	FSMD	Connect different value resistor to GND to select fail-safe mode.
28	ISET	Resistor on this pin to GND sets the maximum output current for OUT1~OUT12 LED channels.
	Thermal Pad	MUST be electrically connected to a large GND plane for optimum thermal dissipation.

6 ORDERING INFORMATION

Automotive Range: -40°C to +125°C

Order Part No.	Package	QTY/Reel
IS32LT3131A-ZLA3-TR IS32LT3131B-ZLA3-TR IS32LT3131C-ZLA3-TR	eTSSOP-28, Lead-free	2500

7 SPECIFICATIONS

7.1 ABSOLUTE MAXIMUM RATINGS

Supply voltage, V_{IN} and V_{INS}	-0.3V ~ +42V
Voltage at FAULTB pin	-0.3V ~ +42V
Voltage at CANLITEH, CANLITEL pins	-20V ~ +20V
Differential voltage between CANLITEH, CANLITEL pins, ($V_{CANLITEH}$-$V_{CANLITEL}$)	-5V ~ +15V
Voltage at CS(RX), SCK(TX), MOSI (ADDR0), MISO(ADDR1), ISET, FSMD, VIO, VDD pins	-0.3V ~ +6V
Voltage at OUT1 to OUT12 pins	-0.3V ~ V_{INS}+0.2V
Maximum operating junction temperature, T_{JMAX}	+150°C
Storage temperature range, T_{STG}	-65°C ~ +150°C
Operating temperature range, T_A=T_J	-40°C ~ +150°C
Package thermal resistance, junction to ambient (4-layer standard test PCB based on JESD 51-2A), θ_{JA}	35.5°C/W
Package thermal resistance, junction to thermal PAD (4-layer standard test PCB based on JESD 51-2A), θ_{JP}	11.08°C/W
ESD (HBM) ESD (CDM)	±2kV ±750V

Note 3: Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other condition beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

7.2 ELECTRICAL CHARACTERISTICS

V_{IN}= 5V~40V, T_J= -40°C ~150°C, the detail refers to each condition description, unless otherwise noted.

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
V_{IN}	Supply voltage		4.5		40	V
V_{INS}	Supply voltage		4.5		40	V
I_{IN}	Quiescent current	R_{ISET}= 20kΩ, GCC= 0x3F, SCAx= 0xFF, PWMx= 0x00		13	16	mA
V_{IN_UV}	VIN undervoltage-lockout threshold	Voltage falling, IC disabled	3.7	3.9	4.1	V
V_{IN_UVHY}	VIN undervoltage-lockout hysteresis		170	220	270	mV
V_{DD}	VDD output voltage	V_{IN}> 5.5V, I_{DD}= 60mA	4.55	5	5.25	V
I_{DD_MAX}	VDD output current capability	V_{IN}> 5.5V, V_{DD}> 4V			80	mA
I_{DD_LIM}	VDD output current limit	V_{IN}> 5.5V, V_{DD}= 2.6V	120			mA
V_{DD_UV}	VDD undervoltage-lockout threshold	Voltage falling, IC disabled	3.5	3.7	3.9	V
V_{DD_UVHY}	VDD undervoltage-lockout hysteresis			200		mV
V_{IO}	TX/MISO power supply input		3		5.5	V
f_{OSC}	System clock frequency		31.2	32	32.8	MHz

ELECTRICAL CHARACTERISTICS (CONTINUE)

"♦" This symbol in the table means these limits are guaranteed at room temp T_J= 25°C.
"◊" This symbol in the table means these limits are guaranteed at full temp range T_J= -40°C~125°C.
V_{IN}= 5V~40V, T_J= -40°C ~150°C, the detail refers to each condition description, unless otherwise noted.

Symbol	Parameter	Condition		Min.	Typ.	Max.	Unit
Output Drivers							
I_{OUT}	Output current per channel	R_{ISET}= 8.2kΩ, GCC= 0x3F, SCA=0xFF, PWM=0xFF, CM=0	♦	-3		3	%
			◊	-5		5	
		R_{ISET}= 20kΩ, GCC= 0x3F, SCA=0xFF, PWM=0xFF, CM=0	♦	-3.5		3.5	
			◊	-7		7	
		R_{ISET}= 8.78kΩ, GCC= 0x3F, SCA=0xFF, PWM=0xFF, CM=1	♦	-3		3	
			◊	-5		5	
		R_{ISET}= 87.8kΩ, GCC= 0x3F, SCA=0xFF, PWM=0xFF, CM=1	♦	-4		4	
			◊	-6.5		6.5	
ΔI_{OUT}	I_{OUT} device to device accuracy (ΔI_{OUT}=1-I_{OUT_AVG}/I_{OUT_IDEAL})	R_{ISET}= 8.2kΩ, GCC=0x3F, SCAx=0xFF, PWMx=0xFF, CM=0	♦	-3		3	%
			◊	-5		5	
		R_{ISET}= 8.2kΩ, GCC=0x10, SCAx=0xFF, PWMx=0xFF, CM=0	♦	-3.5		3.5	
			◊	-6.5		6.5	
		R_{ISET}= 8.2kΩ, GCC=0x08, SCAx=0xFF, PWMx=0xFF, CM=0	♦	-4		4	
			◊	-7.5		7.5	
		R_{ISET}= 8.2kΩ, GCC=0x3F, SCAx=0xFF, PWMx=0xFF, CM=1	♦	-3		3	
			◊	-5		5	
V_{HR_MIN}	Minimum headroom voltage from VIN to OUTx (VIN tied to VINS)	R_{ISET}= 8.2kΩ, GCC= 0x3F, SCA=0xFF, PWM=0xFF, CM=0			0.9	1.2	V
		R_{ISET}= 20kΩ, GCC= 0x3F, SCA=0xFF, PWM=0xFF, CM=0			0.6	0.8	
V_{ISET}	ISET pin voltage	R_{ISET}= 8.2kΩ, GCC= 0x3F, SCAx=0xFF, PWMx=0xFF		0.96	1.0	1.04	V
I_{OZ}	OUTx leakage current	V_{OUTx}= 0V, PWM= 0x00				2	μA
f_{PWM}	PWM frequency of outputs	Frequency setting= 25kHz		23.5	25	26.5	kHz
		Frequency setting= 200Hz		188	200	212	Hz
ΔI_{MAT}	I_{OUT} channel to channel mismatch in one device (ΔI_{MAT}=1-I_{OUTx}/I_{OUT_AVG})	R_{ISET}= 8.2kΩ, GCC=0x3F, SCAx=0xFF, PWMx=0xFF, CM=0		-3		3	%
		R_{ISET}= 8.2kΩ, GCC=0x10, SCAx=0x7F, PWMx=0xFF, CM=0		-3		3	
		R_{ISET}= 8.2kΩ, GCC=0x3F, SCAx=0xFF, PWMx=0xFF, CM=1		-5		5	
		R_{ISET}= 8.2kΩ, GCC=0x10, SCAx=0xFF, PWMx=0xFF, CM=1		-7		7	

ELECTRICAL CHARACTERISTICS (CONTINUE)

V_{IN}= 5V~40V, T_J= -40°C ~150°C, the detail refers to each condition description, unless otherwise noted.

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
Protection and Fault Reporting						
T_{SD}	Thermal shutdown	(Note 4)		165		°C
T_{SD_HYS}	Thermal shutdown hysteresis	(Note 4)		10		°C
V_{IH_FAULTB}	FAULTB logic “1” input voltage		2.2			V
V_{IL_FAULTB}	FAULTB logic “0” input voltage				0.8	V
V_{PD_FAULTB}	FAULTB pull-down capability	I_{SINK}= 1mA		0.1	0.2	V
I_{LKG_FAULTB}	FAULTB leakage current	“One Fail Others On”, no fault condition			1	µA
		“One Fail All Fail”, no fault condition			2	µA
V_{SC_FL}	LED string short detection falling threshold	Measured at OUTx to GND	0.9	1	1.1	V
V_{SC_RS}	LED string short detection rising threshold	Measured at OUTx to GND	1.1	1.2	1.3	V
t_{SC}	LED string short detection deglitch time			4		µs
V_{OC_FL}	LED string open detection falling threshold	Measured at (V_{INS}-V_{OUTx})		240	350	mV
V_{OC_RS}	LED string open detection rising threshold	Measured at (V_{INS}-V_{OUTx})		350	460	mV
t_{OC}	LED string open detection deglitch time			4		µs
V_{SLSTH}	Single LED short detection threshold	LEDx_SLSTH = 03h	4.6	5	5.4	V
t_{SSC}	Single LED short detection deglitch time			9		µs
V_{OVP_TH}	Overvoltage detection threshold	Measured at (V_{OUTx}-V_{INS})		0.2		V
t_{OVP}	Overvoltage retry time			1.23		s
I_{ISET_OC}	ISET pin overcurrent detection		170	200	230	µA
V_{FLT_UV}	UVLO of single LED short and LED string open fault detection	Set by 02h register (Default), voltage rising	7.6	8	8.4	V
ADDRESS and FSMD Pins						
$I_{AD/FS}$	ADDR0/ADDR1/FSMD pins source current		46	50	54	µA
$V_{TH1\_AD/FS}$	ADDR0/ADDR1/FSMD pins threshold-1		0.9	1	1.1	V
$V_{TH2\_AD/FS}$	ADDR0/ADDR1/FSMD pins threshold-2		1.85	2	2.15	V
$V_{TH3\_AD/FS}$	ADDR0/ADDR1/FSMD pins threshold-3		2.8	3	3.2	V

ELECTRICAL CHARACTERISTICS (CONTINUE)

V_{IN}= 5V~40V, T_J= -40°C ~150°C, the detail refers to each condition description, unless otherwise noted.

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
UART Interface (IS32LT3131A Only)						
V_{IH_RX}	RX logic “1” input voltage		2			V
V_{IL_RX}	RX logic “0” input voltage				0.7	V
V_{OL_TX}	TX low level output voltage	I_{SINK}= 5mA	0		0.3	V
V_{OH_TX}	TX high level output voltage	I_{SOURCE}= -5mA	V_{IO}-0.3V		V_{IO}	V
I_{LKG_UART}	TX, RX leakage current	TX high-z state	-1		1	μA
C_{IN_RX}	TX, RX input capacitance	TX high-z state (Note 4)		5	10	pF
CANLITE Interface (IS32LT3131B Only)						
V_{O_DOM}	Dominant output voltage	$V_{CANLITEH}$, R_{LOAD}= 50Ω to 65Ω	2.75	3.5	4.5	V
		$V_{CANLITEL}$, R_{LOAD}= 50Ω to 65Ω	0.5	1.5	2.25	V
V_{O_RES}	Recessive output voltage	$V_{CANLITEH}$ and $V_{CANLITEL}$, R_{LOAD}= open	2	0.5× V_{DD}	3	V
V_{O_DIF}	Differential output voltage ($V_{CANLITEH}$-$V_{CANLITEL}$)	Dominant, R_{LOAD}= 50Ω to 65Ω	1.5	2	3	V
		Dominant, R_{LOAD}= 45Ω to 70Ω	1.4	2	3.3	
		Dominant, R_{LOAD}= 2240Ω	1.5		5	
		Recessive, R_{LOAD}= 60Ω	-120	0	12	mV
		Recessive, R_{LOAD}= open	-500	0	50	
V_{SYM}	Driver symmetry ($V_{CANLITEH}$+$V_{CANLITEL}$)/V_{DD}	R_{LOAD}= 60Ω, operating frequency 1MHz	0.9	1.0	1.1	V/V
V_{SYM_DC}	DC output voltage symmetry (V_{DD}-$V_{CANLITEH}$-$V_{CANLITEL}$)	Dominant or recessive, R_{LOAD}= 60Ω	-400		+400	mV
V_{CM}	Common mode voltage range		-10		12	V
V_{REC_IN}	Recessive state differential input voltage	($V_{CANLITEH}$-$V_{CANLITEL}$), -10V≤ V_{CM}≤ 12V	-3		0.5	V
V_{TH_DIF}	Differential receiver threshold voltage	($V_{CANLITEH}$-$V_{CANLITEL}$), -10V≤ V_{CM}≤ 12V	0.5	0.7	0.9	V
V_{HYS_DIF}	Differential receiver threshold voltage hysteresis	($V_{CANL\ ITEH}$-$V_{CANLITEL}$), -10V≤V_{CM}≤ 12V		200		mV
V_{DOM_IN}	Dominate state differential input voltage	($V_{CANLITEH}$-$V_{CANLITEL}$), -10V≤ V_{CM}≤ 12V	0.9		8	V
I_{O_DOM}	Dominant output current	CANLITEH pin, -3V≤ $V_{CANLITEH}$≤ 18V	-115	-60		mA
		CANLITEL pin, -3V≤ $V_{CANLITEL}$≤ 18V		60	115	mA
I_{O_RES}	Recessive output current	$V_{CANLITEH}$= $V_{CANLITEL}$= -12V to 12V	-5		+5	mA

ELECTRICAL CHARACTERISTICS (CONTINUE)

V_{IN}= 5V~40V, T_J= -40°C ~150°C, the detail refers to each condition description, unless otherwise noted.

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
R_{IN_H}	Single ended input resistance (CANLITEH pin)	-2V≤ $V_{CANLITEH}$≤ 7V	6		50	kΩ
R_{IN_L}	Single ended input resistance (CANLITEL pin)	-2V≤ $V_{CANLITEL}$≤ 7V	6		50	
R_{ID}	Differential input resistance	-2V≤ $V_{CANLITEH}$≤ 7V, -2V≤ $V_{CANLITEL}$≤ 7V	12		100	
M_{RIN}	Input resistance matching $2\times(R_{IN\_H}-R_{IN\_L})/(R_{IN\_H}+R_{IN\_L})$	$V_{CANLITEH}$= $V_{CANLITEL}$= 5V	-3		3	%
I_{LKG_CAN}	Unpowered leakage current	$V_{CANLITEH}$=$V_{CANLITEL}$=5V, V_{IN}=0V	0		30	μA
t_{DOM_TX}	Dominant time-out		1	2	3	ms
SPI Interface: SCK, MISO, MOSI, CS (IS32LT3131C only)						
V_{IL}	Logic “0” input voltage				0.6	V
V_{IH}	Logic “1” input voltage		2.4			V
V_{OH}	MISO high level output voltage	I_{SOURCE}= -5mA	V_{IO}-0.3V		V_{IO}	V
V_{OL}	MISO low level output voltage	I_{SINK}= 5mA	0		0.3	V
I_{IL}	Logic “0” input current	V_{INPUT}= 0V (Note 4)		5		nA
I_{IH}	Logic “1” input current	V_{INPUT}= V_{IO} (Note 4)		5		nA
ADC (10-Bit)						
V_{REFADC}	Reference voltage			1.8		V
DNL	Differential nonlinearity	(Note 4)	-5		+5	LSB
INL	Integral nonlinearity	(Note 4)	-8		+8	LSB
RESADC	Quantization steps		1024			LSB
ADCERR	Quantification error		-0.5		+0.5	LSB
t_{CONV}	Min. conversion Time	(Note 4)		25		μs

7.3 DIGITAL INPUT SPI SWITCHING CHARACTERISTICS (NOTE 4)

Symbol	Parameter	Min.	Typ.	Max.	Units
f_{CLK}	Clock frequency	-		9	MHz
t_{SLCH}	CS active set-up time	34			ns
t_{SHCH}	CS not active set-up time	17			ns
t_{SHSL}	CS detect time	167			ns
t_{CHSH}	CS active hold time	34			ns
t_{CHSL}	CS not active hold time	17			ns
t_{CH}	Clock high time	34			ns
t_{CL}	Clock low time	34			ns
t_{CLCH}	Clock rise time			9	ns
t_{CHCL}	Clock fall time			9	ns
t_{DVCH}	Data in set-up time	7			ns
t_{CHDX}	Data in hold time	9			ns
t_{SHQZ}	Output disable time			34	ns
t_{CLQV}	Clock low to output valid			39	ns
t_{CLQX}	Output hold time	0			ns
t_{QLQH}	Output rise time			17	ns
t_{QHQL}	Output fall time			17	ns

Note 4: Guaranteed by design.

8 TYPICAL PERFORMANCE CHARACTERISTICS

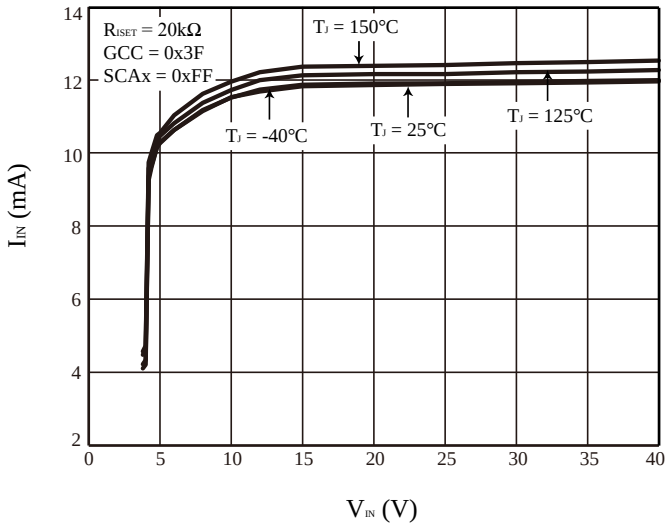


Figure 5 I_{IN} vs. V_{IN}

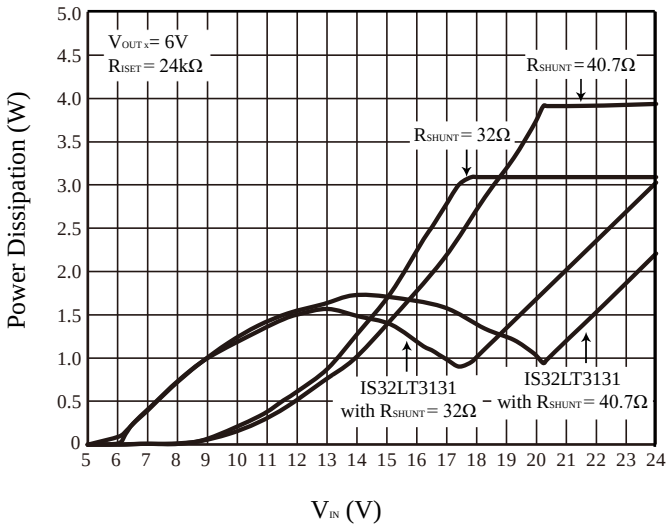


Figure 6 Power Dissipation vs. V_{IN}

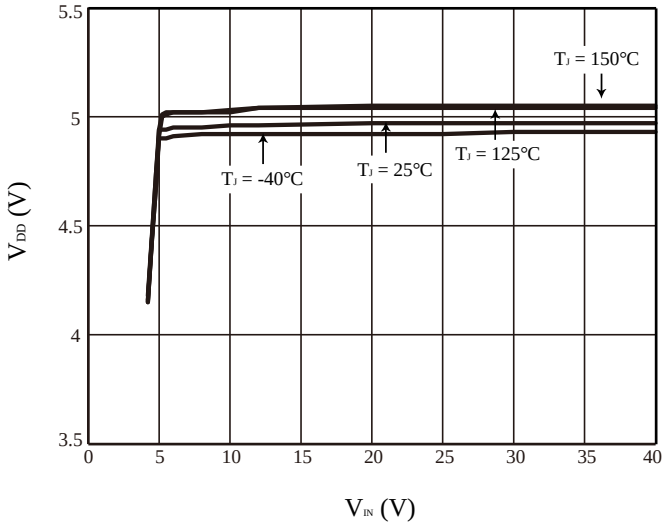


Figure 7 V_{DD} vs. V_{IN}

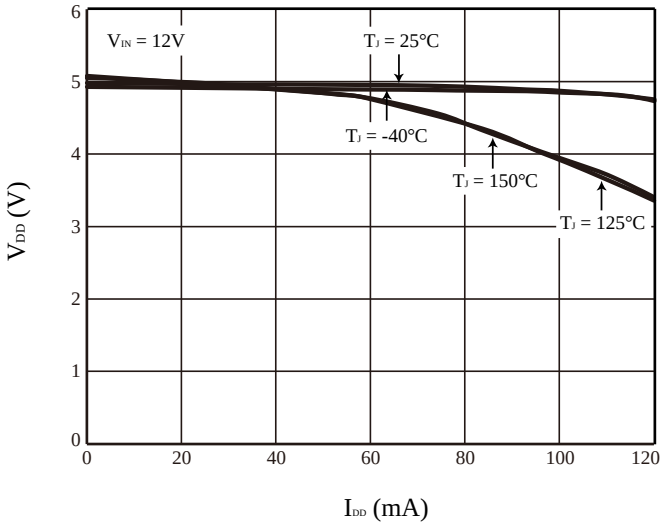


Figure 8 V_{DD} vs. I_{DD}

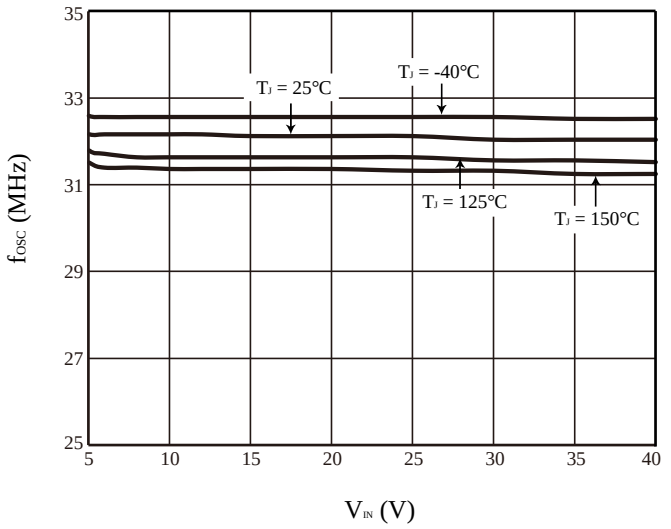


Figure 9 f_{OSC} vs. V_{IN}

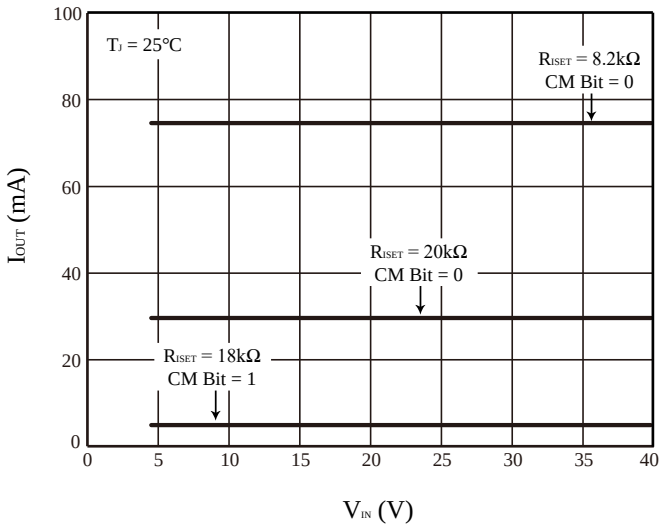


Figure 10 I_{OUT} vs. V_{IN}

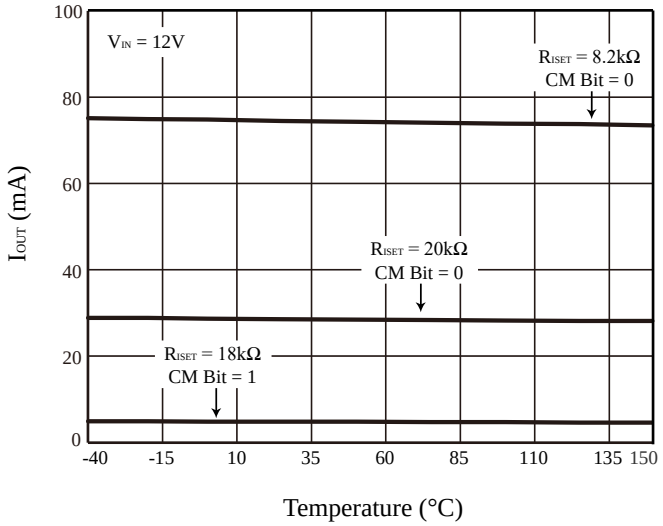


Figure 11 I_{OUT} vs. T_A

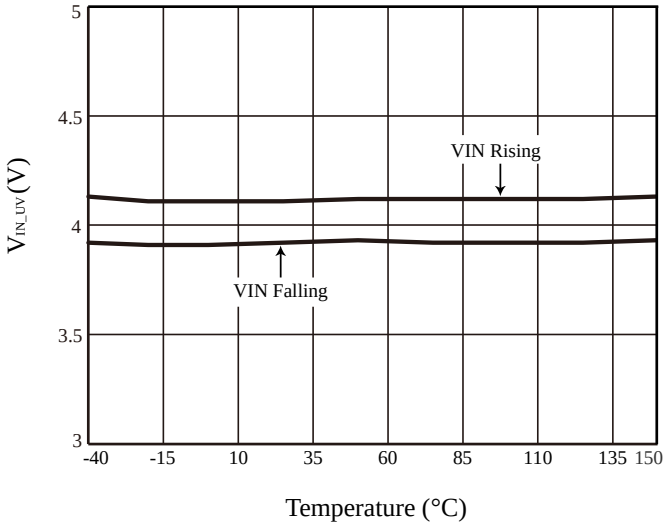


Figure 12 V_{IN_UV} vs. T_A

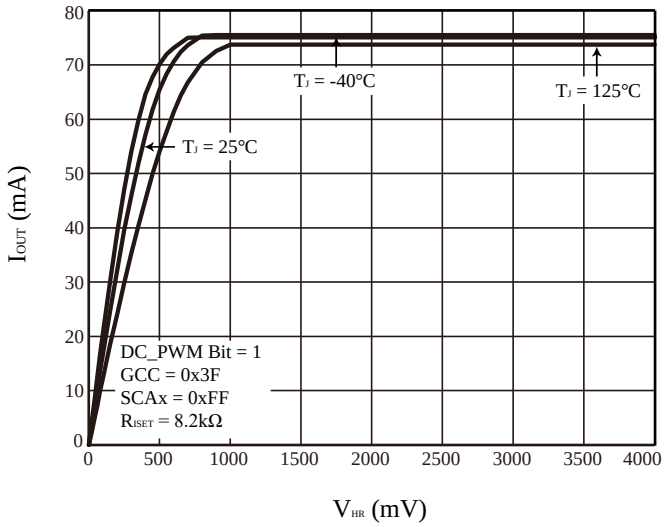


Figure 13 I_{OUT} vs. V_{HR}

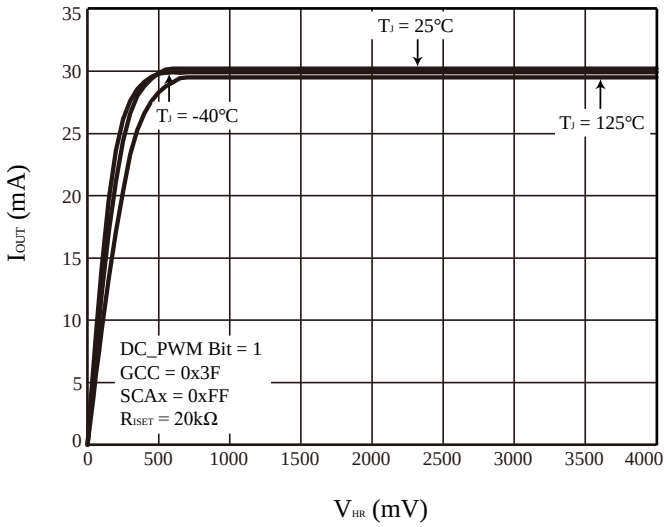


Figure 14 I_{OUT} vs. V_{HR}

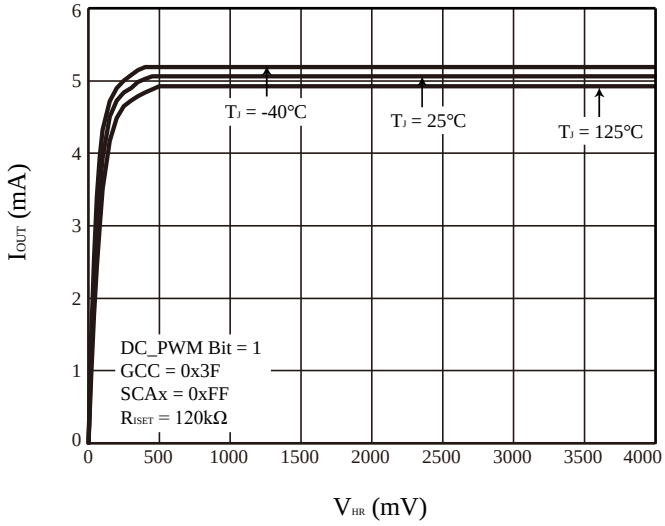


Figure 15 I_{OUT} vs. V_{HR}

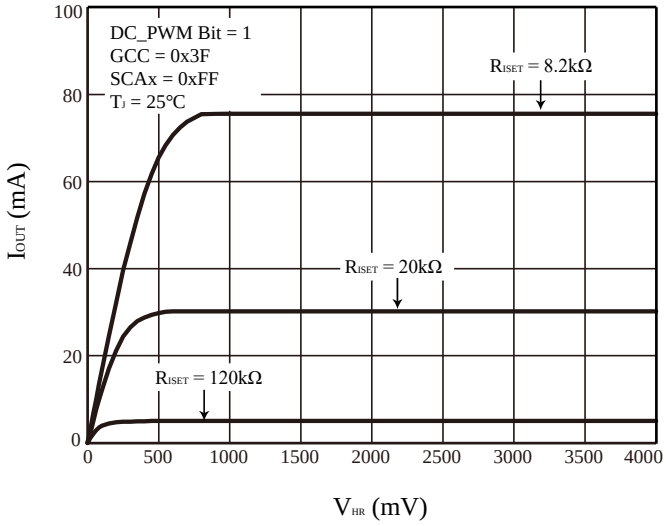


Figure 16 I_{OUT} vs. V_{HR}

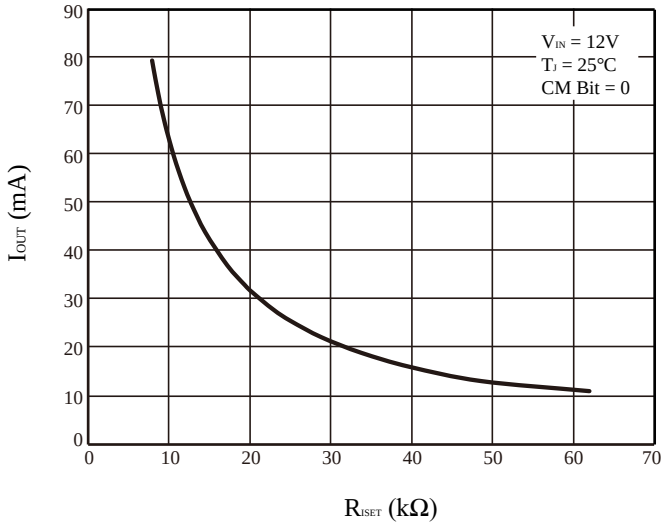


Figure 17 I_{OUT} vs. R_{ISET}

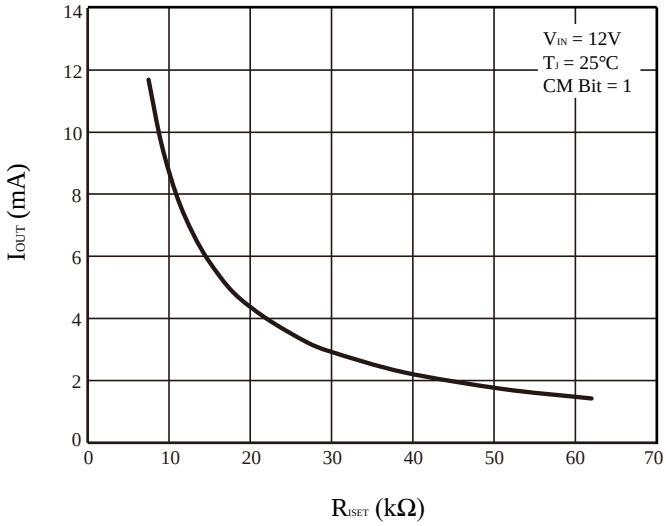


Figure 18 I_{OUT} vs. R_{ISET}

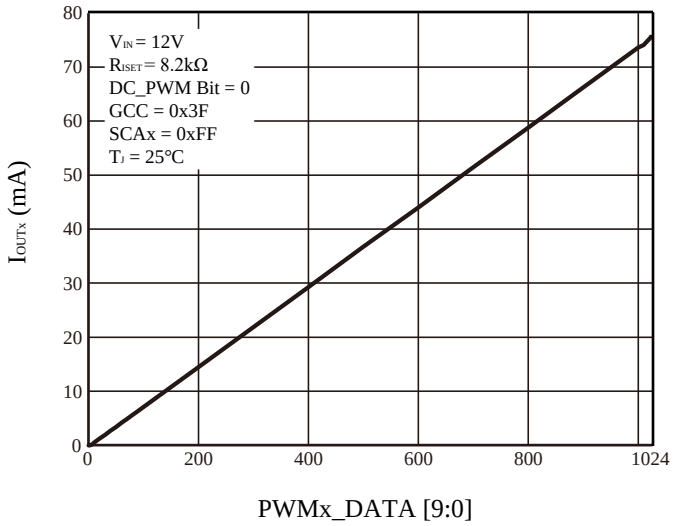


Figure 19 I_{OUT} vs. PWMx_DATA [9:0]

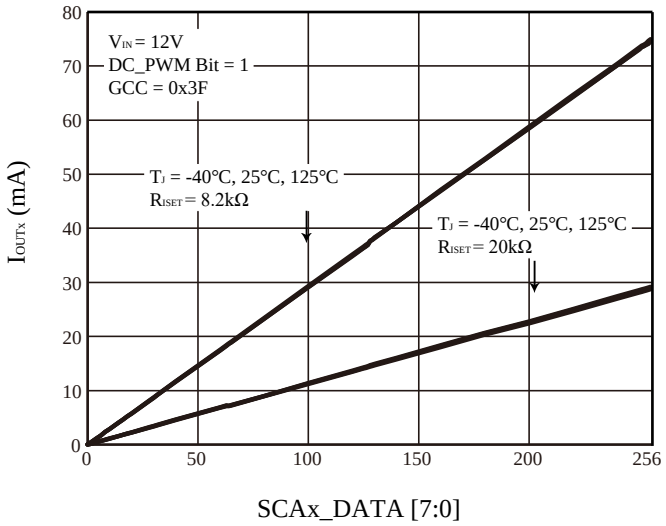


Figure 20 I_{OUT} vs. SCAx_DATA [7:0]

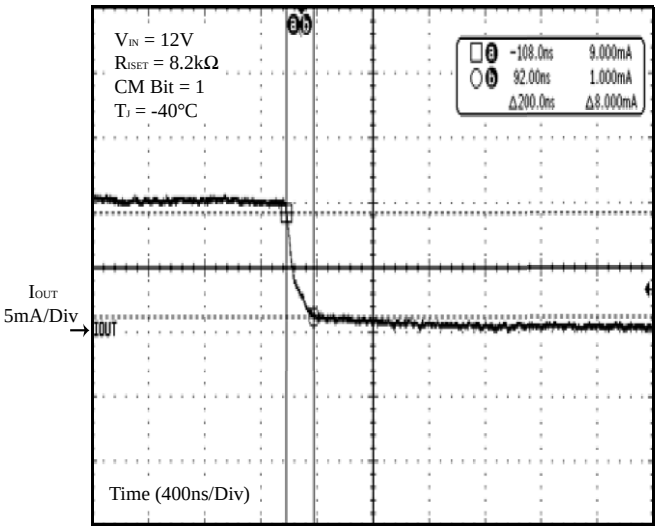


Figure 21 I_{OUT} Falling Time

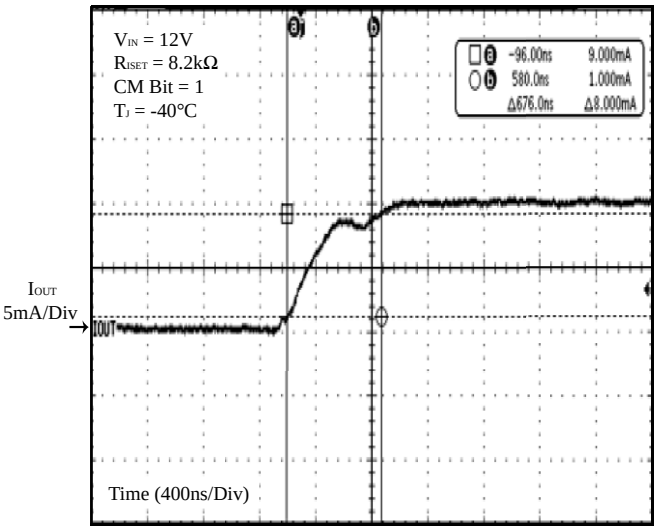


Figure 22 I_{OUT} Rising Time

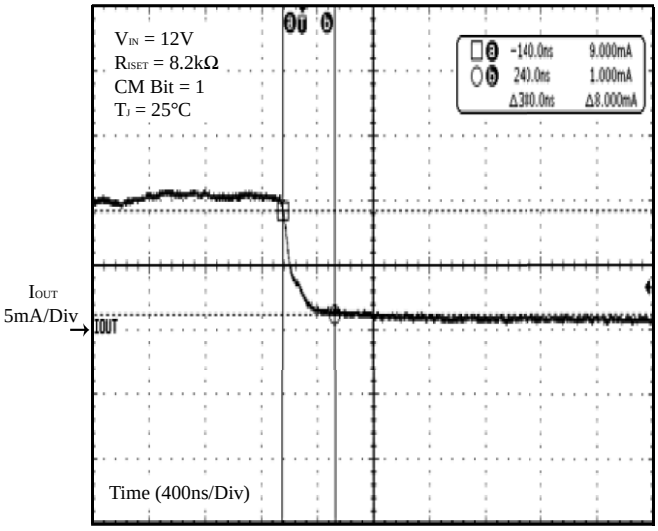


Figure 23 I_{OUT} Falling Time

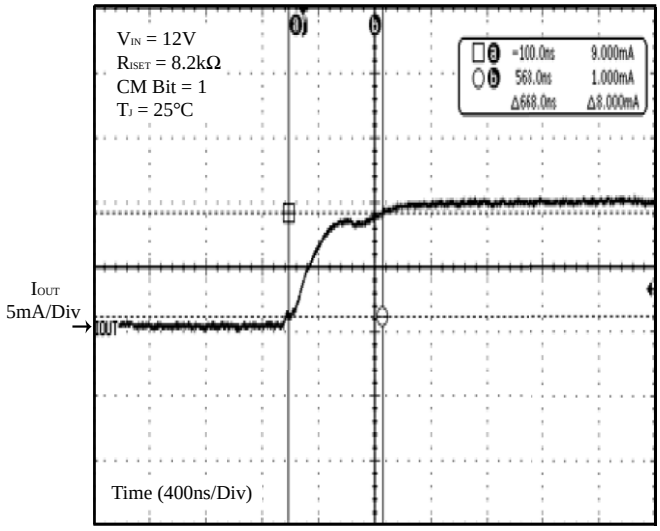


Figure 24 I_{OUT} Rising Time

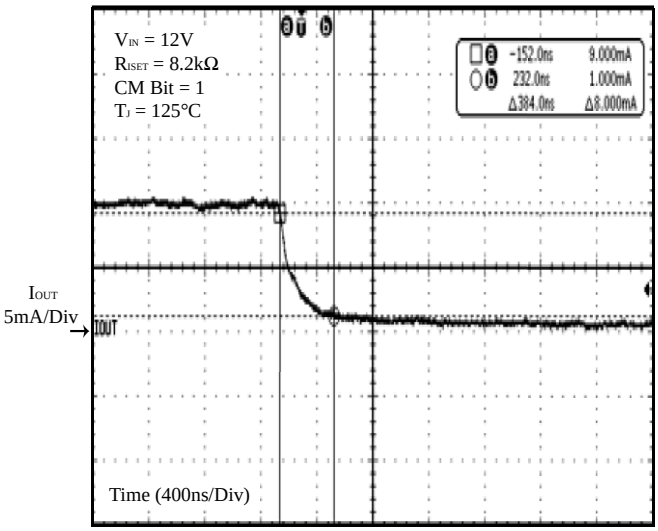


Figure 25 I_{OUT} Falling Time

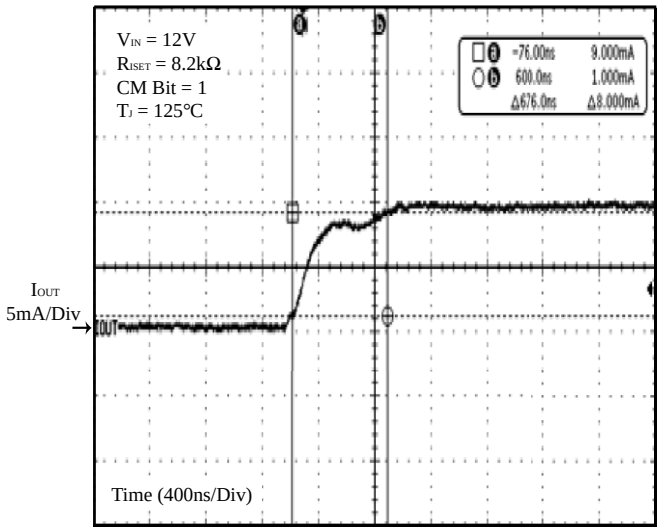


Figure 26 I_{OUT} Rising Time

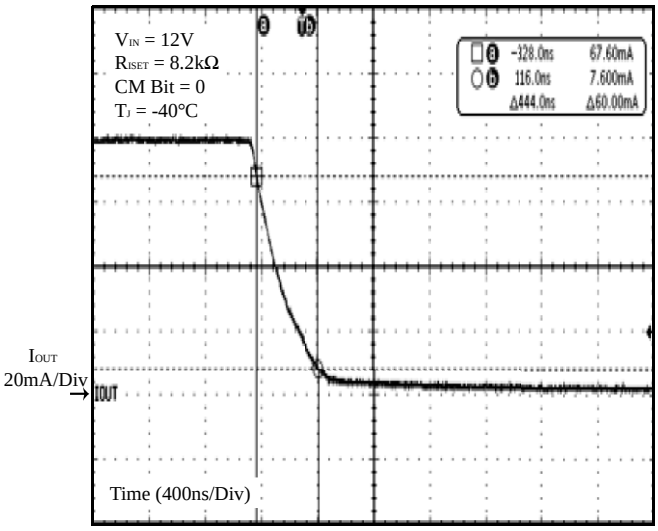


Figure 27 I_{OUT} Falling Time

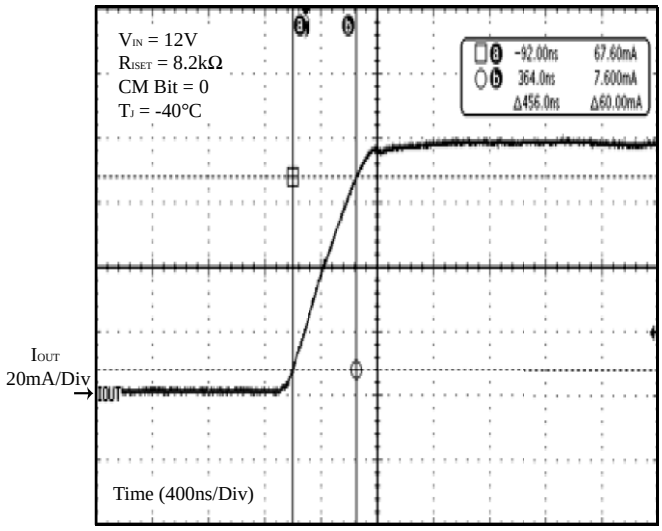


Figure 28 I_{OUT} Rising Time

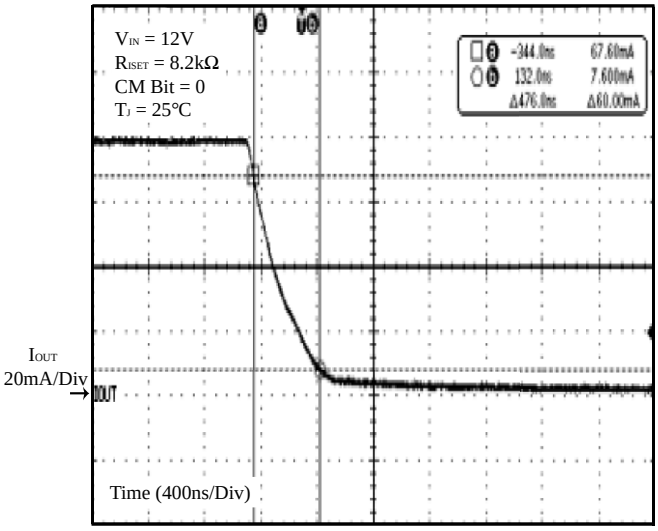


Figure 29 I_{OUT} Falling Time

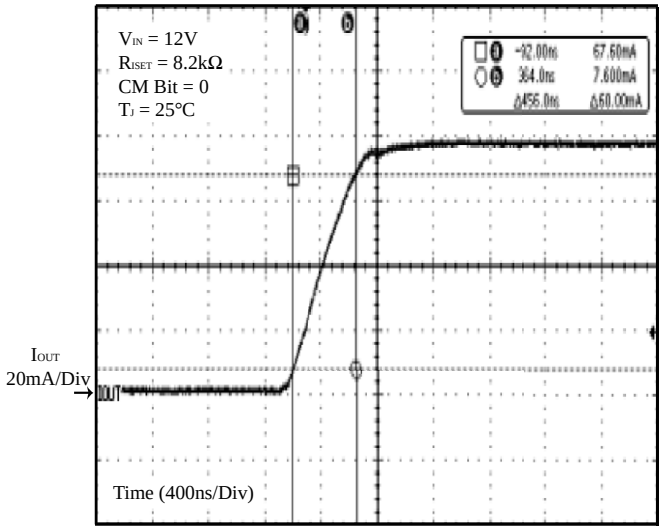


Figure 30 I_{OUT} Rising Time

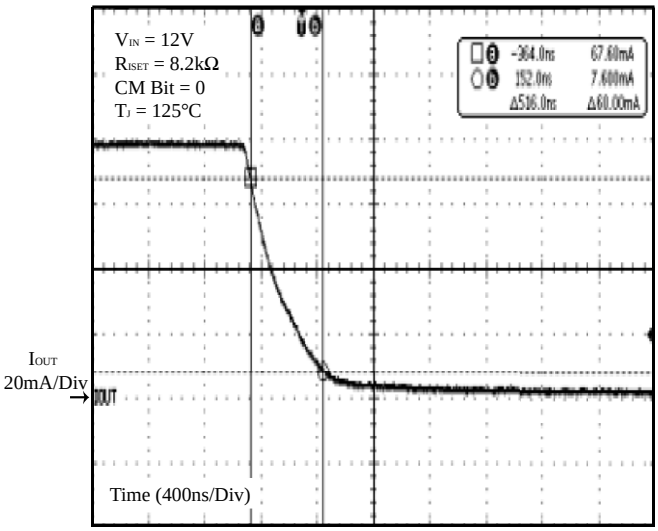


Figure 31 I_{OUT} Falling Time

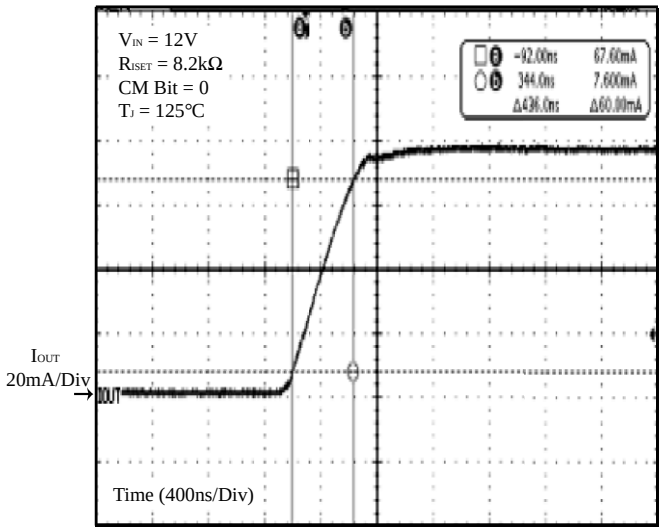


Figure 32 I_{OUT} Rising Time

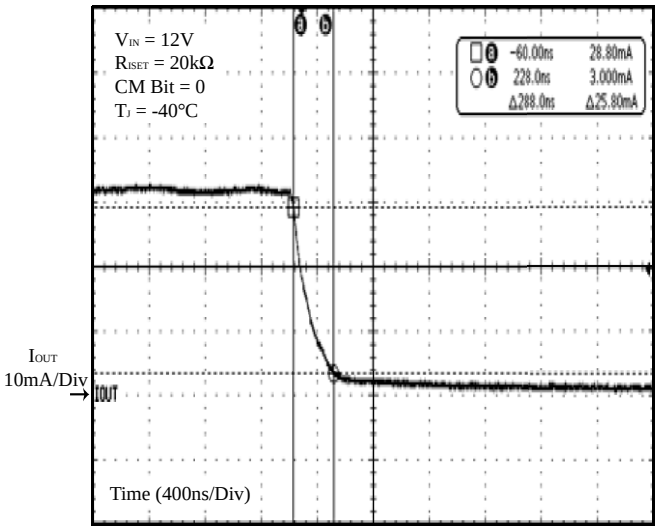


Figure 33 I_{OUT} Falling Time

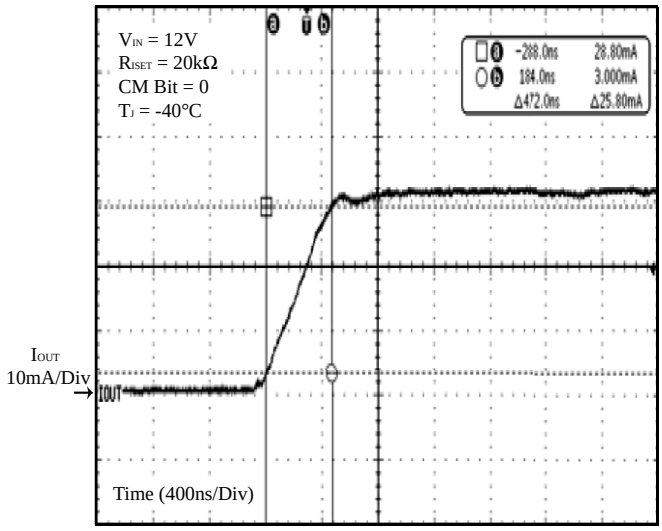


Figure 34 I_{OUT} Rising Time

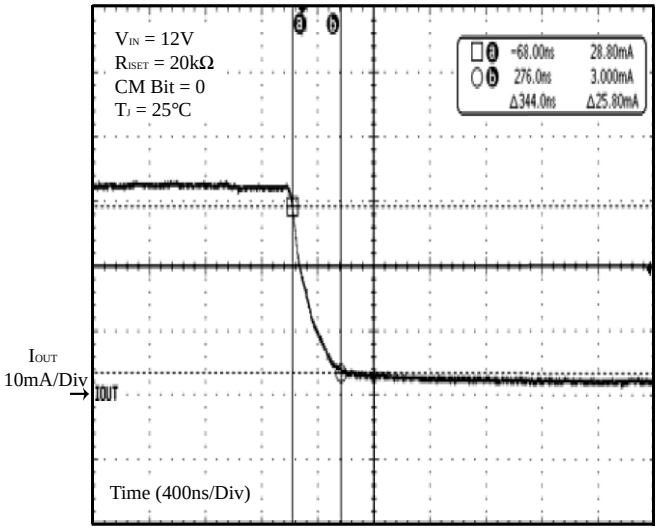


Figure 35 I_{OUT} Falling Time

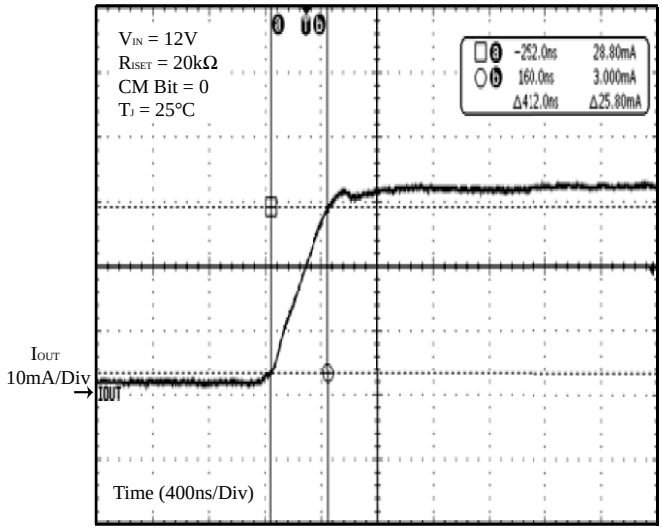


Figure 36 I_{OUT} Rising Time

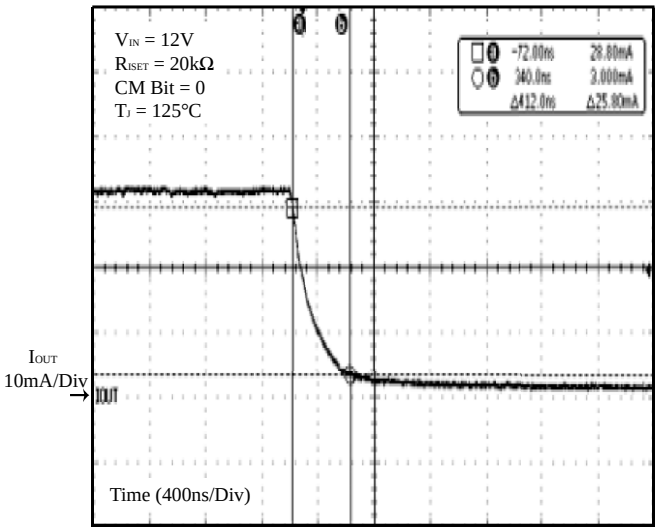


Figure 37 I_{OUT} Falling Time

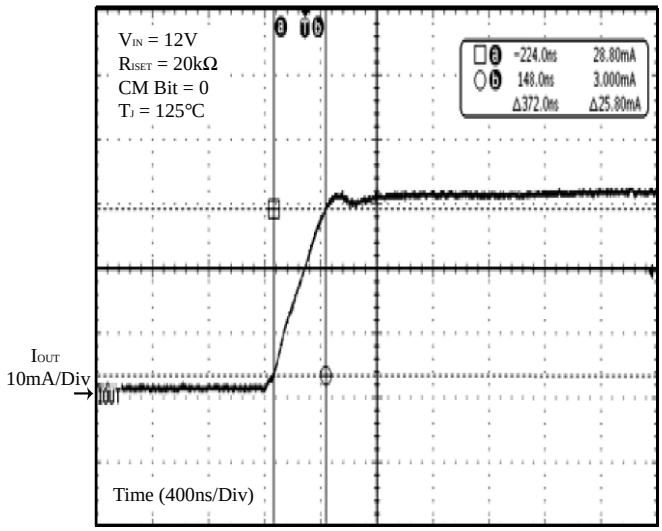
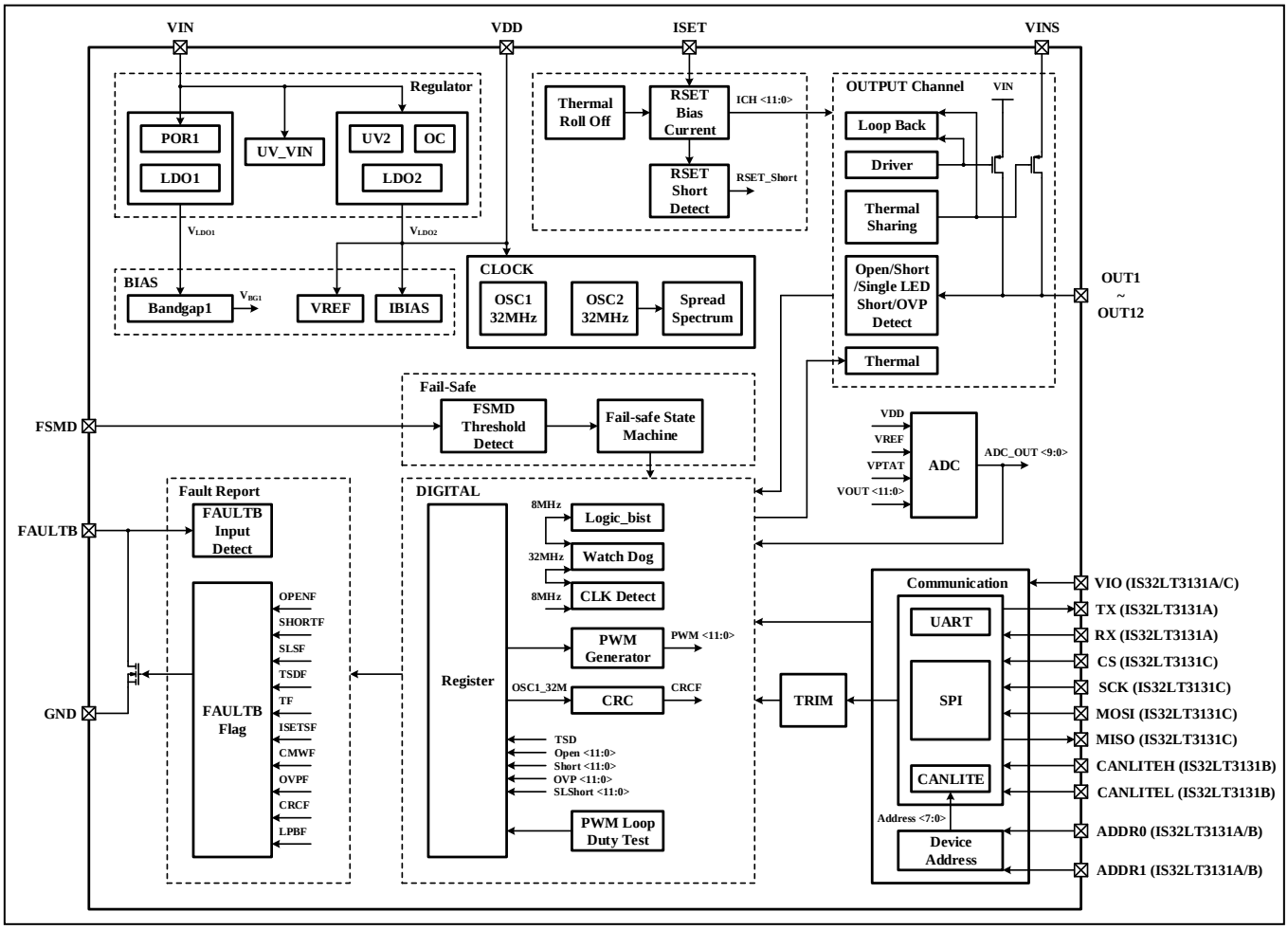


Figure 38 I_{OUT} Rising Time

9 FUNCTION BLOCK DIAGRAM



10 APPLICATION INFORMATION

10.1 OVERVIEW

The IS32LT3131 is an automotive 12-channel LED driver with multiple bus interfaces for accessing individual control of each LED string. Each current source channel is capable of up to 75mA and supports both individual channel current adjustment and PWM dimming. The output current and PWM duty cycle of each channel can be individually configured through the bus interface. Multiple output channels can be combined in parallel to create a higher LED current channel. The unique thermal shunt resistor (power shunt) mechanism utilizes an external power resistor to shunt IC power dissipation to minimize thermal stress on the device.

For added system reliability, the IS32LT3131 features various fault protections, including LED string open, LED string shorted, single LED shorted, overvoltage, overcurrent (ISET pin shorted), over temperature, CRC error and watchdog timeout (fail-safe modes) conditions for robust operation. Detection of these failures is reported by a dedicated reporting pin, FAULTB. There are also dedicated flag bits in registers for each failure which can be read back by the external host MCU through the bus interfaces. To optimize EMI performance, the IS32LT3131 features spread spectrum on the internal PWM base clock to spread the total electromagnetic emitting energy into a wider range that significantly degrades the peak energy of EMI. In addition, the output current source ON/OFF transitions during PWM dimming have a proper slew rate control and programmable phase delay to mitigate EMI and power supply inrush current.

The IS32LT3131 provides three types of interfaces, UART (IS32LT3131A), CANLITE (IS32LT3131B) and SPI (IS32LT3131C), between a host MCU and multiple slave IS32LT3131 devices. The device address can be configured by the two address pins (IS32LT3131A/B only). The interfaces receive data to control all output channels and send back fault information to the host MCU. The CANLITE interface allows long distance off-board communication between boards in same lamp module (as shown in Figure 39). While the UART and SPI interface allow on-board communication. The UART interface along with an external industrial-standard CAN transceiver also enables long distance off-board communication with a host MCU placed outside of the lamp module (as shown in Figure 40). Based on the CAN physical layer, it can achieve excellent EMS and EMI performance. The embedded CRC correction can ensure robust communication in automotive environments. These interfaces are easily supported by most MCUs available in the market.

To further increase robustness, the device will automatically switch to a fail-safe state in case of the communication loss, for example, host MCU failure or communication cables broken. The device supports different fail-safe modes which can be configured by the FSMD pin.

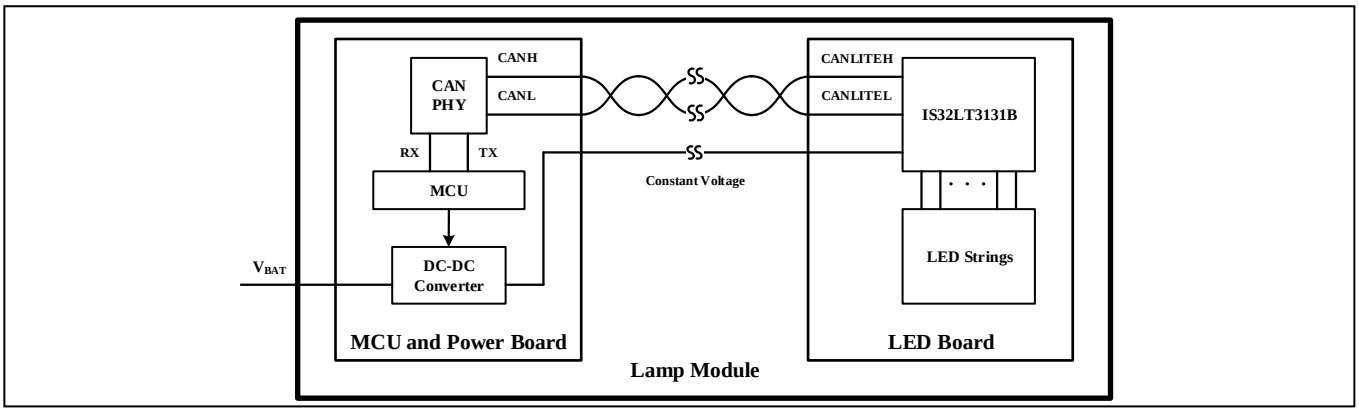


Figure 39 CANLITE Interface for Long Distance Intramodular Communication

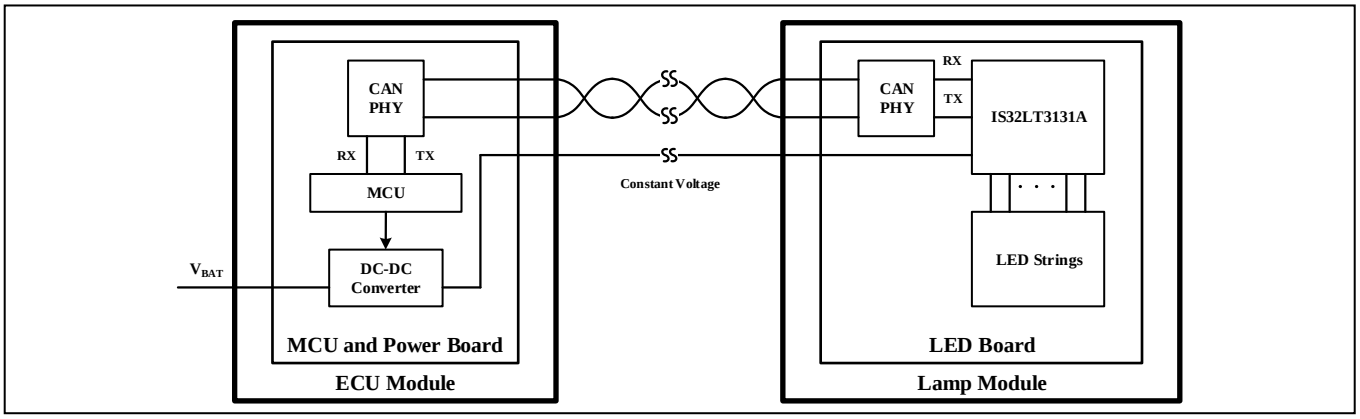


Figure 40 UART Interface with External CAN Transceiver for Long Distance Intermodular Communication

10.2 POWER SUPPLY

10.2.1 VIN UNDERVOLTAGE-LOCKOUT (UVLO)

The IS32LT3131 features an undervoltage-lockout (UVLO) function on the VIN pin to prevent unintended operation at too low input voltages. UVLO threshold is an internally fixed value and cannot be modified. Entering UVLO will reset all the registers to their default value. The device is disabled when the VIN voltage drops below V_{IN_UV} and resumes normal operation when the VIN voltage rises above (V_{IN_UV}+V_{IN_UVHY}). Due to the LBIST (Logic Built-in Self-test) and device address detection, all registers are accessible 20ms after UVLO is released.

10.2.2 INTERNAL 5V LINEAR REGULATOR (VDD)

The IS32LT3131 device integrates an internal linear regulator (LDO) with 5V (Typ.) and I_{DD_MAX} current to power the internal analog and digital circuits, including internal CANLITE transceiver (IS32LT3131B). During operation, the internal circuit will draw transient high current from this linear regulator. Therefore, a 4.7μF low ESR, X7R type ceramic capacitor is necessary from VDD pin to GND, it must be placed as close to VDD pin as possible. This linear regulator also has the UVLO feature. The device is disabled when the V_{DD} voltage drops below V_{DD_UV} and resumes normal operation when the VDD voltage rises above (V_{DD_UV}+V_{DD_UVHY}). Entering UVLO will reset all registers to their default value. An I_{DD_LIM} current limit on VDD pin protects the IS32LT3131 from VDD output overload or short-circuit conditions.

For IS32LT3131B device, do not power high current external devices using the VDD pin since the internal CANLITE transceiver will draw high continuous current during communication.

10.2.3 VIO VOLTAGE SUPPLY

The positive voltage rail of the UART interface (IS32LT3131A) and SPI interface (IS32LT3131C) are supplied with the VIO which must be connected to the same power supply as the MCU or CAN PHY. The VIO pin can be connected to the device VDD pin if a 5V MCU or CAN PHY is interfaced to the IS32LT3131A/C.

It requires a 1μF low ESR, X7R type ceramic capacitor from this pin to GND, which must be placed close to this pin.

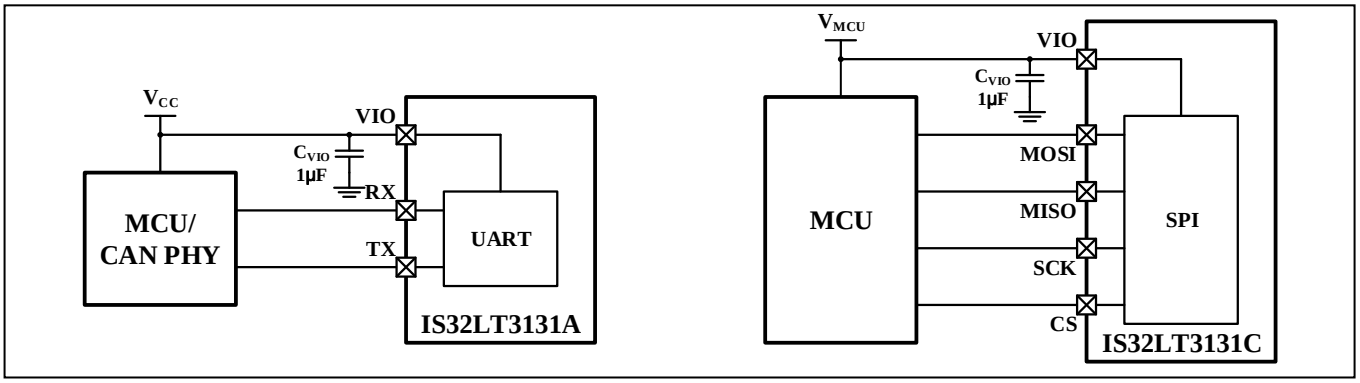


Figure 41 VIO Voltage Supply

10.2.4 THERMAL SHUNT TOPOLOGY

For any linear constant current LED driver, its power dissipation can be calculated by multiplying the voltage drop across the driver by the current flowing through it. This value is expressed in watts.

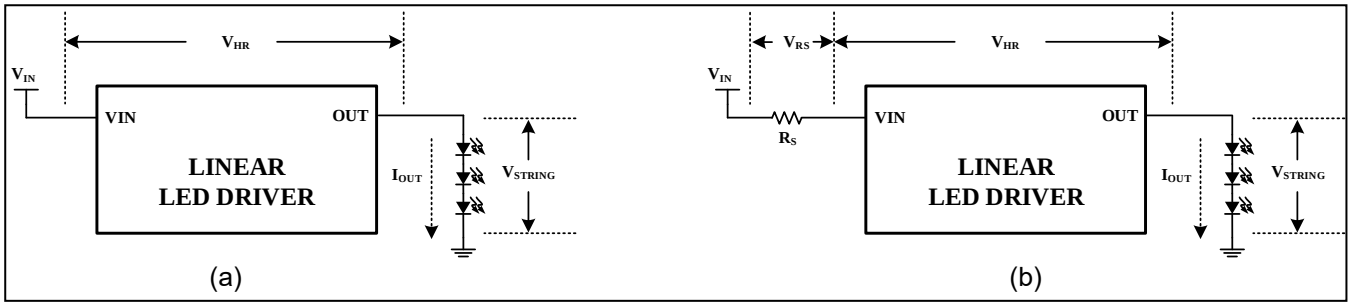


Figure 42 Linear LED Driver Power Dissipation

As shown in Figure 42(a), the thermal dissipation of the driver can be calculated by the following equation:

$$P_{DRIVER} = V_{HR} \times I_{OUT} = (V_{IN} - V_{STRING}) \times I_{OUT} \qquad (1)$$

According to the above equation, a higher input voltage will result in greater thermal dissipation. A power resistor, R_S, can be added to shunt some thermal away from the driver. As shown in Figure 42(b). The resultant driver thermal dissipation becomes:

$$P_{DRIVER} = V_{HR} \times I_{OUT} = (V_{IN} - R_S \times I_{OUT} - V_{STRING}) \times I_{OUT} \qquad (2)$$

Note: The device's internal circuit current consumption, I_{IN} is negligible compared to I_{OUT}. Hence, I_{VIN} is equal to I_{OUT}.

A large R_S value is able to significantly derate the power dissipation on the driver at high input voltage levels. However, for automotive applications, the nominal battery voltage can vary from 9V to 16V. A large R_S value will result in insufficient operating V_{HR} headroom voltage at low input voltages resulting in a drop of the I_{OUT} output current. To address this, the IS32LT3131 has two current input paths through the VIN and VINS pins. VIN is connected directly to the power supply and VINS is connected to the power supply via a thermal shunt resistor, R_{SHUNT}, in series as shown in Figure 43.

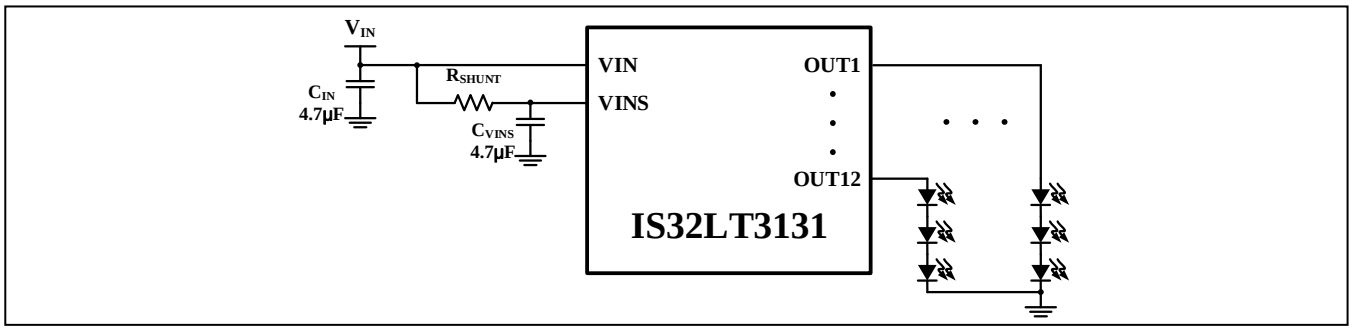


Figure 43 Thermal Shunt Mechanism

This thermal shunt mechanism is enabled by setting the TST_EN bit in the CONFIG register (00h) to "1". It ensures the input current flows through the VINS path as much as possible (the maximum is 23/24 of total output current). However, when the input voltage, V_{IN}, is at a low level, the thermal shunt resistor R_{SHUNT} limits the input current through the VINS path so the major input current (the maximum is 23/24 of total output current) flows through the VIN path directly to ensure sufficient V_{HR} headroom voltage for the driver to maintain a constant output current. When the input voltage V_{IN} increases, the device gradually transfers more input current from the VIN path to the VINS path. The higher the V_{IN} voltage level, the more current flows through the VINS path. So the R_{SHUNT} can significantly shunt thermal dissipation away from the driver at high input voltage level to ensure the junction temperature of the driver remains at a reasonable level.

Note that when the thermal shunt mechanism is implemented, the maximum regulated current through either VIN path or VINS path is 23/24 of total output current. To optimize the dynamic response of the thermal shunt regulation, connect a X7R ceramic capacitor C_{VINS} (not less than 4.7μF) from the VINS pin to GND.

As shown in Figure 44, the IS32LT3131 has different operating areas when using the thermal shunt mechanism. Within the Low Headroom Area, the input voltage is too low. Even though most input current flows through the VIN path, the headroom voltage is insufficient to reach the setting value. So, the power dissipation of the driver is small.

When the input voltage rises above (V_{OUT_MAX}+1.5V), the transition voltage V_{TR} splits the operation into two areas: Thermal Shunt Area and Thermal Increasing Area.

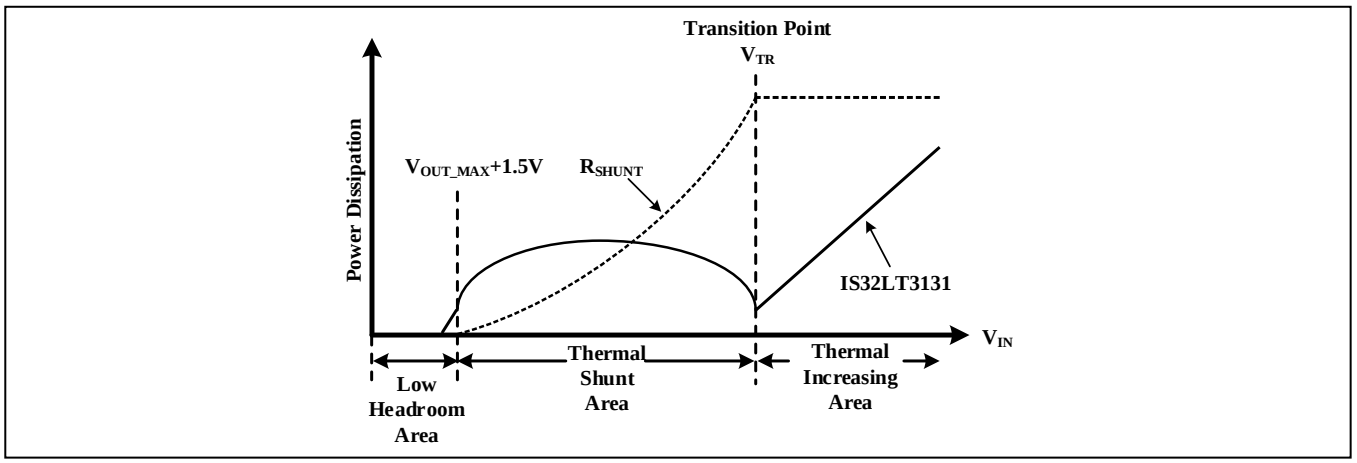


Figure 44 Power Dissipation Distribution With Thermal Shunt Resistor

10.2.4.1 Thermal Shunt Area

All output currents are in constant regulation mode only when the input voltage is greater than V_{OUT_MAX}+1.5V. As the input voltage increases, the input current starts to be gradually transferred from the VIN path to the VINS path. Therefore, the power dissipation on R_{SHUNT} increases and the power dissipation of the driver is maintained at a reasonably low level. The VINS path current can be calculated by:

$$I_{VINS} = \frac{V_{IN} - V_{OUT\_MAX} - 1.5V}{R_{SHUNT}} \qquad (3)$$

Where, V_{OUT_MAX} is the maximum voltage of all OUTx pins and 1.5V is the typical dropout voltage from VINS to the OUTx pin.

So the VIN path current is:

$$I_{VIN} = (\sum_{x=1}^{12} I_{OUTx} - I_{VINS}) + I_{IN} \qquad (4)$$

Where, I_{IN} is the power supply quiescent current and x is the 1 to 12 output channels.

The power dissipation on the R_{SHUNT} resistor is:

$$P_{SHUNT} = \frac{(V_{IN} - V_{OUT\_MAX} - 1.5V)^2}{R_{SHUNT}} \qquad (5)$$

The power dissipation on IS32LT3131 is:

$$P_{3131\_TSA} = V_{IN} \times (\sum_{x=1}^{12} I_{OUTx} + I_{IN}) - \frac{(V_{IN} - V_{OUT\_MAX} - 1.5V)^2}{R_{SHUNT}} - \sum_{x=1}^{12}(I_{OUTx} \times V_{OUTx}) \qquad (6)$$

10.2.4.2 Thermal Increasing Area

When the input voltage is equal or greater than the Transition Voltage V_{TR}, most of the input current (23/24 of total output current) will flow through R_{SHUNT} into VINS pin. The power dissipation on the R_{SHUNT} resistor is constant while the power dissipation on the driver increases linearly. V_{TR} voltage point can be adjusted by the resistance value of R_{SHUNT}:

$$V_{TR} = R_{SHUNT} \times \frac{23}{24} \times \sum_{x=1}^{12} I_{OUTx} + V_{OUT\_MAX} + 1.5V \qquad (7)$$

The maximum regulated current flow through the VINS path is 23/24 of the total output current, and the remaining 1/24 of total output current continues flowing through the VIN path.

To optimize the power dissipation on the driver, the R_{SHUNT} value should be chosen to make sure the V_{TR} is equal to the maximum input voltage V_{IN_MAX}:

$$R_{SHUNT} = \frac{V_{IN\_MAX} - V_{OUT\_MAX} - 1.5V}{\frac{23}{24} \times \sum_{x=1}^{12} I_{OUTx}} \qquad (8)$$

The power dissipation on the R_{SHUNT} resistor is constant at maximum value:

$$P_{SHUNT\_MAX} = (\frac{23}{24} \times \sum_{x=1}^{12} I_{OUTx})^2 \times R_{SHUNT} \qquad (9)$$

The power rating of R_{SHUNT} should be carefully considered. A single high wattage resistor or several small wattage resistors in parallel can be used to sustain the power dissipation.

The power dissipation on IS32LT3131 is:

$$P_{3131\_TIA} = V_{IN} \times (\sum_{x=1}^{12} I_{OUTx} + I_{IN}) - (\frac{23}{24} \times \sum_{x=1}^{12} I_{OUTx})^2 \times R_{SHUNT} - \sum_{x=1}^{12}(I_{OUTx} \times V_{OUTx}) \qquad (10)$$

The larger the R_{SHUNT} value with low V_{IN} results in a lower dropout voltage from the VINS to OUTx pins. Since the LED string open protection is achieved by detecting this dropout (refer to the "LED STRING OPEN DETECTION" section), a large R_{SHUNT} value could falsely trigger the LED string open protection when the input voltage V_{IN} is at a low level. To prevent falsely triggering, a proper fault undervoltage-lockout voltage threshold V_{FLT_UV} should be programmed by the FLT_UV register (02h). The recommended can be calculated as:

$$V_{FLT\_UV} \geq R_{SHUNT} \times \frac{1}{24} \times \sum_{x=1}^{12} I_{OUTx} + V_{OUT\_MAX} + 1.5V \qquad (11)$$

When PWM dimming is implemented, the PWM off-time must not be less than 400ns to ensure the normal operation of the thermal shunt mechanism.

Applications with a large power supply voltage variation, should utilize the thermal shunt mechanism to minimize thermal stress on the IS32LT3131 device. There is no need for the thermal shunt in applications with a steady power supply voltage. When the thermal shunt mechanism is not implemented, set the TST_EN bit in the CONFIG register (00h) to "0" and connect both of VIN and VINS pins directly to the power supply and the C_{VINS} capacitor can be omitted.

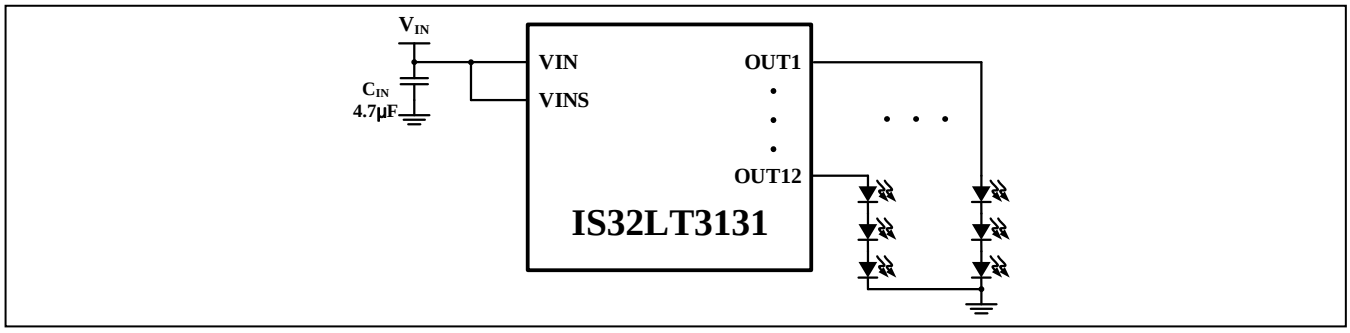


Figure 45 Thermal Shunt Mechanism Unused

10.3 OUTPUT CURRENT SETTING

The full DC output current (I_{OUT_FU}) for each channel is simultaneously set by the resistor (R_{ISET}) from the ISET pin to GND. The value for this current set resistor is computed using the following equation:

If the CM bit in the CONFIG register (00h) is set to "0":

$$I_{OUT\_FU} = \frac{V_{ISET}}{R_{ISET}} \times 614.4 \qquad (12)$$

(8.2kΩ ≤ R_{ISET} ≤ 62kΩ)

If the CM bit in the CONFIG register (00h) is set to "1":

$$I_{OUT\_FU} = \frac{V_{ISET}}{R_{ISET}} \times 87.77 \qquad (13)$$

(8.2kΩ ≤ R_{ISET} ≤ 62kΩ)

Where, V_{ISET} = 1V (Typ.). R_{ISET} is in Ω and I_{OUT_FU} is in Amp. When the target current is lower than 10mA, setting CM bit to "1" can get better current accuracy.

It is recommended that R_{ISET} be a 1% accuracy resistor with good temperature characteristic to ensure stable output current. R_{ISET} must be placed as close to the ISET pin as possible on PCB layout to avoid noise interference and ground bounce. The device is protected from an output overcurrent condition caused by R_{ISET} resistor. The output current is reduced to 17mA (Typ.) if the ISET pin is shorted to ground or if the R_{ISET} resistor value is too low.

When R_{ISET} is fixed, the DC output current for each channel can be 32-step programmed by the GCC[5:0] bits in the GC_CTRL register (01h). Furthermore, based on the GCC[5:0] setting, each channel also supports individual 256-step programmable DC output current adjustment. This feature can be used to set binning values for output LEDs or to calibrate the LEDs to achieve high brightness homogeneity based on external visual system to further save binning cost. The 8-bit Scaling Registers SCAx (10h~1Bh) individually set the DC output current of each channel.

GCC[5:0] and SCAx control the OUTx current (I_{OUTx}) as shown in the following equation:

$$I_{OUTx} = I_{OUT\_FU} \times \frac{GCC}{32} \times \frac{SCAx}{256} \qquad (14)$$

Where, x is from 1 to 12 for different output channel.

If GCC[5:0] ≤ 31 (“01 1111”),

$$GCC = \sum_{n=0}^{5} D[n] \cdot 2^n \qquad (15)$$

If GCC[5:0] ≥ 32 (“10 0000”), GCC=32.

For example: assume GCC[5:0] = 0x05 and SCA1 = 0x80. GCC[5:0] ≤ 31 so GCC = 5. Then the DC output current of OUT1 is:

$$I_{OUT1} = I_{OUT\_FU} \times \frac{5}{32} \times \frac{128}{256} \qquad (16)$$

If GCC[5:0] = 0x2F and SCA1= 0x80, GCC[5:0] ≥ 32 so GCC=32. Then the DC output current of OUT1 is:

$$I_{OUT1} = I_{OUT\_FU} \times \frac{32}{32} \times \frac{128}{256} \qquad (17)$$

If any channel(s) are unused, please connect the corresponding OUTx pin(s) to the VINS pin directly to avoid false fault detection and set the corresponding PWM and scaling registers to “0x00” to turn off output(s).

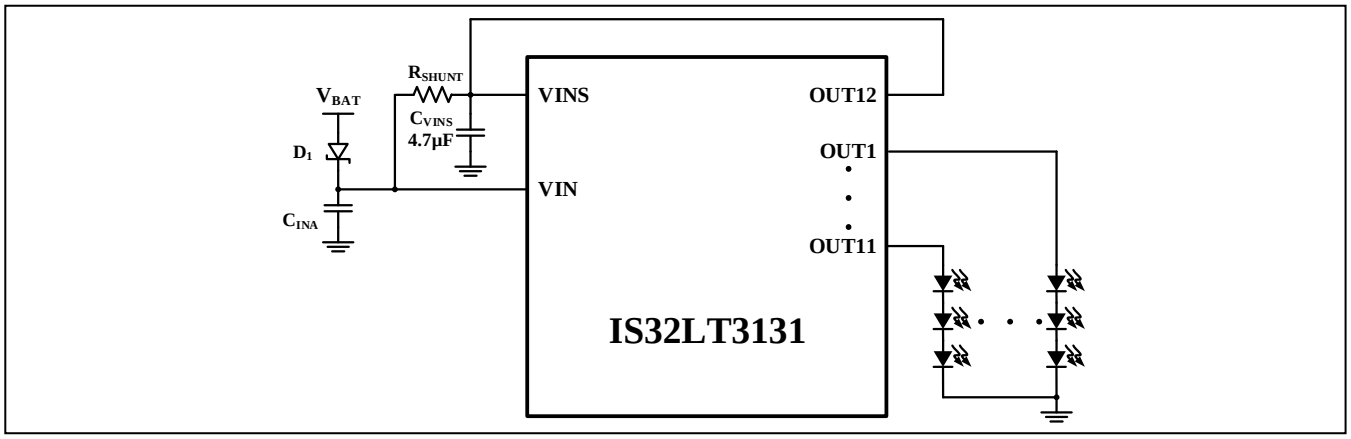


Figure 46 Example of OUT12 Unused

10.4 PWM DIMMING

The IS32LT3131 integrates independent 10-bit PWM generators for each output channel. The output current for each channel is turned on and off by the PWM generator. The average current of each output channel can be adjusted by the PWM duty cycle to control the brightness of LEDs. The PWM Registers (20h~2Eh) individually set the PWM duty cycle of each channel.

The frequency of the PWM dimming is programmable by the PWMTICK register (46h) and PRESCALE register (47h). The maximum PWM frequency can be up to 31.25kHz (Typ.). Due to slew rate control of the output current rising and falling, a high frequency PWM signal has a shorter period time that will degrade the PWM dimming linearity. Therefore, a low frequency PWM signal is good for achieving better dimming contrast ratio. At a 100Hz~500Hz PWM frequency, the dimming duty cycle can be varied from 100% down to 1% or lower. Select the frequency of PWM dimming based on the minimum brightness requirement in application.

The PWM dimming is enabled/disabled by the DC_PWM bit in DC_PWM_SEL register (05h). When the DC_PWM bit is set to “1”, the PWM generators are disabled, and all outputs are DC current which is given by equation (14). When the DC_PWM bit is set to “0”, the PWM generators are enabled to dim the LEDs by its duty cycle:

$$I_{OUTx\_PWM} = I_{OUTx} \times D_{PWMx} \qquad (18)$$

Where, D_{PWMx} is duty cycle of each channel independently programmed by PWM Registers (20h~2Eh):

$$D_{PWMx} = \frac{\sum_{n=0}^{9} D[n] \cdot 2^n}{1024} \qquad (19)$$

10.4.1 PWM PHASE DELAY AND CLOCK PHASE SHIFT

To mitigate the input transient current and power supply ripple, the IS32LT3131 features PWM phase delay and clock phase shift schemes. When both of PWM phase delay and clock phase shift are disabled (Phase Control register (04h) is set to "0x00"), all channels are simultaneously turned on at the beginning of each PWM cycle that draws large current from power supply and leads to high voltage ripple on power supply rail. As shown in below Figure 47.

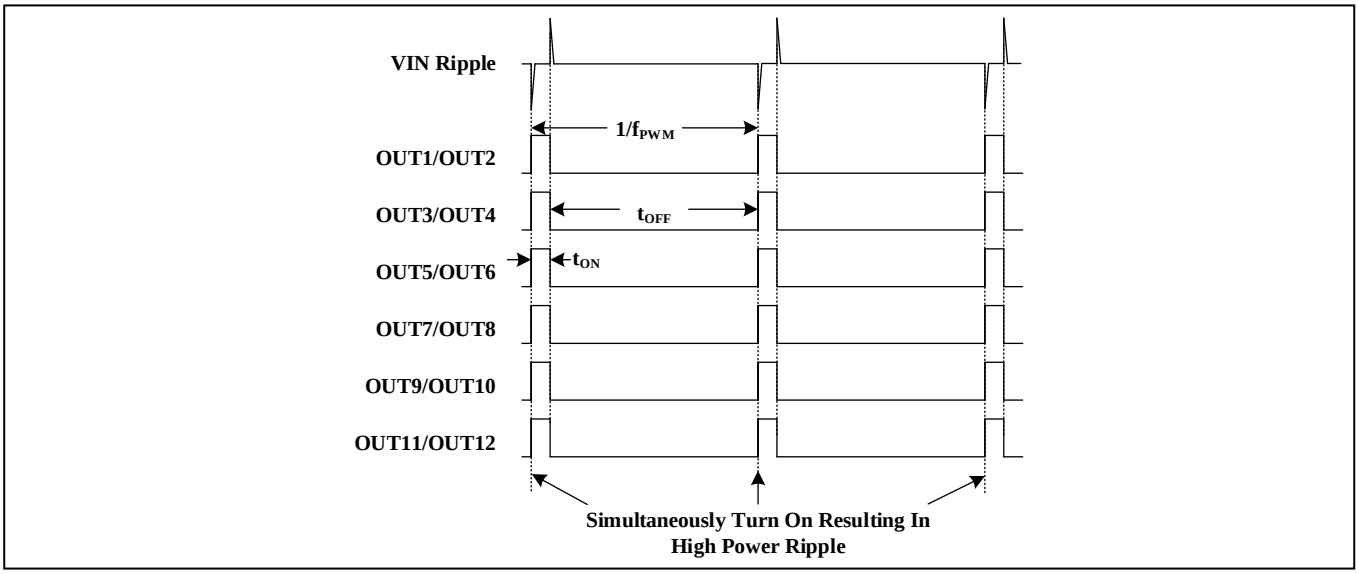


Figure 47 PWM Phase Delay Disabled and Clock Phase Shift Disabled

The IS32LT3131 divides the 12 output channels into 6 groups to perform PWM phase delay and clock phase shift, OUT1/OUT2 as group 1, OUT3/OUT4 as group 2, …OUT11/OUT12 as group 6. When only the PDE bit in PHASE_CTRL register (04h) is set to "1", the phase delay is enabled, and each group is successively turned on with an interval delay time t_{DELAY} of 1/6 PWM period ($1/f_{PWM}$) from the beginning of each PWM cycle. For each group, two channels are simultaneously turned on. That mitigates the voltage ripple on the VIN power supply rail. As shown in below Figure 48.

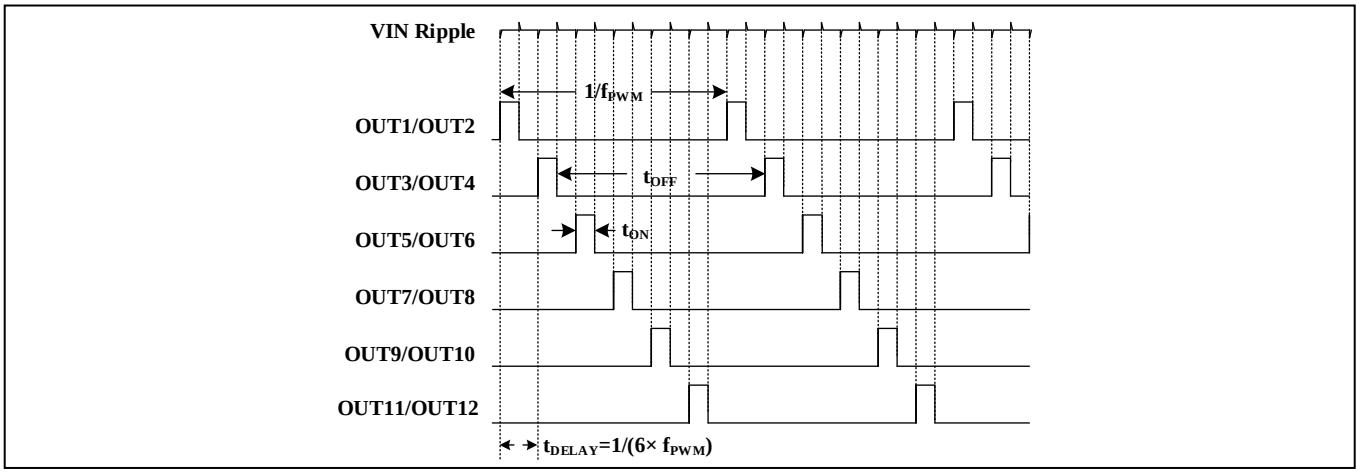


Figure 48 PWM Phase Delay Enabled and Clock Phase Shift Disabled

The PS1~PS6 bits in PHASE_CTRL register (04h) respectively enable/disable the PWM clock phase shift of group 1 ~ group 6. When the PWM clock phase shift is disabled (PSx bit is set to "0"), two channels in the corresponding group are simultaneously turned on at the beginning of the PWM cycle. As shown in below Figure 49.

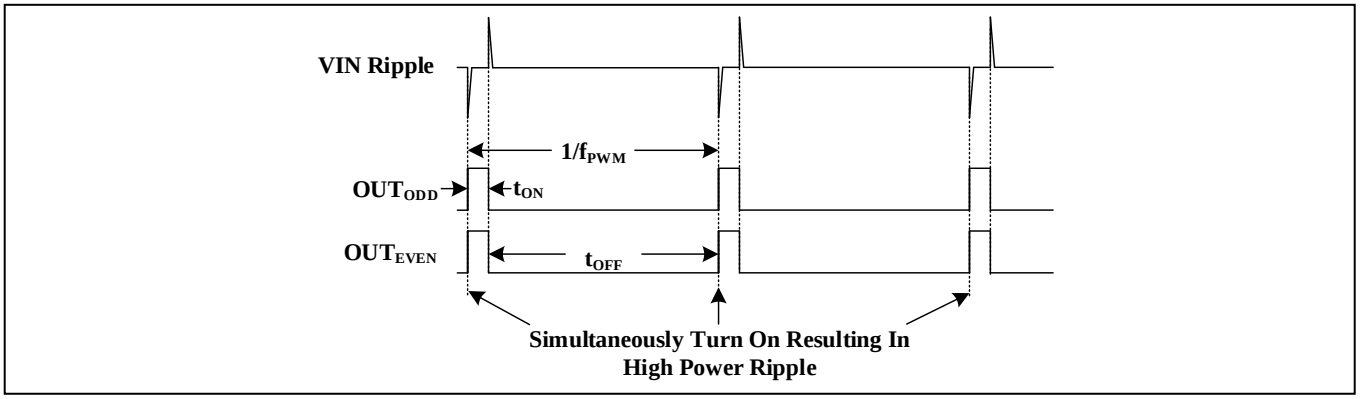


Figure 49 Clock Phase Shift Disabled

When the PSx bit in PHASE_CTRL register (04h) is set to "1", the PWM clock phase shift of the corresponding group is enabled. The PWM duty cycle of odd number channel in the corresponding group counts from beginning of PWM cycle while PWM duty cycle of even number channel in the corresponding group counts in reverse from ending of PWM cycle. The PWM rising edge and falling edge cancel the voltage ripple on the VIN power rail. As shown in below Figure 50.

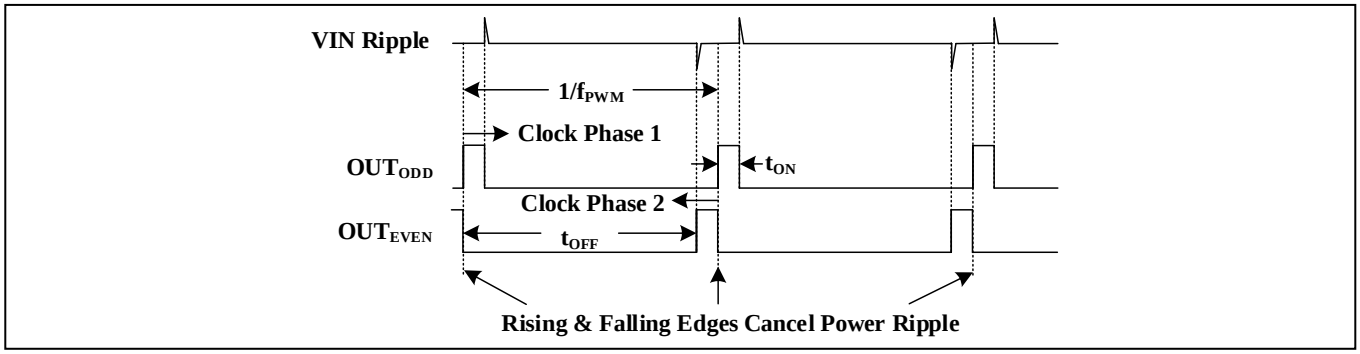


Figure 50 Clock Phase Shift Enabled

When the PHASE_CTRL register (04h) is set to "0bx1111111", both of PWM phase delay and clock phase shift are enabled and the voltage ripple on the VIN power rail is further minimized that also optimizes the EMI performance. The PWM operation sequence of all groups is shown in below Figure 51.

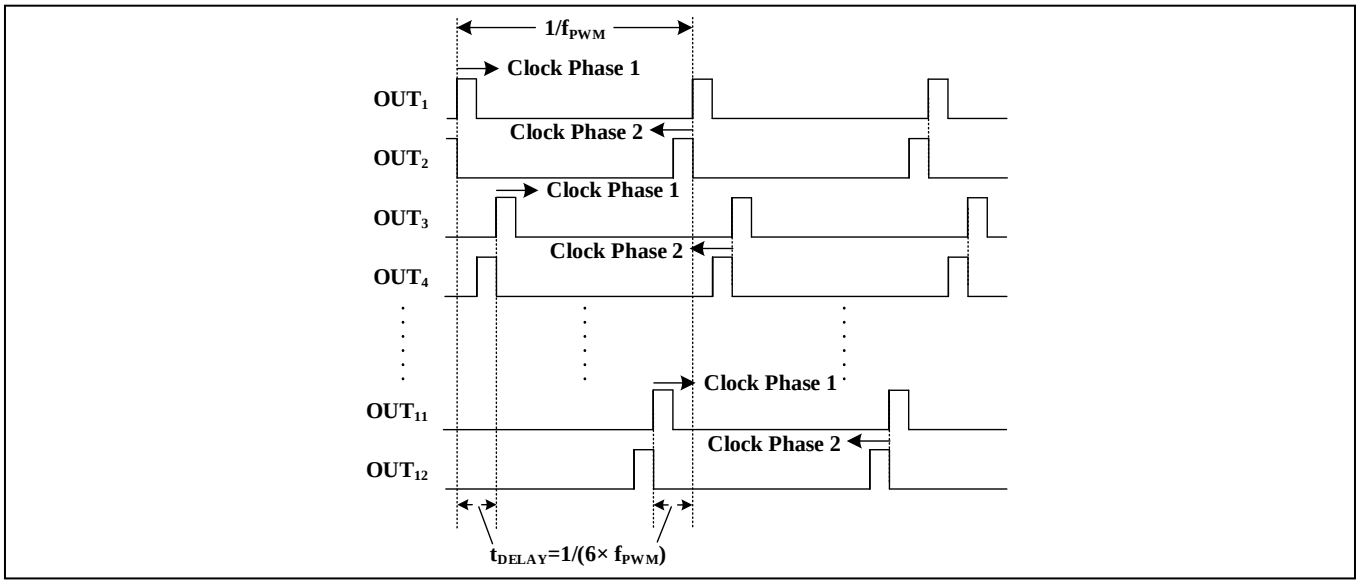


Figure 51 PWM Phase Delay Enabled and Clock Phase Shift Enabled

10.4.2 PWM SPREAD SPECTRUM

To optimize the EMI performance, the IS32LT3131 includes a spread spectrum feature on the PWM base clock. Spread spectrum can spread the total electromagnetic emitting energy into a wider range that significantly degrades

the peak energy of EMI. With spread spectrum, the EMI test can be passed with a smaller size and lower cost filter circuit. Spread spectrum is enabled/disabled by the SSCEN bit and the frequency is selected by the SSF[1:0] bits in the SSCCFG register (43h). When the spread spectrum function is enabled, the PWM frequency must be set to at least two times of the spread spectrum frequency to avoid flickering issue.

10.5 FAULT PROTECTION

10.5.1 FAULT REPORTING

For added system reliability, the IS32LT3131 integrates various fault detections for LED string open/short, single LED short, overvoltage, overcurrent (ISET shorted), over temperature, CRC error and watchdog timeout (fail-safe modes) conditions. The open drain pin FAULTB can be used as a fault status reporting. If any fault occurs, the corresponding bit in FLT_TYPE_L or FLT_TYPE_H registers (5Ah or 5Bh) will be set to “1” and the FAULTB pin will go low after a delay time (programmed by FT[3:0] bits in FLT_CONFIG register) to report fault condition. When it’s monitored by a host MCU, a pull-up resistor R_{FPU} (10kΩ recommended) from the FAULTB pin to the supply of the host MCU is required.

IS32LT3131 supports both “One Fail All Fail” and “One Fail Others On” fault action modes which can be selected by OFA[1:0] bits in FLT_CONFIG register (51h). In the “One Fail All Fail” mode, if any channel encounters a fault then all other normal channels will be turned off. The FAULTB pin supports both input and output functions. In the “One Fail Others On” mode, if any channel encounters a fault then all other normal channels will keep normal operation. The FAULTB pin supports output functions only.

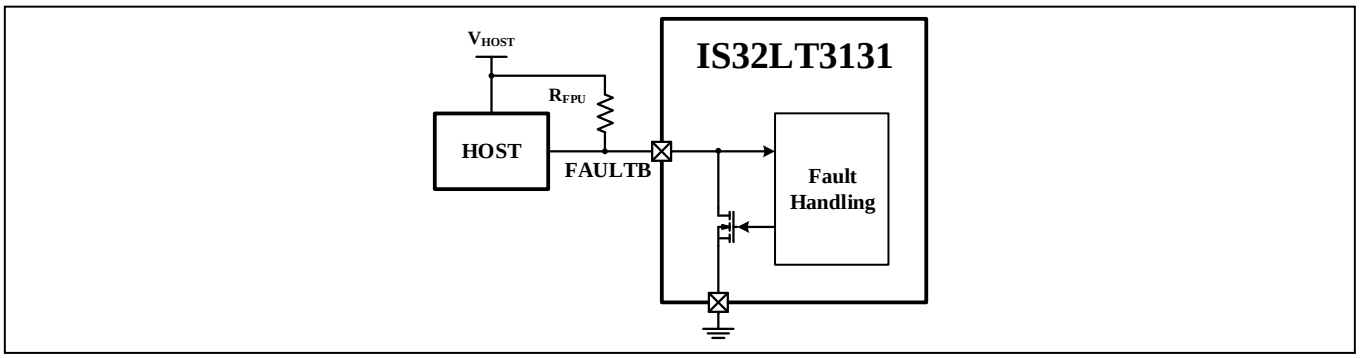


Figure 52 Host Monitors The Fault Reporting

In the “One Fail All Fail” mode, the FAULTB pin supports both input and output functions. Externally pulling FAULTB pin low will disable all outputs, so the FAULTB pin is not allowed to float in this mode. An external pull-up resistor, R_{FPU}, must be added to pull up FAULTB pin high for normal operation. The recommended resistor value is 10kΩ. For lighting systems with multiple IS32LT3131 devices which requires the complete lighting system be shut down when a fault is detected, the FAULTB pin can be used in a parallel connection. A fault output by one device will pull low the FAULTB pins of the other parallel connected devices and simultaneously turn them off. This satisfies the multiple devices “One Fail All Fail” operating requirement.

10.5.2 LED STRING OPEN DETECTION

The LED string open detection is enabled by setting the ODE bit in FLT_DET_EN register (50h) to “1”. Then the LED string open detection is active after VIN voltage rising above a setting fault undervoltage-lockout voltage threshold V_{FLT_UV}, which can be programmed by FLT_UV register (02h). This helps prevent a false fault detection due to insufficient power supply voltage, such as power up transients. If any LED string is open, the corresponding OUTx pin will be pulled up close to VINS by its internal current source. When $V_{IN}>V_{FLT\_UV}$ and the dropout voltage from the VINS pin to the OUTx pin, (V_{INS}-V_{OUTx}), falls below the LED string open detection voltage, V_{OC_FL}, and persists for longer than a deglitch time (typical 4μs), the LED string open protection will be triggered. The corresponding fault flag bits in OPEN_FLTL or OPEN_FLTH register (54h or 55h) and the OPENF bit in FLT_TYPE_L register (5Ah) will be set to “1”. The FAULTB pin will go low after the delay time (programmed by FT[3:0] bits in FLT_CONFIG register) to report the fault condition. The faulty channel will reserve a 4mA retry current for recovery detection. If the fault action mode is “One Fail All Fail”, all other normal channels will be turned off. If the fault action mode is “One Fail Others On”, all other normal channels will keep normal operation.

No matter in which fault protection mode, the device recovers to normal operation and the FAULTB pin will go back to a high impedance after the delay time (programmed by FT[3:0] bits in FLT_CONFIG register) once the open condition is removed, (V_{INS}-V_{OUTx}) rising above the LED string open detection voltage, V_{OC_RS}. The corresponding fault flag bit in OPEN_FLTL or OPEN_FLTH register (54h or 55h) will reset to “0”. However, the OPENF bit in

FLT_TYPE_L register (5Ah) is latched, which means it cannot automatically reset to “0” after open condition being removed but must be cleared by the host MCU writing it back to “0”.

When PWM dimming is implemented, the LED string open detection is only enabled during PWM ON phase. If the PWM on-time is less than the deglitch time (typical 4μs), the device does not report any LED string open fault.

10.5.3 LED STRING SHORT DETECTION

The LED string short detection is enabled by setting the SDE bit in FLT_DET_EN register (50h) to “1”. If any LED string is shorted, the corresponding OUTx pin voltage will be pulled down close to zero. When the OUTx pin voltage, V_{OUTx}, falls below the LED string short detection voltage, V_{SC_FL} and persists for longer than a deglitch time (typical 4μs), the LED string short protection will be triggered. The corresponding fault flag bits in SHORT_FLTL or SHORT_FLTH register (52h or 53h) and the SHORTF bit in FLT_TYPE_L register (5Ah) will be set to “1”. The FAULTB pin will go low after the delay time (programmed by FT[3:0] bits in FLT_CONFIG register) to report the fault condition. The faulty channel will reserve a 4mA retry current for recovery detection. If the fault action mode is “One Fail All Fail”, all other normal channels will be turned off. If the fault action mode is “One Fail Others On”, all other normal channels will keep normal operation.

No matter in which fault protection mode, the device recovers to normal operation and the FAULTB pin will go back to a high impedance after the delay time (programmed by FT[3:0] bits in FLT_CONFIG register) once the short condition is removed, V_{OUTx} rising above the LED string short detection voltage, V_{SC_RS}. The corresponding fault flag bit in SHORT_FLTL or SHORT_FLTH register (52h or 53h) will reset to “0”. However, the SHORTF bit in FLT_TYPE_L register (5Ah) is latched, which means it cannot automatically reset to “0” after short condition being removed but must be cleared by the host MCU writing it back to “0”.

When PWM dimming is implemented, the LED string short detection is only enabled during PWM ON phase. If the PWM on-time is less than the deglitch time (typical 4μs), the device does not report any LED string short fault.

10.5.4 SINGLE LED SHORT DETECTION

The single LED short detection is enabled by setting the SLSDE bit in FLT_DET_EN register (50h) to “1”. Then the single LED short detection is active after VIN voltage rising above the fault undervoltage-lockout voltage threshold V_{FLT_UV}. This helps prevent a false fault detection due to insufficient power supply voltage, such as power up transients. The single LED short detect threshold V_{SLSTH} of each channel is individually programmed by the corresponding LEDx_SLSTH[4:0] bits in LEDx_SLS registers (30h~3Bh). If single LED of any string is shorted, the corresponding OUTx pin voltage will drop down. When the OUTx pin voltage, V_{OUTx}, falls below single LED short detect threshold, V_{SLSTH}, and persists for longer than a deglitch time (typical 9μs), the single LED short protection will be triggered. The corresponding fault flag bits in SLS_FLTL or SLS_FLTH register (56h or 57h) and the SLSF bit in FLT_TYPE_L register (5Ah) will be set to “1”. The FAULTB pin will go low after the delay time (programmed by FT[3:0] bits in FLT_CONFIG register) to report the fault condition. If the fault action mode is “One Fail All Fail (single LED short latches all outputs off)”, all channels will be latched in completely off state until next power cycle or set the OFA[1:0] bits to “10” or “11”. If the fault action mode is “One Fail All Fail (single LED short auto recover)”, all other normal channels will be turned off and the faulty channel will reserve a current for recovery detection. The reserved current can be either normal current or 4mA (Typ.), which can be set by the SLSHCR bit in FLT_CONFIG register (51h). If the fault action mode is “One Fail Others On”, all other normal channels will keep normal operation.

Besides the “One Fail All Fail (single LED short latches all outputs off)” mode, the device recovers to normal operation and the FAULTB pin will go back to a high impedance after the delay time (programmed by FT[3:0] bits in FLT_CONFIG register) once the single LED short condition is removed, V_{OUTx} rising above the LED string short detection voltage, V_{SLSTH}. The corresponding fault flag bit in SLS_FLTL or SLS_FLTH register (56h or 57h) will reset to “0”. However, the SLSF bit in FLT_TYPE_L register (5Ah) is latched, which means it cannot automatically reset to “0” after single LED short condition being removed but must be cleared by the host MCU writing it back to “0”.

When PWM dimming is implemented, the single LED string short detection is only enabled during PWM ON phase. If the PWM on-time is less than the deglitch time (typical 9μs), the device does not report any single LED short fault.

10.5.5 OVERVOLTAGE PROTECTION

There is an inherent body diode from each OUTx pin to VINS pin. If any OUTx pin voltage exceeds the VINS pin voltage, for example either OUTx pin is shorted to VIN or VINS pin shorted to GND, a high current could flow through the body diode that may lead to permanent damage to the device. To protect that, an overvoltage detection is integrated to monitor the voltage from each OUTx pin to VINS pin, (V_{OUTx}-V_{INS}). The overvoltage detection is enabled by setting the OVE bit in FLT_DET_EN register (50h) to “1”. If (V_{OUTx}-V_{INS}) exceeds the overvoltage protection threshold V_{OVP_TH} and persists for longer than a deglitch time (typical 20μs), the device will turn off all outputs for 1.15s (Typ.). The corresponding fault flag bits in OVP_FLTL or OVP_FLTH register (58h or 59h) and the OVPF bit

in FLT_TYPE_H register (5Bh) will be set to “1”. The FAULTB pin will go low after the delay time (programmed by FT[3:0] bits in FLT_CONFIG register) to report the fault condition. The device will recover to normal operation once the 1.15s (Typ.) timer has expired. Under sustained overvoltage condition, the device operates in hiccup mode, attempting to recover every 1.15s (Typ.).

The device recovers to normal operation and the FAULTB pin will go back to a high impedance after the delay time (programmed by FT[3:0] bits in FLT_CONFIG register) once the overvoltage condition is removed. The corresponding fault flag bit in OVP_FLTL or OVP_FLTH register (58h or 59h) will reset to “0”. However, the OVPF bit in FLT_TYPE_H register (5Bh) is latched, which means it cannot automatically reset to “0” after overvoltage condition being removed but must be cleared by the host MCU writing it back to “0”.

10.5.6 OUTPUT OVERCURRENT (ISET PIN SHORT)

The device is protected from an output overcurrent condition caused by the R_{ISET} resistor. All output current is limited to 110mA (Typ.) in case of the ISET pin is shorted to ground or too low a value R_{ISET} resistor is connected to ISET pin. If the condition persists for longer than the deglitch time (typical 1μs), the ISET pin short detection will be triggered. All output current will be reduced to 17mA (Typ.). The ISETSF bit in FLT_TYPE_L register (5Ah) will be set to “1” and the FAULTB pin will go low after the delay time (programmed by FT[3:0] bits in FLT_CONFIG register) to report the fault condition.

Once the resistance from the ISET pin to GND resumes to a normal range, all channels will recover to normal operation and the FAULTB pin will recover to a high impedance after the delay time (programmed by FT[3:0] bits in FLT_CONFIG register). However, the ISETSF bit in FLT_TYPE_L register (5Ah) is latched, which means it cannot automatically reset to “0” after ISET short condition is removed but must be cleared by the host MCU writing it back to “0”.

10.5.7 THERMAL SHUTDOWN

In the event that the junction temperature exceeds T_{SD} (Typ. 165˚C), all output channels will go to the OFF state and the TSDF bit in FLT_TYPE_L register (5Ah) will be set to “1”. If the TRE bit in TEMP_SEN register (03h) to “1”, the FAULTB pin will go low after the delay time (programmed by FT[3:0] bits in FLT_CONFIG register) to report the fault condition. At this point, the device presumably begins to cool off. Any attempt to toggle the channels back to the source condition before the device cooled to below (T_{SD}-T_{SD_HYS}) (Typ. 155˚C) will be blocked and the device will not be allowed to restart. The FAULTB pin will recover to a high impedance after the delay time (programmed by FT[3:0] bits in FLT_CONFIG register) once the device cools down. However, the TSDF bit in FLT_TYPE_L register (5Ah) is latched, which means it cannot automatically reset to “0” but must be cleared by the host MCU writing it back to “0”.

10.5.8 THERMAL ROLL-OFF PROTECTION

The device integrates thermal shutdown protection to prevent the device from overheating. In addition, to preventing the LEDs from flickering due to rapid thermal changes, the device also includes a programmable thermal roll-off feature to reduce power dissipation at high junction temperatures.

The output current will be equal to the set value I_{OUTx} as long as the junction temperature of the device remains below thermal roll-off temperature threshold TS which can be programmed by the TS[1:0] bits in the TEMP_SEN register (03h). If the junction temperature exceeds the temperature threshold TS, the output current of all channels will begin to linearly reduce following the junction temperature ramping up until thermal shutdown. The TF bit in FLT_TYPE_L register (5Ah) will be set to “1”. If the TRRE bit in TEMP_SEN register (03h) to “1”, the FAULTB pin will go low after the delay time (programmed by FT[3:0] bits in FLT_CONFIG register) to report the fault condition. The percentage of the output current before thermal shutdown is also programmable by the TROF[1:0] bits in the TEMP_SEN register (03h).

The output current will resume to the set value I_{OUTx} and the FAULTB pin will recover to a high impedance after the delay time (programmed by FT[3:0] bits in FLT_CONFIG register) once the junction temperature cools down below the thermal roll-off temperature threshold TS. However, the TF bit in FLT_TYPE_L register (5Ah) is latched, which means it cannot automatically reset to “0” but must be cleared by the host MCU writing it back to “0”.

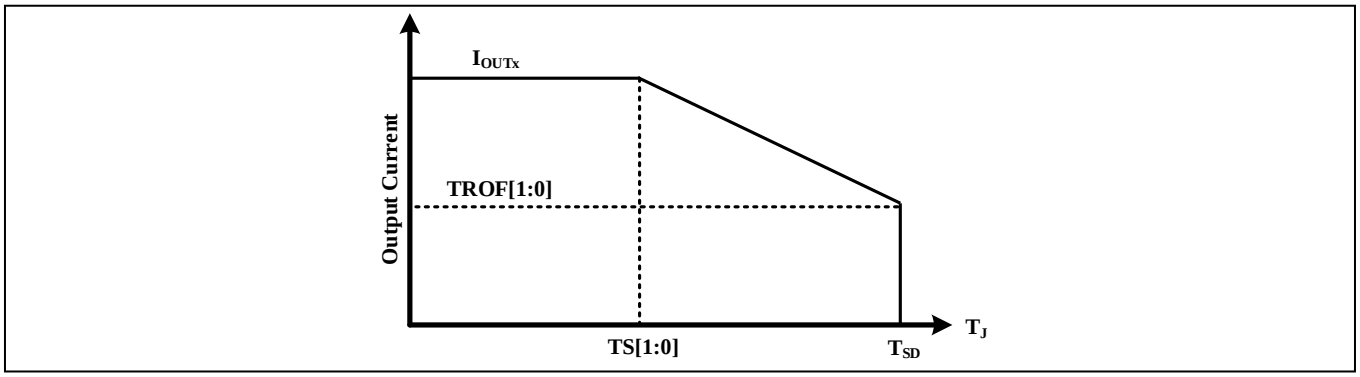


Figure 53 Thermal Roll-off Protection

By mounting the IS32LT3131 device on the same thermal substrate as the LEDs, use of this feature can also limit thermal dissipation of the LEDs.

Fault Action Table (Both Normal State And Fail-Safe State)

Fault Type	Detection	Conditions		Actions	Fault Flags	FAULTB Pin	Recovery
Supply UVLO	$V_{IN}<V_{IN\_UV}$ or $V_{DD}<V_{DD\_UV}$	-		Turn off all channels and reset all registers to default value	-	-	$V_{IN}>(V_{IN\_UV}+V_{IN\_UVHY})$ or $V_{DD}>(V_{DD\_UV}+V_{DD\_UVHY})$
LED string open	$V_{IN}>V_{FLT\_UV}$ and $(V_{INS}-V_{OUTx})<V_{OC\_FL}$	PWM pulse width greater than 4μs (Typ.) and ODE bit = 1	OFA[1:0] ≠ 11	Faulty channel outputs 4mA and other channels off	OPEN_FLTL/ OPEN_FLTH OPENF bit	Pull low	$(V_{INS}-V_{OUTx})>V_{OC\_RS}$ Write OPENF bit to “0”
			OFA[1:0] = 11	Faulty channel outputs 4mA and other channels on			
LED string short	$V_{OUTx}<V_{SC\_FL}$	PWM pulse width greater than 4μs (Typ.) and SDE bit = 1	OFA[1:0] ≠ 11	Faulty channel outputs 4mA and other channels off	SHORT_FLTL/ SHORT_FLTH SHORTF bit	Pull low	$V_{OUTx}>V_{SC\_RS}$ Write SHORTF bit to “0”
			OFA[1:0] = 11	Faulty channel outputs 4mA and other channels on			
Single LED short	$V_{IN}>V_{FLT\_UV}$ and $V_{OUTx}<V_{SLSTH}$	PWM pulse width greater than 9μs (Typ.) and SLSDE bit = 1	OFA[1:0] = 0x	All channels off	SLS_FLTL/ SLST_FLTH SLSF bit	Pull low	Power cycle or set OFA[1:0] to “10”/“11” Write SLSF bit to “0”
			OFA[1:0] = 10	Faulty channel outputs reserve current and other channels off			$V_{OUTx}>V_{SLSTH}$ Write SLSF bit to “0”
			OFA[1:0] = 11	All channels keep on			
Overvoltage	$(V_{OUTx}-V_{INS})>V_{OVP\_TH}$	Longer than 20μs (Typ.) deglitch time and OVE bit =1		Turn off all channels and retry after 1.15s (Typ.)	OVP_FLTL/ OVP_FLTH OVPF bit	Pull low	$(V_{OUTx}-V_{INS})<V_{OVP\_TH}$ Write OVPF bit to “0”
ISET pin short (Overcurrent)	I_{OUTx} limited to 110mA (Typ.)	Longer than 1μs (Typ.) deglitch time		All channels reduced to 17mA (Typ.)	ISETSF bit	Pull low	ISET pin to GND resistance resumes to normal range, Write ISETSF bit to “0”
Thermal shutdown	$T_J>T_{SD}$	-		All channels off	TSDF bit	Pull low (TRE = 1)	$T_J<(T_{SD}-T_{SD\_HYS})$ Write TSDF bit to “0”
Thermal roll-off	$T_J>TS$	TROF[1:0] ≠ 00		All channels linearly reduce output current	TF bit	Pull low (TRRE = 1)	$T_J<TS$ Write TF bit to “0”
CRC error	Calculated CRC does not match CRC data	-		Increments CRC Error Count register	CRCF bit	Pull low	Write CRCF bit to “0”
Communication loss	Watchdog times out	R_{FSMD}=30kΩ, 51kΩ or 68kΩ and no error-free communication		Enter fail-safe modes	CMWF bit	Pull low	Write CMWF bit to “0”
Loopback verification	PWM duty cycle deviation exceeds preset tolerance	VFYEN bit = 1		-	DUTYF_L/ DUTYF_H LPBF bit	Pull low	Deviation drops within preset tolerance Write LPBF bit to “0”

Note 5: OPENF, SHORTF, SLSF, OVPF, ISETSF, TSDF, TF, CRCF, CMWF and LPBF bits are latched. Even though the fault conditions are removed, they cannot automatically reset to “0” but must be cleared by the host MCU writing it back to “0”.

10.6 ADC OPERATION

The IS32LT3131 device includes an integrated 10-bit ADC with fifteen multiplexed input channels (CH0~CH14). First input channel (CH0) is connected to the internal 1V reference voltage. The second input channel (CH1) is connected to the internal PTAT which can be used for junction temperature measurement. The third input channel (CH2) is connected to the internal 5V linear regulator (VDD) via a 1/4 resistor divider. The remaining twelve input channels (CH3~CH14) are respectively connected to the OUTx pin via a 1/13 resistor divider. Setting the ADCEN bit in ADCCFG register (62h) to "1" enables the ADC block. The CHSEL[14:0] selects the desired input channels for ADC measurement. Writing the SADC bit in ADCCTL register (63h) to "1" starts the ADC measurement and clears ADCCYC_F bit to "0", and resets all ADC result registers (65h~7Dh) to default value if the ADCRST bit in ADCCTL register (63h) is set "1". The selected input channels are periodically measured in turn. As long as all selected channel measurement are completed and all ADC results are available, the ADCCYC_F bit will be set to "1". Their 10-bit results are independently stored in the ADC result registers (65h~7Dh). If the LOOP bit in ADCCTL register (63h) is set to "0", all selected channels will only be measured once. If the LOOP bit is set to "1", the ADC will continuously measure all the selected channels all the time.

The reference voltage for the ADC is V_{REFADC} = 1.8V (Typ.). The ADC operating frequency is 1MHz.

When PWM dimming is implemented, the ADC samples/holds the OUTx pin voltage for a period time, which is programmed by ADCSH[1:0] bits in ADCCFG register (62h), after each PWM rising edge with 3μs (Typ.) delay time then ADC conversion starts. To get a more stable result, the ADC measures multiple PWM cycles, which is programmed by the ADCCYC_T[1:0] bits in the ADCCTL register (63h) and stores the average value into the corresponding result register.

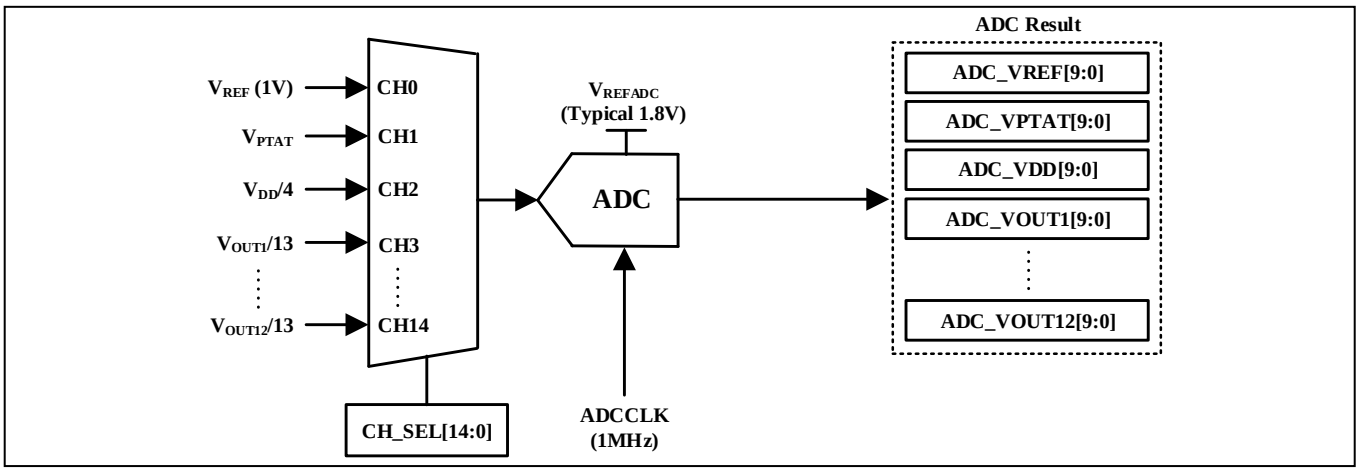


Figure 54 ADC Block

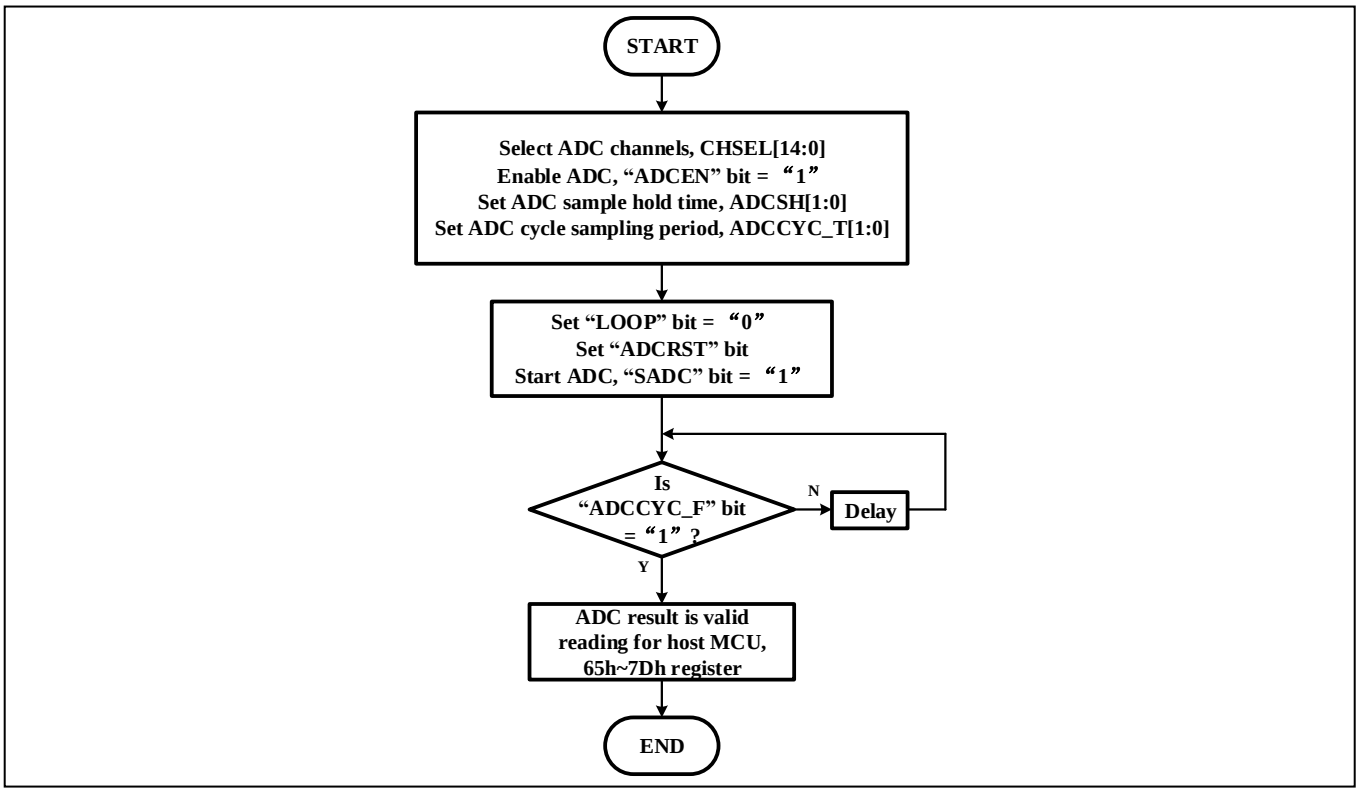


Figure 55 ADC Programming Sequence of Single Mode

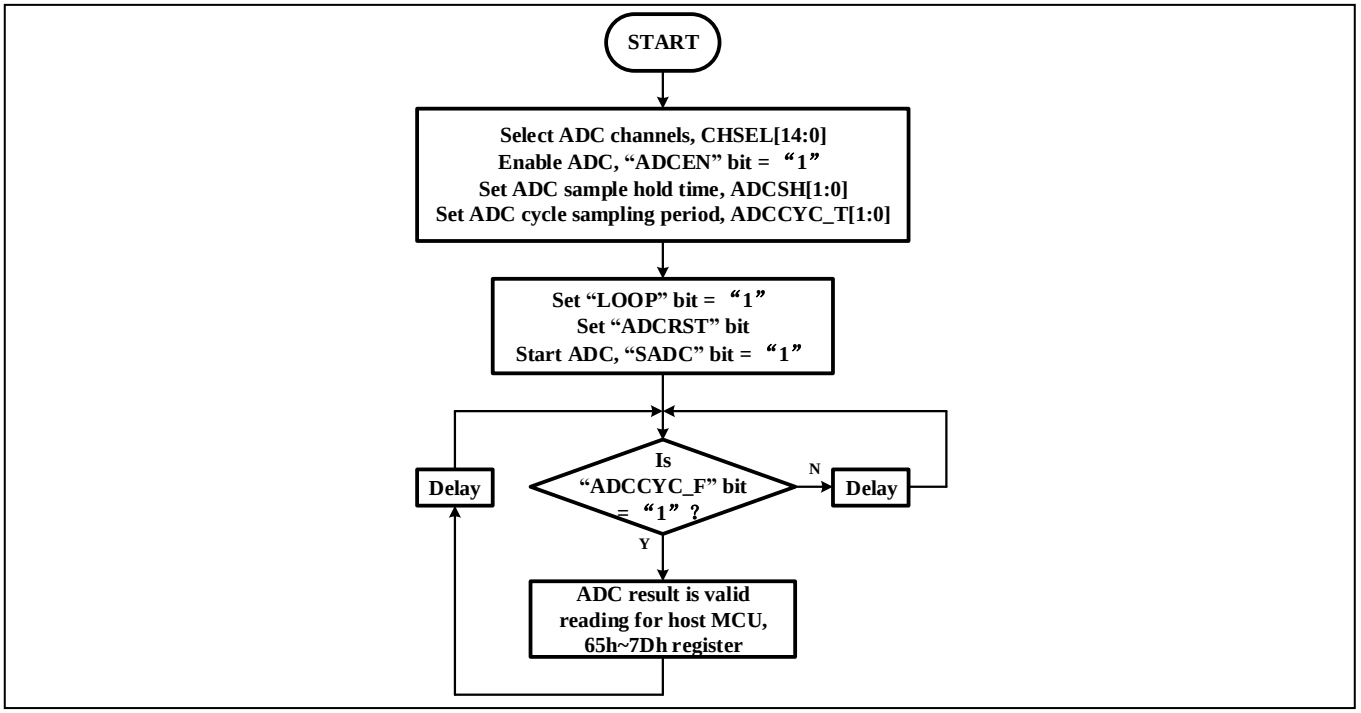


Figure 56 ADC Programming Sequence of Loop Mode

10.7 COMMUNICATION INTERFACES

10.7.1 UART INTERFACE (IS32LT3131A ONLY)

The host MCU can communicate with the IS32LT3131A device using a Universal Asynchronous Receiver and Transmitter (UART). The UART communication process uses a command and response protocol (Lumibus protocol) mastered by the host MCU to write and read the registers to and from each IS32LT3131A device. The IS32LT3131A UART interface utilizes half-duplex communications (transmit and receive cannot overlap). A tri-state buffer drives

the TX pin, it is recommended to place an external pull-up resistor (R_{PU}, 10kΩ typical) on the RX input return line of the host MCU. This allows multiple IS32LT3131A devices to share a common pair of TX and RX signals by connecting all IS32LT3131A TX lines together and all IS32LT3131A RX lines together. The baud rate can support 100kbps~1Mbps.

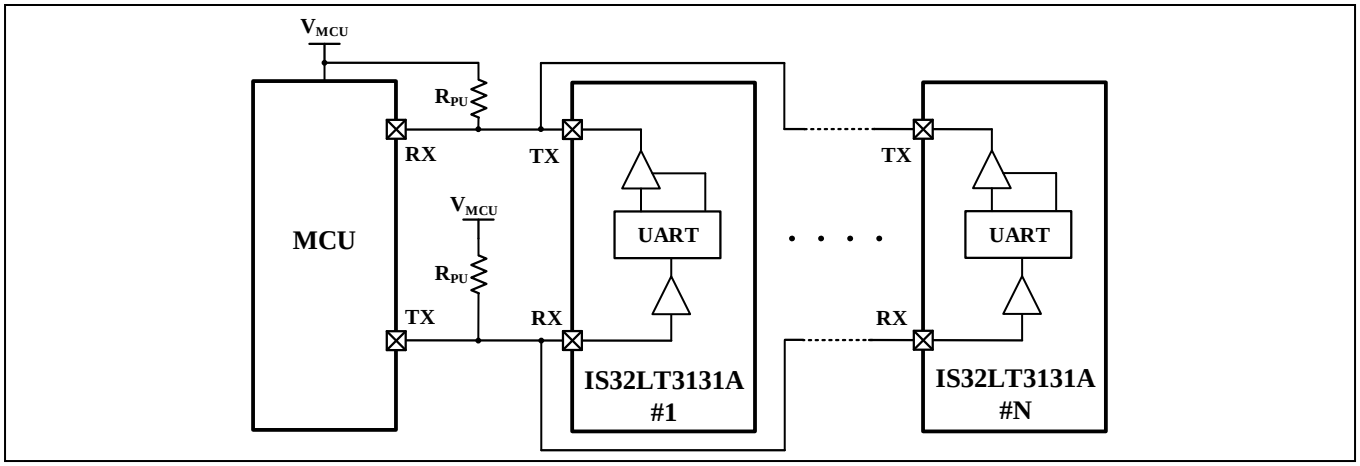


Figure 57 UART Interface Connection to a MCU

Additionally, the physical TX and RX connections of IS32LT3131A can be joined together through an industrial-standard CAN transceiver (CAN PHY). This has the added advantage of protection from shorts to battery and/or shorts to ground on the cables and/or harnesses between the host MCU board and the IS32LT3131A board. The CAN physical layer has excellent EMI and EMS performance with long distance off-board connection.

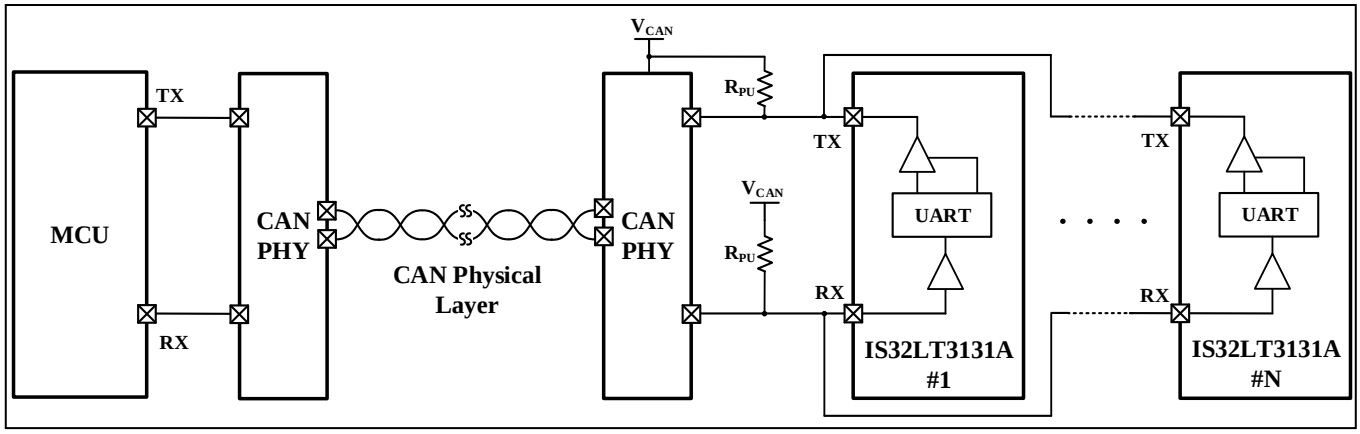


Figure 58 UART Interface with Industrial-standard CAN Transceiver Connection

10.7.2 CANLITE INTERFACE (IS32LT3131B ONLY)

The IS32LT3131B integrates CANLITE, which is compatible to an industrial-standard CAN transceiver (CAN PHY). The CANLITE interface can communicate with the industrial-standard CAN transceiver by connecting the CANLITEH and CANLITEL to the CAN bus. Therefore, the host MCU can control the IS32LT3131B devices via CANLITE interface through a CAN transceiver. The integrated high-speed transceiver of CANLITE interface can support 100kbps~1Mbps baud rate.

The internal CANLITE transceiver converts the single-ended input (TX) of an internal UART interface from internal Lumibus protocol handling circuitry to differential outputs for the BUS lines (CANLITEH and CANLITEL). The CANLITE transceiver reads differential inputs from the BUS lines (CANLITEH and CANLITEL) and transfers this data as the single-ended output (RX) of the internal UART interface to internal Lumibus protocol handling circuitry. This internal UART interface is identical as IS32LT3131A's UART interface and both uses the Lumibus protocol.

Like the industrial-standard CAN termination, resistors should be used to terminate both ends of the CANLITE bus. The termination may be on the cable or in a node. The recommended value of R_{TER1}, R_{TER2} and C_{TER} are 62Ω and 4.7nF.

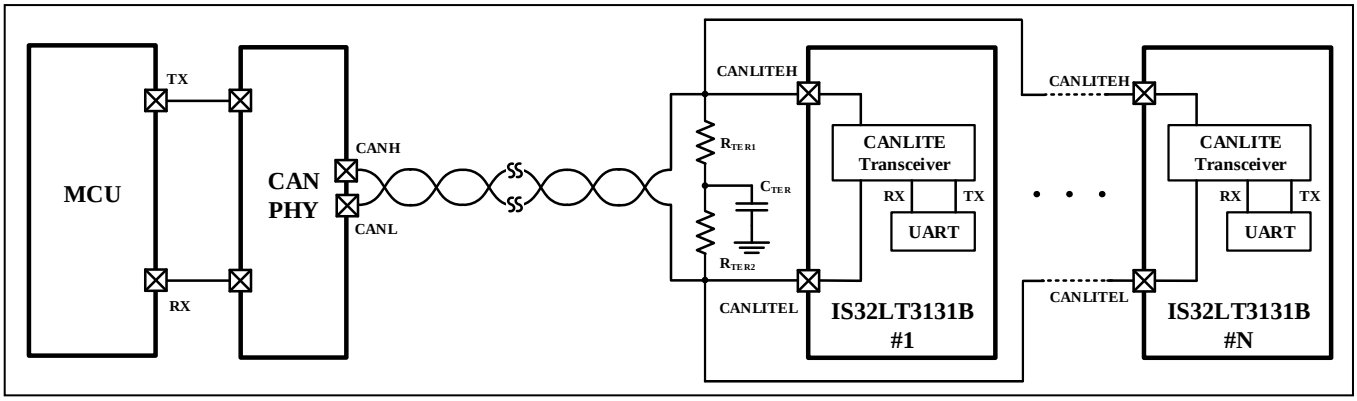


Figure 59 CANLITE Interface Connection

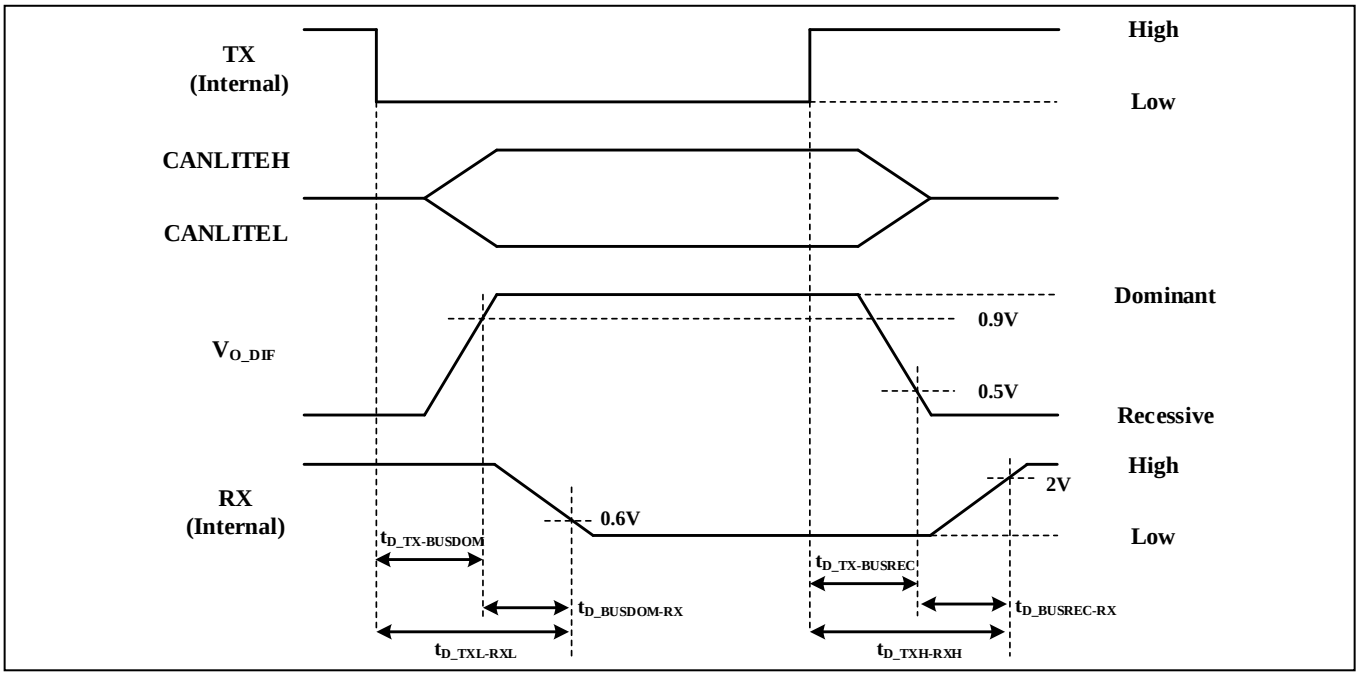


Figure 60 CANLITE Interface Timing

10.7.3 UART DATA FORMAT (IS32LT3131A/B)

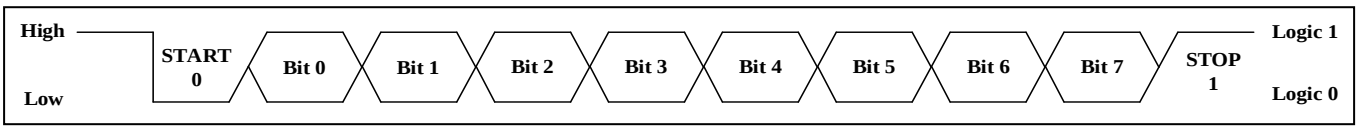


Figure 61 UART Data Byte Format

The UART operates with one start bit, eight data bits (LS bit first) and one stop bit. Above Figure 61 shows the waveform for an individual byte transfer on the UART. A logic “1” state occurs when the device drives the line to high voltage. A logic “0” state occurs when the device drives the line to ground. Below Figure 62 shows actual data bytes with UART data format.

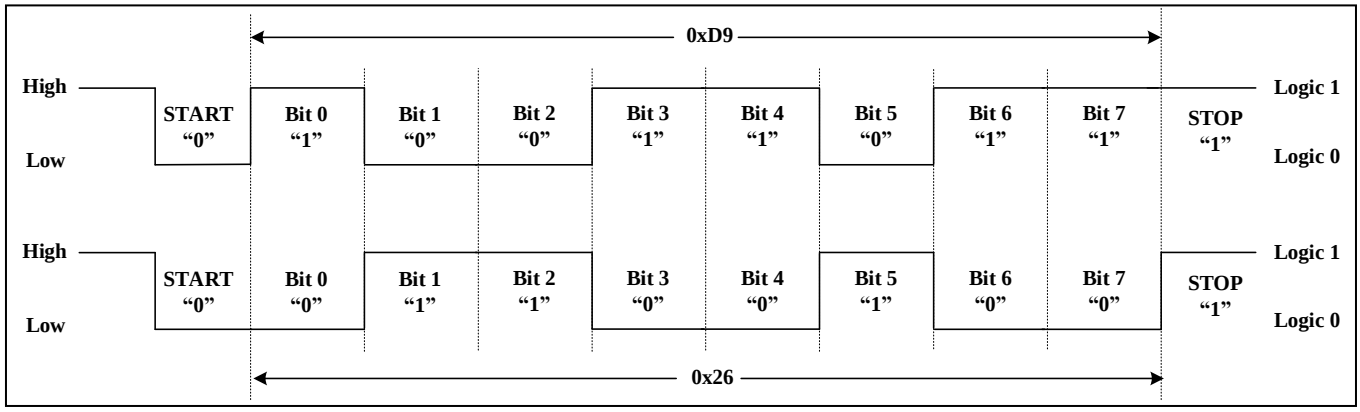


Figure 62 UART Data Transaction Example

The baud rate of UART communication can be 100kbps to 1Mbps which is synchronized by the baud rate of the SYNC byte of the BUS Reset command. UART uses 32x over-sampling on the incoming asynchronous RX signal. Between UART data bytes, at least one bit is required as a STOP bit.

10.7.4 SPI INTERFACE (IS32LT3131C ONLY)

The host MCU can communicate with the IS32LT3131C device using a SPI interface which consists of four signals: CS, SCK, MOSI and MISO. The SPI BUS allows connection to multiple IS32LT3131C devices by star connection (one individual CS per device, while SCK, MOSI, MISO are common). The SPI transfer data packet size is 8-bit and the maximum SCK frequency supported by IS32LT3131C is up to 9MHz. The SPI transaction is initiated by the host MCU on the falling edge of CS. While CS is low, the input data present on the MOSI pin is sampled by the IS32LT3131C device on the rising edge of SCK, MS bit first. The output data is asserted on the MISO pin by IS32LT3131C device at the falling edge of SCK, MS bit first. The host MCU SPI port must be configured to match this operation.

When multiple IS32LT3131C devices are connected to the SPI bus, pulling all CS pins low can write data to all IS32LT3131C devices. Due to SPI bus conflict, the read transmission cannot be implemented this way.

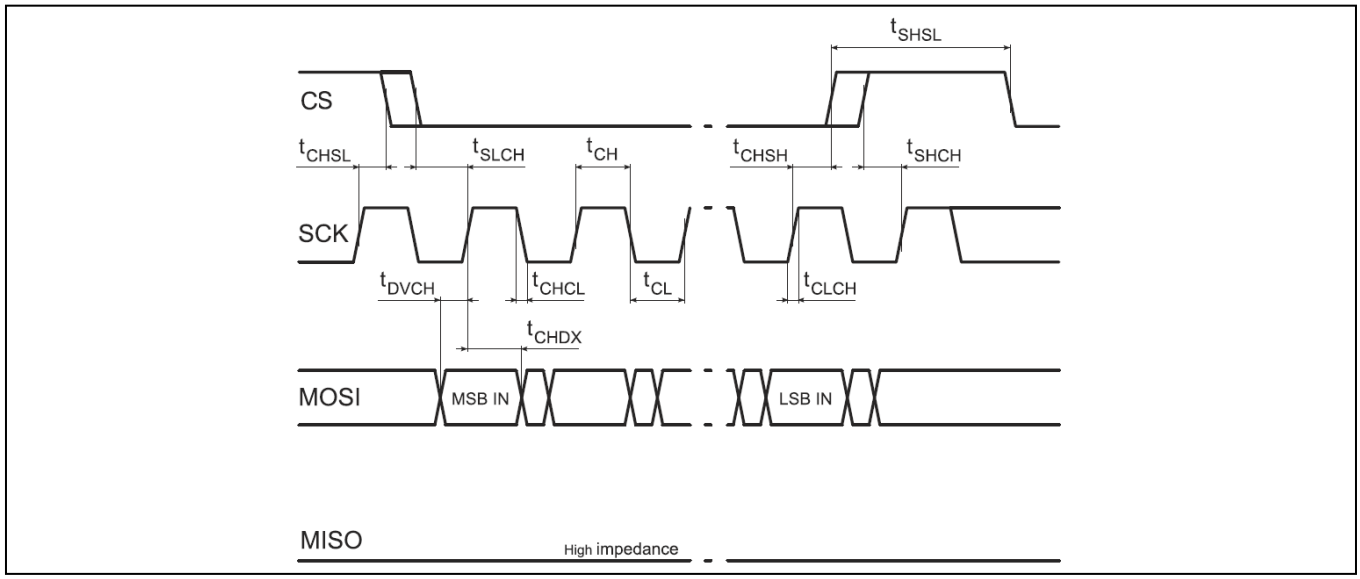


Figure 63 SPI Write Timing

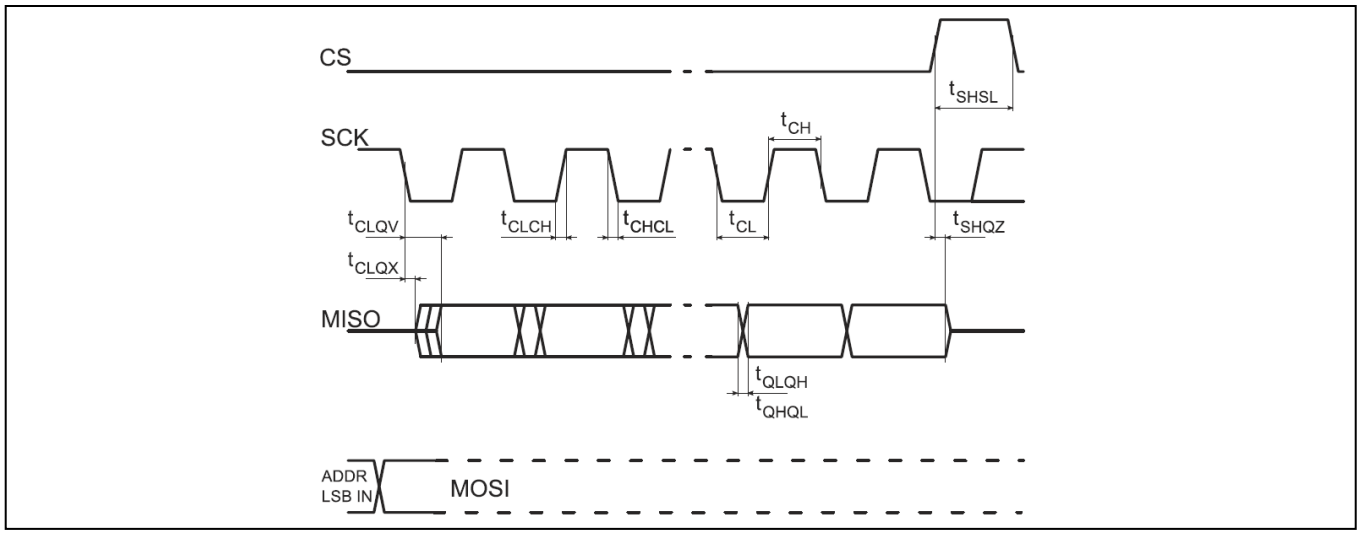


Figure 64 SPI Read Timing

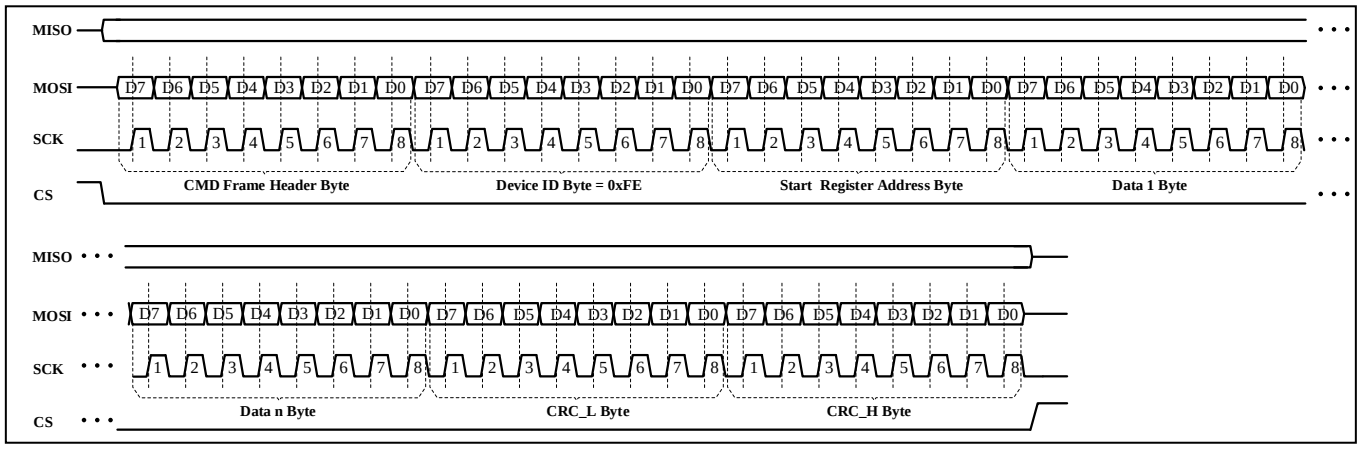


Figure 65 SPI Writing N Bytes of Data to IS32LT3131C

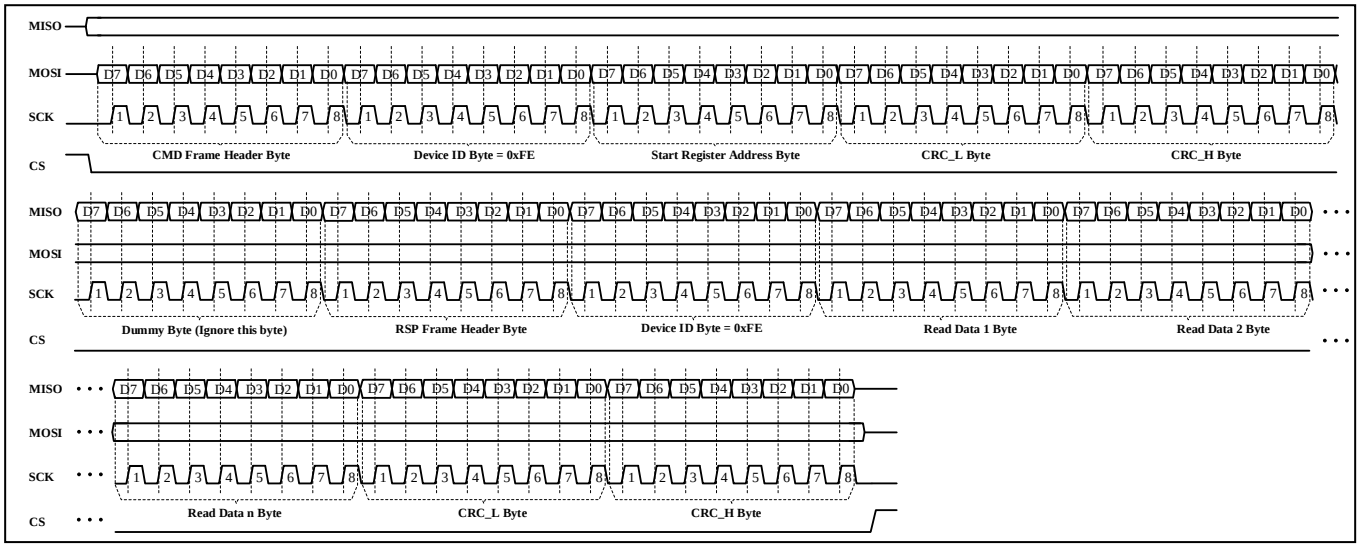


Figure 66 SPI Reading N Bytes of Data from IS32LT3131C

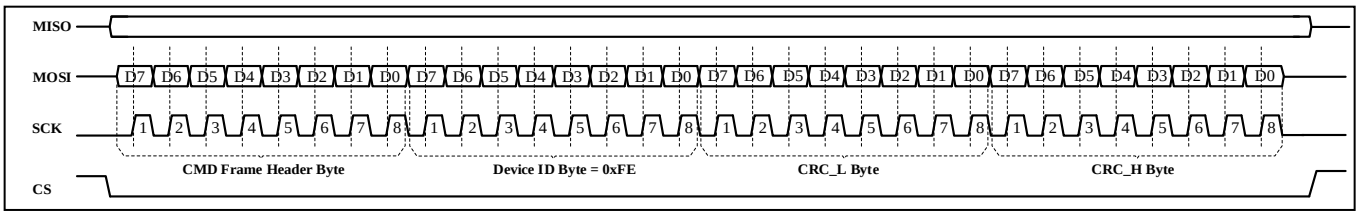


Figure 67 SPI Special Command Writing to IS32LT3131C

10.8 LUMIBUS PROTOCOL

The communication uses the Lumibus protocol which is a UART-based protocol supported by most MCUs. The communication process of all three interfaces uses a command and response protocol mastered by the host MCU to write and read the registers to and from each IS32LT3131 device. This means that the IS32LT3131 device never initiates traffic on the network. The Lumibus protocol maps the registers into an address space on each device. The host MCU uses the Lumibus protocol to initiate a communication transaction by sending a command frame. This command frame addresses either one IS32LT3131 device directly or broadcasts to all IS32LT3131 devices on the network. This addressing may cause a response frame to be sent back from the slave IS32LT3131 device depending on the command type of the command frame. There are four types of commands:

1) BUS Reset Command: resets the UART/CANLITE BUS (SPI interface does not support)
2) Write Command: writes data from host MCU to IS32LT3131 device(s)
3) Read Command: reads data from specific IS32LT3131 device to host MCU
4) Special Command: specifies IS32LT3131 device(s) to implement specific function.

There is no response frame following a broadcast write command frame. Therefore, only two types of response frames exist that an IS32LT3131 device sends back to the host MCU: Write Acknowledge (if enabled) and Read Response.

10.8.1 COMMAND FRAME TYPES

10.8.1.1 BUS Reset Command Frame (IS32LT3131A/B Only)

The host MCU can reset the device UART/CANLITE and Lumibus protocol state machine at any time by sending BUS Reset command. The BUS Reset command consists of reset signal and SYNC byte (0x55). The reset signal includes at least 150μs break low and a logic high break delimiter (2μs~100μs). Upon receiving the bus reset signal, the Lumibus protocol state machine of all IS32LT3131A/B devices on the bus will be reset to a known-good state. The bus reset signal must be followed by a SYNC byte with desired baud rate (within 100kbps to 1Mbps) to synchronize the baud rate to all IS32LT3131A/B devices. The subsequent communication must use the same baud rate. With this synchronization approach, the cost of an external crystal oscillator is saved. To avoid clock drift over time and ambient temperature, it's recommended to periodically send a BUS Reset Command to the IS32LT3131A/B devices.

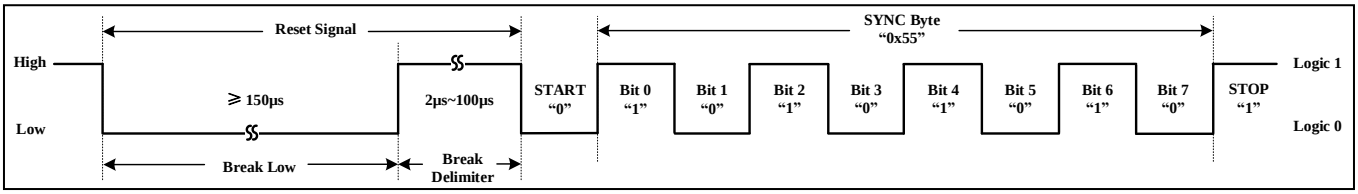


Figure 68 BUS Reset Command

Upon system power up, the host MCU must initialize the interface bus by sending a BUS Reset Command before communication. This BUS reset operation also can be optionally performed by the host MCU for several application scenarios: (1) upon system power up, (2) communication watchdog times out, (3) communication fault is detected.

Note that the BUS Reset command only resets the interface state machine (including stored communication baud rate). It does not reset the registers and does not halt normal LED PWM operation. IS32LT3131C SPI interface does not support the BUS Reset Command.

10.8.1.2 Write Command Frame

The Write Command Frame is comprised of the following sequence.

CMD Frame Header (One Byte)	Device ID (One Byte)	Start Register Address (One Byte)	Data 1 (One Byte)	…	Data N (One Byte)	CRC_L (One Byte)	CRC_H (One Byte)

10.8.1.3 Acknowledge Frame (IS32LT3131A/B Only)

If the ACKEN bit is set to "1" in the SYSCFG register (40h), the addressed device transmits an acknowledge back to the host MCU upon a successful single device write. The Acknowledge Frame is comprised of a single byte (ACK=0x7F) as the following sequence. IS32LT3131C SPI interface does not support acknowledge function.

ACK (0x7F)

10.8.1.4 Read Command Frame

The Read Command Frame (transferred by the host MCU) is comprised of the following sequence.

CMD Frame Header (One Byte)	Device ID (One Byte)	Start Register Address (One Byte)	CRC_L (One Byte)	CRC_H (One Byte)

A successfully addressed IS32LT3131 device then transfers back the appropriate Read Response Frame.

The Read Response Frame is comprised of the following sequence.

RSP Frame Header (One Byte)	Device ID (One Byte)	Data 1 (One Byte)	…	Data N (One Byte)	CRC_L (One Byte)	CRC_H (One Byte)

10.8.1.5 Special Command Frame

The special command specifies the IS32LT3131 device to implement specific function which includes:

1) Update Command

   This special command is used for below scenarios:

- Update the configuration of the PWM registers data and Scaling registers data into output stages at the next PWM boundary after this command is issued.
- Update the configuration of the PHASE_CTRL register (04h).
- Update the configuration of the DC_PWM_SEL register (05h).

2) Registers Reset Command

   Resets all registers to default value, excluding the PWR bit in SYSCFG register (40h).

The Special Command Frame is comprised of the following sequence:

CMD Frame Header (One Byte)	Device ID (One Byte)	CRC_L (One Byte)	CRC_H (One Byte)

One complete command frame can be received successfully even if the bytes in the frame are not sent continuously.

10.8.2 TRANSACTION FRAME DESCRIPTION

The command frames include the following byte types:

1) Frame Header Byte
2) Device ID Byte
3) Start Register Address Byte
4) N Data Byte(s) (N = 1~16, 32)
5) CRC Bytes (CRC_L and CRC_H)
6) Acknowledge Byte (ACK)

10.8.2.1 Frame Header Byte

The Frame Header Byte identifies the transaction as either a write/read command frame or a response frame. In

addition, the Frame Header Byte indicates how many data bytes are being written/read or responded. The number of data bytes to be written/read or responded can be 1~16 or 32.

Frame Header Type	D7	D6	D5	D4:D0
CMD Frame Header	FRM_TYPE	W/R	BCON	CMD
RSP Frame Header	FRM_TYPE	RSVD	RSVD	RSP

The fields shown in the Frame Header Byte above are described in the table below.

	Value (BIN)	Description
FRM_TYPE (Bit 7)	**Frame type configuration bit:**	
	0	Response frame sent back from the IS32LT3131 device to host MCU
	1	Command frame sent from host MCU to the IS32LT3131 device
W/R (Bit 6)	**Write/read configuration bit:**	
	0	Write command frame
	1	Read command frame
BCON (Bit 5)	**Broadcast command configuration bit:**	
	0	Single device write or read.
	1	Broadcast write. The Device ID Byte must be 0xBF to broadcast to all IS32LT3131A/B devices. Broadcast only accepts write command
CMD (Bit 4:0)	**Specify transmit data length for write/read command frame:**	
	00000 ~ 01111	1 byte ~ 16 bytes of data length
	10000	32 bytes of data length
	Special commands (W/R bit must be set to "0"):	
	11000	Update Command. Valid for both single device and broadcast write
	11110	Registers Reset Command. Valid for both single device and broadcast write
RSP (Bit 4:0)	**Specify transmit data length for response frame:**	
	00000 ~ 01111	1 byte ~ 16 bytes of data length
	10000	32 bytes of data length

Note that SPI command doesn't support broadcast command frame. The BCON bit must be set to "0" for SPI communication.

10.8.2.2 Device ID Byte

D7	D6	D5	D4:D0
p[1]	p[0]	1	DEV_ID [4:0]

IS32LT3131A/B supports a maximum of 16 slave devices. The Device ID Byte specifies the device of the destination. There are five DEV_ID bits, one reserved bit and two parity bits. The parity bits for the Device ID Byte are calculated with the equations below:

p[1] = ~(dev_id[1] ^ dev_id[3] ^ dev_id[4] ^ 1)

p[0] = dev_id[0] ^ dev_id[1] ^ dev_id[2] ^ dev_id[4]

The DEV_ID [4:0] of each IS32LT3131A/B device is determined by the two address pins of ADDR0 and ADDR1. As following mapping for the Device ID Byte.

For a broadcast command of UART and CANLITE interfaces (IS32LT3131A/B), the DEV_ID[4:0] must be 0b 11111, otherwise the broadcast command will be invalid.

For SPI interface communication (IS32LT3131C), the DEV_ID[4:0] must be 0b 11110, otherwise the command will

be invalid.

Device Address Decoded Table:

R_{AD0} (kΩ)	R_{AD1} (kΩ)	Bit [7:5] (BIN)	Bit [4:0] (BIN)	Device ID Byte (HEX)
0	0	001	00000	20
0	30	011	00001	61
0	51	111	00010	E2
0	68	101	00011	A3
30	0	011	00100	64
30	30	001	00101	25
30	51	101	00110	A6
30	68	111	00111	E7
51	0	101	01000	A8
51	30	111	01001	E9
51	51	011	01010	6A
51	68	001	01011	2B
68	0	111	01100	EC
68	30	101	01101	AD
68	51	001	01110	2E
68	68	011	01111	6F
-	-	101	11111	BF (For broadcast command only)
-	-	111	11110	FE (For IS32LT3131C SPI only)

10.8.2.3 Start Register Address Byte

The Lumibus protocol allows up to 32 successive register locations from the addressed register to be written or read by a single command frame. The Start Register Address Byte is single byte which specifies the first register being written or read. The Start Register Address byte is only present in Write and Read Command transactions, not in Read Response and Special command transactions

10.8.2.4 N Data Byte(s)

The Frame Header Byte specifies the number of data bytes to be included in the frame.

10.8.2.5 CRC Bytes (CRC_L and CRC_H)

The host MCU sends command to the IS32LT3131 using CRC-16-IBM standard for CRC checksum calculation, which will cover the whole frame bytes, e.g., Frame Header Byte, Device ID Byte, Start Register Address Byte, N Data Bytes. Lower byte first followed by higher byte. The CRC Bytes allow detection of errors within the transaction frame. The device increments the CRC Error Count Register (5Ch) each time a CRC error occurs on an incoming command frame and the CRCF bit in FLT_TYPE_L register (5Ah) will be set to “1” and the FAULTB pin will go low to report fault condition after the delay time (programmed by FT[3:0] bits in FLT_CONFIG register).

The CRCF bit in FLT_TYPE_L register (5Ah) is latched, which means it cannot automatically reset to “0” when no CRC error occurs but must be cleared by the host MCU writing it back to “0”. Once the CRCF bit is cleared, the FAULTB pin will go back to a high impedance after the delay time (programmed by FT[3:0] bits in FLT_CONFIG register).

The CRC bytes are also calculated by the addressed device during its Read Response. The CRC bytes are then appended to the end of the read data, lower byte first followed by higher byte. This allows the host MCU to check the read data coming from the IS32LT3131 device for any transmission errors. The following is a reference CRC checksum C code for a transmission to the IS32LT3131 devices.

```
Uint16 crc_16_ibm (Uint8 *buf, Uint8 len)
{
        Uint16 crc = 0;
        Uint16 I;
        while (len--)
        {
                crc ^= *buf++;
                for (I = 0; I < 8; I++){
                crc = (crc >> 1) ^ ((crc & 1) ? 0xa001 : 0);
                }
        }
        return crc;
}
```

Upon reading data from the IS32LT3131 device, the host MCU should calculate and compare the CRC to determine whether valid data was received. When IS32LT3131 sends back CRC bytes to the host MCU, the calculated CRC bytes must be bit-reversed before comparison to the received CRC bytes. The following is a reference code to perform received CRC bit reversal.

```
Uint8 reverse_byte(Uint8 byte)
{
        // First, swap the nibbles
        byte = (((byte & 0xF0) >> 4)| | ((byte & 0x0F) << 4));
        // Then, swap bit pairs
        byte = (((byte & 0xCC) >> 2) | ((byte & 0x33) << 2));
        // Finally, swap adjacent bits
        byte = (((byte & 0xAA) >> 1) | ((byte & 0x55) << 1));
        // We should now be reversed (bit 0 <--> bit 7, bit 1 <--> bit 6, etc.)
        return byte;
}
```

The following is a reference code for checking the read data against received CRC bytes.

```
bool is_crc_valid(Uint8 *rx_buf, Uint8 crc_start)
{
        Uint16 crc_calc; // Calculated CRC
        Uint8 crc_msb, crc_lsb; // Individual bytes of calculated CRC
        // Calculate the CRC based on bytes received
        crc_calc = crc_16_ibm(rx_buf, crc_start);
        crc_lsb = (crc_calc & 0x00FF);
        crc_msb = ((crc_calc >> 8) & 0x00FF);
        // Perform the bit reversal within each byte
        crc_msb = reverse_byte(crc_msb);
        crc_lsb = reverse_byte(crc_lsb);
        // Do they match?
        if((*(rx_buf + crc_start) == crc_lsb) && (*(rx_buf + crc_start + 1) == crc_msb))
        {
                return TRUE;
        }
        else
        {
                return FALSE;
        }
}
```

10.8.2.6 Acknowledge Byte

The Acknowledge Byte (“ACK”) consists of a single byte (ACK=0x7F):

ACK is sent back by the addressed IS32LT3131A/B device only if the ACKEN bit is set to “1” in the SYSCFG register (40h) and only if the write is successful. A successful write yields no CRC checksum error or parity errors. Note that

the acknowledge is only valid for single device write transaction of IS32LT3131A/B. The SPI interface of IS32LT3131C does not support the acknowledge function.

10.8.2.7 Turnaround Time

When considering back-to-back data transfer, the turnaround time (additional time required between the end of the previous byte stop bit and the beginning of the next byte start bit) is required, that means a finite amount of dead time must be inserted between two bytes or two command frames. As the requirement shown in Figure 69~73. It's recommended to use dual stop bits mode for the UART interface.

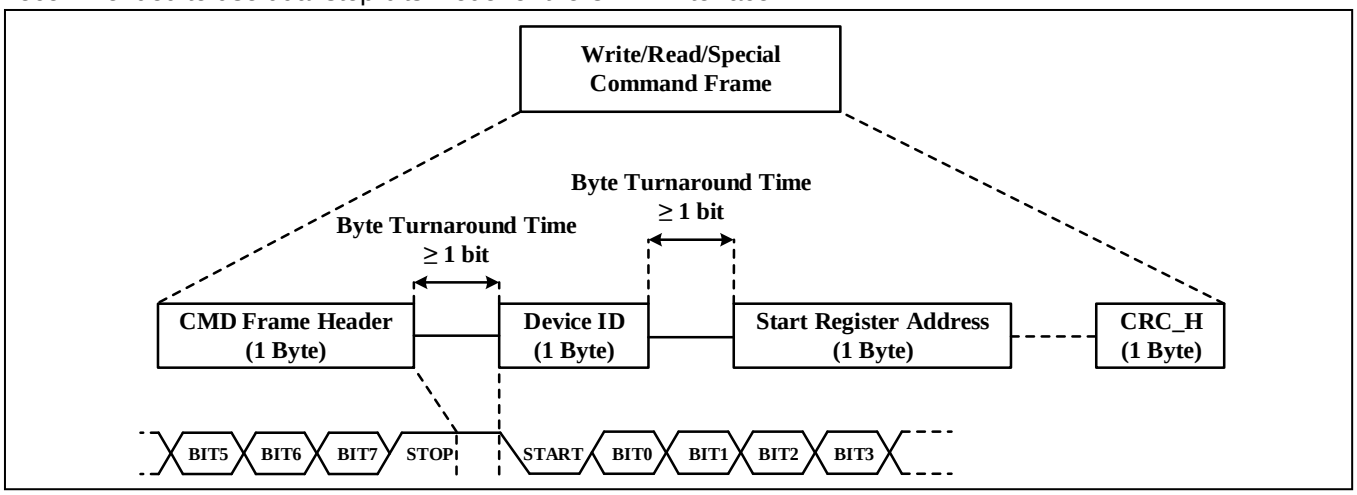


Figure 69 Turnaround Time Between Byte and Byte of Write/Read/Special Command Frame

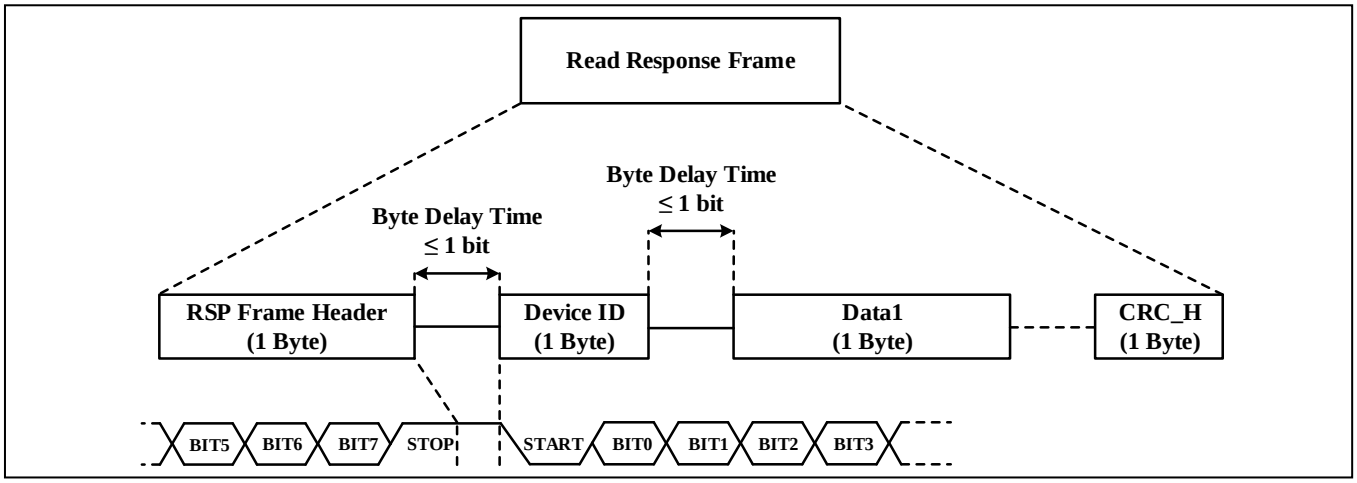


Figure 70 Delay Time Between Byte and Byte of Read Response Frame

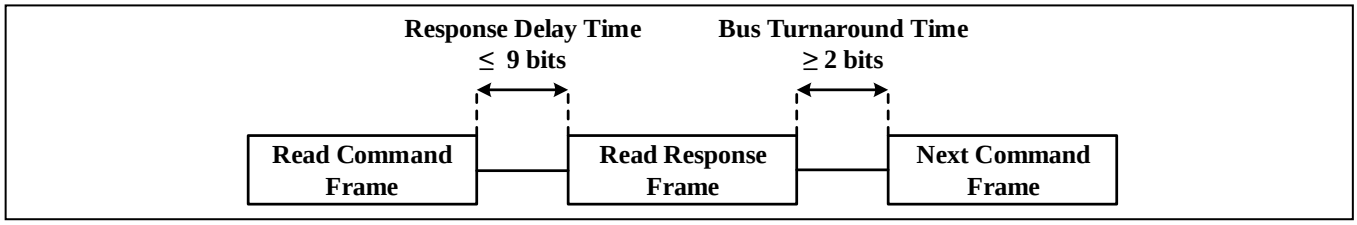


Figure 71 Turnaround Time Between Read Response Frame and Next Command Frame

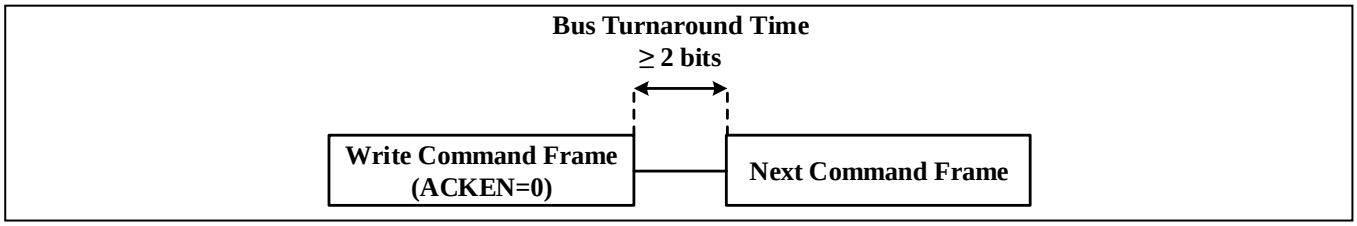


Figure 72 Turnaround Time Between Write Command Frame and Next Command Frame (ACK Disabled)

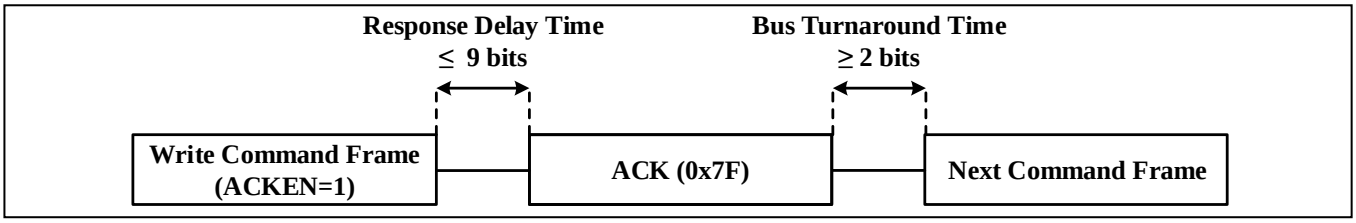


Figure 73 Turnaround Time Between ACK and Next Command Frame (ACK Enabled)

10.8.3 COMMUNICATIONS EXAMPLES

The total number of transmitted bytes depends on the specific task being performed. The examples below show the sequence of transmitted bytes for a given transaction.

Example 1: Single Device Write of 3 Bytes

Write to Device ID=0x05 (Device ID with parity = 0x25, R_{AD0}=30kΩ, R_{AD1}=30kΩ): beginning at register 20h, PWM1_H=0x1F, PWM2_H=0x2F, PWM3_H=0x3F.

Byte Types	Number of Bytes
CMD Frame Header Byte	1
Device ID Byte	1
Start Register Address Byte	1
Data Bytes	3
CRC Bytes	2
Total	8

Interface	Command Frame							
	CMD Frame Header	Device ID	Start Register Address	Data 1	Data 2	Data 3	CRC_L	CRC_H
UART/ CANLITE	0x82 (0b10000010)	0x25	0x20	0x1F	0x2F	0x3F	0x35	0xC3
SPI	0x82 (0b10000010)	0xFE	0x20	0x1F	0x2F	0x3F	0x51	0xD0

Acknowledge from addressed device (if enabled ACKEN bit for IS32LT3131A/B)

Acknowledge Frame
ACK
0x7F

Example 2: Single Device Read of 2 Bytes

Read from Device ID=0x03 (Device ID with parity = 0xA3, R_{AD0}=0Ω, R_{AD1}=68kΩ): beginning at register 5Ah, read FLT_TYPE_L and FLT_TYPE_H

Byte Types	Number of Bytes
CMD Frame Header Byte	1
Device ID Byte	1
Start Register Address Byte	1
CRC Bytes	2
Total	5

Interface	Command Frame				
	CMD Frame Header	Device ID	Start Register Address	CRC_L	CRC_H
UART/ CANLITE	0xC1 (0b11000001)	0xA3	0x5A	0xA9	0x37
SPI	0xC1 (0b11000001)	0xFE	0x5A	0x91	0xA7

Read Response: FLT_TYPE_L=0x00, FLT_TYPE_H=0x00

Byte Types	Number of Bytes
RSP Frame Header Byte	1
Device ID Byte	1
Data Bytes	2
CRC Bytes	2
Total	6

Interface	Command Frame					
	RSP Frame Header	Device ID	Data 1	Data 2	CRC_L	CRC_H
UART/ CANLITE	0x01 (0b00000001)	0XA3	0x00	0x00	0x8F	0x7B
SPI	0x01 (0b00000001)	0xFE	0x00	0x00	0x06	0x30

Example 3: Broadcast Write of 3 Bytes

Broadcast write to all devices (fixed Device ID with parity = 0xBF): beginning at register 10h, SCA1=0x0F, SCA2=0x1F, SCA3=0x2F

Note: for SPI interface, single device write transaction with pulling all CS pins low can broadcast data to all IS32LT3131C devices.

Byte Types	Number of Bytes
CMD Frame Header Byte	1
Device ID Byte	1
Start Register Address Byte	1
Data Bytes	3
CRC Bytes	2
Total	8

Interface	Command Frame							
	CMD Frame Header	Device ID	Start Register Address	Data 1	Data 2	Data 3	CRC_L	CRC_H
UART/ CANLITE	0xA2 (0b10100010)	0xBF	0x10	0x0F	0x1F	0x2F	0x71	0xB6
SPI	0x82 (0b10000010)	0xFE	0x10	0x0F	0x1F	0x2F	0x4A	0xD9

Example 4: Broadcast Registers Reset Command (Special Command)

Broadcast Registers Reset Command to all devices (fixed Device ID with parity = 0xBF):

Byte Types	Number of Bytes
CMD Frame Header Byte	1
Device ID Byte	1
CRC Bytes	2
Total	4

Interface	Command Frame			
	CMD Frame Header	Device ID	CRC_L	CRC_H
UART/ CANLITE	0xBE (0b10111110)	0xBF	0x30	0x10
SPI	0x9E (0b10011110)	0xFE	0xE9	0xE0

Example 5: Broadcast Update Command (Special Command)

Broadcast Update Command to all devices (fixed Device ID with parity = 0xBF):

Byte Types	Number of Bytes
CMD Frame Header Byte	1
Device ID Byte	1
CRC Bytes	2
Total	4

Interface	Command Frame			
	CMD Frame Header	Device ID	CRC_L	CRC_H
UART/ CANLITE	0xB8 (0b10111000)	0xBF	0x33	0xB0
SPI	0x98 (0b10011000)	0xFE	0xEA	0x40

10.9 DEVICE FUNCTIONAL MODES

The IS32LT3131 device operates in one of several states.

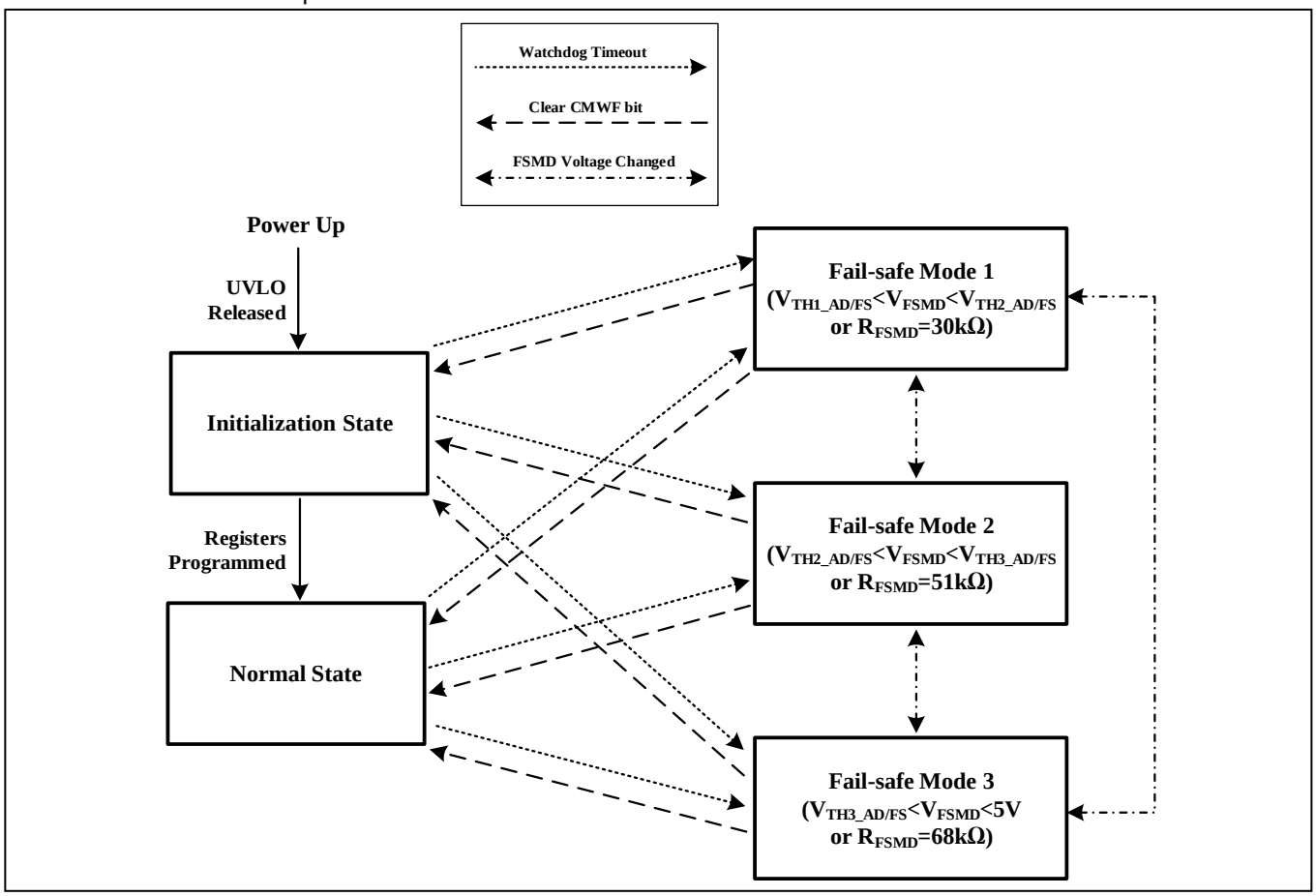


Figure 74 Operation States

10.9.1 INITIALIZATION STATE

Upon power up and released from UVLO, the device operates in initialization state. In this state, all registers are reset to default values and all outputs are in off state. The device is waiting for master to control it through the interfaces.

10.9.2 NORMAL STATE

In normal state, the digital circuitry controls the IS32LT3131 outputs by accepting interface commands and by monitoring and responding to real-time events on the inputs associated with the analog and power circuitry. This allows dimming of the LED outputs using the registers settings.

10.9.3 FAIL-SAFE STATE

This state allows the user to preset the outputs' state if the communication is broken. The device integrates a communication watchdog timer that operates based on the system clock pulse. The tap point, programmed via CMWTAP register (41h), defines the timing of the communication watchdog timer (a 25-bit counter). By default, the tap point is set to bit 22, which means the device requires 2^22 system clock cycles for the communication watchdog timer to time out. If the communication watchdog times out (no error-free communication is successfully received for the programmed number of system clock cycles), the device will enter fail-safe state which includes three modes, Mode 1 ~ Mode 3.

The FSMD pin is used to configure the fail-safe modes. When the resistor R_{FSMD} is connected to the FSMD pin, the internal $I_{AD/FS}$ (typical 50μA) current source creates a voltage on the FSMD pin, V_{FSMD}. The device compares the V_{FSMD} with internal different reference voltage levels ($V_{TH1\_AD/FS}$, $V_{TH2\_AD/FS}$ and $V_{TH3\_AD/FS}$) to determine the fail-safe mode. It also allows to externally apply proper voltage on the FSMD pin to either choose or change the fail-safe mode. Refer to the Fail-safe Mode Setting Table.

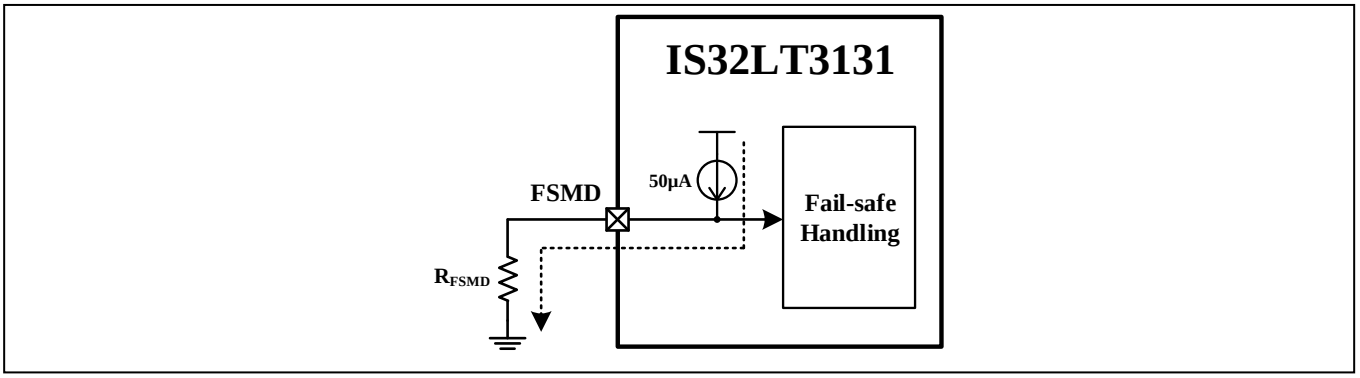


Figure 75 Fail-safe Mode Setting

When $0V<V_{FSMD}<V_{TH1\_AD/FS}$, or $R_{FSMD}=10k\Omega$, the internal communication watchdog is invalid, and the fail-safe mode is disabled. The outputs are always controlled by the scaling and PWM registers (10h~2Eh).

When $V_{TH1\_AD/FS}<V_{FSMD}<V_{TH2\_AD/FS}$, or $R_{FSMD}=30k\Omega$, the internal communication watchdog is active, and the fail-safe mode is Mode 1. If the watchdog times out, the device will enter fail-safe Mode 1 and the outputs will be determined by the DEFAULT registers (07h~0Fh). The CMWF bit in FLT_TYPE_L register (5Ah) will be set to "1" and the FAULTB pin will go low after the delay time (programmed by FT[3:0] bits in FLT_CONFIG register) to report the fault condition. To quit from the fail-safe mode to normal state, the CMWF bit in FLT_TYPE_L register (5Ah) must be cleared by the host MCU writing it to "0". The watchdog timer will be reset and the FAULTB pin will go back to a high impedance after the delay time (programmed by FT[3:0] bits in FLT_CONFIG register).

When $V_{TH2\_AD/FS}<V_{FSMD}<V_{TH3\_AD/FS}$, or $R_{FSMD}=51k\Omega$, the internal communication watchdog is active, and the fail-safe mode is Mode 2. If the watchdog times out, the device will enter fail-safe Mode 2 and all outputs will be forced into completely off. The CMWF bit in FLT_TYPE_L register (5Ah) will be set to "1" and the FAULTB pin will go low after the delay time (programmed by FT[3:0] bits in FLT_CONFIG register) to report the fault condition. To quit from the fail-safe mode to normal state, the CMWF bit in FLT_TYPE_L register (5Ah) must be cleared by the host MCU writing it to "0". The watchdog timer will be reset and the FAULTB pin will go back to a high impedance after the delay time (programmed by FT[3:0] bits in FLT_CONFIG register).

When $V_{TH3\_AD/FS}<V_{FSMD}<5V$, or $R_{FSMD}=68k\Omega$, the internal communication watchdog is active, and the fail-safe mode is Mode 3. If the watchdog times out, the device will enter fail-safe Mode 3 and all outputs will be forced into almost fully on (with 98% PWM duty cycle). The CMWF bit in FLT_TYPE_L register (5Ah) will be set to "1" and the FAULTB pin will go low after the delay time (programmed by FT[3:0] bits in FLT_CONFIG register) to report the fault condition. To quit from the fail-safe mode to normal state, the CMWF bit in FLT_TYPE_L register (5Ah) must be cleared by the host MCU writing it to "0". The watchdog timer will be reset and the FAULTB pin will go back to a high impedance after the delay time (programmed by FT[3:0] bits in FLT_CONFIG register).

In the fail-safe modes, the fault protections also are valid, including LED string open/short, single LED short, overvoltage, overcurrent (ISET shorted), and over temperature.

Note that the device must be re-initialized after quitting from the fail-safe mode to normal state.

Fail-safe Mode Setting Table

FSMD Pin	Fail-safe Mode	LED State In Fail-safe Mode
$0V<V_{FSMD}<V_{TH1\_AD/FS}$ or $R_{FSMD}=10k\Omega$	Disabled	-
$V_{TH1\_AD/FS}<V_{FSMD}<V_{TH2\_AD/FS}$ or $R_{FSMD}=30k\Omega$	Mode 1	Determined by Default Registers (07h~0Fh)
$V_{TH2\_AD/FS}<V_{FSMD}<V_{TH3\_AD/FS}$ or $R_{FSMD}=51k\Omega$	Mode 2	All Completely Off
$V_{TH3\_AD/FS}<V_{FSMD}<5V$ or $R_{FSMD}=68k\Omega$	Mode 3	All On with 98% PWM duty cycle

10.10 PWM DUTY CYCLE LOOPBACK VERIFICATION

To enhance its operation reliability, the IS32LT3131 integrates a loopback verification circuit with twelve multiplexed inputs to monitor the PWM duty cycle of output channels. The twelve input channels (LPBCH1~LPBCH12) are

respectively connected to each current source output stage. The VFYCHSEL[3:0] bits in VFYCTL register (F1h) selects the desired input channel for PWM duty cycle monitoring. Setting the VFYEN bit in VFYCTL register (F1h) to “1” enables the loopback verification and clears VFYRDY bit in the VFYCFG register (F2h) to “0”. Once the verification is completed, the VFYRDY bit will be set to “1” and the PWM duty cycle measurement result is stored in the PWMDUTY_H (F5h) and PWMDUTY_L (F6h) registers. The loopback verification circuit compares the measurement result with the PWM duty cycle setting value in the PWM buffer. If the deviation is out of the tolerance, preset by the TOLERANCE[4:0] bits in the VFYCFG register (F2h), the corresponding loopback fault flag bit in DUTYF_L or DUTYF_H (F3h or F4h) and the LPBF bit in FLT_TYPE_H (5Bh) will be set to “1”. The FAULTB pin will go low after the delay time (programmed by FT[3:0] bits in FLT_CONFIG register) to report the fault condition.

The corresponding loopback fault flag bit in DUTYF_L or DUTYF_H (F3h or F4h) will reset to “0” and the FAULTB pin will go back to a high impedance after the delay time (programmed by FT[3:0] bits in FLT_CONFIG register) once the deviation drops within the tolerance. However, the LPBF bit in FLT_TYPE_H register (5Bh) is latched, which means it cannot automatically reset to “0” after tolerance fault condition disappears but must be cleared by the host MCU writing it back to “0”.

The tolerance, preset by the TOLERANCE[4:0] bits in the VFYCFG register (F2h), should not be set too low, especially at high PWM frequency applications. Otherwise, the loopback fault would be falsely triggered due to the accuracy of the PWM duty cycle measurement. To ensure valid loopback verification result, the minimum tolerance available for selected PWM frequency can be calculated by:

$$\text{Tolerance}_{\text{MIN}} = \frac{\frac{2\mu s \times 1024}{t_{PWM}} - 3}{4} \qquad (20)$$

Where t_{PWM} is the period time of the selected PWM frequency in μs.

For example,

Assume the selected PWM frequency is 10kHz (t_{PWM}=100μs), the minimum tolerance should be:

$$\text{Tolerance}_{\text{MIN}} = \frac{\frac{2\mu s \times 1024}{100\mu s} - 3}{4} = 4.37$$

So, the TOLERANCE[4:0] must be set to not less than 5.

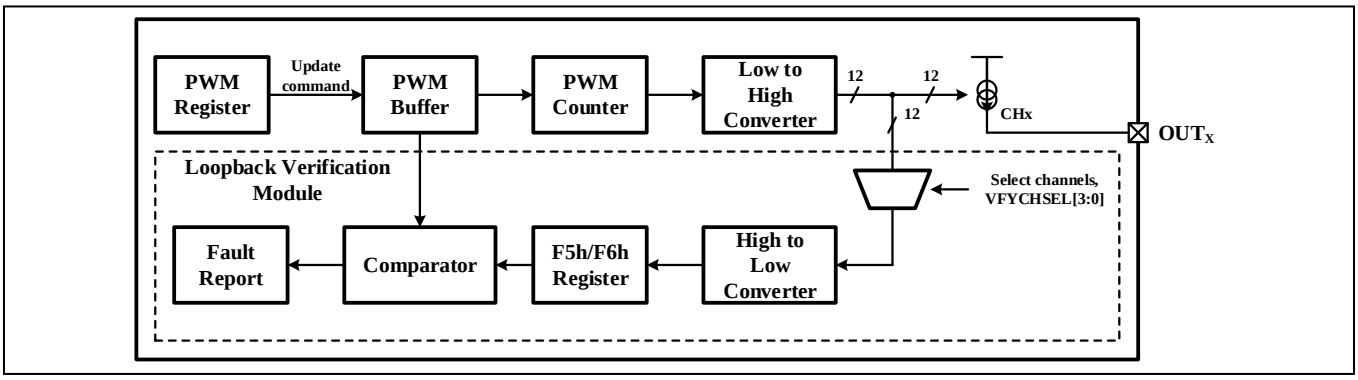


Figure 76 Loopback Verification Block

10.11 THERMAL CONSIDERATIONS

The package thermal resistance, θ_{JA}, determines the amount of heat that can pass from the silicon die to the surrounding ambient environment. The θ_{JA} is a measure of the temperature rise created by power dissipation and is usually measured in degree Celsius per watt (°C/W). The junction temperature, T_J, can be calculated by the rise of the silicon temperature, ΔT, the power dissipation on IS32LT3131, P_{3131}, and the package thermal resistance, θ_{JA}, as in Equation (21):

$$T_J = T_A + \Delta T = T_A + P_{3131} \times \theta_{JA} \qquad (21)$$

The P_{3131} is descripted in the “THERMAL SHUNT TOPOLOGY” section.

When operating the chip at high ambient temperatures, or when the supply voltage is high, care must be taken to avoid exceeding the package power dissipation limits. The maximum power dissipation at T_A=25°C can be calculated using the following Equation (22):

$$P_{D(MAX)} = \frac{150℃-25℃}{\theta_{JA}} \qquad (22)$$

So,

$$P_{D(MAX)} = \frac{150℃ - 25℃}{35.5℃/W} \approx 3.52W$$

for eTSSOP-28 package.

Figure 77, shows the power derating of the IS32LT3131 on a JEDEC board (in accordance with JESD 51-5 and JESD 51-7) standing in still air.

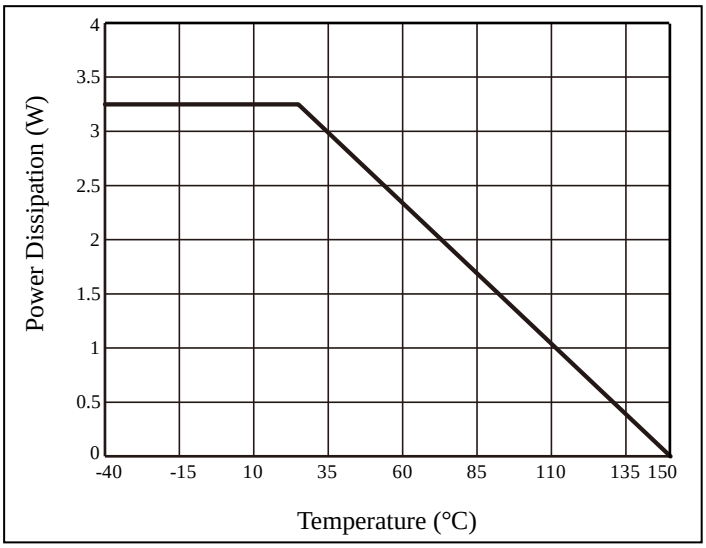


Figure 77 Dissipation Curve (eTSSOP-28)

In the thermal shunt application, the R_P will share quite a lot power dissipation; therefore its package power rating should be sufficient to prevent heat run away.

When designing the Printed Circuit Board (PCB) layout, double-sided PCB with a large copper area on each side of the board directly under the IS32LT3131 and the thermal shunt resistor. Multiple thermal vias, as shown in Figure 78, will help to conduct heat from the exposed pad of the IS32LT3131 and the thermal shunt resistor to the copper on each side of the board. To avoid the heat buildup, the thermal shunt resistor should be spread out on the PCB board with some distance from IS32LT3131.

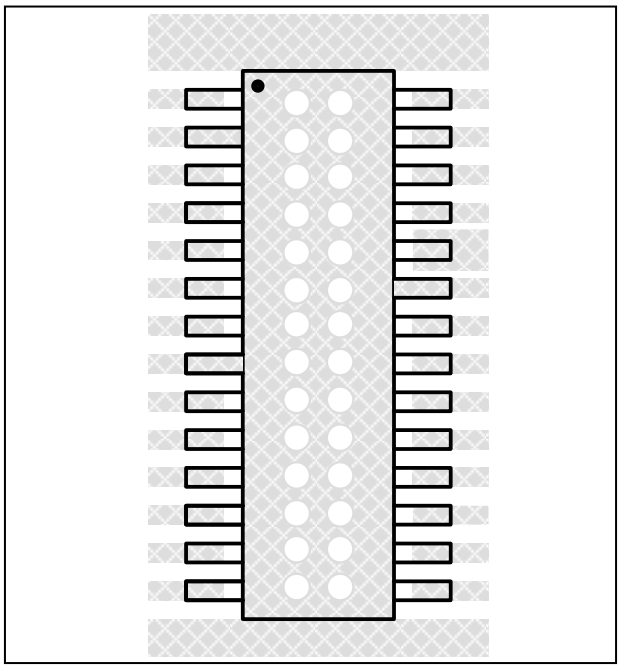


Figure 78 Board Via Layout For Thermal Dissipation

11 REGISTERS

11.1 REGISTER MAP

ADDR	REG NAME	D7	D6	D5	D4	D3	D2	D1	D0	DEFAULT
00h	CONFIG	TST_EN	RSVD	CM	PFS	RSVD				0b 00000000
01h	GC_CTRL	RSVD		GCC[5:0]						0b 00111111
02h	FLT_UV	RSVD			FLT_UV[4:0]					0b 00000010
03h	TEMP_ SEN	TRE	TRRE	RSVD		TROF[1:0]		TS[1:0]		0b 00000000
04h	PHASE_CTRL	RSVD	PS6	PS5	PS4	PS3	PS2	PS1	PDE	0b 00000001
05h	DC_PWM_SEL	RSVD							DC_PWM	0b 00000000
06h	Reserved	-								-
07h	DEFGCC	RSVD	DEFDC_PWM	DEFGCC[5:0]						0b 00000000
08h	DEFLED_L	DEFLED(8:1)								0b 00000000
09h	DEFLED_H	RSVD				DEFLED(12:9)				0b 00000000
0Ah	DEFPWM_G1	DEFPWM2[3:0]				DEFPWM1[3:0]				0b 00000000
0Bh	DEFPWM_G2	DEFPWM4[3:0]				DEFPWM3[3:0]				0b 00000000
0Ch	DEFPWM_G3	DEFPWM6[3:0]				DEFPWM5[3:0]				0b 00000000
0Dh	DEFPWM_G4	DEFPWM8[3:0]				DEFPWM7[3:0]				0b 00000000
0Eh	DEFPWM_G5	DEFPWM10[3:0]				DEFPWM9[3:0]				0b 00000000
0Fh	DEFPWM_G6	DEFPWM12[3:0]				DEFPWM11[3:0]				0b 00000000
10h	SCA1	SCA1_DATA[7:0]								0b 11111111
11h	SCA2	SCA2_DATA[7:0]								0b 11111111
12h	SCA3	SCA3_DATA[7:0]								0b 11111111
13h	SCA4	SCA4_DATA[7:0]								0b 11111111
14h	SCA5	SCA5_DATA[7:0]								0b 11111111
15h	SCA6	SCA6_DATA[7:0]								0b 11111111
16h	SCA7	SCA7_DATA[7:0]								0b 11111111
17h	SCA8	SCA8_DATA[7:0]								0b 11111111
18h	SCA9	SCA9_DATA[7:0]								0b 11111111
19h	SCA10	SCA10_DATA[7:0]								0b 11111111
1Ah	SCA11	SCA11_DATA[7:0]								0b 11111111
1Bh	SCA12	SCA12_DATA[7:0]								0b 11111111
20h	PWM1_H	PWM1_DATA[9:2]								0b 00000000
21h	PWM2_H	PWM2_DATA[9:2]								0b 00000000
22h	PWM3_H	PWM3_DATA[9:2]								0b 00000000
23h	PWM4_H	PWM4_DATA[9:2]								0b 00000000
24h	PWM1/2/3/4_L	PWM4_DATA[1:0]		PWM3_DATA[1:0]		PWM2_DATA[1:0]		PWM1_DATA[1:0]		0b 00000000
25h	PWM5_H	PWM5_DATA[9:2]								0b 00000000
26h	PWM6_H	PWM6_DATA[9:2]								0b 00000000
27h	PWM7_H	PWM7_DATA[9:2]								0b 00000000
28h	PWM8_H	PWM8_DATA[9:2]								0b 00000000
29h	PWM5/6/7/8_L	PWM8_DATA[1:0]		PWM7_DATA[1:0]		PWM6_DATA[1:0]		PWM5_DATA[1:0]		0b 00000000
2Ah	PWM9_H	PWM9_DATA[9:2]								0b 00000000
2Bh	PWM10_H	PWM10_DATA[9:2]								0b 00000000
2Ch	PWM11_H	PWM11_DATA[9:2]								0b 00000000
2Dh	PWM12_H	PWM12_DATA[9:2]								0b 00000000

ADDR	REG NAME	D7	D6	D5	D4	D3	D2	D1	D0	DEFAULT
2Eh	PWM9/10/11/12_L	PWM12_DATA[1:0]		PWM11_DATA[1:0]		PWM10_DATA[1:0]		PWM9_DATA[1:0]		0b 00000000
30h	LED1_SLS	RSVD			LED1_SLSTH[4:0]					0b 00000000
31h	LED2_SLS	RSVD			LED2_SLSTH[4:0]					0b 00000000
32h	LED3_SLS	RSVD			LED3_SLSTH[4:0]					0b 00000000
33h	LED4_SLS	RSVD			LED4_SLSTH[4:0]					0b 00000000
34h	LED5_SLS	RSVD			LED5_SLSTH[4:0]					0b 00000000
35h	LED6_SLS	RSVD			LED6_SLSTH[4:0]					0b 00000000
36h	LED7_SLS	RSVD			LED7_SLSTH[4:0]					0b 00000000
37h	LED8_SLS	RSVD			LED8_SLSTH[4:0]					0b 00000000
38h	LED9_SLS	RSVD			LED9_SLSTH[4:0]					0b 00000000
39h	LED10_SLS	RSVD			LED10_SLSTH[4:0]					0b 00000000
3Ah	LED11_SLS	RSVD			LED11_SLSTH[4:0]					0b 00000000
3Bh	LED12_SLS	RSVD			LED12_SLSTH[4:0]					0b 00000000
40h	SYSCFG	RSVD		ACKEN	RSVD				PWR	0b 00000000
41h	CMWTAP	RSVD					CMWTAP [2:0]			0b 00000100
42h	Reserved	-								-
43h	SSCCFG	SSCEN	RSVD					SSF[1:0]		0b 00000000
44h	Reserved	-								-
45h	Reserved	-								-
46h	PWMTICK	PTBASE [1:0]		PTCNT [5:0]						0b 00000000
47h	PRESCALE	PRESCALE [7:0]								0b 00000000
48h	Reserved	-								-
50h	FLT_DET_EN	RSVD	OVE	RSVD	SLSDE	RSVD	SDE	RSVD	ODE	0b 11001111
51h	FLT_CONFIG	RSVD	SLSHCR	FT[3:0]				OFA[1:0]		0b 11001111
52h	SHORT_FLTL	SHORT_FLT(8:1)								0b 00000000
53h	SHORT_FLTH	RSVD				SHORT_FLT(12:9)				0b 00000000
54h	OPEN_FLTL	OPEN_FLT(8:1)								0b 00000000
55h	OPEN_FLTH	RSVD				OPEN_FLT(12:9)				0b 00000000
56h	SLS_FLTL	SLS_FLT(8:1)								0b 00000000
57h	SLS_FLTH	RSVD				SLS_FLT(12:9)				0b 00000000
58h	OVP_FLTL	OVP_FLT(8:1)								0b 00000000
59h	OVP_FLTH	RSVD				OVP_FLT(12:9)				0b 00000000
5Ah	FLT_TYPE_L	TF	CRCF	ISETSF	CMWF	TSDF	SLSF	SHORTF	OPENF	0b 00000000
5Bh	FLT_TYPE_H	RSVD						LPBF	OVPF	0b 00000000
5Ch	CERRCNT	CERRCNT [7:0]								0b 00000000
60h	CHSEL_L	CHSEL[7:0]								0b 00000000
61h	CHSEL_H	RSVD	CHSEL[14:8]							0b 00000000
62h	ADCCFG	RSVD			ADCEN	RSVD		ADCSH[1:0]		0b 00100010
63h	ADCCTL	ADCCYC_F	ADCCYC_T[1:0]		LOOP	SADC	ADCRST	RSVD		0b 00000000
64h	Reserved	-								-
65h	ADC_VREF_L	RSVD						ADC_VREF[1:0]		0b 00000000
66h	ADC_VREF_H	ADC_VREF[9:2]								0b 00000000
67h	ADC_VPTAT_L	RSVD						ADC_VPTAT[1:0]		0b 00000000

ADDR	REG NAME	D7	D6	D5	D4	D3	D2	D1	D0	DEFAULT
68h	ADC_VPTAT_H	ADC_VPTAT[9:2]								0b 00000000
69h	ADC_VDD_L	RSVD						ADC_VDD[1:0]		0b 00000000
6Ah	ADC_VDD_H	ADC_VDD[9:2]								0b 00000000
6Bh	Reserved	-								-
6Ch	Reserved	-								-
6Dh	Reserved	-								-
6Eh	Reserved	-								-
6Fh	ADC_VOUT1_H	ADC_VOUT1[9:2]								0b 00000000
70h	ADC_VOUT2_H	ADC_VOUT2[9:2]								0b 00000000
71h	ADC_VOUT3_H	ADC_VOUT3[9:2]								0b 00000000
72h	ADC_VOUT4_H	ADC_VOUT4[9:2]								0b 00000000
73h	ADC_VOUT1_2_3_4_L	ADC_VOUT4[1:0]		ADC_VOUT3[1:0]		ADC_VOUT2[1:0]		ADC_VOUT1[1:0]		0b 00000000
74h	ADC_VOUT5_H	ADC_VOUT5[9:2]								0b 00000000
75h	ADC_VOUT6_H	ADC_VOUT6[9:2]								0b 00000000
76h	ADC_VOUT7_H	ADC_VOUT7[9:2]								0b 00000000
77h	ADC_VOUT8_H	ADC_VOUT8[9:2]								0b 00000000
78h	ADC_VOUT5_6_7_8_L	ADC_VOUT8[1:0]		ADC_VOUT7[1:0]		ADC_VOUT6[1:0]		ADC_VOUT5[1:0]		0b 00000000
79h	ADC_VOUT9_H	ADC_VOUT9[9:2]								0b 00000000
7Ah	ADC_VOUT10_H	ADC_VOUT10[9:2]								0b 00000000
7Bh	ADC_VOUT11_H	ADC_VOUT11[9:2]								0b 00000000
7Ch	ADC_VOUT12_H	ADC_VOUT12[9:2]								0b 00000000
7Dh	ADC_VOUT9_10_11_12_L	ADC_VOUT12[1:0]		ADC_VOUT11[1:0]		ADC_VOUT10[1:0]		ADC_VOUT9[1:0]		0b 00000000
F0h	BSTSTA	RSVD						FAIL	FINISH	0b 00000000
F1h	VFYCTL	VFYCHSEL[3:0]				RSVD			VFYEN	0b 00001000
F2h	VFYCFG	RSVD		VFYRDY	TOLERANCE[4:0]					0b 00011111
F3h	DUTYF_L	DUTYFLT(8:1)								0b 00000000
F4h	DUTYF_H	RSVD				DUTYFLT(12:9)				0b 00000000
F5h	PWMDUTY_H	PWMDUTY[9:2]								0b 00000000
F6h	PWMDUTY_L	RSVD						PWMDUTY[1:0]		0b 00000000

Note 6: **"**RSVD" means "Reserved".

11.2 REGISTERS DEFINITION

Configuration Register – Read/Write

ADDR	REG NAME	D7	D6	D5	D4	D3:D0	DEFAULT
00h	CONFIG	TST_EN	RSVD	CM	PFS	RSVD	0b 00000000

TST_EN Thermal shunt mechanism enable
0 Disable
1 Enable

CM Current multiplier
0 Output current range of 10~75mA
1 Output current range of 1.5~10mA
When the target current is lower than 10mA, setting CM bit to "1" can get better current accuracy.

PFS PWM frequency setting for thermal shunt mechanism
0 High PWM frequency (PWM frequency > 2kHz)
1 Low PWM frequency (PWM frequency < 2kHz)
To get better thermal shunt effect during PWM dimming, properly set the PFS bit according to the PWM frequency selection.

Global Current Control Register – Read/Write

ADDR	REG NAME	D7:D6	D5:D0	DEFAULT
01h	GC_CTRL	RSVD	GCC[5:0]	0b 00111111

GCCx Simultaneously adjusts the output current of all channels by 32-step. Refer to the "OUTPUT CURRENT SETTING" section for more details.

Fault UVLO Setting Register – Read/Write

ADDR	REG NAME	D7:D5	D4:D0	DEFAULT
02h	FLT_UV	RSVD	FLT_UV[4:0]	0b 00000010

FLT_UVx Set UVLO threshold V_{FLT_UV} for the LED open fault detection and single LED short fault detection to prevent false fault triggering due to insufficient power supply voltage:

$$V_{FLT\_UV}(V) = \sum_{n=0}^{4} D[n] \cdot 2^n + 6 \qquad (21)$$

If the thermal shunt mechanism is implemented:

$$V_{FLT\_UV}(V) \geq R_{SHUNT} \times \frac{1}{24} \times \sum_{x=1}^{12} I_{OUTx} + V_{OUT\_MAX} + 1.5 \qquad (22)$$

Refer to the "THERMAL SHUNT TOPOLOGY" section for more details.

If the thermal shunt mechanism is not implemented:

$$V_{FLT\_UV}(V) \geq V_{OUT\_MAX} + 1.5 \qquad (23)$$

Temperature Sensor Setting Register – Read/Write

ADDR	REG NAME	D7	D6	D5:D4	D3:D2	D1:D0	DEFAULT
03h	TEMP_SEN	TRE	TRRE	RSVD	TROF[1:0]	TS[1:0]	0b 00000000

TRE Thermal shutdown FAULTB pin reporting enable
0 Do not report
1 Report (FAULTB pin pulls low)

TRRE Thermal roll-off FAULTB pin reporting enable
0 Do not report
1 Report (FAULTB pin pulls low)

TROF Percentage of output current before thermal shutdown happens
00 100% (Default)
01 75%
10 55%
11 30%

TS Thermal roll-off start temperature point
00 140°C (Default)
01 120°C
10 100°C
11 90°C

Phase Control Register – Read/Write

ADDR	REG NAME	D7	D6	D5	D4	D3	D2	D1	D0	DEFAULT
04h	PHASE_CTRL	RSVD	PS6	PS5	PS4	PS3	PS2	PS1	PDE	0b 00000001

PDE PWM Phase delay enable
0 Disable
1 Enable (1/6 PWM cycle time delay)

PSx PWM clock phase shift enable (PS1 is for OUT1 &OUT2, PS2 is for OUT3 & OUT4…)
0 Disable. Both channels PWM counting from beginning of PWM cycle
1 Enable. Odd number channel PWM duty cycle counts from beginning of PWM cycle while even number channel PWM duty cycle reversely counts from ending of PWM cycle

The configuration of this register must be updated by the “Update Command”.

DC_PWM Select Register – Read/Write

ADDR	REG NAME	D7:D1	D0	DEFAULT
05h	DC_PWM_SEL	RSVD	DC_PWM	0b 00000000

DC_PWM DC or PWM output select for all outputs
0 PWM dimming. PWM duty cycle is determined by PWM registers 20h~2Eh
1 DC output. PWM dimming is disabled, and all outputs are DC current (I_{OUTx})

The configuration of this register must be updated by the “Update Command”.

Fail-safe Mode 1 Default Registers – Read/Write

ADDR	REG NAME	D7	D6	D5	D4	D3	D2	D1	D0	DEFAULT
07h	DEFGCC	RSVD	DEFDC_PWM	DEFGCC[5:0]						0b 00000000
08h	DEFLED_L	DEFLED(8:1)								0b 00000000
09h	DEFLED_H	RSVD				DEFLED(12:9)				0b 00000000
0Ah	DEFPWM_G1	DEFPWM2[3:0]				DEFPWM1[3:0]				0b 00000000
0Bh	DEFPWM_G2	DEFPWM4[3:0]				DEFPWM3[3:0]				0b 00000000
0Ch	DEFPWM_G3	DEFPWM6[3:0]				DEFPWM5[3:0]				0b 00000000
0Dh	DEFPWM_G4	DEFPWM8[3:0]				DEFPWM7[3:0]				0b 00000000
0Eh	DEFPWM_G5	DEFPWM10[3:0]				DEFPWM9[3:0]				0b 00000000
0Fh	DEFPWM_G6	DEFPWM12[3:0]				DEFPWM11[3:0]				0b 00000000

When $V_{TH1\_AD/FS}<V_{FSMD}<V_{TH2\_AD/FS}$ (or R_{FSMD}=30kΩ) and the watchdog times out, the device will enter fail-safe Mode 1. In the case, the outputs will be determined by these Default Registers (07h~0Fh).

DEFDC_PWM DC or PWM output select for all outputs
0 PWM dimming. PWM duty cycle is determined by DEFPWM registers 0Ah~0Fh
1 DC output. PWM dimming is disabled, and all outputs are DC current ($I_{OUTx\_DEF} = I_{OUT\_FU} \times \frac{DEFGCC}{32}$).

DEFGCCx Simultaneously adjusts the output current of all channels by 32-step.

If DEFGCC[5:0] ≤ 31 (“01 1111”),

$$DEFGCC = \sum_{n=0}^{5} D[n] \cdot 2^n \qquad (24)$$

If DEFGCC[5:0] ≥ 32 (“10 0000”), DEFGCC=32.

DEFLEDx Individually Enable/disable OUT1~OUT12
0 Disable
1 Enable (the corresponding DEFPWMx register must not be “0x00”)

DEFPWMx Individual 16-step PWM duty cycle setting to OUT1~OUT12

The duty cycle $D_{DEFPWMx}$ can be computed by:

$$D_{DEFPWMx} = \frac{\sum_{n=0}^{3} D[n] \cdot 2^n}{16} \quad (25)$$

So, the output current of each channel will be:

$$I_{OUTx\_DEFPWM} = I_{OUT\_FU} \times \frac{DEFGCC}{32} \times D_{DEFPWMx} \quad (26)$$

Scaling Registers – Read/Write

ADDR	REG NAME	D7:D0	DEFAULT
10h	SCA1	SCA1_DATA[7:0]	0b 11111111
11h	SCA2	SCA2_DATA[7:0]	0b 11111111
12h	SCA3	SCA3_DATA[7:0]	0b 11111111
13h	SCA4	SCA4_DATA[7:0]	0b 11111111
14h	SCA5	SCA5_DATA[7:0]	0b 11111111
15h	SCA6	SCA6_DATA[7:0]	0b 11111111
16h	SCA7	SCA7_DATA[7:0]	0b 11111111
17h	SCA8	SCA8_DATA[7:0]	0b 11111111
18h	SCA9	SCA9_DATA[7:0]	0b 11111111
19h	SCA10	SCA10_DATA[7:0]	0b 11111111
1Ah	SCA11	SCA11_DATA[7:0]	0b 11111111
1Bh	SCA12	SCA12_DATA[7:0]	0b 11111111

SCAx_DATAx Individual 8-bit DC output current adjustment to OUT1~OUT12. Refer to the “OUTPUT CURRENT SETTING” section for more details.

The configuration of these registers must be updated by the “Update Command”.

PWM Registers – Read/Write

ADDR	REG NAME	D7	D6	D5	D4	D3	D2	D1	D0	DEFAULT
20h	PWM1_H	PWM1_DATA[9:2]								0b 00000000
21h	PWM2_H	PWM2_DATA[9:2]								0b 00000000
22h	PWM3_H	PWM3_DATA[9:2]								0b 00000000
23h	PWM4_H	PWM4_DATA[9:2]								0b 00000000
24h	PWM1~4_L	PWM4_DATA[1:0]		PWM3_DATA[1:0]		PWM2_DATA[1:0]		PWM1_DATA[1:0]		0b 00000000
25h	PWM5_H	PWM5_DATA[9:2]								0b 00000000
26h	PWM6_H	PWM6_DATA[9:2]								0b 00000000
27h	PWM7_H	PWM7_DATA[9:2]								0b 00000000
28h	PWM8_H	PWM8_DATA[9:2]								0b 00000000
29h	PWM5~8_L	PWM8_DATA[1:0]		PWM7_DATA[1:0]		PWM6_DATA[1:0]		PWM5_DATA[1:0]		0b 00000000
2Ah	PWM9_H	PWM9_DATA[9:2]								0b 00000000
2Bh	PWM10_H	PWM10_DATA[9:2]								0b 00000000
2Ch	PWM11_H	PWM11_DATA[9:2]								0b 00000000
2Dh	PWM12_H	PWM12_DATA[9:2]								0b 00000000
2Eh	PWM9~12_L	PWM12_DATA[1:0]		PWM11_DATA[1:0]		PWM10_DATA[1:0]		PWM9_DATA[1:0]		0b 00000000

PWMx_DATAx Each output has individual 10-bit to modulate the PWM duty cycle by 1024-step. Refer to the "PWM DIMMING" section for more details.

The configuration of these registers must be updated by the "Update Command".

Single LED Short Detect Threshold Setting Registers – Read/Write

ADDR	REG NAME	D7:D5	D4:D0	DEFAULT
30h	LED1_SLS	RSVD	LED1_SLSTH[4:0]	0b 00000000
31h	LED2_SLS	RSVD	LED2_SLSTH[4:0]	0b 00000000
32h	LED3_SLS	RSVD	LED3_SLSTH[4:0]	0b 00000000
33h	LED4_SLS	RSVD	LED4_SLSTH[4:0]	0b 00000000
34h	LED5_SLS	RSVD	LED5_SLSTH[4:0]	0b 00000000
35h	LED6_SLS	RSVD	LED6_SLSTH[4:0]	0b 00000000
36h	LED7_SLS	RSVD	LED7_SLSTH[4:0]	0b 00000000
37h	LED8_SLS	RSVD	LED8_SLSTH[4:0]	0b 00000000
38h	LED9_SLS	RSVD	LED9_SLSTH[4:0]	0b 00000000
39h	LED10_SLS	RSVD	LED10_SLSTH[4:0]	0b 00000000
3Ah	LED11_SLS	RSVD	LED11_SLSTH[4:0]	0b 00000000
3Bh	LED12_SLS	RSVD	LED12_SLSTH[4:0]	0b 00000000

LEDx_SLSTHx Programe the single LED short detect threshold V_{SLSTH}:

$$V_{SLSTH}(V) = \frac{40}{32} \times (\sum_{n=0}^{4} D[n] \cdot 2^n + 1) \qquad (27)$$

The maximum V_{SLSTH} is 30V (Typ.).

Refer to the “SINGLE LED SHORT DETECTION” section for more details.

To achieve proper single LED short detection and avoid false triggering, the V_{SLSTH} should be programmed according to the minimum and maximum of the LED forward voltage:

$$(N-1) \times V_{F\_MAX} < V_{SLSTH} < N \times V_{F\_MIN} \qquad (28)$$

Where, N is the number of LEDs in the string. V_{F_MAX} and V_{F_MIN} are the maximum and minimum forward voltage of a single LED.

System Configuration Register – Read/Write

ADDR	REG NAME	D7:D6	D5	D4:D1	D0	DEFAULT
40h	SYSCFG	RSVD	ACKEN	RSVD	PWR	0b 00000000

ACKEN Acknowledge enable (IS32LT3131A/B only)
0 No acknowledge is transmitted following successfully received writes
1 Acknowledge (0x7F) is transmitted following successfully received writes

PWR This bit is reset to 0 upon power-up (released from UVLO). It may be written to a “1” by the host MCU. Reading this bit allows the host MCU to detect if there has been a power cycle. Note that the Registers Reset Command cannot reset this bit.
0 A power cycle has occurred since the last write to a “1”
1 No power cycle has occurred since the last write to a “1”

Communications Watchdog Timer Tap Point Register – Read/Write

ADDR	REG NAME	D7:D3	D2:D0	DEFAULT
41h	CMWTAP	RSVD	CMWTAP [2:0]	0b 00000100

CMWTAPx This 3-bit value selects the tap point (i.e., bit number, starting from 0) on the 25-bit communications watchdog timer to establish the timeout condition. The system clock frequency is 32Mhz (Typ.).

CMWTAP [2:0]	Watchdog Timeout Time
7	2^25 SYSCLK (typical 1048.6ms)
6	2^24 SYSCLK (typical 524.3ms)
5	2^23 SYSCLK (typical 262.1ms)
4 (Default)	2^22 SYSCLK (typical 131ms)
3	2^21 SYSCLK (typical 65.5ms)
2	2^20 SYSCLK (typical 32.8ms)
1	2^19 SYSCLK (typical 16.4ms)
0	2^18 SYSCLK (typical 8.2ms)

If the fail-safe mode is enabled ($V_{TH1\_AD/FS}$< V_{FSMD}< 5V), the host MCU must send out first command within 2^22 SYSCLK upon power up. Otherwise, the device will enter fail-safe mode.

Spread Spectrum Register – Read/Write

ADDR	REG NAME	D7	D6:D2	D1:D0	DEFAULT
43h	SSCCFG	SSCEN	RSVD	SSF[1:0]	0b 00000000

SSCEN Spread Spectrum Enable
0 Disable
1 Enable

SSFx Spread Spectrum Frequency
00 125Hz (default)
01 250Hz
10 500Hz
11 1kHz

PWM Frequency Setting Registers – Read/Write

ADDR	REG NAME	D7:D6	D5:D0	DEFAULT
46h	PWMTICK	PTBASE [1:0]	PTCNT [5:0]	0b 00000000
47h	PRESCALE	PRESCALE [7:0]		0b 00000000

PTBASEx PWM Base Frequency Select
00 31.25kHz (Default)
01 488.3Hz
10 244.1Hz
11 122Hz

PTCNTx/PRESCALEx PWM Frequency Setting

The PWM frequency is calculated by following equation:

$$f_{PWM} = \frac{PTBASE}{PTCNT+1} \times \frac{PRESCALE}{255} \quad (29)$$

Where,

$$PTCNT = \sum_{n=0}^{5} D[n] \cdot 2^n \quad (30)$$

And, if PRESCALE[7:0] > 0 (“0b 0000 0000”),

$$PRESCALE = \sum_{n=0}^{7} D[n] \cdot 2^n \quad (31)$$

If PRESCALE[7:0] = 0 (“0b 0000 0000”), PRESCALE=255.

For example: assume PTBASE[1:0] = 0x00, PTCNT[5:0] = 0x00 and PRESCALE[7:0] = 0x08. Then the PWM frequency is:

$$f_{PWM} = \frac{31.25kHz}{1} \times \frac{8}{256} = 977Hz \qquad (32)$$

Fault Detection Enable Register – Read/Write

ADDR	REG NAME	D7	D6	D5	D4	D3	D2	D1	D0	DEFAULT
50h	FLT_DET_EN	RSVD	OVE	RSVD	SLSDE	RSVD	SDE	RSVD	ODE	0b 11001111

OVE Overvoltage Detect Enable
0 Disabled
1 Enabled

SLSDE Single LED Short Detect Enable
0 Disabled
1 Enabled

SDE Short Detect Enable
0 Disabled
1 Enabled

ODE Open Detect Enable
0 Disabled
1 Enabled

Fault Configuration Register – Read/Write

ADDR	REG NAME	D7	D6	D5:D2	D1:D0	DEFAULT
51h	FLT_CONFIG	RSVD	SLSHCR	FT[3:0]	OFA[1:0]	0b 11001111

SLSHCR Single LED short output current reduction of the faulty channel
0 No reduction
1 Faulty channel output current reduced to 4mA (Typ.)

FTx FAULTB pin action delay time setting

0000	32μs	1000	7.8125ms
0001	64μs	1001	15.625ms
0010	128μs	1010	31.25ms
0011	256μs (Default)	1011	62.5ms
0100	512μs	1100	0.125s
0101	1.024ms	1101	0.25s
0110	2.048ms	1110	0.5s
0111	4.096ms	1111	1s

OFAx “One Fail Others On” or “One Fail All Fail” fault action mode setting
0X “One Fail All Fail” (single LED short latches all outputs off)
10 “One Fail All Fail” (single LED short auto recover)
11 “One Fail Others On”

Fault Flag Registers (52h~59h – Read only, 5Ah and 5Bh – Read/Write)

ADDR	REG NAME	D7	D6	D5	D4	D3	D2	D1	D0	DEFAULT
52h	SHORT_FLTL	SHORT_FLT(8:1)								0b 00000000
53h	SHORT_FLTH	RSVD				SHORT_FLT(12:9)				0b 00000000
54h	OPEN_FLTL	OPEN_FLT(8:1)								0b 00000000
55h	OPEN_FLTH	RSVD				OPEN_FLT(12:9)				0b 00000000
56h	SLS_FLTL	SLS_FLT(8:1)								0b 00000000
57h	SLS_FLTH	RSVD				SLS_FLT(12:9)				0b 00000000
58h	OVP_FLTL	OVP_FLT(8:1)								0b 00000000
59h	OVP_FLTH	RSVD				OVP_FLT(12:9)				0b 00000000
5Ah	FAULT_TYPE_L	TF	CRCF	ISETSF	CMWF	TSDF	SLSF	SHORTF	OPENF	0b 00000000
5Bh	FAULT_TYPE_H	RSVD						LPBF	OVPF	0b 00000000

SHORT_FLTx LED string short fault flag for each OUT1~OUT12
0 No LED string shorted
1 LED string shorted

OPEN_FLTx LED string open fault flag for each OUT1~OUT12
0 No LED string open
1 LED string open

SLS_FLTx Single LED short fault flag for each OUT1~OUT12
0 No single LED shorted
1 Single LED shorted

OVP_FLTx Overvoltage fault flag for each OUT1~OUT12
0 No overvoltage
1 Overvoltage

TF Thermal roll-off fault flag
0 No thermal roll-off
1 Thermal roll-off

ISETSF ISET pin short fault flag
0 No ISET pin shorted
1 ISET pin Shorted

CRCF Interface communication CRC fault flag
0 No CRC Failure
1 CRC Failure

CMWF Communication watchdog timeout fault flag
0 No watchdog timeout
1 Watchdog timeout

TSDF Thermal shutdown fault flag
0 No thermal shutdown
1 Thermal shutdown

SLSF Single LED short fault flag. Any output occurs single LED short, this bit will set to “1”.
0 No single LED shorted
1 Single LED shorted

SHORTF LED string short fault flag. Any output occurs LED string short, this bit will set to “1”.
0 No LED string shorted
1 LED string shorted

OPENF LED string open fault flag. Any output occurs LED string open, this bit will set to “1”.
0 No LED string open
1 LED string open

OVPF Overvoltage fault flag. Any output occurs overvoltage, this bit will set to “1”.
0 No overvoltage
1 Overvoltage

LPBF Loopback fault flag. Any output occurs loopback verification failure, this bit will set to “1”.
0 No loopback verification failure
1 Loopback verification failure

The FLT_TYPE_L and FLT_TYPE_H registers are latched. Even though the fault conditions are removed, they cannot automatically reset to “0” but must be cleared by the host MCU writing it back to “0”.

CRC Error Count Register – Read/Write

ADDR	REG NAME	D7:D0	DEFAULT
5Ch	CERRCNT	CERRCNT [7:0]	0b 00000000

CERRCNTx CRC error count register

This register value is incremented each time a CRC error is received. This register may be read by the MCU and then written back to “0” to clear the count. The CERRCNT value saturates at “0xFF”; it does not wrap back to 0 when it reaches “0xFF”. The CERRCNT register is not automatically cleared when a BUS reset command is received. It must be cleared manually by writing it back to “0”. Note that the CERRCNT register can be written to any 8-bit value. This is intended for diagnostic purposes.

ADC Input Channels Select Registers – Read/Write

ADDR	REG NAME	D7	D6	D5	D4	D3	D2	D1	D0	DEFAULT
60h	CHSEL_L	CHSEL[7:0]								0b 00000000
61h	CHSEL_H	RSVD	CHSEL[14:8]							0b 00000000

CHSELx ADC sampling channels select.
0 Not selected
1 Selected

The ADC has fifteen multiplexed input channels (CH0~CH14) which can be individually selected by the CHSEL[0]~CHSEL[14] bits. As below table. Multiple channels can be selected which will be periodically measured in turn.

Input Channel Select Bit	Channel No.	Input Signal	Setting
CHSEL[0]	CH0	V_{REF} (1V)	"0" = Not Selected "1" = Selected
CHSEL[1]	CH1	V_{PTAT}	
CHSEL[2]	CH2	V_{DD}/4	
CHSEL[3]	CH3	V_{OUT1}/13	
CHSEL[4]	CH4	V_{OUT2}/13	
…	…	…	
CHSEL[14]	CH14	V_{OUT12}/13	

ADC Configuration Register – Read/Write

ADDR	REG NAME	D7:D5	D4	D3:D2	D1:D0	DEFAULT
62h	ADCCFG	RSVD	ADCEN	RSVD	ADCSH[1:0]	0b 00100010

ADCEN ADC enable

0 Disabled

1 Enabled

ADCSHx ADC sample/hold time setting

00 Invalid

01 ADC sample/hold time = 2μs

10 ADC sample/hold time = 4μs (Default)

11 ADC sample/hold time = 8μs

ADC Control Register (D7 – Read only, D2~D6 – Read/Write)

ADDR	REG NAME	D7	D6:D5	D4	D3	D2	D1:D0	DEFAULT
63h	ADCCTL	ADCCYC_F	ADCCYC_T[1:0]	LOOP	SADC	ADCRST	RSVD	0b 00000000

ADCCYC_F ADC sampling finished flag

0 ADC sampling in progress, ADC result is not valid

1 ADC sampling finished, ADC result is valid reading for host MCU

ADCCYC_Tx ADC cycle sampling period

00 ADC Cycle sampling for 2 PWM cycles (Default)

01 ADC Cycle sampling for 4 PWM cycles

10 ADC Cycle sampling for 8 PWM cycles

11 ADC Cycle sampling for 16 PWM cycles

To get more stable and precise result, OUTx voltage is always sampled for multiple PWM cycles to calculate the average value.

LOOP ADC sampling mode

0 ADC single conversion

1 ADC continuous conversion

If the LOOP bit set to "0", all selected channels will be only measured once. If the LOOP bit is set to "1", the ADC will repeat the measurement of all selected channels all the time.

SADC Start ADC measurement
0 ADC measurement stops
1 ADC measurement starts
Please set ADCEN bit at first, then set SADC bit, otherwise ADC cannot measure voltage.

ADCRST Reset all ADC result registers (65h~6Ah, 6Fh~7Dh) to default value when ADC measurement starts
0 Not reset
1 Reset

ADC Internal Reference Voltage Result Registers – Read only

ADDR	REG NAME	D7:D2	D1:D0	DEFAULT
65h	ADC_VREF_L	RSVD	ADC_VREF[1:0]	0b 00000000
66h	ADC_VREF_H	ADC_VREF[9:2]		0b 00000000

ADC_VREFx The ADC result of the internal reference voltage.

$$V_{REF}(V) = \frac{\sum_{n=0}^{9} D[n]\cdot 2^n}{1024} \times V_{REFADC} \qquad (33)$$

Where, V_{REFADC} is the reference voltage of the ADC, typical 1.8V.

ADC PTAT Result Registers – Read only

ADDR	REG NAME	D7:D2	D1:D0	DEFAULT
67h	ADC_VPTAT_L	RSVD	ADC_VPTAT[1:0]	0b 00000000
68h	ADC_VPTAT_H	ADC_VPTAT[9:2]		0b 00000000

ADC_VPTATx The ADC result of internal PTAT voltage.

This result can be used to estimate the device junction temperature by following equation:

$$T_J(°C) = \frac{(\frac{\sum_{n=0}^{9} D[n]\cdot 2^n}{1024} \times V_{REFADC} - 1.065)}{0.0037} + 25 \qquad (34)$$

ADC 5V LDO Result Registers – Read only

ADDR	REG NAME	D7:D2	D1:D0	DEFAULT
69h	ADC_VDD_L	RSVD	ADC_VDD[1:0]	0b 00000000
6Ah	ADC_VDD_H	ADC_VDD[9:2]		0b 00000000

ADC_VDDx The ADC result of internal 5V LDO voltage.

This result can be used to calculate the 5V LDO voltage by following equation:

$$V_{V5}(V) = \frac{\sum_{n=0}^{9} D[n]\cdot 2^n}{1024} \times V_{REFADC} \times 4 \qquad (35)$$

ADC Output Voltage Result Registers – Read only

ADDR	REG NAME	D7	D6	D5	D4	D3	D2	D1	D0	DEFAULT
6Fh	ADC_VOUT1_H	ADC_VOUT1[9:2]								0b 00000000
70h	ADC_VOUT2_H	ADC_VOUT2[9:2]								0b 00000000
71h	ADC_VOUT3_H	ADC_VOUT3[9:2]								0b 00000000
72h	ADC_VOUT4_H	ADC_VOUT4[9:2]								0b 00000000
73h	ADC_VOUT1~4_L	ADC_VOUT4[1:0]		ADC_VOUT3[1:0]		ADC_VOUT2[1:0]		ADC_VOUT1[1:0]		0b 00000000
74h	ADC_VOUT5_H	ADC_VOUT5[9:2]								0b 00000000
75h	ADC_VOUT6_H	ADC_VOUT6[9:2]								0b 00000000
76h	ADC_VOUT7_H	ADC_VOUT7[9:2]								0b 00000000
77h	ADC_VOUT8_H	ADC_VOUT8[9:2]								0b 00000000
78h	ADC_VOUT5~8_L	ADC_VOUT8[1:0]		ADC_VOUT7[1:0]		ADC_VOUT6[1:0]		ADC_VOUT5[1:0]		0b 00000000
79h	ADC_VOUT9_H	ADC_VOUT9[9:2]								0b 00000000
7Ah	ADC_VOUT10_H	ADC_VOUT10[9:2]								0b 00000000
7Bh	ADC_VOUT11_H	ADC_VOUT11[9:2]								0b 00000000
7Ch	ADC_VOUT12_H	ADC_VOUT12[9:2]								0b 00000000
7Dh	ADC_VOUT9~12_L	ADC_VOUT12[1:0]		ADC_VOUT11[1:0]		ADC_VOUT10[1:0]		ADC_VOUT9[1:0]		0b 00000000

ADC_VOUTx The ADC result of each OUTx pin voltage.

This result can be used to calculate the OUTx pin voltage by following equation:

$$V_{OUTx}(V) = \frac{\sum_{n=0}^{9} D[n] \cdot 2^n}{1024} \times V_{REFADC} \times 13 \qquad (36)$$

LBIST State Register – Read only

ADDR	REG NAME	D7:D2	D1	D0	DEFAULT
F0h	BSTSTA	RSVD	FAIL	FINISH	0b 00000000

FINISH LBIST state flag

0 LBIST in progress

1 LBIST finished

The device will do Logic Built-in Self-test (LBIST) upon UVLO being released. When it is finished, this flag will be set to “1”.

FAIL LBIST result

0 Pass

1 Failure

This result is only available after LBIST has finished, FINISH bit set to “1”. In case of LBIST result is failure, the device is defective and cannot be used.

Loopback Control Register – Read/Write

ADDR	REG NAME	D7:D4	D3:D1	D0	DEFAULT
F1h	VFYCTL	VFYCHSEL[3:0]	RSVD	VFYEN	0b 00001000

VFYEN Loopback verification function enable

0 Disabled

1 Enabled

VFYCHSELx Loopback verification channel select

The PWM duty cycle loopback verification circuit has twelve multiplexed inputs to monitor the PWM duty cycle of output channels. The twelve input channels (LPBCH1~LPBCH12) are respectively connected to each current source output stage. As below table. Only one channel can be verified at a time.

VFYCHSEL[3:0]	Input Channel Selected	Input Signal
0	LPBCH1	PWM signal from output stage of OUT1
1	LPBCH2	PWM signal from output stage of OUT2
2	LPBCH3	PWM signal from output stage of OUT3
…	…	…
11	LPBCH12	PWM signal from output stage of OUT12
12~15	Invalid	-

Loopback Configuration Register (D5 - Read only, D0~D4 - Read/Write)

ADDR	REG NAME	D7:D6	D5	D4:D0	DEFAULT
F2h	VFYCFG	RSVD	VFYRDY	TOLERANCE[4:0]	0b 00011111

VFYRDY Loopback verification state flag

0 Verification in progress

1 Verification finished

TOLERANCEx Loopback comparison tolerance setting

Preset PWM duty cycle deviation tolerance between the measurement result and the PWM duty cycle setting value in the PWM buffer.

$$Tolerance = \sum_{n=0}^{4} D[n] \cdot 2^n \times 4 + 3 \qquad (37)$$

Loopback Fault Flag Registers – Read only

ADDR	REG NAME	D7	D6	D5	D4	D3	D2	D1	D0	DEFAULT
F3h	DUTYF_L	DUTYFLT(8:1)								0b 00000000
F4h	DUTYF_H	RSVD				DUTYFLT(12:9)				0b 00000000

DUTYFLTx Loopback fault flag for each OUT1~OUT12

0 No loopback failure

1 Loopback failure

Loopback PWM Duty Cycle Registers – Read only

ADDR	REG NAME	D7	D6	D5	D4	D3	D2	D1	D0	DEFAULT
F5h	PWMDUTY_H	PWMDUTY[9:2]								0b 00000000
F6h	PWMDUTY_L	RSVD						PWMDUTY[1:0]		0b 00000000

PWMDUTYx The PWM duty cycle measure result of the selected channel.

12 CLASSIFICATION REFLOW PROFILES

Profile Feature	Pb-Free Assembly
Preheat & Soak Temperature min (Tsmin) Temperature max (Tsmax) Time (Tsmin to Tsmax) (ts)	150°C 200°C 60-120 seconds
Average ramp-up rate (Tsmax to Tp)	3°C/second max.
Liquidous temperature (TL) Time at liquidous (tL)	217°C 60-150 seconds
Peak package body temperature (Tp)*	Max 260°C
Time (tp)** within 5°C of the specified classification temperature (Tc)	Max 30 seconds
Average ramp-down rate (Tp to Tsmax)	6°C/second max.
Time 25°C to peak temperature	8 minutes max.

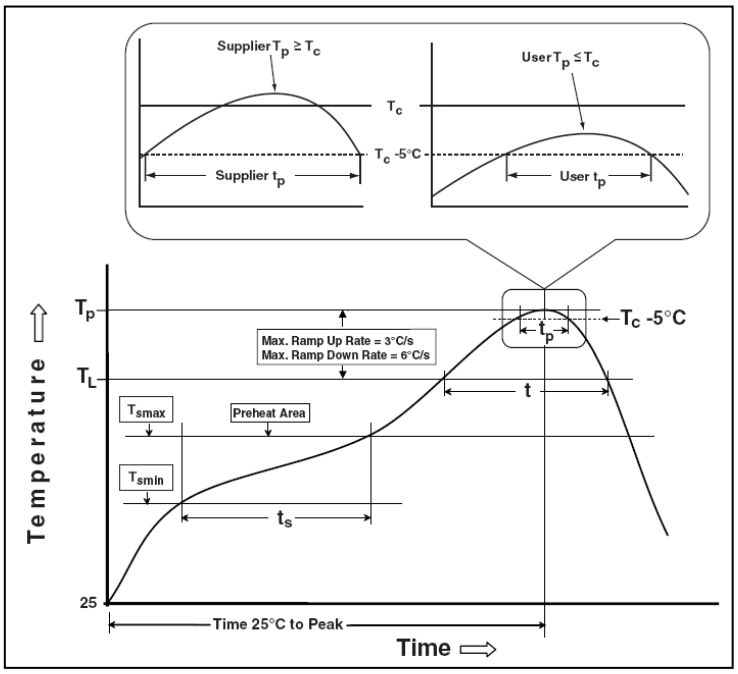
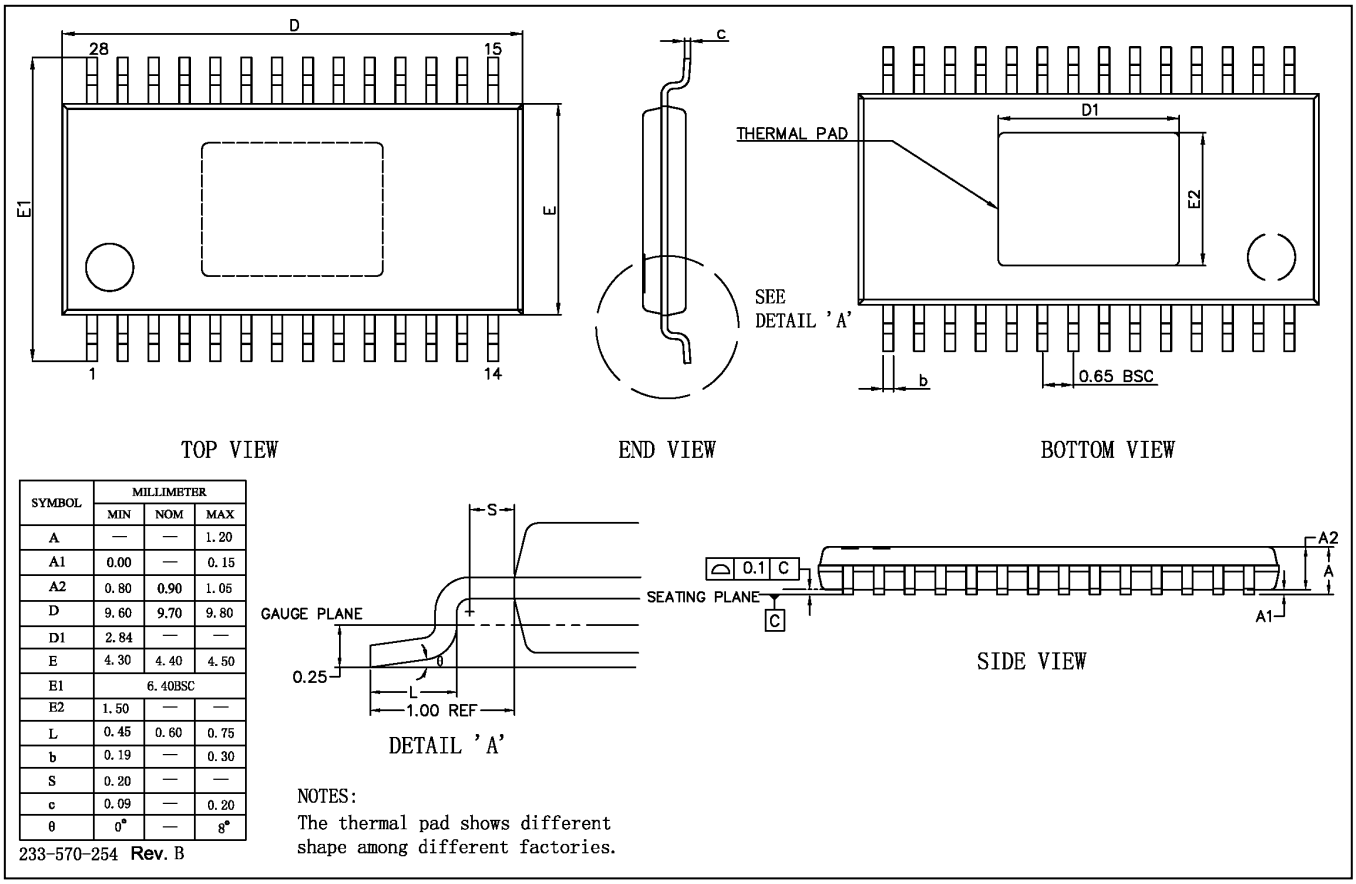


Figure 79 Classification Profile

13 PACKAGE INFORMATION

eTSSOP-28



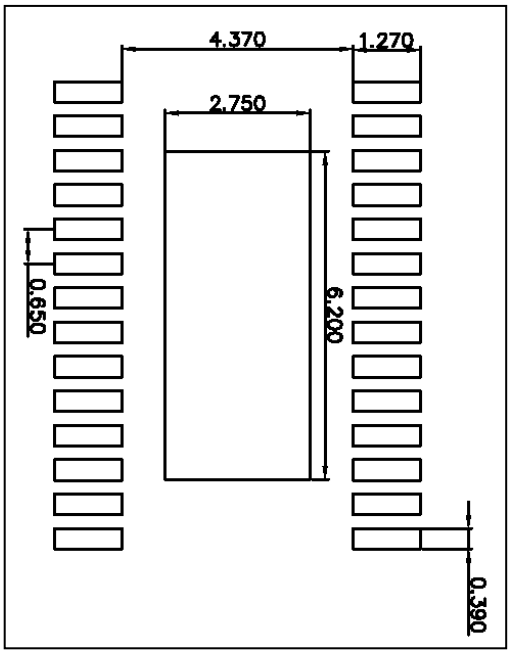
SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	—	—	1.20
A1	0.00	—	0.15
A2	0.80	0.90	1.05
D	9.60	9.70	9.80
D1	2.84	—	—
E	4.30	4.40	4.50
E1	6.40BSC		
E2	1.50	—	—
L	0.45	0.60	0.75
b	0.19	—	0.30
S	0.20	—	—
c	0.09	—	0.20
θ	0°	—	8°

233-570-254 Rev. B

NOTES:
The thermal pad shows different shape among different factories.

14 RECOMMENDED LAND PATTERN

eTSSOP-28



Note:

1. Land pattern complies to IPC-7351.
2. All dimensions in MM.
3. This document (including dimensions, notes & specs) is a recommendation based on typical circuit board manufacturing parameters. Since land pattern design depends on many factors unknown (eg. user's board manufacturing specs), user must determine suitability for use.

15 REVISION HISTORY

Revision	Detail Information	Date
A	Initial release	2023.11.13
B	Update to new Lumissil logo	2024.04.25