

## 2M x 16 (32-Mbit) PSEUDO STATIC RAM

MAY 2004

### FEATURES

- Access time: 70ns
- TTL compatible inputs and outputs; tri-state I/O
- Wide Power supply voltage: 2.2V to 3.6V
- CMOS Standby: 70µA (32-Mbit)
- Deep Power Down Standby: 5µA (32-Mbit)
- Deep Power-Down Mode: Data Invalid
- Page Operation Mode: Four Word Access
- Logic compatible with SRAM R/W ( $\overline{WE}$ ) pin.
- Industrial Temperature Range: -40°C to 85°C

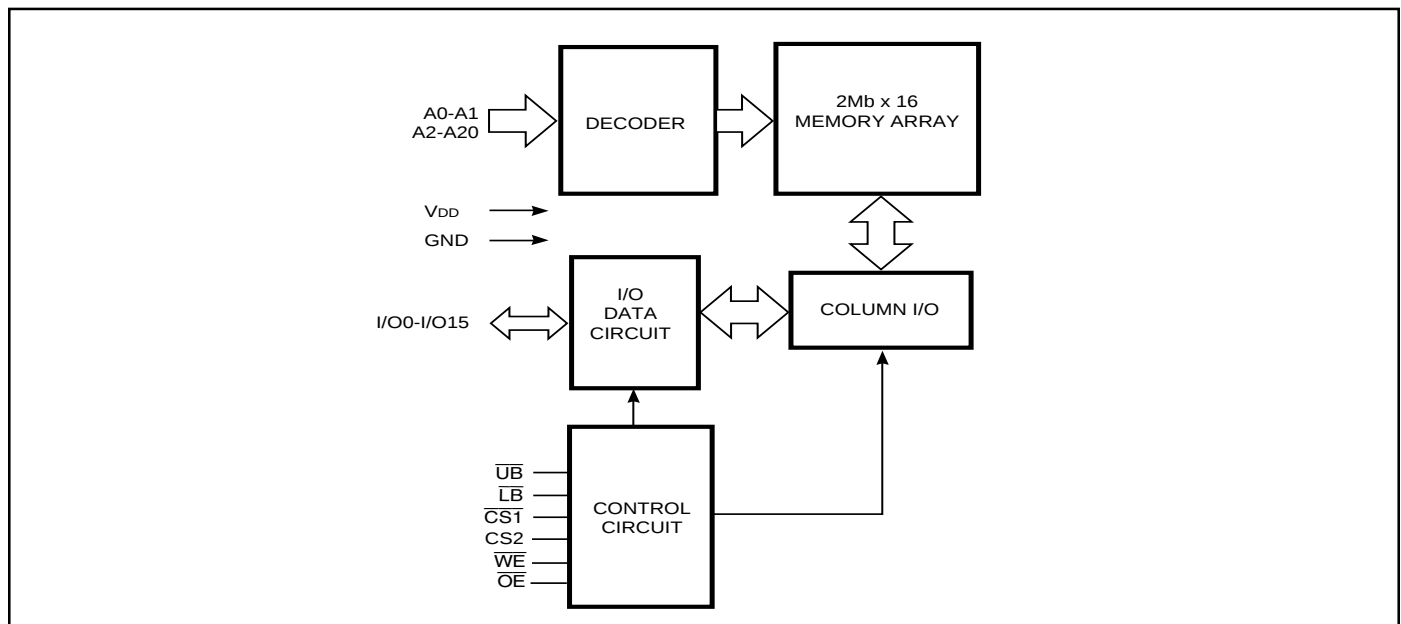
### DESCRIPTION

The ISSI IS32WV204816B is a high-performance CMOS Pseudo Static RAM, organized as 2Meg x 16 bits.

ISSI CMOS technology provides high density, high speed low power devices that features SRAM-like write timing. Data is written to memory cells on the rising edge of the  $\overline{WE}$  signal. With a page size of 4 words, the device has a page access operation. The device also supports deep power-down mode providing low-power standby.

The IS32WV204816B is packaged in a 48-pin mini-BGA (6mm x 8mm).

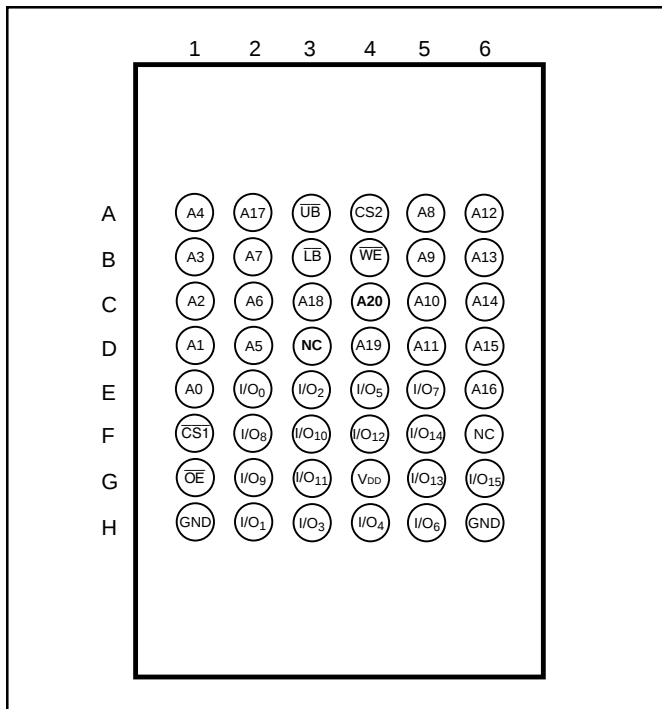
### FUNCTIONAL BLOCK DIAGRAM



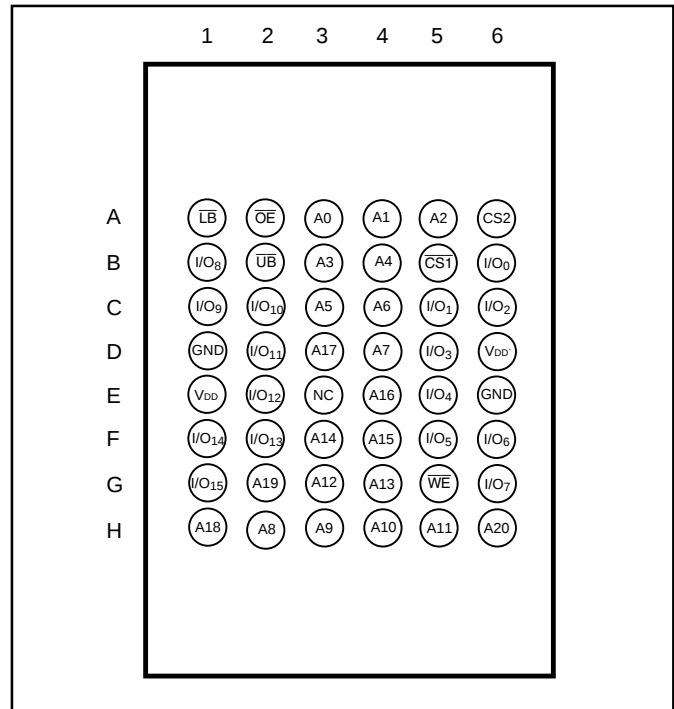
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## PIN CONFIGURATIONS

48-pin mini-BGA (M) (6mm x 8mm)



48-pin mini-BGA (B) (6mm x 8mm)



## PIN DESCRIPTIONS

|                                   |                                       |
|-----------------------------------|---------------------------------------|
| A0-A20                            | Address Inputs                        |
| A0-A1                             | Page Address Inputs                   |
| I/O0 to I/O15                     | Data Input/Outputs                    |
| $\overline{WE}$                   | Write Enable                          |
| $\overline{OE}$                   | Output Enable                         |
| $\overline{CS1}$                  | Chip Enable Input                     |
| CS2                               | Chip Select Input                     |
| $\overline{LB}$ , $\overline{UB}$ | Lower & Upper Data Byte Control Input |
| V <sub>DD</sub>                   | Power                                 |
| GND                               | Ground                                |
| NC                                | No Connection                         |

## TRUTH TABLE

| Function                | $\overline{CS1}$ | CS2 | $\overline{OE}$ | $\overline{WE}$ | $\overline{LB}$ | $\overline{UB}$ | ADD | I/O0 to I/O7       | I/O8 to I/O15      | Power            |
|-------------------------|------------------|-----|-----------------|-----------------|-----------------|-----------------|-----|--------------------|--------------------|------------------|
| Read: Word              | L                | H   | L               | H               | L               | L               | XX  | I/O <sub>OUT</sub> | I/O <sub>OUT</sub> | I <sub>CC1</sub> |
| Read: Lower Byte        | L                | H   | L               | H               | L               | H               | XX  | I/O <sub>OUT</sub> | HIGH-Z             | I <sub>CC1</sub> |
| Read: Upper Byte        | L                | H   | L               | H               | H               | L               | XX  | HIGH-Z             | I/O <sub>OUT</sub> | I <sub>CC1</sub> |
| Write: Word             | L                | H   | X               | L               | L               | L               | XX  | D <sub>IN</sub>    | D <sub>IN</sub>    | I <sub>CC1</sub> |
| Write: Lower            | L                | H   | X               | L               | L               | H               | XX  | D <sub>IN</sub>    | INVALID            | I <sub>CC1</sub> |
| Write: Upper            | L                | H   | X               | L               | H               | L               | XX  | INVALID            | D <sub>IN</sub>    | I <sub>CC1</sub> |
| Outputs Disabled        | L                | H   | H               | H               | X               | X               | XX  | HIGH-Z             | HIGH-Z             | I <sub>SB</sub>  |
| Standby                 | H                | H   | X               | X               | X               | X               | X   | HIGH-Z             | HIGH-Z             | I <sub>SB</sub>  |
| Deep Power-Down Standby | H                | L   | X               | X               | X               | X               | X   | HIGH-Z             | HIGH-Z             | I <sub>SB3</sub> |

L = V<sub>IL</sub>, H = V<sub>IH</sub>, X = V<sub>IL</sub> or V<sub>IH</sub>, High-Z = High-impedance. XX = At  $\overline{CS1}$  falling edge, all addresses (A2 to A20) are valid "IN".  
 Page address signals (A0 and A1) must be V<sub>IH</sub> or V<sub>IL</sub>, during entire cycle.

**ABSOLUTE MAXIMUM RATINGS<sup>(1)</sup>**

| Symbol           | Parameters                         | Rating                       | Unit |
|------------------|------------------------------------|------------------------------|------|
| V <sub>T</sub>   | Voltage on Any Pin Relative to GND | −0.2 to V <sub>DD</sub> +3.6 | V    |
| V <sub>DD</sub>  | Supply Voltage                     | −0.2 to V <sub>DD</sub> +3.6 | V    |
| I <sub>OUT</sub> | Output Current                     | 50                           | mA   |
| P <sub>D</sub>   | Power Dissipation                  | 0.6                          | W    |
| T <sub>STG</sub> | Storage Temperature                | −55 to +150                  | °C   |

**Note:**

1. Stress greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

**CAPACITANCE<sup>(1,2)</sup>**

| Symbol           | Parameter                                                                                                                                           | Max. | Unit |
|------------------|-----------------------------------------------------------------------------------------------------------------------------------------------------|------|------|
| C <sub>IN1</sub> | Input Capacitance: A0-A20                                                                                                                           | 10   | pF   |
| C <sub>IN2</sub> | Input Capacitance: $\overline{\text{CS1}}$ , CS2, $\overline{\text{OE}}$ , $\overline{\text{WE}}$ , $\overline{\text{LB}}$ , $\overline{\text{UB}}$ | 10   | pF   |
| C <sub>IO</sub>  | Data Input/Output Capacitance: I/O0-I/O15                                                                                                           | 10   | pF   |

**Notes:**

1. Tested initially and after any design or process changes that may affect these parameters.
2. Test conditions: T<sub>A</sub> = 25°C, f = 1 MHz.

**RECOMMENDED OPERATING CONDITIONS** (Voltages are referenced to GND.)

| Symbol          | Parameter                     | Min. | Typ. | Max.                  | Unit |
|-----------------|-------------------------------|------|------|-----------------------|------|
| V <sub>DD</sub> | Supply Voltage                | 2.2  |      | 3.6                   | V    |
| V <sub>IH</sub> | Input High Voltage            | 2.0  | —    | V <sub>DD</sub> + 0.3 | V    |
| V <sub>IL</sub> | Input Low Voltage             | −0.2 | —    | 0.4                   | V    |
| V <sub>DH</sub> | Data Retention Supply Voltage | 2.0  | —    | 3.0                   | V    |

**ELECTRICAL CHARACTERISTICS<sup>(1)</sup>****(Recommended Operating Conditions unless otherwise noted.)**

| Symbol           | Parameter                           | Test Condition                                                                                                           | Min. | Max. | Unit |
|------------------|-------------------------------------|--------------------------------------------------------------------------------------------------------------------------|------|------|------|
| I <sub>IL</sub>  | Input Leakage Current               | Any input 0V ≤ V <sub>IN</sub> ≤ V <sub>DD</sub><br>Other inputs not under test = 0V                                     | −1.0 | 1.0  | μA   |
| I <sub>IO</sub>  | Output Leakage Current              | Output is disabled (Hi-Z)<br>0V ≤ V <sub>OUT</sub> ≤ V <sub>DD</sub>                                                     | −1.0 | 1.0  | μA   |
| V <sub>OH</sub>  | Output High Voltage Level           | I <sub>OH</sub> = −0.5 mA                                                                                                | 1.9  | —    | V    |
| V <sub>OL</sub>  | Output Low Voltage Level            | I <sub>OL</sub> = 1.0 mA                                                                                                 | —    | 0.2  | V    |
| I <sub>CC1</sub> | Operating Current                   | $\overline{CS1} = V_{IH}$ , I <sub>OUT</sub> = 0mA<br>$\overline{CS1}$ Cycling, t <sub>RC</sub> = t <sub>RC</sub> (min.) | —    | 30   | mA   |
| I <sub>CC2</sub> | Page Access<br>Operating Current    | $\overline{CS1} = V_{IL}$ , CS2 = V <sub>IH</sub> , I <sub>OUT</sub> = 0mA<br>Page Add. Cycling, t <sub>PC</sub> (min.)  | —    | 25   | mA   |
| I <sub>SB1</sub> | Standby Current: TTL                | $\overline{CS1} = V_{IH}$ , CS2 = V <sub>IH</sub>                                                                        | —    | 1    | mA   |
| I <sub>SB2</sub> | Standby Current: CMOS               | $\overline{CS1} = V_{SS} - 0.2V$ , CS2 = V <sub>DD</sub> − 0.2V                                                          | —    | 70   | μA   |
| I <sub>SB3</sub> | Standby Current:<br>Deep Power-down | $\overline{CS1} = 0.2V$                                                                                                  | —    | 5    | μA   |

## AC CHARACTERISTICS

(Recommended Operating Conditions unless otherwise noted.)

| Symbol                              | Parameter                                                               | Min. | Max. | Units |
|-------------------------------------|-------------------------------------------------------------------------|------|------|-------|
| t <sub>RC</sub>                     | Random Read or Write Cycle Time                                         | 85   | —    | ns    |
| t <sub>CE</sub>                     | $\overline{\text{CS1}}$ Pulse Width                                     | 70   | 10K  | ns    |
| t <sub>P</sub>                      | Pre-charge Time                                                         | 15   | —    | ns    |
| t <sub>CEA</sub>                    | $\overline{\text{CS1}}$ Access Time                                     | —    | 70   | ns    |
| t <sub>OEA</sub>                    | $\overline{\text{OE}}$ Access Time                                      | —    | 70   | ns    |
| t <sub>OEP</sub>                    | $\overline{\text{OE}}$ Pulse Width                                      | 70   | —    | ns    |
| t <sub>BEA</sub>                    | $\overline{\text{LB}}, \overline{\text{UB}}$ Access Time                | —    | 25   | ns    |
| t <sub>APH</sub>                    | Address (A0 and A1) Hold Time                                           | 70   | —    | ns    |
| t <sub>ASC</sub>                    | Address Setup Time                                                      | -10  | —    | ns    |
| t <sub>AHC</sub>                    | Address Hold Time                                                       | 65   | —    | ns    |
| t <sub>ASO</sub> , t <sub>ASW</sub> | Address Setup Time                                                      | -10  | —    | ns    |
| t <sub>AHO</sub> , t <sub>AHW</sub> | Address Hold Time                                                       | 30   | —    | ns    |
| t <sub>WHC</sub>                    | $\overline{\text{WE}}$ Hold Time                                        | 8    | —    | ns    |
| t <sub>RCS</sub>                    | Read Command Setup Time                                                 | 8    | —    | ns    |
| t <sub>WOS</sub>                    | Write Command Setup Time                                                | 18   | —    | ns    |
| t <sub>RCH</sub>                    | Read Command Hold Time                                                  | 8    | —    | ns    |
| t <sub>WP</sub>                     | $\overline{\text{WE}}$ Pulse Width                                      | 70   | —    | ns    |
| t <sub>WCH</sub>                    | $\overline{\text{CS1}}$ to End of Write                                 | 70   | —    | ns    |
| t <sub>CWL</sub>                    | Write Command to $\overline{\text{CS1}}$ Lead Time                      | 70   | —    | ns    |
| t <sub>WBH</sub>                    | $\overline{\text{LB}}, \overline{\text{UB}}$ to End of Write            | 45   | —    | ns    |
| t <sub>BWL</sub>                    | Write Command to $\overline{\text{LB}}, \overline{\text{UB}}$ Lead time | 70   | —    | ns    |
| t <sub>WR</sub>                     | Write Recovery Time                                                     | 0    | —    | ns    |
| t <sub>DSW</sub>                    | Data Set-up Time from $\overline{\text{WE}}$                            | 25   | —    | ns    |
| t <sub>DSC</sub>                    | Data Set-up Time from $\overline{\text{CS1}}$                           | 25   | —    | ns    |
| t <sub>DSB</sub>                    | Data Set-up Time from $\overline{\text{LB}}, \overline{\text{UB}}$      | 25   | —    | ns    |
| t <sub>DHW</sub>                    | Data Hold Time from $\overline{\text{WE}}$                              | 0    | —    | ns    |
| t <sub>DHC</sub>                    | Data Hold Time from $\overline{\text{CS1}}$                             | 0    | —    | ns    |
| t <sub>DHB</sub>                    | Data Hold Time from $\overline{\text{LB}}, \overline{\text{UB}}$        | 0    | —    | ns    |

Continued

## AC CHARACTERISTICS Continued

(Recommended Operating Conditions unless otherwise noted.)

| Symbol | Parameter                                               | Min.             | Max. | Units |
|--------|---------------------------------------------------------|------------------|------|-------|
| tCLZ   | $\overline{CS1}$ Low to Output Active                   | 10               | —    | ns    |
| tOLZ   | $\overline{OE}$ Low to Output Active                    | 0                | —    | ns    |
| tBLZ   | $\overline{LB}$ , $\overline{UB}$ Low to Output Active  | 0                | —    | ns    |
| tWLZ   | $\overline{WE}$ Low to Output Active                    | 0                | —    | ns    |
| tCHZ   | $\overline{CS1}$ High to Output High-Z                  | —                | 20   | ns    |
| tOHZ   | $\overline{OE}$ High to Output High-Z                   | —                | 20   | ns    |
| tBHZ   | $\overline{LB}$ , $\overline{UB}$ High to Output High-Z | —                | 20   | ns    |
| tWHZ   | $\overline{OE}$ High to Output High-Z                   | —                | 20   | ns    |
| tPC    | Page Mode Cycle Time                                    | 25               | —    | ns    |
| tAA    | Page Mode Address Access Time                           | —                | 25   | ns    |
| tAOH   | Page Mode Output Data Hold Time                         | 5 <sup>(1)</sup> | —    | ns    |
| tCS    | $\overline{CS1}$ Set-up Time                            | 0                | —    | ns    |
| tCH    | $\overline{CS1}$ Hold Time                              | 200              | —    | μs    |
| tDPD   | $\overline{CS1}$ Pulse Width (Deep Power Down)          | 10               | —    | ms    |

## AC Notes:

1. Guarantee minimum 10ns of data valid time under any specific operating condition.
2. After power-up, an initial pause of 200 μs with CS2 high is required with the output open condition.
3. Parameters tCHZ, tOHZ, tBHZ and tWHZ define the time at which the output goes the into the open condition and are not output voltage reference levels.
4. During write cycles, input data is latched on the earliest of  $\overline{WE}$ ,  $\overline{LB/UB}$ , or  $\overline{CS1}$  rising edge. Therefore, input data must be valid during the set-up time (tDSC, tDSB or tDSW) and hold time (tDHC, tDHB or tDHW).
5. Address (A2 to A20) inputs are latched on the falling edge of  $\overline{OE}$  or  $\overline{WE}$ . Address (A2 to A20) input must be valid during the set-up time (tASO or tASW) and hold time (tAHO or tAHW).
6. Data can not be retained at deep power-down stand-by mode.
7. If  $\overline{OE}$  is high during the write cycle, the outputs will remain at high impedance.
8. During the output state of I/O signals, input signals of reverse polarity must not be applied.
9. <sup>1</sup>rising = <sup>1</sup>falling = 5ns for inputs.

## AC TEST CONDITIONS

| Parameter                                   | Unit                               |
|---------------------------------------------|------------------------------------|
| Input Pulse Level                           | $V_{DD}-0.2V$ to $V_{DD}+0.2V$     |
| Input Rise and Fall Time                    | 5 ns                               |
| Input and Output Timing and Reference Level | $V_{REF}$                          |
| Output Load                                 | See Figures 1 and 2 <sup>(1)</sup> |

Note 1. All AC test to output Load Figure 1, except High-Z use output load Figure 2.

| 2.2V to 3.6V   |      |
|----------------|------|
| R1( $\Omega$ ) | 3070 |
| R2( $\Omega$ ) | 3150 |
| $V_{REF}$      | 1.5V |
| $V_{TM}$       | 2.8V |

## AC TEST LOADS

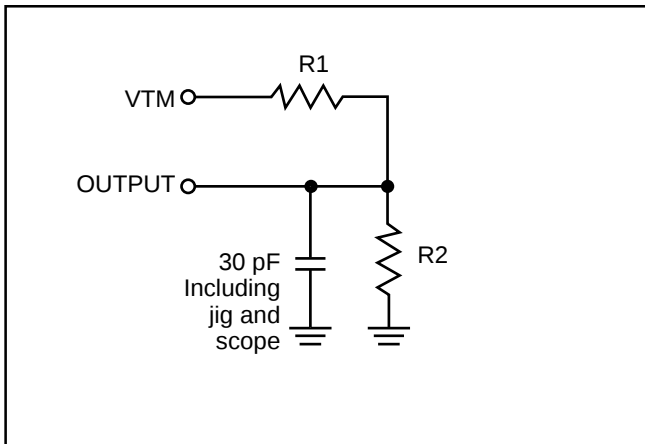


Figure 1

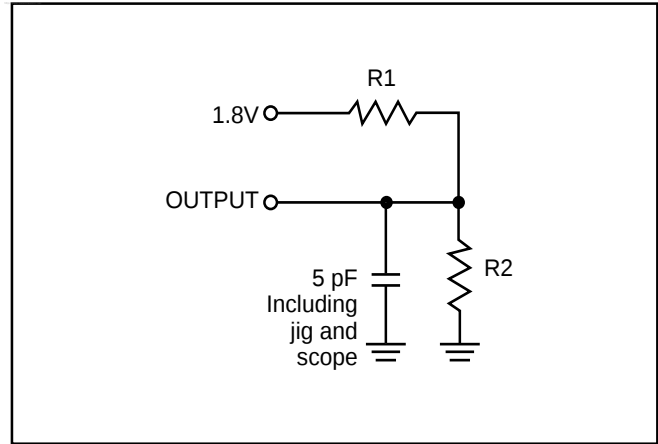
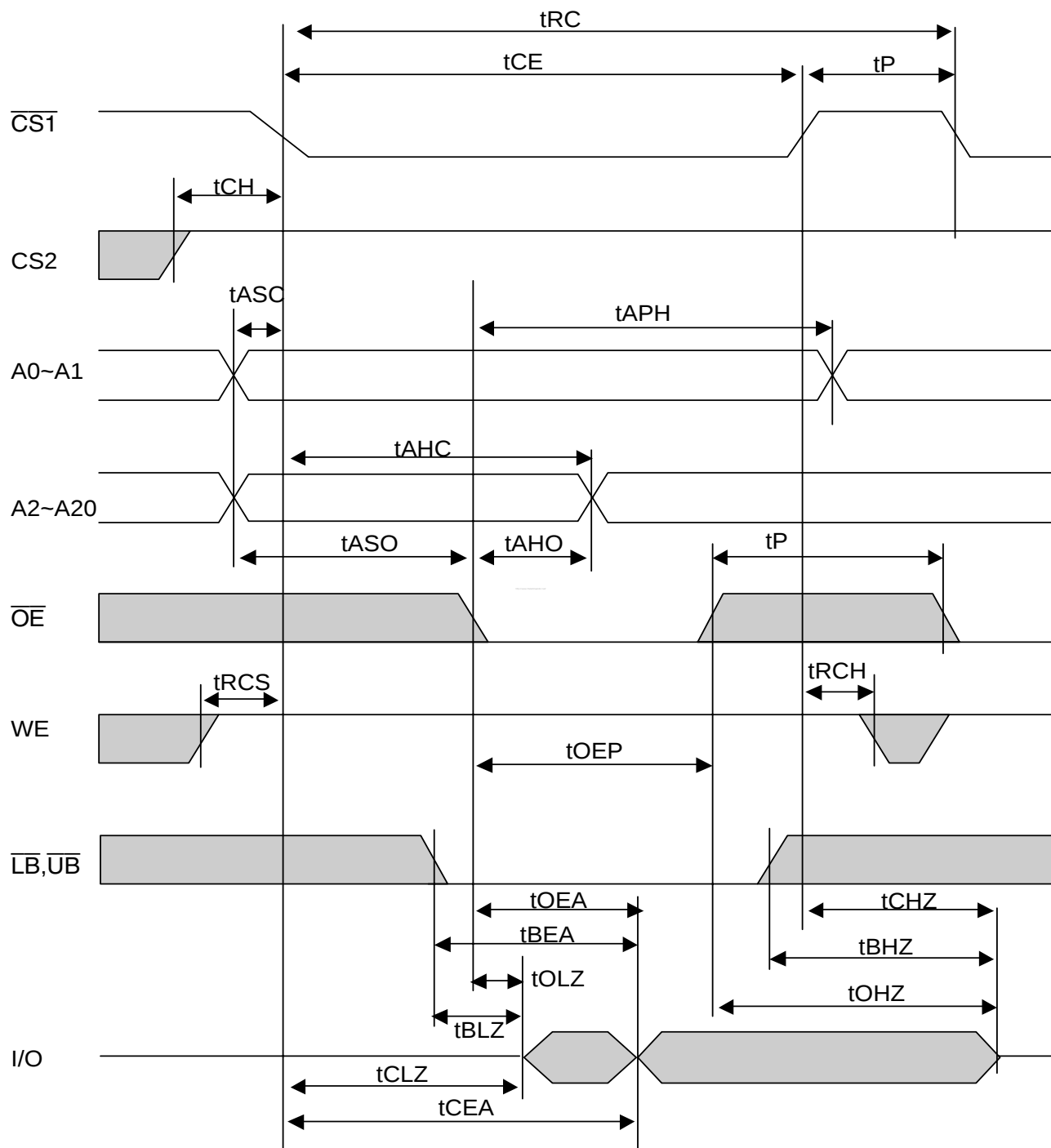


Figure 2

## AC WAVEFORMS

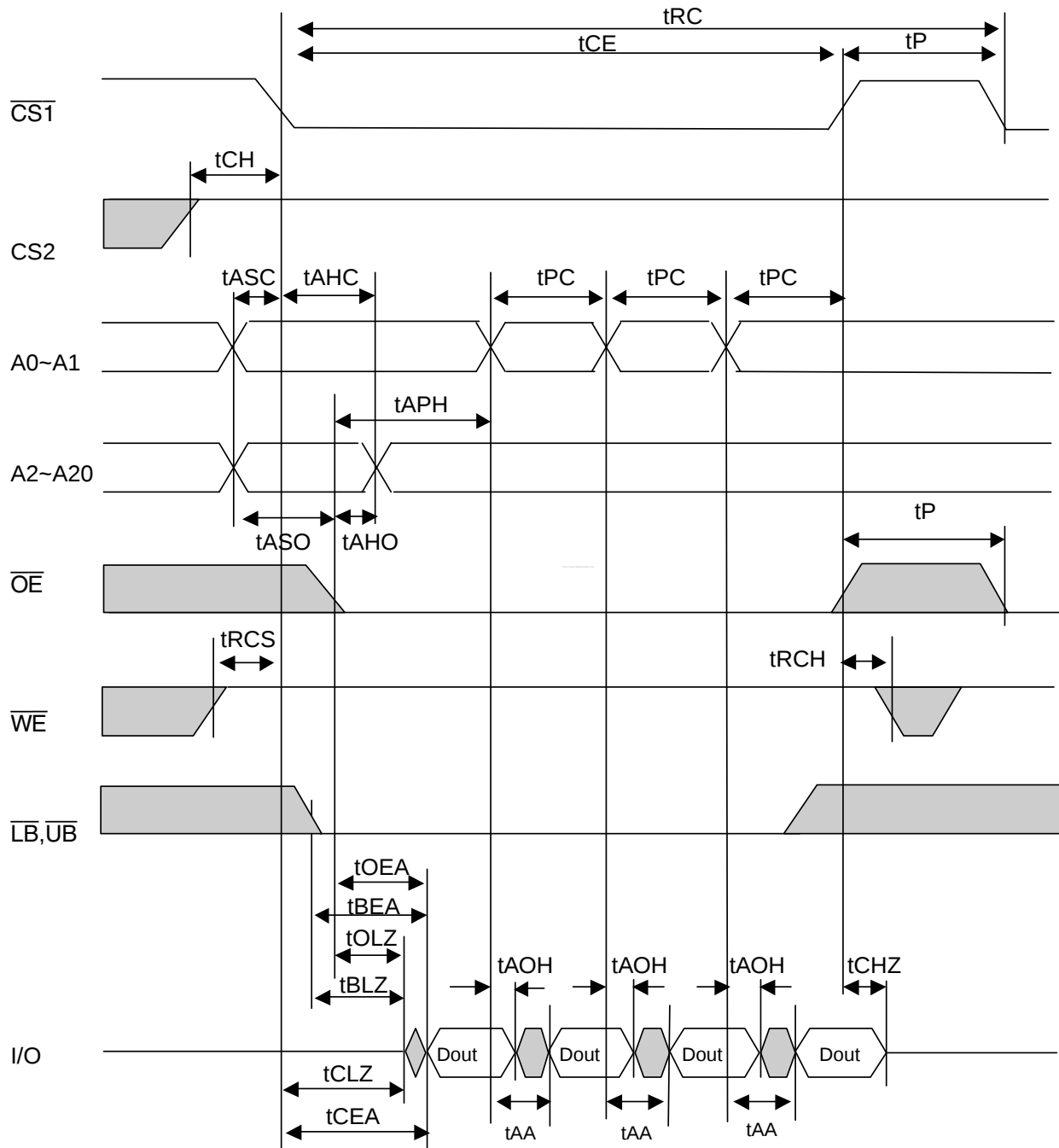
## Read Timing



For shaded areas either  $\overline{OE}$  or  $\overline{CS1}$  = High.

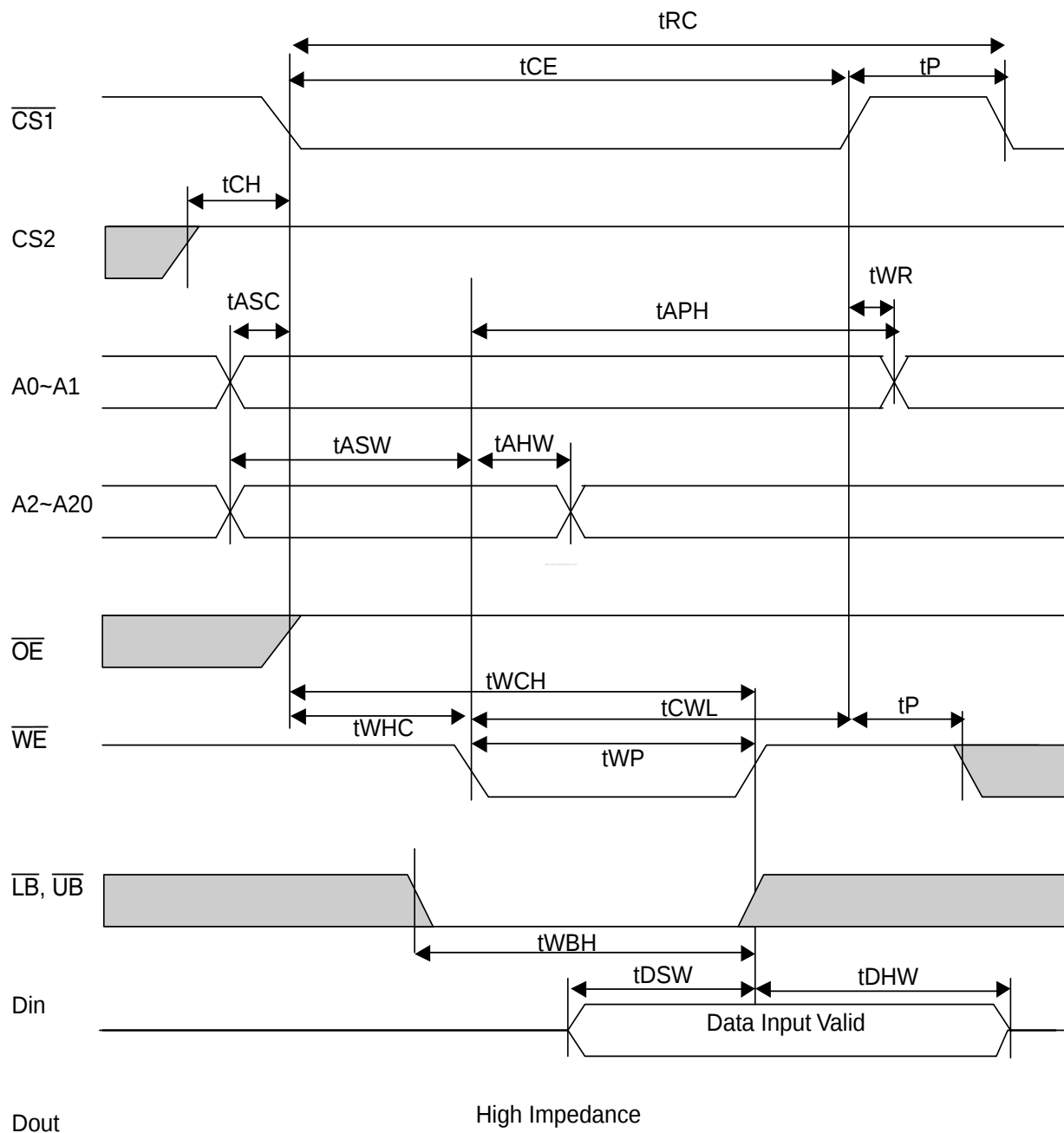
## AC WAVEFORMS

## Page Read timing (four word access)



For shaded areas either  $\overline{OE}$  or  $\overline{CS1}$  = High.

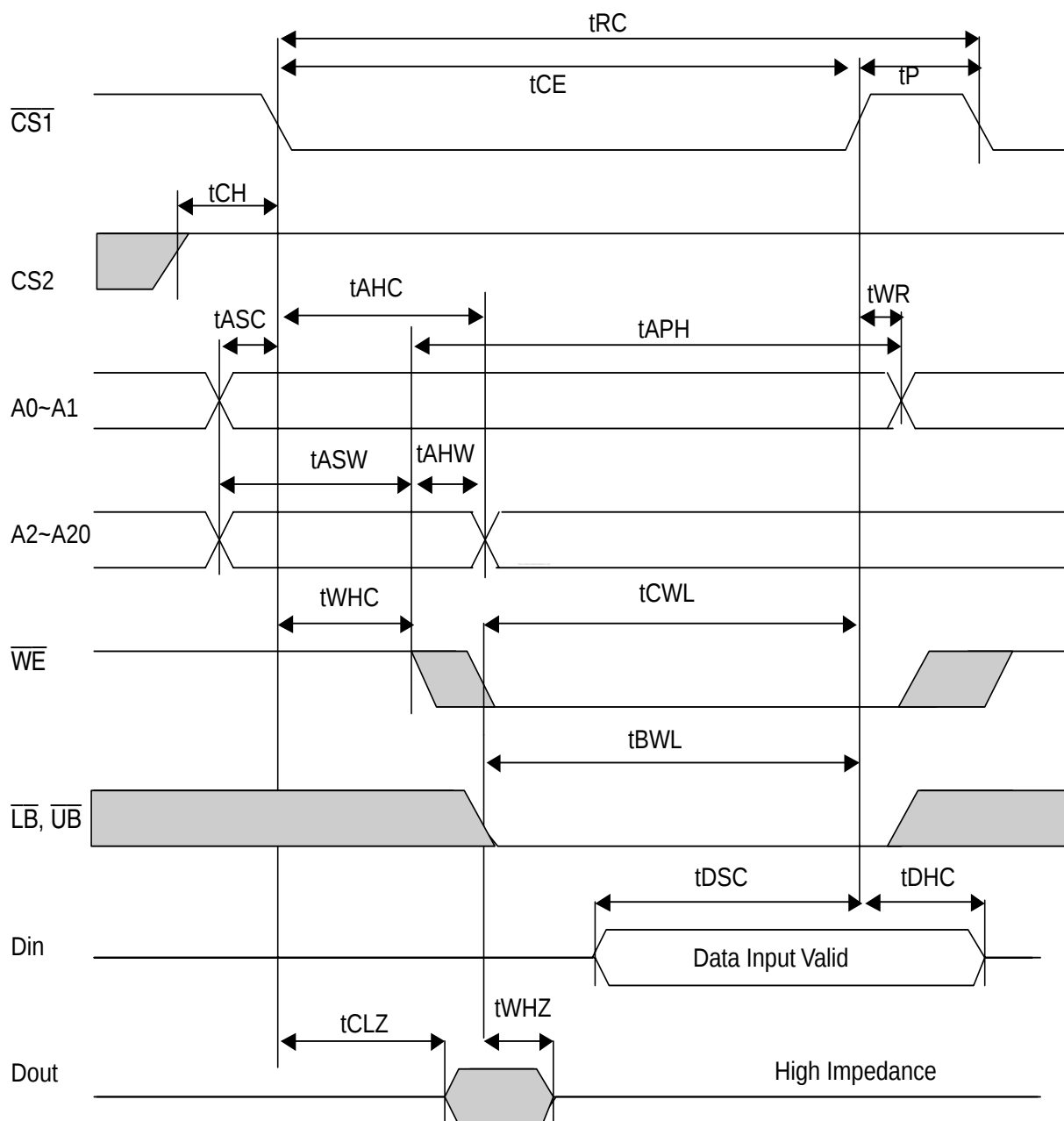
## AC WAVEFORMS

Write Timing ( $\overline{\text{WE}}$  Control Write)

### Write Timing ( $\overline{\text{LB}}/\overline{\text{UB}}$ Control Write)

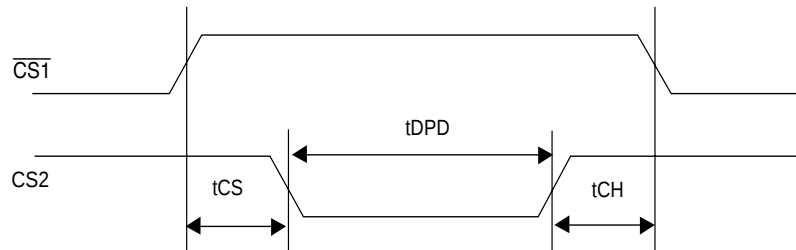


## AC Wave Forms

Write Timing ( $\overline{\text{CS1}}$  Control Write)

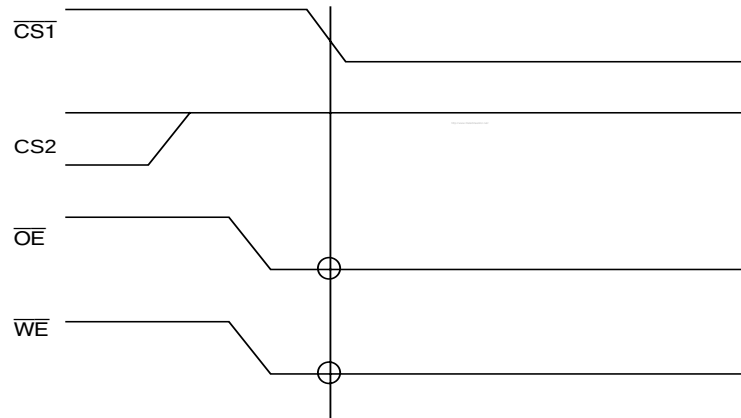
$\overline{\text{OE}}$  = High.

## Deep Power-Down Timing



Note: During deep power-down stand-by mode, data can not be retained.

## Prohibition Timing (Timing shown is prohibited.)



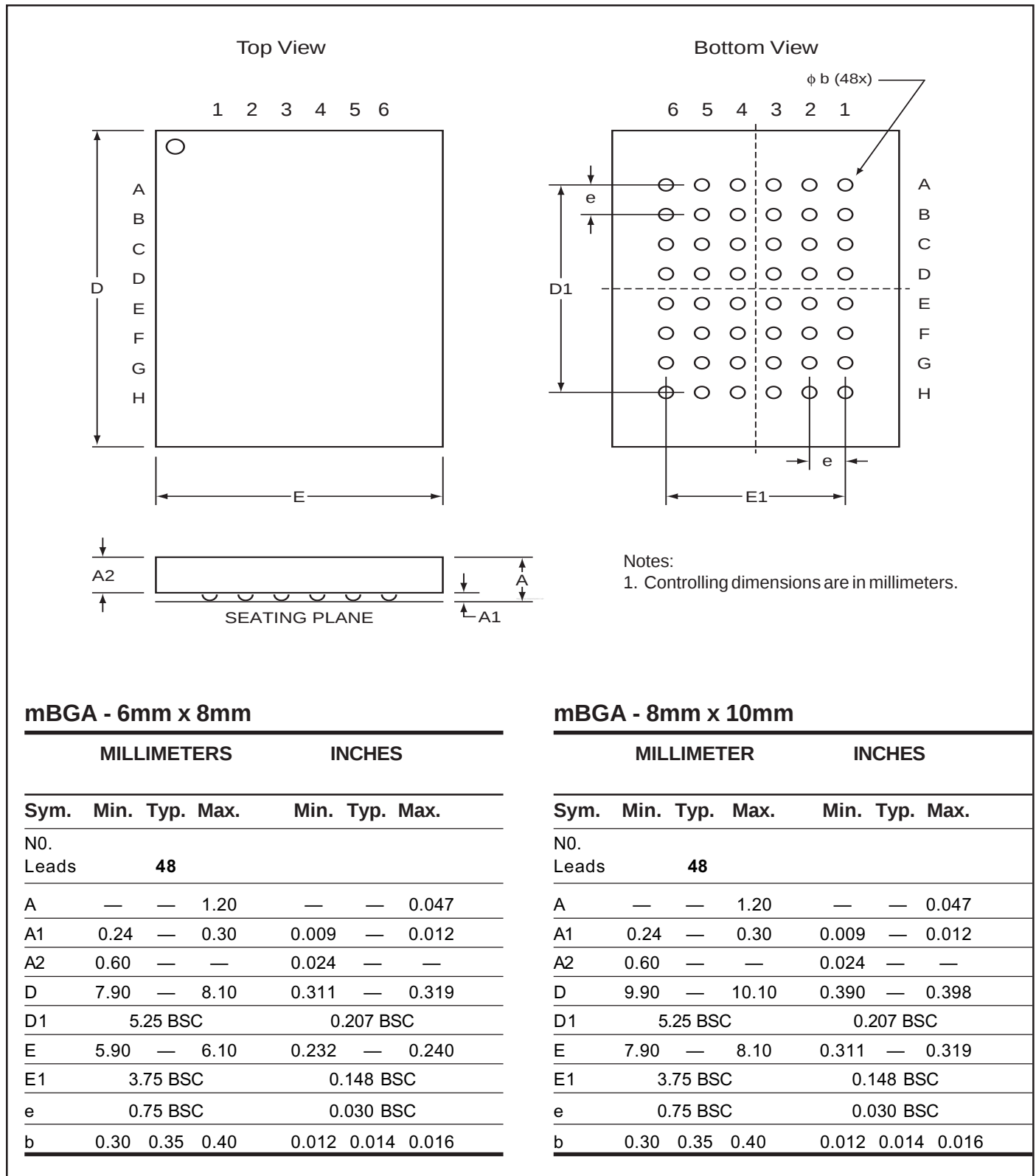
Note: A malfunction may occur, since devices go into test modes for internal use, if both  $\overline{OE}$  and  $\overline{WE}$  go Low coincident with or before falling edge of  $\overline{CS1}$ .

**ORDERING INFORMATION****Industrial Range: –40°C to +85°C**

| <b>Speed<br/>(ns)</b> | <b>Order Part No.</b> | <b>Package</b>                       |
|-----------------------|-----------------------|--------------------------------------|
| 70                    | IS32WV204816B-70MI    | Mini BGA (6mm x 8mm) (0.8 mm Pitch)  |
|                       | IS32WV204816B-70BI    | Mini BGA (6mm x 8mm) (0.75 mm Pitch) |

# PACKAGING INFORMATION

## Mini Ball Grid Array Package Code: B (48-pin)



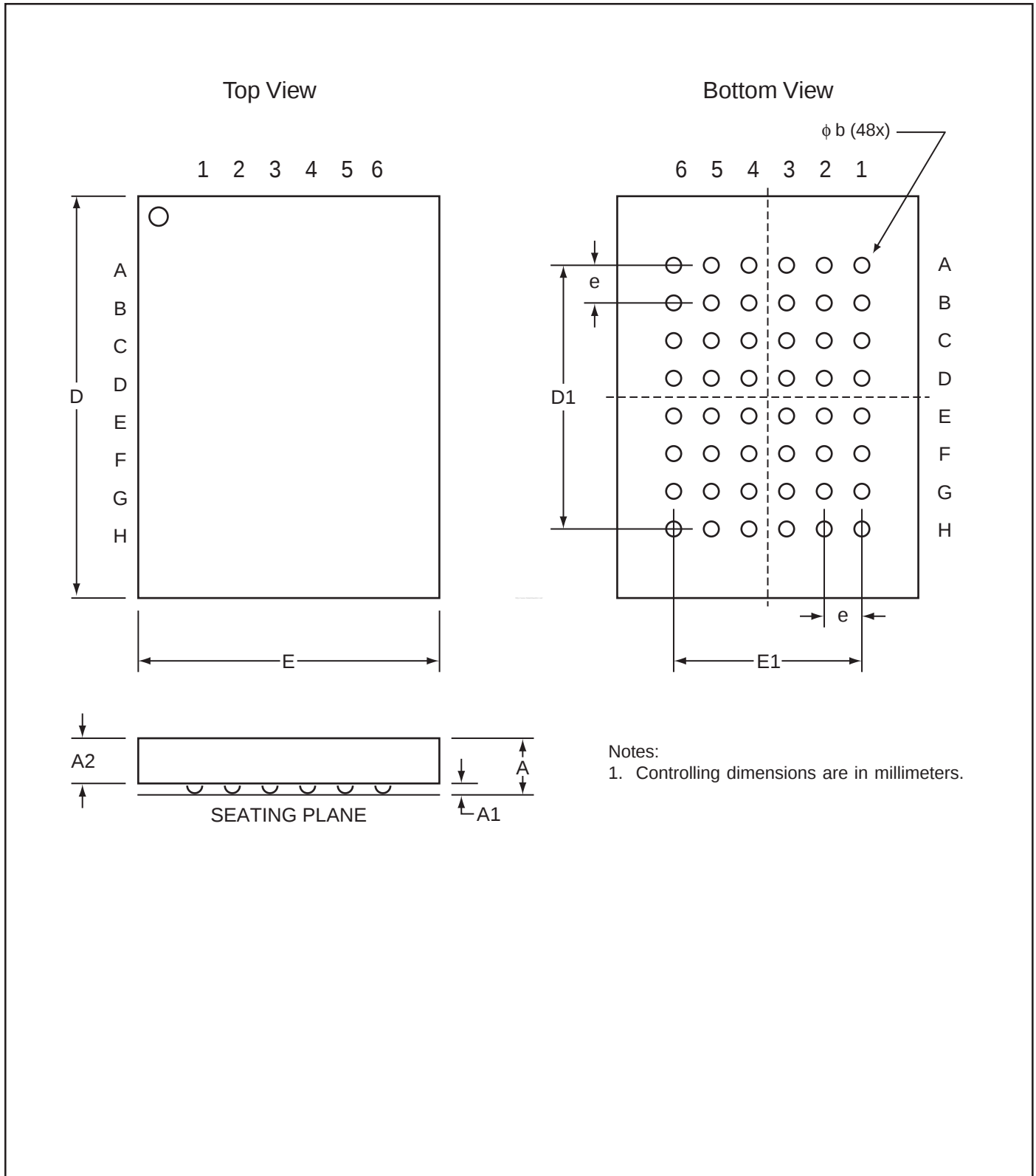
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Rev. D  
01/15/03

# PACKAGING INFORMATION

## Mini Ball Grid Array Package Code: M (48-pin)



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## Mini Ball Grid Array

Package Code: M (48-pin)

### mBGA - 6mm x 8mm

| MILLIMETERS  |         |      |      | INCHES   |       |       |
|--------------|---------|------|------|----------|-------|-------|
| Sym.         | Min.    | Typ. | Max. | Min.     | Typ.  | Max.  |
| NO.<br>Leads |         |      |      |          |       |       |
| 48           |         |      |      |          |       |       |
| A            | —       | —    | 1.20 | —        | —     | 0.047 |
| A1           | 0.25    | —    | 0.40 | 0.010    | —     | 0.016 |
| A2           | 0.60    | —    | —    | 0.024    | —     | —     |
| D            | 7.90    | 8.00 | 8.10 | 0.311    | 0.314 | 0.319 |
| D1           | 5.60BSC |      |      | 0.220BSC |       |       |
| E            | 5.90    | 6.00 | 6.10 | 0.232    | 0.236 | 0.240 |
| E1           | 4.00BSC |      |      | 0.157BSC |       |       |
| e            | 0.80BSC |      |      | 0.031BSC |       |       |
| b            | 0.40    | 0.45 | 0.50 | 0.016    | 0.018 | 0.020 |

### mBGA - 7.2mm x 8.7mm

| MILLIMETERS  |         |      |      | INCHES   |       |       |
|--------------|---------|------|------|----------|-------|-------|
| Sym.         | Min.    | Typ. | Max. | Min.     | Typ.  | Max.  |
| NO.<br>Leads |         |      |      |          |       |       |
| 48           |         |      |      |          |       |       |
| A            | —       | —    | 1.20 | —        | —     | 0.047 |
| A1           | 0.24    | —    | 0.30 | 0.009    | —     | 0.012 |
| A2           | 0.60    | —    | —    | 0.024    | —     | —     |
| D            | 8.60    | 8.70 | 8.80 | 0.339    | 0.343 | 0.346 |
| D1           | 5.25BSC |      |      | 0.207BSC |       |       |
| E            | 7.10    | 7.20 | 7.30 | 0.280    | 0.283 | 0.287 |
| E1           | 3.75BSC |      |      | 0.148BSC |       |       |
| e            | 0.75BSC |      |      | 0.030BSC |       |       |
| b            | 0.30    | 0.35 | 0.40 | 0.012    | 0.014 | 0.016 |

### mBGA - 9mm x 11mm

| MILLIMETERS  |         |       |       | INCHES   |       |       |
|--------------|---------|-------|-------|----------|-------|-------|
| Sym.         | Min.    | Typ.  | Max.  | Min.     | Typ.  | Max.  |
| NO.<br>Leads |         |       |       |          |       |       |
| 48           |         |       |       |          |       |       |
| A            | —       | —     | 1.20  | —        | —     | 0.047 |
| A1           | 0.24    | —     | 0.30  | 0.009    | —     | 0.012 |
| A2           | 0.60    | —     | —     | 0.024    | —     | —     |
| D            | 10.90   | 11.00 | 11.10 | 0.429    | 0.433 | 0.437 |
| D1           | 5.25BSC |       |       | 0.207BSC |       |       |
| E            | 8.90    | 9.00  | 9.10  | 0.350    | 0.354 | 0.358 |
| E1           | 3.75BSC |       |       | 0.148BSC |       |       |
| e            | 0.75BSC |       |       | 0.030BSC |       |       |
| b            | 0.30    | 0.35  | 0.40  | 0.012    | 0.014 | 0.016 |