IS41C4400x IS41LV4400x Series



4M x 4 (16-MBIT) DYNAMIC RAM WITH EDO PAGE MODE

JUNE, 2001

FEATURES

- Extended Data-Out (EDO) Page Mode access cycle
- TTL compatible inputs and outputs
- · Refresh Interval:
 - 2,048 cycles/32 ms
 - 4,096 cycles/64 ms
- Refresh Mode: RAS-Only,
 - CAS-before-RAS (CBR), and Hidden
- Single power supply:
 - $-5V\pm10\%$ or $3.3V\pm10\%$
- Byte Write and Byte Read operation via two CAS
- Industrial temperature range -40°C to 85°C

DESCRIPTION

The *ISSI* 4400 Series is a 4,194,304 x 4-bit high-performance CMOS Dynamic Random Access Memory. These devices offer an accelerated cycle access called EDO Page Mode. EDO Page Mode allows 2,048 or 4096 random accesses within a single row with access cycle time as short as 20 ns per 4-bit word.

These features make the 4400 Series ideally suited for high-bandwidth graphics, digital signal processing, high-performance computing systems, and peripheral applications.

The 4400 Series is packaged in a 24-pin 300-mil SOJ with JEDEC standard pinouts.

PRODUCT SERIES OVERVIEW

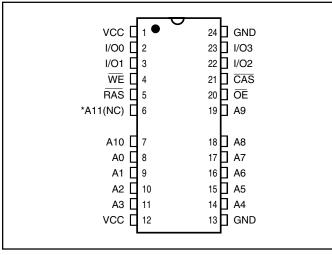
Part No.	Refresh	Voltage
IS41C44002	2K	5V ± 10%
IS41C44004	4K	5V ± 10%
IS41LV44002	2K	3.3V ± 10%
IS41LV44004	4K	3.3V ± 10%

KEY TIMING PARAMETERS

Parameter	-50	-60	Unit
RAS Access Time (trac)	50	60	ns
CAS Access Time (tcac)	13	15	ns
Column Address Access Time (taa)	25	30	ns
EDO Page Mode Cycle Time (tpc)	20	25	ns
Read/Write Cycle Time (trc)	84	104	ns

PIN CONFIGURATION

24 Pin SOJ



PIN DESCRIPTIONS

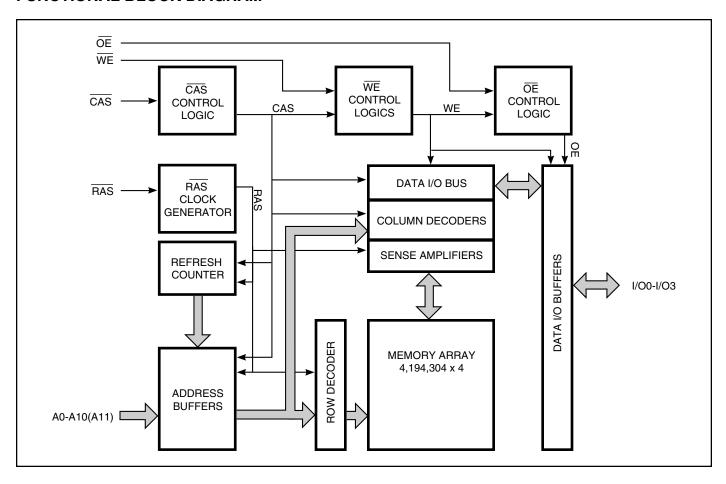
A0-A11	Address Inputs (4K Refresh)
A0-A10	Address Inputs (2K Refresh)
I/O0-3	Data Inputs/Outputs
WE	Write Enable
ŌĒ	Output Enable
RAS	Row Address Strobe
CAS	Column Address Strobe
Vcc	Power
GND	Ground
NC	No Connection

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^{*} A11 is NC for 2K Refresh devices.



FUNCTIONAL BLOCK DIAGRAM



TRUTH TABLE

Function		RAS	CAS	WE	ŌĒ	Address tr/tc	I/O
Standby		Н	Н	Χ	Χ	Χ	High-Z
Read		L	L	Н	L	ROW/COL	Dоит
Write: Word (Early Write	e)	L	L	L	Χ	ROW/COL	DIN
Read-Write		L	L	H→L	L→H	ROW/COL	Dout, Din
EDO Page-Mode Read	1st Cycle:	L	H→L	Н	L	ROW/COL	D оит
	2nd Cycle:	L	$H{ ightarrow} L$	Н	L	NA/COL	D оит
EDO Page-Mode Write	1st Cycle:	L	$H{ ightarrow} L$	L	Χ	ROW/COL	DIN
	2nd Cycle:	L	$H{ ightarrow} L$	L	Χ	NA/COL	DIN
EDO Page-Mode	1st Cycle:	L	H→L	H→L	L→H	ROW/COL	Dout, Din
Read-Write	2nd Cycle:	L	$H{ ightarrow} L$	$H{ ightarrow} L$	$L{ ightarrow}H$	NA/COL	Dout, DIN
Hidden Refresh	Read	L→H→L	L	Н	L	ROW/COL	D оит
	Write ⁽¹⁾	$L{\rightarrow}H{\rightarrow}L$	L	L	Χ	ROW/COL	Douт
RAS-Only Refresh		L	Н	Х	Х	ROW/NA	High-Z
CBR Refresh		H→L	L	Χ	Х	Х	High-Z

Note:

1. EARLY WRITE only.



Functional Description

The IS41C4400x and IS41LV4400x are CMOS DRAMs optimized for high-speed bandwidth, low power applications. During READ or WRITE cycles, each bit is uniquely addressed through the 11 or 12 address bits. These are entered 11 bits (A0-A10) at a time for the 2K refresh device or 12 bits (A0-A11) at a time for the 4K refresh device. The row address is latched by the Row Address Strobe (RAS). The column address is latched by the Column Address Strobe (CAS). RAS is used to latch the first nine bits and \overline{CAS} is used the latter ten bits.

Memory Cycle

A memory cycle is initiated by bring RAS LOW and it is terminated by returning both RAS and CAS HIGH. To ensures proper device operation and data integrity any memory cycle, once initiated, must not be ended or aborted before the minimum tras time has expired. A new cycle must not be initiated until the minimum precharge time trp, tcp has elapsed.

Read Cycle

A read cycle is initiated by the falling edge of \overline{CAS} or \overline{OE} , whichever occurs last, while holding WE HIGH. The column address must be held for a minimum time specified by tar. Data Out becomes valid only when trac, taa, toac and toea are all satisfied. As a result, the access time is dependent on the timing relationships between these parameters.

Write Cycle

A write cycle is initiated by the falling edge of CAS and WE, whichever occurs last. The input data must be valid at or before the falling edge of \overline{CAS} or \overline{WE} , whichever occurs last.

Auto Refresh Cycle

To retain data, 2,048 refresh cycles are required in each 32 ms period, or 4,096 refresh cycles are required in each 64ms period. There are two ways to refresh the memory:

- 1. By clocking each of the 2,048 row addresses (A0 through A10) or 4096 row addresses (A0 through A11) with RAS at least once every 32 ms or 64ms respectively. Any read, write, read-modify-write or RAS-only cycle refreshes the addressed row.
- 2. Using a CAS-before-RAS refresh cycle. CAS-before-RAS refresh is activated by the falling edge of RAS, while holding CAS LOW. In CAS-before-RAS refresh cycle, an internal 9-bit counter provides the row addresses and the external address inputs are ignored.

CAS-before-RAS is a refresh-only mode and no data access or device selection is allowed. Thus, the output remains in the High-Z state during the cycle.

Power-On

After application of the Vcc supply, an initial pause of 200 μs is required followed by a minimum of eight initialization cycles (any combination of cycles containing a RAS signal).

During power-on, it is recommended that RAS track with Vcc or be held at a valid ViH to avoid current surges.



ABSOLUTE MAXIMUM RATINGS(1)

Symbol	Parameters		Rating	Unit
V T	Voltage on Any Pin Relative to GND	5V 3.3V	-1.0 to +7.0 -0.5 to +4.6	V
Vcc	Supply Voltage	5V 3.3V	-1.0 to +7.0 -0.5 to +4.6	V
Іоит	Output Current		50	mA
Po	Power Dissipation		1	W
Та	Commercial Operation Temperature Industrial Operation Temperature		0 to +70 -40 to +85	°C
Тѕтс	Storage Temperature		-55 to +125	°C

Note:

RECOMMENDED OPERATING CONDITIONS (Voltages are referenced to GND.)

Symbol	Parameter		Min.	Тур.	Max.	Unit
Vcc	Supply Voltage	5V 3.3V	4.5 3.0	5.0 3.3	5.5 3.6	V
VIH	Input High Voltage	5V 3.3V	2.4 2.0	_	Vcc + 1.0 Vcc + 0.3	V
VIL	Input Low Voltage	5V 3.3V	-1.0 -0.3	_	0.8 0.8	V
Та	Commercial Ambient Temperature Industrial Ambient Temperature		0 -40	_	70 85	°C °C

CAPACITANCE(1,2)

Symbol	Parameter	Max.	Unit
CIN1	Input Capacitance: A0-A10(A11)	5	pF
CIN2	Input Capacitance: RAS, CAS, WE, OE	7	pF
Сю	Data Input/Output Capacitance: I/O0-I/O3	7	pF

Notes

Stress greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device.
 This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

^{1.} Tested initially and after any design or process changes that may affect these parameters.

^{2.} Test conditions: T_A = 25°C, f = 1 MHz.



ELECTRICAL CHARACTERISTICS(1)

(Recommended Operating Conditions unless otherwise noted.)

Parameter	Test Condition	Vcc	Speed	Min.	Max.	Unit
Input Leakage Current	Any input $0V \le V_{IN} \le V_{CC}$ Other inputs not under test = $0V$			- 5	5	μA
Output Leakage Current	Output is disabled (Hi-Z) 0V ≤ Vouт ≤ Vcc			- 5	5	μA
Output High Voltage Level	$I_{OH} = -5.0 \text{ mA}, V_{CC} = 5V$ $I_{OH} = -2.0 \text{ mA}, V_{CC} = 3.3V$			2.4	_	V
Output Low Voltage Level	IoL = 4.2 mA, Vcc = 5V IoL = 2 mA, Vcc = 3.3V			_	0.4	V
Standby Current: TTL	\overline{RAS} , $\overline{CAS} \ge V_{IH}$ Commercial	5V		_	2	mA
•		3.3V		_	0.5	
	Industrial	5V		_	3	
		3.3V		_	2	
Standby Current: CMOS	RAS, CAS ≥ Vcc – 0.2V	5V		_	1	mA
•		3.3V		_	0.5	
Operating Current:	RAS, CAS,		-50	_	120	mA
Random Read/Write ^(2,3,4) Average Power Supply Current	Address Cycling, tac = tac (min.)		-60	_	110	
Operating Current:	RAS = VIL. CAS.		-50		90	mA
EDO Page Mode ^(2,3,4) Average Power Supply Current	Cycling tpc = tpc (min.)		-60	_	80	
Refresh Current:	RAS Cycling, CAS ≥ V _{IH}		-50	_	120	mA
RAS-Only ^(2,3) Average Power Supply Current	trc = trc (min.)		-60	_	110	
Refresh Current:	RAS, CAS Cycling		-50	_	120	mA
CBR ^(2,3,5) Average Power Supply Current	tac = tac (min.)		-60	_	110	
	Input Leakage Current Output Leakage Current Output High Voltage Level Output Low Voltage Level Standby Current: TTL Standby Current: CMOS Operating Current: Random Read/Write(2,3,4) Average Power Supply Current Operating Current: EDO Page Mode(2,3,4) Average Power Supply Current Refresh Current: RAS-Only(2,3) Average Power Supply Current Refresh Current: CBR(2,3,5)		$ \begin{array}{llllllllllllllllllllllllllllllllllll$	$ \begin{array}{llllllllllllllllllllllllllllllllllll$	$ \begin{array}{c ccccccccccccccccccccccccccccccccccc$	$ \begin{array}{c ccccccccccccccccccccccccccccccccccc$

Notes:

^{1.} An initial pause of 200 μs is required after power-up followed by eight RAS refresh cycles (RAS-Only or CBR) before proper device operation is assured. The eight RAS cycles wake-up should be repeated any time the tree refresh requirement is exceeded.

^{2.} Dependent on cycle rates.

^{3.} Specified values are obtained with minimum cycle time and the output open.

^{4.} Column-address is changed once each EDO page cycle.

^{5.} Enables on-chip refresh and address counters.



AC CHARACTERISTICS(1,2,3,4,5,6)

(Recommended Operating Conditions unless otherwise noted.)

Symbol Parameter Min. Max. Min. Max. Units IRC Random READ or WRITE Cycle Time 84 — 104 — ns IRAC Access Time from RAS ^(6, 7) — 50 — 60 ns ItAA Access Time from Column-Address ⁽⁶⁾ — 25 — 30 ns ItAA Access Time from Column-Address ⁽⁶⁾ — 25 — 30 ns ItAA Access Time from Column-Address ⁽⁶⁾ — 25 — 30 ns ItAA Access Time from Column-Address ⁽⁶⁾ — 25 — 30 ns ItAA Access Time from Column-Address Selup Time 30 — 40 — ns ItAA ACCES Pulse Width ⁽⁶⁰⁾ 8 10K 10 10 — ns ItABA ACA Pollay Time ⁽⁶⁰⁾ 38 — 40 — ns ItABA COAS Hold Time 8 — 10 — <th></th> <th></th> <th>-5</th> <th>60</th> <th>-6</th> <th>60</th> <th></th>			-5	60	-6	60	
thac Access Time from RAS ^(n, n) — 50 — 60 ns tox Access Time from CAS ^(n, n, n) — 13 — 15 ns tox Access Time from Column-Address ⁽ⁿ⁾ — 25 — 30 ns tras RAS Pulse Width 50 10K 60 10K ns tras RAS Precharge Time 30 — 40 — ns tcp CAS Pulse Width ^(co) 8 10K 10 10K ns tcp CAS Precharge Time ⁽ⁿ⁾ 9 — 9 — ns tcp CAS Precharge Time ⁽ⁿ⁾ 38 — 40 — ns tcp CAS Precharge Time ⁽ⁿ⁾ 38 — 40 — ns tcp CAS Precharge Time ⁽ⁿ⁾ 38 — 40 — ns tcp CAS Precharge Time ⁽ⁿ⁾ 38 — 10 — ns tcp CAS O CAS Pre	Symbol	Parameter			Min.	Max.	Units
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toD Output Disable Time(¹¹9, ²⁴) 3 15 3 15 ns toE Output Enable Time(¹¹5, ¹₆) — 12 — 15 ns toED Output Enable Data Delay (Write) 12 — 15 — ns toED OE HIGH Hold Time from CAS HIGH 5 — 5 — ns toEP OE HIGH Pulse Width 10 — 10 — ns toEP OE LOW to CAS HIGH Setup Time 5 — 5 — ns toEs OE LOW to CAS HIGH Setup Time 5 — 5 — ns tRCS Read Command Setup Time(¹¹7, ²⁰) 0 — 0 — ns tRCH Read Command Hold Time (referenced to CAS)(¹²2, ¹²7, ²²1) 0 — 0 — ns twch Write Command Hold Time (row CAS)(¹²2, ¹²7, ²²1) 8 — 10 — ns twch Write Command Hold Time (row CAS)(¹²2, ¹²7, ²²1) 0 — 0	tcLz	CAS to Output in Low-Z(15, 24)	0	_	0	_	ns
toE Output Enable Time(15, 16) — 12 — 15 ns toED Output Enable Data Delay (Write) 12 — 15 — ns toEHC OE HIGH Hold Time from CAS HIGH 5 — 5 — ns toEP OE HIGH Pulse Width 10 — 10 — ns toES OE LOW to CAS HIGH Setup Time 5 — 5 — ns tRCS Read Command Setup Time(17, 20) 0 — 0 — ns tRRH Read Command Hold Time (referenced to RAS)(12) 0 — 0 — ns twch Write Command Hold Time (referenced to RAS)(12, 17, 21) 8 — 10 — ns twch Write Command Hold Time (referenced to RAS)(17) 8 — 10 — ns twch Write Command Pulse Width(17) 8 — 10 — ns	tcrp	CAS to RAS Precharge Time(21)	5	_	5	_	ns
TOED Output Enable Data Delay (Write) 12 — 15 — ns TOEHC OE HIGH Hold Time from CAS HIGH 5 — 5 — ns TOEP OE HIGH Pulse Width 10 — 10 — ns TOES OE LOW to CAS HIGH Setup Time 5 — 5 — ns TRCS Read Command Setup Time(17, 20) 0 — 0 — ns TRRH Read Command Hold Time (referenced to RAS)(12) 0 — 0 — ns TWCH Write Command Hold Time (referenced to RAS)(12, 17, 21) 8 — 10 — ns TWCR Write Command Hold Time (referenced to RAS)(17) 40 — 50 — ns TWP Write Command Pulse Width(17) 8 — 10 — ns	top	Output Disable Time(19, 24)	3	15	3	15	ns
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toep OE HIGH Pulse Width 10 — 10 — ns toes OE LOW to CAS HIGH Setup Time 5 — 5 — ns tres Read Command Setup Time(17, 20) 0 — 0 — ns treferenced to RAS)(12) 0 — 0 — ns treferenced to RAS)(12) 0 — 0 — ns twch Write Command Hold Time (17) 8 — 10 — ns twch Write Command Hold Time (17) 40 — 50 — ns twch Write Command Pulse Width(17) 8 — 10 — ns	toed	Output Enable Data Delay (Write)	12	_	15	_	ns
toes $\overline{\text{OE}}$ LOW to $\overline{\text{CAS}}$ HIGH Setup Time5—5—nstracsRead Command Setup Time $^{(17, 20)}$ 0—0—nstrachRead Command Hold Time (referenced to $\overline{\text{RAS}})^{(12)}$ 0—0—nstwchWrite Command Hold Time $^{(17)}$ 8—10—nstwcrWrite Command Hold Time (referenced to $\overline{\text{RAS}})^{(17)}$ 40—50—nstwpWrite Command Pulse Width $^{(17)}$ 8—10—ns	toehc	OE HIGH Hold Time from CAS HIGH	5	_	5	_	ns
tRCSRead Command Setup Time $^{(17, 20)}$ 0—0—nstRRHRead Command Hold Time (referenced to $\overline{RAS})^{(12)}$ 0—0—nstRCHRead Command Hold Time (referenced to $\overline{CAS})^{(12, 17, 21)}$ 0—0—nstwchWrite Command Hold Time $^{(17)}$ 8—10—nstwchWrite Command Hold Time (referenced to $\overline{RAS})^{(17)}$ 40—50—nstwpWrite Command Pulse Width $^{(17)}$ 8—10—ns	toep	OE HIGH Pulse Width	10	_	10	_	ns
triangle Read Command Hold Time (referenced to RAS) ⁽¹²⁾ 0 — 0 — ns (referenced to RAS) ⁽¹²⁾ triangle Read Command Hold Time (referenced to CAS) ^(12, 17, 21) 0 — 0 — ns twch Write Command Hold Time (referenced to RAS) ⁽¹⁷⁾ 8 — 10 — ns twp Write Command Pulse Width ⁽¹⁷⁾ 8 — 10 — ns	toes	OE LOW to CAS HIGH Setup Time	5	_	5	_	ns
(referenced to RAS) ⁽¹²⁾ tRCH Read Command Hold Time (referenced to CAS) ^(12, 17, 21) 0 — 0 — ns (referenced to RAS) ^(12, 17, 21) twch Write Command Hold Time (17) 8 — 10 — ns (referenced to RAS) ⁽¹⁷⁾ twp Write Command Pulse Width ⁽¹⁷⁾ 8 — 10 — ns	trcs	Read Command Setup Time(17, 20)	0	_	0	_	ns
twch Write Command Hold Time (17) 8 — 10 — ns twch Write Command Hold Time 40 — 50 — ns (referenced to RAS)(17) twp Write Command Pulse Width(17) 8 — 10 — ns	trrh		0	_	0	_	ns
twch Write Command Hold Time ⁽¹⁷⁾ 8 — 10 — ns twcn Write Command Hold Time (referenced to RAS) ⁽¹⁷⁾ 40 — 50 — ns twp Write Command Pulse Width ⁽¹⁷⁾ 8 — 10 — ns	tпсн		0	_	0	_	ns
(referenced to RAS) ⁽¹⁷⁾ twp Write Command Pulse Width ⁽¹⁷⁾ 8 — 10 — ns	twch	Write Command Hold Time(17)	8		10		ns
	twcr		40	_	50	_	ns
twpz WE Pulse Widths to Disable Outputs 7 — 7 — ns	twp	Write Command Pulse Width(17)	8	_	10		ns
	twpz	WE Pulse Widths to Disable Outputs	7	_	7		ns



AC CHARACTERISTICS (Continued)(1,2,3,4,5,6)

(Recommended Operating Conditions unless otherwise noted.)

		-5	60	-60)	
Symbol	Parameter	Min.	Max.	Min.	Max.	Units
trwL	Write Command to RAS Lead Time(17)	13	_	15	_	ns
tcwL	Write Command to CAS Lead Time(17, 21)	8		10	_	ns
twcs	Write Command Setup Time(14, 17, 20)	0	_	0	_	ns
tdhr	Data-in Hold Time (referenced to RAS)	39	_	39	_	ns
tach	Column-Address Setup Time to CAS Precharge during WRITE Cycle	15	_	15	_	ns
tоен	OE Hold Time from WE during READ-MODIFY-WRITE cycle ⁽¹⁸⁾	8	_	10	_	ns
tos	Data-In Setup Time(15, 22)	0	_	0	_	ns
tDH	Data-In Hold Time(15, 22)	8	_	10	_	ns
trwc	READ-MODIFY-WRITE Cycle Time	108	_	133	_	ns
trwd	RAS to WE Delay Time during READ-MODIFY-WRITE Cycle ⁽¹⁴⁾	64	_	77	_	ns
tcwp	CAS to WE Delay Time(14, 20)	26		32	_	ns
tawd	Column-Address to WE Delay Time(14)	39	_	47	_	ns
tPC	EDO Page Mode READ or WRITE Cycle Time	20	_	25	_	ns
trasp	RAS Pulse Width in EDO Page Mode	50	100K	60	100K	ns
tcpa	Access Time from CAS Precharge(15)	_	30	_	35	ns
tprwc	EDO Page Mode READ-WRITE Cycle Time	56	_	68	_	ns
tсон	Data Output Hold after CAS LOW	5	_	5	_	ns
toff	Output Buffer Turn-Off Delay from CAS or RAS (13,15,19, 24)	0	12	0	15	ns
twnz	Output Disable Delay from WE	3	10	3	10	ns
tcsr	CAS Setup Time (CBR REFRESH)(20, 25)	5	_	5	_	ns
tchr	CAS Hold Time (CBR REFRESH)(21, 25)	8	_	10	_	ns
tord	OE Setup Time prior to RAS during HIDDEN REFRESH Cycle	0	_	0	_	ns
tref	Auto Refresh Period 2,048 Cycles 4,096 Cycles	_	32 64	_	32 64	ms
tт	Transition Time (Rise or Fall)(2, 3)	1	50	1	50	ns

AC TEST CONDITIONS

Output load: Two TTL Loads and 50 pF

Input timing reference levels: $V_{IH} = 2.4V$, $V_{IL} = 0.8V$ Output timing reference levels: $V_{OH} = 2.0V$, $V_{OL} = 0.8V$

IS41C4400x IS41LV4400x Series

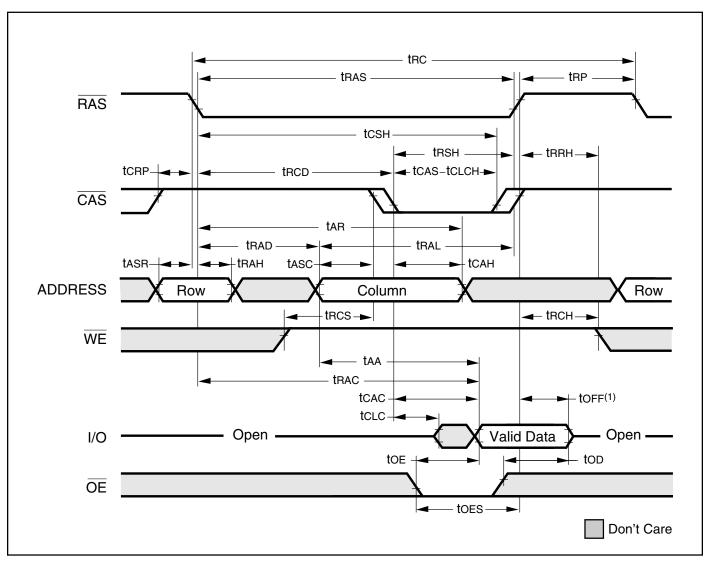


Notes:

- 1. An initial pause of 200 µs is required after power-up followed by eight \overline{RAS} refresh cycle (\overline{RAS} -Only or CBR) before proper device operation is assured. The eight \overline{RAS} cycles wake-up should be repeated any time the tree refresh requirement is exceeded.
- 2. ViH (MIN) and ViL (MAX) are reference levels for measuring timing of input signals. Transition times, are measured between ViH and ViL (or between ViH and ViH) and assume to be 1 ns for all inputs.
- 3. In addition to meeting the transition rate specification, all input signals must transit between V_IH and V_IL (or between V_IL and V_IH) in a monotonic manner.
- 4. If \overline{CAS} and $\overline{RAS} = V_{IH}$, data output is High-Z.
- 5. If $\overline{CAS} = V_{IL}$, data output may contain data from the last valid READ cycle.
- 6. Measured with a load equivalent to one TTL gate and 50 pF.
- 7. Assumes that troo troo (MAX). If troo is greater than the maximum recommended value shown in this table, trac will increase by the amount that troo exceeds the value shown.
- 8. Assumes that trcp trcp (MAX).
- 9. If CAS is LOW at the falling edge of RAS, data out will be maintained from the previous cycle. To initiate a new cycle and clear the data output buffer, CAS and RAS must be pulsed for tcp.
- 10. Operation with the troo (MAX) limit ensures that trac (MAX) can be met. troo (MAX) is specified as a reference point only; if troo is greater than the specified troo (MAX) limit, access time is controlled exclusively by trac.
- 11. Operation within the trad (MAX) limit ensures that trad (MAX) can be met. trad (MAX) is specified as a reference point only; if trad is greater than the specified trad (MAX) limit, access time is controlled exclusively by trad.
- 12. Either trich or trinh must be satisfied for a READ cycle.
- 13. toff (MAX) defines the time at which the output achieves the open circuit condition; it is not a reference to Voh or Vol.
- 14. twcs, trwb, tawb and tcwb are restrictive operating parameters in LATE WRITE and READ-MODIFY-WRITE cycle only. If twcs twcs (MIN), the cycle is an EARLY WRITE cycle and the data output will remain open circuit throughout the entire cycle. If trwb trwb (MIN), tawb tawb (MIN) and tcwb tcwb (MIN), the cycle is a READ-WRITE cycle and the data output will contain data read from the selected cell. If neither of the above conditions is met, the state of I/O (at access time and until CAS and RAS or OE go back to Vih) is indeterminate. OE held HIGH and WE taken LOW after CAS goes LOW result in a LATE WRITE (OE-controlled) cycle.
- 15. Output parameter (I/O) is referenced to corresponding CAS input.
- 16. During a READ cycle, if OE is LOW then taken HIGH before CAS goes HIGH, I/O goes open. If OE is tied permanently LOW, a LATE WRITE or READ-MODIFY-WRITE is not possible.
- 17. Write command is defined as WE going low.
- 18. LATE WRITE and READ-MODIFY-WRITE cycles must have both top and toeh met (OE HIGH during WRITE cycle) in order to ensure that the output buffers will be open during the WRITE cycle. The I/Os will provide the previously written data if CAS remains LOW and OE is taken back to LOW after toeh is met.
- 19. The I/Os are in open during READ cycles once top or toff occur.
- 20. Determined by falling edge of CAS.
- 21. Determined by rising edge of CAS.
- 22. These parameters are referenced to $\overline{\text{CAS}}$ leading edge in EARLY WRITE cycles and $\overline{\text{WE}}$ leading edge in LATE WRITE or READ-MODIFY-WRITE cycles.
- 23. CAS must meet minimum pulse width.
- 24. The 3 ns minimum is a parameter guaranteed by design.
- 25. Enables on-chip refresh and address counters.



READ CYCLE

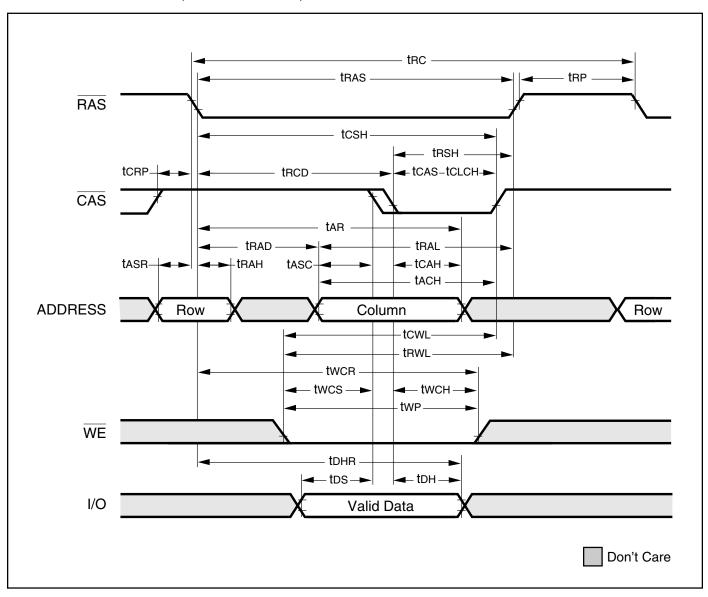


Note:

1. toff is referenced from rising edge of \overline{RAS} or \overline{CAS} , whichever occurs last.

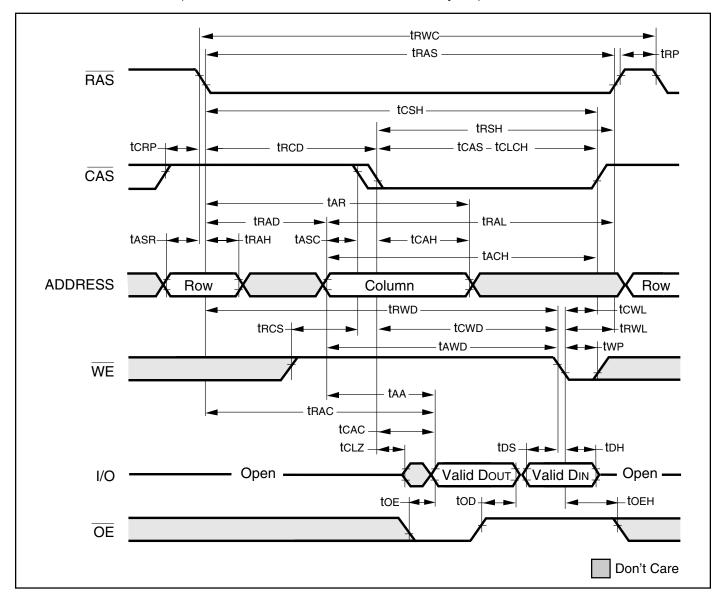


EARLY WRITE CYCLE (OE = DON'T CARE)



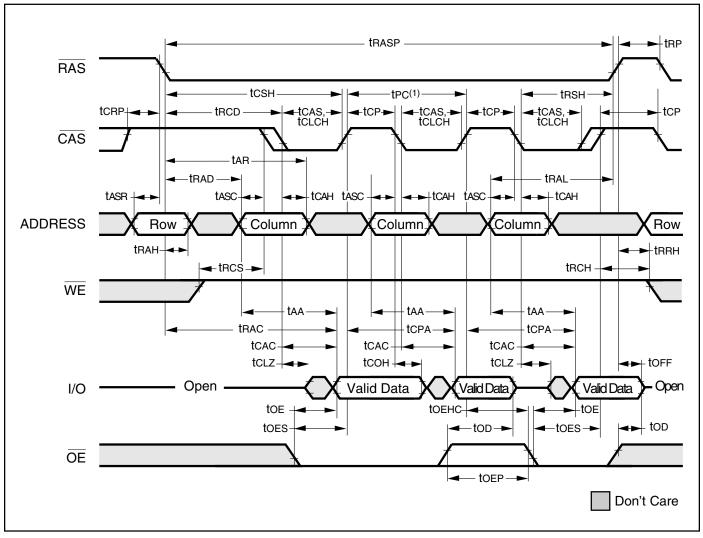


READ WRITE CYCLE (LATE WRITE and READ-MODIFY-WRITE Cycles)





EDO-PAGE-MODE READ CYCLE

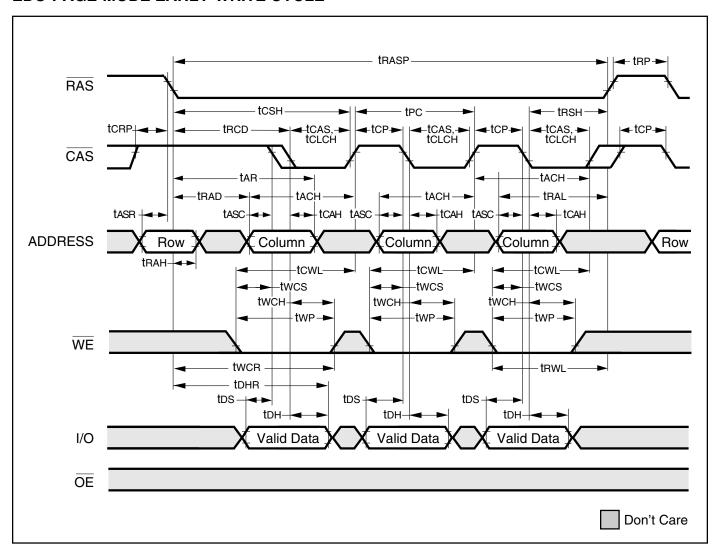


Note:

1. trc can be measured from falling edge of \overline{CAS} to falling edge of \overline{CAS} , or from rising edge of \overline{CAS} to rising edge of \overline{CAS} . Both measurements must meet the trc specifications.

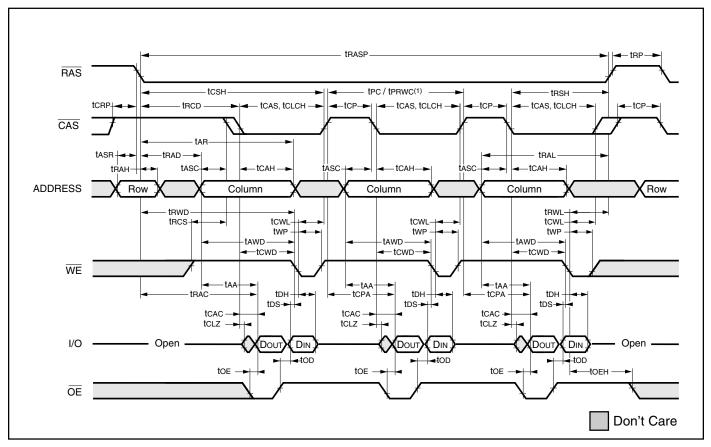


EDO-PAGE-MODE EARLY-WRITE CYCLE





EDO-PAGE-MODE READ-WRITE CYCLE (LATE WRITE and READ-MODIFY WRITE Cycles)

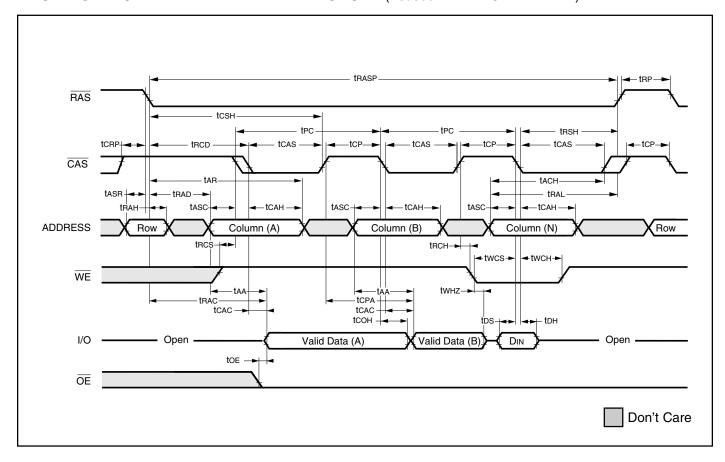


Note:

1. tec can be measured from falling edge of \overline{CAS} to falling edge of \overline{CAS} , or from rising edge of \overline{CAS} to rising edge of \overline{CAS} . Both measurements must meet the tec specifications.



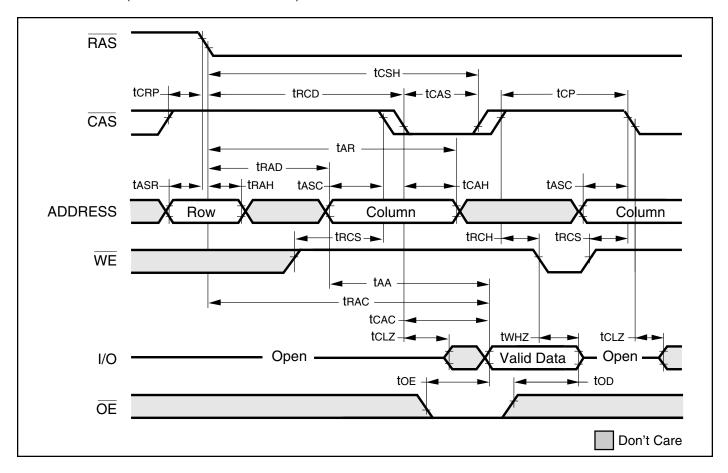
EDO-PAGE-MODE READ-EARLY-WRITE CYCLE (Psuedo READ-MODIFY WRITE)



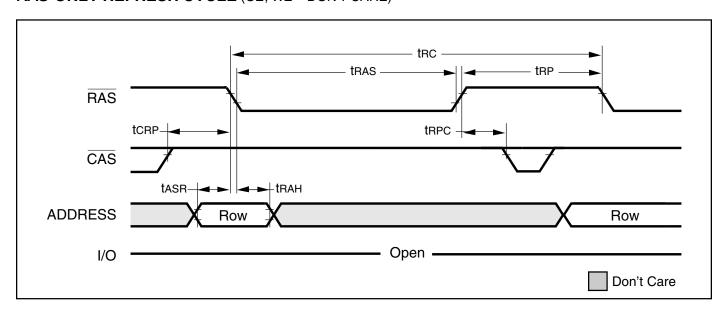


AC WAVEFORMS

READ CYCLE (With WE-Controlled Disable)

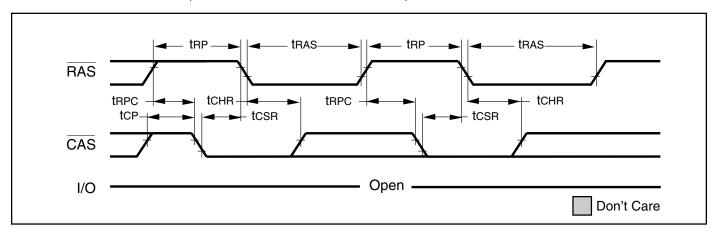


RAS-ONLY REFRESH CYCLE (OE, WE = DON'T CARE)

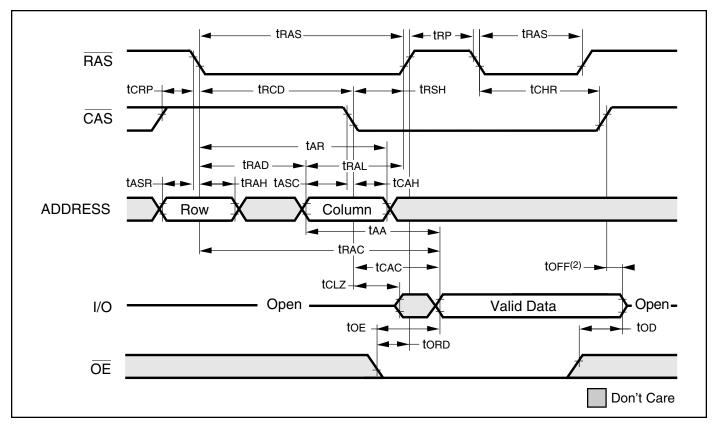




CBR REFRESH CYCLE (Addresses; WE, OE = DON'T CARE)



HIDDEN REFRESH CYCLE(1) (WE = HIGH; OE = LOW)



Notes:

- 1. A Hidden Refresh may also be perfor<u>med</u> after a Write Cycle. In this case, $\overline{WE} = LOW$ and $\overline{OE} = HIGH$.
- 2. toff is referenced from rising edge of RAS or CAS, whichever occurs last.



ORDERING INFORMATION

Commercial Range: 0°C to 70°C

Voltage: 5V

Speed (ns)	Order Part No.	Refresh	Package
50	IS41C44002-50J	2K	300-mil SOJ
60	IS41C44002-60J	2K	300-mil SOJ

Speed (ns)	Order Part No.	Refresh	Package
50	IS41C44004-50J	4K	300-mil SOJ
60	IS41C44004-60J	4K	300-mil SOJ

Voltage: 3.3V

Speed (ns)	Order Part No.	Refresh	Package
50	IS41LV44002-50J	2K	300-mil SOJ
60	IS41LV44002-60J	2K	300-mil SOJ

Speed (ns)	Order Part No.	Refresh	Package
50	IS41LV44004-50J	4K	300-mil SOJ
60	IS41LV44004-60J	4K	300-mil SOJ



ORDERING INFORMATION

Industrial Range: -40°C to 85°C

Voltage: 5V

Speed (ns)	Order Part No.	Refresh	Package
50	IS41C44002-50JI	2K	300-mil SOJ
60	IS41C44002-60JI	2K	300-mil SOJ

Speed (ns)	Order Part No.	Refresh	Package
50	IS41C44004-50JI	4K	300-mil SOJ
60	IS41C44004-60JI	4K	300-mil SOJ

Voltage: 3.3V

Speed (ns)	Order Part No.	Refresh	Package
50	IS41LV44002-50JI	2K	300-mil SOJ
60	IS41LV44002-60JI	2K	300-mil SOJ

Speed (ns)	Order Part No.	Refresh	Package
50	IS41LV44004-50JI	4K	300-mil SOJ
60	IS41LV44004-60JI	4K	300-mil SOJ



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