4Meg x 32
128-MBIT DDR SDRAM

PRELIMINARY INFORMATION
FEBRUARY 2006

FEATURES

- Clock Frequency: 200, 166, 100 MHz
- Power supply (V_{DD} and V_{DDQ}): 2.5V
- SSTL 2 interface
- Four internal banks to hide row Pre-charge and Active operations
- Commands and addresses register on positive clock edges (CLK)
- Bi-directional Data Strobe signal for data capture
- Differential clock inputs (CLK and $\overline{CLK}$) for two data accesses per clock cycle
- Data Mask feature for Writes supported
- DLL aligns data I/O and Data Strobe transitions with clock inputs
- Half-strength and Matched drive strength options
- Programmable burst length for Read and Write operations
- Programmable CAS Latency (3, 4, 5 clocks)
- Programmable burst sequence: sequential or interleaved

- Burst concatenation and truncation supported for maximum data throughput
- Auto Pre-charge option for each Read or Write burst
- 4096 refresh cycles every 32ms
- Auto Refresh and Self Refresh Modes
- Pre-charge Power Down and Active Power Down Modes
- Industrial Temperature Availability
- Lead-free Availability

DEVICE OVERVIEW

ISSI's 128-Mbit DDR SDRAM achieves high-speed data transfer using pipeline architecture and two data word accesses per clock cycle. The 134,217,728-bit memory array is internally organized as four banks of 32M-bit to allow concurrent operations. The pipeline allows Read and Write burst accesses to be virtually continuous, with the option to concatenate or truncate the bursts. The programmable features of burst length, burst sequence and CAS latency enable further advantages. The device is available in 32-bit data word size. Input data is registered on the I/O pins on both edges of Data Strobe signal(s), while output data is referenced to both edges of Data Strobe and both edges of CLK. Commands are registered on the positive edges of CLK. Auto Refresh, Active Power Down, and Pre-charge Power Down modes are enabled by using clock enable (CKE) and other inputs in an industry-standard sequence. All input and output voltage levels are compatible with SSTL 2.

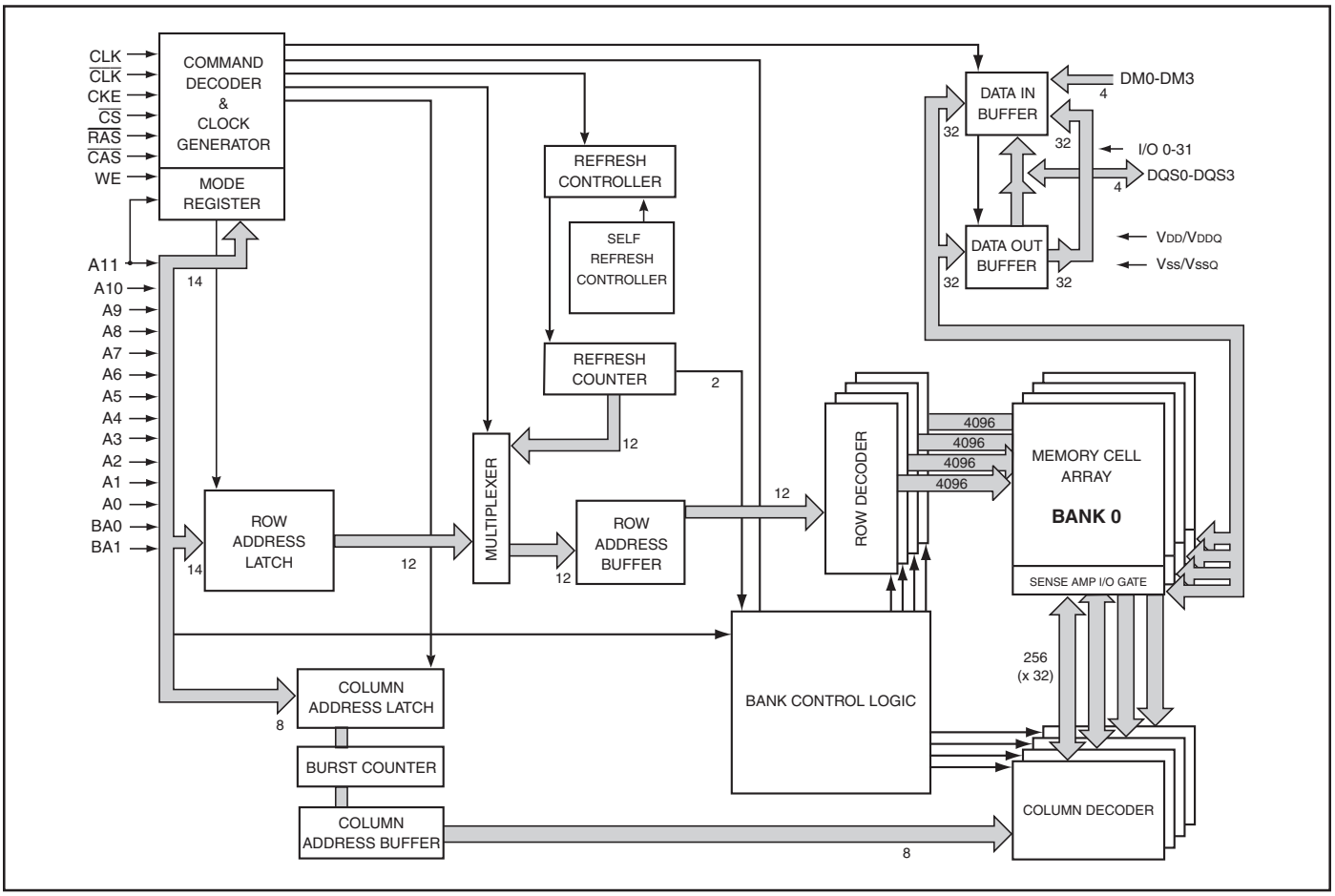
IS43R32400A

1M x32x4 Banks
V_{DD}: 2.5V
V_{DDQ}: 2.5V
144-ball BGA

KEY TIMING PARAMETERS

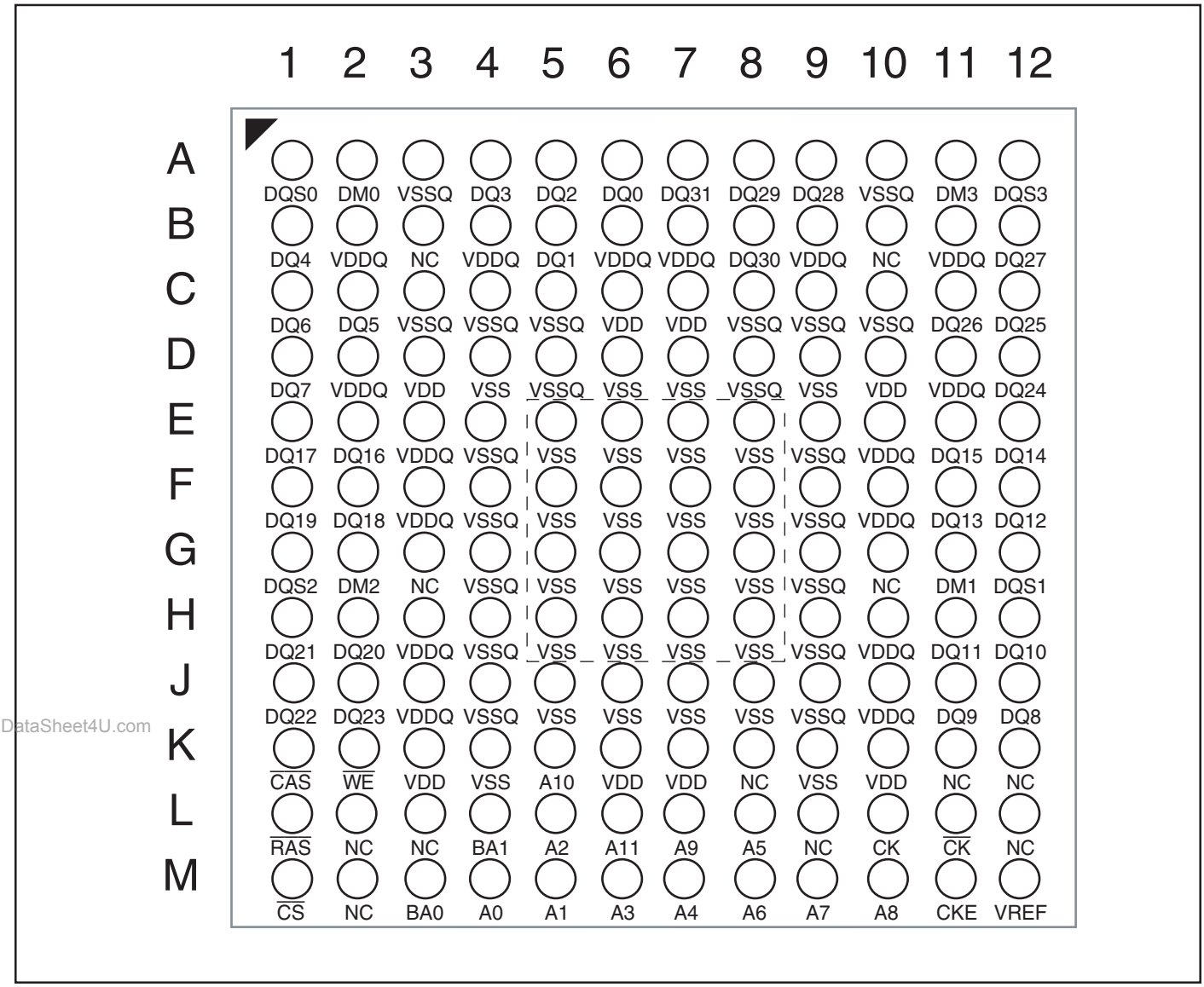
Parameter	-5	-6	Unit
CLK Cycle Time (min.)			
$\overline{CAS}$ Latency = 5	5	6	ns
$\overline{CAS}$ Latency = 4	5	6	ns
$\overline{CAS}$ Latency = 3	5	6	ns
CLK Frequency (max.)			
$\overline{CAS}$ Latency = 5	200	166	MHz
$\overline{CAS}$ Latency = 4	200	166	MHz
$\overline{CAS}$ Latency = 3	200	166	MHz

FUNCTIONAL BLOCK DIAGRAM (x32)



PIN CONFIGURATION

PACKAGE CODE: B 144-BALL FBGA (Top View)
(12.00 mm x 12.00 mm Body, 0.8 mm Ball Pitch)



	1	2	3	4	5	6	7	8	9	10	11	12
A	DQS0	DM0	VSSQ	DQ3	DQ2	DQ0	DQ31	DQ29	DQ28	VSSQ	DM3	DQS3
B	DQ4	VDDQ	NC	VDDQ	DQ1	VDDQ	VDDQ	DQ30	VDDQ	NC	VDDQ	DQ27
C	DQ6	DQ5	VSSQ	VSSQ	VSSQ	VDD	VDD	VSSQ	VSSQ	VSSQ	DQ26	DQ25
D	DQ7	VDDQ	VDD	VSS	VSSQ	VSS	VSS	VSSQ	VSS	VDD	VDDQ	DQ24
E	DQ17	DQ16	VDDQ	VSSQ	VSS	VSS	VSS	VSS	VSSQ	VDDQ	DQ15	DQ14
F	DQ19	DQ18	VDDQ	VSSQ	VSS	VSS	VSS	VSS	VSSQ	VDDQ	DQ13	DQ12
G	DQS2	DM2	NC	VSSQ	VSS	VSS	VSS	VSS	VSSQ	NC	DM1	DQS1
H	DQ21	DQ20	VDDQ	VSSQ	VSS	VSS	VSS	VSS	VSSQ	VDDQ	DQ11	DQ10
J	DQ22	DQ23	VDDQ	VSSQ	VSS	VSS	VSS	VSS	VSSQ	VDDQ	DQ9	DQ8
K	$\overline{CAS}$	$\overline{WE}$	VDD	VSS	A10	VDD	VDD	NC	VSS	VDD	NC	NC
L	$\overline{RAS}$	NC	NC	BA1	A2	A11	A9	A5	NC	CK	$\overline{CK}$	NC
M	$\overline{CS}$	NC	BA0	A0	A1	A3	A4	A6	A7	A8	CKE	VREF

Note: Vss balls inside the dotted box are optional for purposes of thermal dissipation.

PIN FUNCTIONS

Symbol	Type	Function (In Detail)
A0-A11	Input Pin	Address inputs are sampled during several commands. During an Active command, A0-A11 select a row to open. During a Read or Write command, A0-A7 select a starting column for a burst. During a Pre-charge command, A8 determines whether all banks are to be pre-charged, or a single bank. During a Load Mode Register command, the address inputs select an operating mode.
BA0, BA1	Input Pin	Bank Address inputs are used to select a bank during Active, Pre-charge, Read, or Write commands. During a Load Mode Register command, BA0 and BA1 are used to select between the Base or Extended Mode Register
$\overline{CAS}$	Input Pin	$\overline{CAS}$ is Column Access Strobe, which is an input to the device command along with $\overline{RAS}$ and $\overline{WE}$. See "Command Truth Table" for details.
CKE	Input Pin	Clock Enable: CKE High activates and CKE Low de-activates internal clock signals and input/output buffers. When CKE goes Low, it can allow Self Refresh, Pre-charge Power Down, and Active Power Down. CKE must be High during entire Read and Write accesses. Input buffers except CLK, $\overline{CLK}$, and CKE are disabled during Power Down. CKE uses an SSTL 2 input, but will detect a LVCMOS Low level after VDD is applied.
CLK, $\overline{CLK}$	Input Pin	All address and command inputs are sampled on the rising edge of the clock input CLK and the falling edge of the differential clock input $\overline{CLK}$. Output data is referenced from the crossings of CLK and $\overline{CLK}$.
$\overline{CS}$	Input Pin	The Chip Select input enables the Command Decoding block of the device. When $\overline{CS}$ is disabled, a NOP occurs. See "Command Truth Table" for details. Multiple DDR SDRAM devices can be managed with $\overline{CS}$.
DM0-DM3	Input Pin	These are the Data Mask inputs. During a Write operation, the Data Mask input allows masking of the data bus. DM is sampled on each edge of DQS. There are four Data Mask input pins for the x32 DDR SDRAM. Each input applies to DQ0-DQ7, DQ8-DQ15, DQ16-DQ23, or DQ24-DQ31.
DQS0-DQS3	Input/Output Pin	These are the Data Strobe inputs. The Data Strobe is used for data capture. During a Read operation, the DQS output signal from the device is edge-aligned with valid data on the data bus. During a Write operation, the DQS input should be issued to the DDR SDRAM device when the input values on DQ inputs are stable. There are four Data Strobe pins for the x32 DDR SDRAM. Each of the four Data Strobe pins applies to DQ0-DQ7, DQ8-DQ15, DQ16-DQ23, or DQ24-DQ31.
DQ0-DQ31	Input/Output Pin	The pins DQ0 to DQ31 represent the data bus. For Write operations, the data bus is sampled on Data Strobe. For Read operations, the data bus is sampled on the crossings of CK and $\overline{CK}$.
NC	—	No Connect: This pin should be left floating. These pins could be used for 256Mbit or higher density DDR SDRAM.
$\overline{RAS}$	Input Pin	$\overline{RAS}$ is Row Access Strobe, which is an input to the device command along with $\overline{CAS}$ and $\overline{WE}$. See "Command Truth Table" for details.
$\overline{WE}$	Input Pin	$\overline{WE}$ is Write Enable, which is an input to the device command along with $\overline{RAS}$ and $\overline{CAS}$. See "Command Truth Table" for details.
VDDQ	Power Supply Pin	VDDQ is the output buffer power supply.
VDD	Power Supply Pin	VDD is the device power supply.
VREF	Power Supply Pin	VREF is the reference voltage for SSTL 2.
VSSQ	Power Supply Pin	VSSQ is the output buffer ground.
VSS	Power Supply Pin	VSS is the device ground.

COMMAND TRUTH TABLE

Function	CKE (n - 1)	CKE (n)	$\overline{CS}$	RAS	$\overline{CAS}$	$\overline{WE}$	BA1	BA0	Address
Device Deselect (NOP)	H	x	H	x	x	x	x	x	x
No Operation (NOP)	H	x	L	H	H	H	x	x	x
Burst Stop(2)	H	H	L	H	H	L	x	x	x
Read(3)	H	x	L	H	L	H	V	V	V
Write(3)	H	x	L	H	L	L	V	V	V
Bank and Row Activate	H	x	L	L	H	H	V	V	V
Pre-charge select bank	H	x	L	L	H	L	V	V	x
Pre-charge all banks	H	x	L	L	H	L	x	x	x
Load Mode Register (Base)	H	x	L	L	L	L	L	L	V
Load Extended Mode Register	H	x	L	L	L	L	L	H	V
Auto Refresh	H	x	L	L	L	H	x	x	x
Self Refresh	L	x	L	L	L	H	x	x	x

Notes:
1. H = VIH, L = VIL, x = VIH or VIL, V = Valid Data.
2. This command only applies to Read command with Auto Pre-charge disabled.
3. Auto Pre-charge is enabled with A8 = H (x32).

DATA MASK TRUTH TABLE

Function	CKE (n - 1)	CKE (n)	DM0	DM1	DM2	DM3
Write Enable for Data Byte DQ_0-DQ_7	H	x	L	x	x	x
Write Disable for Data Byte DQ_0-DQ_7	H	x	H	x	x	x
Write Enable for Data Byte DQ_8-DQ_{15}	H	x	x	L	x	x
Write Disable for Data Byte DQ_8-DQ_{15}	H	x	x	H	x	x
Write Enable for Data Byte DQ_{16}-DQ_{23}	H	x	x	x	L	x
Write Disable for Data Byte DQ_{16}-DQ_{23}	H	x	x	x	H	x
Write Enable for Data Byte DQ_{24}-DQ_{31}	H	x	x	x	x	L
Write Disable for Data Byte DQ_{24}-DQ_{31}	H	x	x	x	x	H

Notes:
1. H = VIH, L = VIL, x = VIH or VIL, V = Valid Data.

DETAILED COMMAND TRUTH TABLE - SAME BANKS

Function (n)	Command (n)	Prior State (n - 1)	CKE (n - 1)	CKE (n)	$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$
NOP or Continue previous operation	Deselect	Any	H	H	H	X	X	X
NOP or Continue previous operation	NOP	Any	H	H	L	H	H	H
Activate row	Active	Idle	H	H	L	L	H	H
Issue Auto Refresh	Auto Refresh	Idle	H	H	L	L	L	H
Load the Base/ Extended Mode Register	Load Mode Register	Idle	H	H	L	L	L	L
Start Read Burst	Read	Row active	H	H	L	H	L	H
	Read	Read underway	H	H	L	H	L	H
	Read	Write underway	H	H	L	H	L	H
Start Write Burst	Write	Row active	H	H	L	H	L	L
	Write[1]	Read underway	H	H	L	H	L	L
	Write	Write underway	H	H	L	H	L	L
De-activate Row, start Pre-charge	Pre-charge	Row active	H	H	L	L	H	L
Truncate Read Burst, start Pre-charge	Pre-charge	Read underway	H	H	L	L	H	L
Truncate Write Burst, start Pre-charge	Pre-charge	Write underway	H	H	L	L	H	L
Terminate Read Burst	Burst Terminate	Read underway	H	H	L	H	H	L

Note:
1. A Write command may be terminated only at the completion of the Read burst. However, a Burst Terminate can be transmitted to end the Read burst early so that a Write command can be asserted.

DETAILED COMMAND TRUTH TABLE - DIFFERENT BANKS (bank b, then bank g)

Function (n)	Command (n)	Prior State (n - 1)	CKE (n - 1)	CKE (n)	$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$
NOP or Continue previous operation	Deselect	Any	H	H	H	X	X	X
NOP or Continue previous operation	NOP	Any	H	H	L	H	H	H
Issue any command to bank g otherwise valid	Any command	Idle	H	H	X	X	X	X
Start Read Burst in bank g	Read	Row in bank b active, activating, or pre-charging	H	H	L	H	L	H
	Read	Read underway in bank b (Auto Pre-charge disabled)	H	H	L	H	L	H
	Read	Write underway in bank b (Auto Pre-charge disabled)	H	H	L	H	L	H
	Read	Read underway in bank b (Auto Pre-charge enabled)	H	H	L	H	L	H
	Read	Write underway in bank b (Auto Pre-charge enabled)	H	H	L	H	L	H
Start Write Burst in bank g	Write	Row in bank b active, activating, or pre-charging	H	H	L	H	L	L
	Write[1]	Read underway in bank b (Auto Pre-charge disabled)	H	H	L	H	L	L
	Write	Write underway in bank b (Auto Pre-charge disabled)	H	H	L	H	L	L
	Write[1]	Read underway in bank b (Auto Pre-charge enabled)	H	H	L	H	L	L
	Write	Write underway in bank b (Auto Pre-charge enabled)	H	H	L	H	L	L

DETAILED COMMAND TRUTH TABLE - DIFFERENT BANKS (bank b, then bank g) -cont.

Function (n)	Command (n)	Prior State (n - 1)	CKE (n - 1)	CKE (n)	$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$
Start Pre-charge	Pre-charge	Row in bank b active, activating, or pre-charging	H	H	L	L	H	L
	Pre-charge	Read underway in bank b (Auto Pre-charge disabled)	H	H	L	L	H	L
	Pre-charge	Write underway in bank b (Auto Pre-charge disabled)	H	H	L	L	H	L
	Pre-charge	Read underway in bank b (Auto Pre-charge enabled)	H	H	L	L	H	L
	Pre-charge	Write underway in bank b (Auto Pre-charge enabled)	H	H	L	L	H	L

Note:
1. A Write command may be terminated only at the completion of the Read burst. However, a Burst Terminate can be transmitted to end the Read burst early so that a Write command can be asserted.

DETAILED COMMAND TRUTH TABLE - LOW POWER MODES

Function (n)	Command (n)	Prior State (n - 1)	CKE (n - 1)	CKE (n)	$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$
Maintain Power Down	don't care	Power Down Mode	L	L	X	X	X	X
Maintain Self Refresh	don't care	Self Refresh Mode	L	L	X	X	X	X
Exit Power Down	Deselect or NOP	Power Down	L	H	X	X	X	X
Exit Self Refresh Mode	Deselect or NOP	Self Refresh Mode	L	H	X	X	X	X
Enter Pre-Charge Power Down Mode	Deselect or NOP	All Banks Idle	H	L	X	X	X	X
Enter Active Power Down Mode	Deselect or NOP	Bank(s) Active	H	L	X	X	X	X
Enter Self Refresh Mode	Auto Refresh	All Banks Idle	H	L	L	L	L	H

ABSOLUTE MAXIMUM RATINGS(1)

Symbol	Parameters		Rating	Unit
$V_{DD\ MAX}$	Maximum Supply Voltage		–0.3 to +3.6	V
$V_{DDQ\ MAX}$	Maximum Supply Voltage for Output Buffer		0.3 to +3.6	V
V_{IN}, V_{REF}	Input Voltage, Reference Voltage		–0.3 to V_{DDQ} + 0.3	V
V_{OUT}	Output Voltage		–0.3 to V_{DDQ} + 0.3	V
$P_{D\ MAX}$	Allowable Power Dissipation		2	W
I_{CS}	Output Shorted Current		50	mA
T_{OPR}	Operating Temperature	Com. Ind.	0 to +70 –40 to +85	°C
T_{STG}	Storage Temperature		–55 to +150	°C

Notes:
1. Stress greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
2. All voltages are referenced to Vss.

RECOMMENDED DC OPERATING CONDITIONS (SSTL_2 Input/Output, T_A = 0°C to +70°C)

Symbol	Parameter	Test Condition	Min	Typ.	Max	Unit
V_{DD}	Supply Voltage		2.375	2.500	2.625	V
V_{DDQ}	I/O Supply Voltage		2.375	2.500	2.625	V
V_{TT}	I/O Termination Voltage		V_{REF} - 0.04	V_{REF}	V_{REF} + 0.04	V
V_{IH}	Input High Voltage		V_{REF} + 0.15	—	V_{DDQ} + 0.3	V
V_{IL}	Input Low Voltage		V_{SSQ} - 0.3	—	V_{DDQ} - 0.15	V
V_{REF}	I/O Reference Voltage		0.49 x V_{DDQ}	0.5 x V_{DDQ}	0.51 x V_{DDQ}	V
I_{IL}	Input Leakage Current	0 ≤ V_{REF} ≤ V_{DD}, with all inputs at V_{SS}, except tested input	-5	—	5	µA
I_{OL}	Output Leakage Current	Output disabled; 0V ≤ V_{OUT} ≤ V_{DDQ}	-5	—	5	µA
V_{OH}	Output High Voltage Level	I_{OH} = -15.2mA	V_{TT} + 0.76	—	—	V
V_{OL}	Output Low Voltage Level	I_{OL} = +15.2mA	—	—	V_{REF} - 0.76	V

Note:
1. V_{DDQ} must always be less than or equal to V_{DD}.

CAPACITANCE CHARACTERISTICS (At T_A = 0 to +25°C, V_{DD} = V_{DDQ} = 2.5V, f = 1 MHz)

Symbol	Parameter	Min.	Max.	Unit
C_{IN1}	Input Capacitance: Address, B0, B1	4	5	pF
C_{IN2}	Input Capacitance:All other input pins	3	5	pF
C_{IN3}	Data Mask Input/Output Capacitance: DM0-DM3	6	8	pF
C_{OUT}	Data Input/Output Capacitance: DQ and DQS	6	8	pF

DC ELECTRICAL CHARACTERISTICS (V_{DD} = 2.5V +/- 5%, T_A = 0°C to +70°C)

Symbol	Parameter	Test Condition		Unit
I_{DD0}	Operating Current	One bank operation; Active-Precharge; DQ, DM and DQS inputs change once per clock cycle; Address and Control inputs change once per two clock cycles; tRC = tRC (min); tCK = tCK (min)	160	mA
I_{DD1}	Operating Current	One bank operation; Active-Read-Precharge; BL = 4; CL = 4; Address and Control inputs change once per clock cycle; tRCDRD = 4 x tCK; tRC = tRC (min); tCK = tCK (min); IOUT = 0mA;	240	mA
I_{DD2P}	Precharge Power-Down Standby Current	All banks Idle; tCK = tCK (min); CKE = Low	40	mA
I_{DD2N}	Idle Standby Current	All banks idle; Address and control inputs change once per clock cycle; CKE = High; $\overline{CS}$ = High (Deselect); VIN = VREF for DQ, DQS, and DM; tCK = tCK (min)	80	mA
I_{DD3P}	Active Power-Down Standby Current	One bank Active; CKE = Low; tCK = tCK (min)	40	mA
I_{DD3N}	Active Standby Current	One bank Active; $\overline{CS}$ = High; CKE = High; Address and Control inputs change once per clock cycle; DQ, DQS, and DM change twice per clock cycle; tRC = tRC (max); tCK = tCK (min)	100	mA
I_{DD4R}	Operating Current Burst Read	One bank Active; BL = 2; Address and Control inputs change once per clock cycle; tCK = tCK (min); IOUT = 0mA	420	mA
I_{DD4W}	Operating Current Burst Write	One bank Active; BL = 2; Address and Control inputs change once per clock cycle; DQ, DQS, DM change twice per clock cycle; tCK = tCK (min)	270	mA
I_{DD5}	Auto Refresh Current	tRC = tRFC (min); tCK = tCK (min)	280	mA
I_{DD6}	Self Refresh Current	CKE ≤ 0.2V; tCK = tCK (min)	3	mA
I_{DD7}	Operating Current	Four bank interleaved Reads with Auto Precharge; BL = 4; Address and Controls inputs change per Read, Write, or Active command; tRC = tRC (min); tCK = tCK (min)	550	mA

Notes:

1.Operating outside the “Absolute Maximum Ratings” may lead to temporary or permanent device failure.

2.Power up sequence describe in “Initialization” section.

3. All voltages are referenced to V_{SS}.

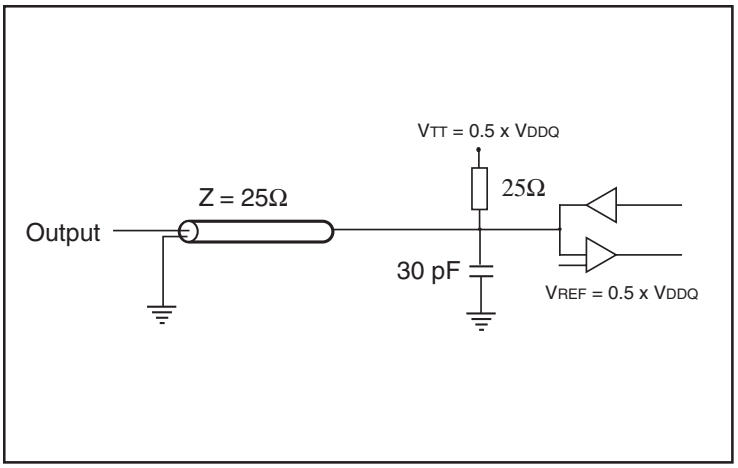
AC ELECTRICAL CHARACTERISTICS (V_{DD} = 2.5V +/- 5%, T_A = 0°C to +70°C)

			-5		-6		
Symbol	**Parameter**	**Test Condition**	**Min.**	**Max.**	**Min.**	**Max.**	**Unit**
tCK	Clock Cycle Time	CL = 3	5	10	6	10	ns
		CL = 4	5	10	6	10	ns
		CL = 5	5	10	6	10	ns
tCH	Clock High Level Width		0.45	0.55	0.45	0.55	tCK
tCL	Clock Low Level Width		0.45	0.55	0.45	0.55	tCK
tDQSCK	DQS-Out Access Time from CLK, $\overline{CLK}$		-0.7	0.7	-0.7	0.7	ns
tAC	Output Access Time from CLK, $\overline{CLK}$		-0.85	0.85	-0.85	0.85	ns
tDQSQ	DQS-DQ Skew		—	0.45	—	0.45	ns
tRPRE	Read Preamble		0.9	1.1	0.9	1.1	tCK
tRPST	Read Postamble		0.4	0.6	0.4	0.6	tCK
tDQSS	CLK to Valid DQS-In		0.85	1.15	0.85	1.15	tCK
tWPRES	DQS-In Setup Time		0	—	0	—	ns
tWPREH	DQS-In Hold Time		0.35	—	0.35	—	ns
tWPST	DQS Write Post Postamble		0.4	0.6	0.4	0.6	tCK
tDQSH	DQS-In High Level Pulse Width		0.4	0.6	0.4	0.6	tCK
tDQSL	DQS-In Low Level Pulse Width		0.4	0.6	0.4	0.6	tCK
tIS	Address and Control Input Setup Time		0.9	—	0.9	—	ns
tDS	DQ and DM Setup Time to DQS		0.5	—	0.5	—	ns
tDH	DQ and DM Hold Time to DQS		0.7	—	0.7	—	ns
tHP	Clock Half Period		tCH or tCL	—	tCH or tCL	—	ns
tQH	Output DQS Valid Window		tHP - 0.5	—	tHP - 0.55	—	ns
tRC	Row Cycle Time		12	—	11	—	tCK
tRFC	Refresh Row Cycle Time		14	—	12	—	tCK
tRAS	Row Active Time		8	100K	7	120K	tCK
tRCDRD	$\overline{RAS}$ to $\overline{CAS}$ Delay in Read		4	—	4	—	tCK
tRCDWR	$\overline{RAS}$ to $\overline{CAS}$ Delay in Write		2	—	2	—	tCK
tRP	Row Pre-charge Time		3	—	3	—	tCK
tRRD	Row Active to Row Active Delay		2	—	2	—	tCK
tWR	Write Recovery Time		2	—	2	—	tCK
tCDLR	Last Data-In to Read Command		2	—	2	—	tCK
tCCD	Column Address to Column Address Delay		1	—	1	—	tCK
tMRD	Mode Register Load Delay		2	—	2	—	tCK
tDAL	Auto Pre-charge Write Recovery + Pre-charge		7	—	7	—	tCK
tXSA	Self Refresh Exit to Read Command Delay		200	—	200	—	tCK
tPDEX	Power Down Exit Time		tIS + 2 x tCK	—	tIS + 2 x tCK	—	ns
tREF	Refresh Interval Time		—	7.8	—	7.8	µs

Notes:
1. Operating outside the "Absolute Maximum Ratings" may lead to temporary or permanent device failure.
2. Power up sequence describe in "Initialization" section.
3. All voltages are referenced to Vss.

AC TEST CONDITIONS

Output Load



AC TEST CONDITIONS

Parameter	Unit
Input Signal Levels	VREF + 0.4V / VREF - 0.4V
Input Signal Slew Rate	1V / ns
Input Timing Reference Level	VREF
Output Timing Measurement Reference Level	VTT
CLK and $\overline{CLK}$ Signal Maximum Peak Swing	1.5V
Reference Level of Input/Ouput Signals	0.5 x VDDQ

FUNCTIONAL DESCRIPTION

The 128Mbit DDR SDRAM is a high-speed CMOS device with four banks that operate at 2.5V. Each 32Mbit bank is organized as 4,096 rows of 256 columns for the x32 options. Pre-fetch architecture allows Read and Write accesses to be double-data rate and burst oriented. Accesses start at a selected column location and continue every half-clock cycle for a programmed number of times. The Read or Write operation begins with an Active command to transmit the selected bank and row (A0-A11 bits are sampled). This is followed by a Read or Write command to sample the address bits again to determine the first column to access. When access to the memory is not necessary, the device can be put into a Power Down mode in which current consumption is minimized. Prior to normal operation, the device must be initialized in a defined procedure to function properly. The following sections describe the steps of initialization, the mode register definitions, command descriptions, and device operation.

INITIALIZATION

The DDR SDRAM must be powered-on and initialized in a series of defined steps for proper operation. First, power is applied simultaneously to VDD and VDDQ. After these reaching stable values, a VREF is ramped up. If this sequence is not followed, latch-up could occur and cause damage to the device. The input CKE must be asserted and held to a LVCMOS Low level during this time to prevent unwanted commands from being executed. The outputs I/O and DQS remain in high impedance until driven during a normal operation. Once VDD, VDDQ, VREF, and CKE are stable values, the clock inputs can begin to be applied. For a time period of at least 200µs, valid CLK and $\overline{\text{CLK}}$ cycles must be applied prior to any command being issued to the device. CKE needs to then be raised to SSTL 2 logic High and issue a NOP or Deselect command to initialize the internal logic of the DRAM. Next, a Pre-charge All command is given to the device, followed by a NOP/Deselect command on each clock cycle for at least tRP. The Load Extended Mode Register should be issued to enable DLL, followed by another series of NOP/Deselect commands for at least tMRD. After this time, the Load Mode Register command should be issued to reset the DLL, again followed by a series of NOP or Deselect commands for at least tMRD. (Note: whenever the DLL is reset, 200 clock cycles must occur prior to any Read command.) The Pre-charge command is then issued, with NOP/Deselect commands for at least tRP. Next, two Auto-Refresh commands are issued, each followed by NOP/Deselect commands for at least tRFC. At this point, the JEDEC specification recommends that a DDR SDRAM receive another Load Mode Register command to clear the DLL, with NOP/Deselect commands for at least tMRD. The device is now ready to receive a valid command for normal operation.

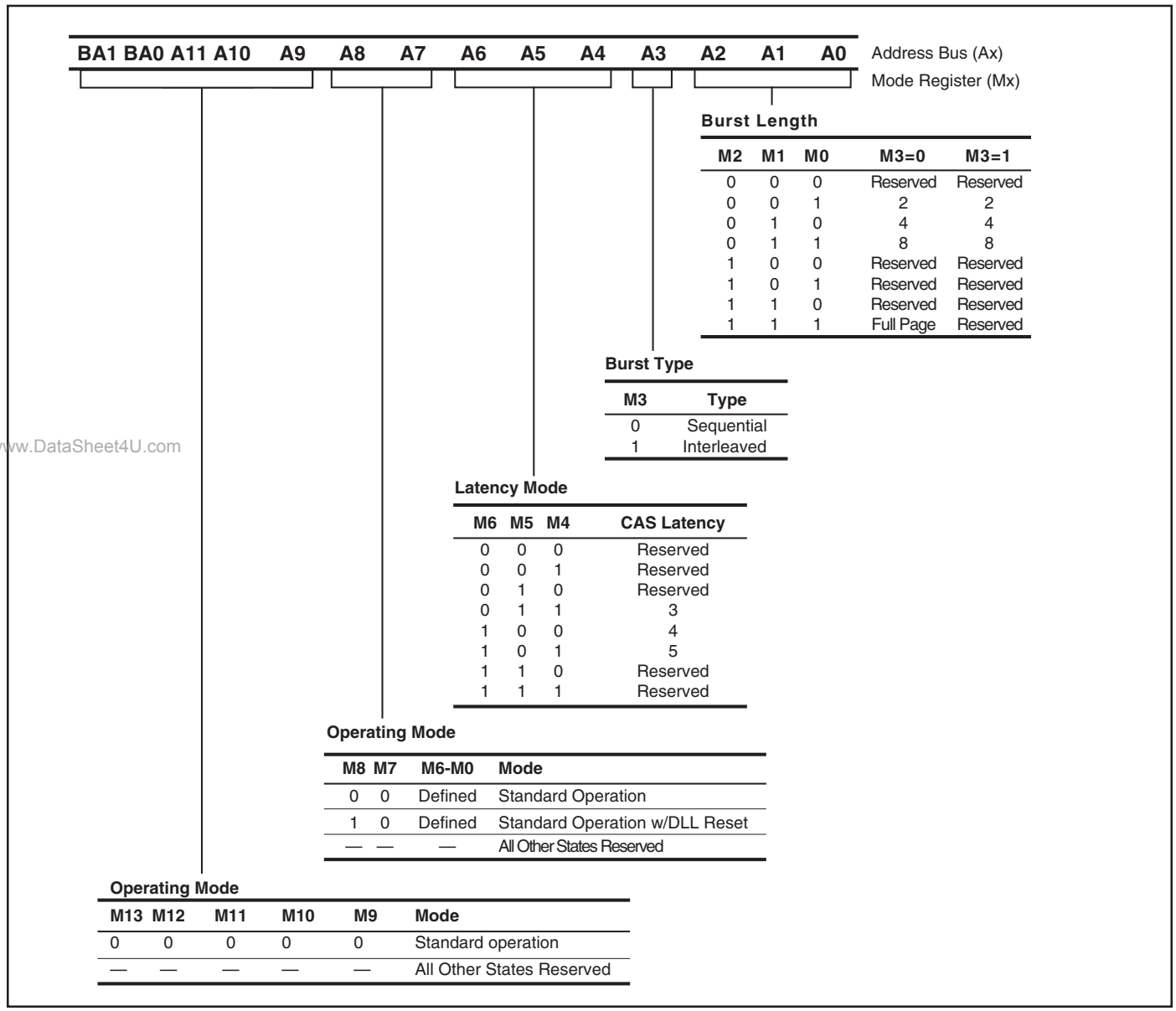
MODE REGISTER DEFINITION

The mode register allows configuration of the operating mode of the DDR SDRAM. This register is loaded as a step in the normal initialization of the device. The Load Mode Register command samples the values on inputs A0-A11, BA0 (Low) and BA1 (Low) and stores them as register values M0-M13. The values in the register determine the burst length, burst type, CAS latency timing, and DLL Reset/Clear. It should be noted that some bit values are reserved and should not be loaded into the register. The data in the mode register is retained until it is re-loaded or the DDR SDRAM loses its power (except for bit M8, which is cleared automatically). The register can be loaded only if all banks are idle. After the Load Mode Register command, a minimum time of tMRD must pass before the subsequent command is issued.

CAS LATENCY

After a Read command is issued to the device, a latency of several clock cycles is necessary prior to the validity of data on the data bus. Also known as CAS Latency (CL), the value can be configured as 3, 4, or 5 depending on the bits M4-M6 loaded into the register. Some CL values are not defined for certain speed ratings, and if they are used, the device may not function properly.

MODE REGISTER DEFINITION



Burst Length

M2	M1	M0	M3=0	M3=1
0	0	0	Reserved	Reserved
0	0	1	2	2
0	1	0	4	4
0	1	1	8	8
1	0	0	Reserved	Reserved
1	0	1	Reserved	Reserved
1	1	0	Reserved	Reserved
1	1	1	Full Page	Reserved

Burst Type

M3	Type
0	Sequential
1	Interleaved

Latency Mode

M6	M5	M4	CAS Latency
0	0	0	Reserved
0	0	1	Reserved
0	1	0	Reserved
0	1	1	3
1	0	0	4
1	0	1	5
1	1	0	Reserved
1	1	1	Reserved

Operating Mode

M8	M7	M6-M0	Mode
0	0	Defined	Standard Operation
1	0	Defined	Standard Operation w/DLL Reset
—	—	—	All Other States Reserved

Operating Mode

M13	M12	M11	M10	M9	Mode
0	0	0	0	0	Standard operation
—	—	—	—	—	All Other States Reserved

BURST LENGTH

The highest access throughput of this device can be achieved by using a burst of either Read or Write accesses. The number of accesses in each burst would be pre-configured to be 2, 4, 8, or full page as shown in Mode Register Definition (bits M0-M2). When a Read or Write command is given to the device, the address bits A0-A7 (x32) select the block of columns and the starting column for the subsequent burst. The accesses in this burst can only reference the selected block, and may wrap-around if a boundary is reached. The Burst Definition table indicates the relationship between the least significant address bits and the starting column. The most significant address bits can select any unique block of columns in the currently activated row. (Note: Full page bursts are possible only in Sequential Mode, with the starting address even.)

BURST TYPE

Bursts can be made in either of two types: sequential or interleaved. The burst type is programmed during a Load Mode Register command (bit M3). During a Read or Write burst, the order of accesses is determined by burst length, starting column, and burst type, as indicated in the Burst Definition table.

DLL RESET/CLEAR

To cause a DLL reset, the bit M8 is set to 1 in the Load Mode Register command. When the DLL is reset, 200 clock cycles are required to occur prior to any Read operation. To clear the DLL for normal operation, the bit M8 is set to 0. This device does not require it, but JEDEC specifications require that any time that the DLL is reset, it later be cleared prior for normal operation.

BURST DEFINITION

Burst Length	Starting Column Address			Order of Accesses in a Burst	
				Sequential	Interleaved
	A2	A1	A0		
2			0	0-1	0-1
			1	1-0	1-0
4		0	0	0-1-2-3	0-1-2-3
		0	1	1-2-3-0	1-0-3-2
		1	0	2-3-0-1	2-3-0-1
		1	1	3-0-1-2	3-2-1-0
8	0	0	0	0-1-2-3-4-5-6-7	0-1-2-3-4-5-6-7
	0	0	1	1-2-3-4-5-6-7-0	1-0-3-2-5-4-7-6
	0	1	0	2-3-4-5-6-7-0-1	2-3-0-1-6-7-4-5
	0	1	1	3-4-5-6-7-0-1-2	3-2-1-0-7-6-5-4
	1	0	0	4-5-6-7-0-1-2-3	4-5-6-7-0-1-2-3
	1	0	1	5-6-7-0-1-2-3-4	5-4-7-6-1-0-3-2
	1	1	0	6-7-0-1-2-3-4-5	6-7-4-5-2-3-0-1
	1	1	1	7-0-1-2-3-4-5-6	7-6-5-4-3-2-1-0
Full Page (up to 256)	Starting address n = A0-A7		0	Cn, Cn + 1, Cn + 2 …Cn - 1, Cn…	Not Supported

EXTENDED MODE REGISTER DEFINITION

The Extended Mode Register is a second register to enable additional functions of the DDR SDRAM. This register is loaded as a step in the normal initialization of the device. The Load Extended Mode Register command samples the values on inputs A0-A11, BA0 (High) and BA1 (Low) and stores them as register values E0-E13. The additional functions are DLL enable/disable and output drive strength. Similarly to the Load Mode Register, the Load Extended Mode Register has reserved bit values, a bank idle pre-requisite, and a tMRD time requirement. The data in the mode register is retained until it is reloaded or the device loses its power.

DLL Enable/Disable

When the Load Extended Mode Register command is issued, DLL should be enabled (E0 = 0). Normal operation of the device requires this, but DLL can be disabled for debugging or evaluation, if necessary.

Output Drive Strength

Normal drive strength for the outputs is specified as SSTL 2. However, there are options for reduced drive strength included.

EXTENDED MODE REGISTER DEFINITION

BA1	BA0	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0

Address Bus (Ax)
Mode Register (Ex)

Operating Mode

E13	E12	E11	E10	E9	E8	E7	Mode
0	1	0	0	0	0	0	Standard Operation
—	—	—	—	—	—	—	All Other States Reserved

DLL

E0	Status
0	Enable
1	Disable

Drive Strength

E6	E5	E4	E3	E2	E1	Type
0	0	0	0	0	0	Full Strength
0	0	0	0	0	1	Weak-60%
1	0	0	0	0	1	Matched Impedence
—	—	—	—	—	—	All Other States Reserved

COMMANDS

All commands described in this section should be issued only when the initialization sequence is obeyed.

Deselect

This feature blocks unwanted commands from being executed. Chip select ($\overline{CS}$) must be taken High to cause Deselect. Operations that are underway are not affected.

No Operation (NOP)

NOP is a command that prevents new commands from being executed. $\overline{CS}$ must be Low, while $\overline{RAS}$, $\overline{CAS}$, and $\overline{WE}$ must be High to issue NOP. NOP or Deselect commands must be issued during wait states to allow operations that are underway to continue uninterrupted.

Load Mode Register

The Base Mode Register is loaded during a step of initialization to configure the DDR SDRAM. Load Mode Register (LMR) is issued when BA0 and BA1 are Low, and A0-A11 are selected according to the Mode Register Definition.

Load Extended Mode Register

The Extended Mode Register is loaded during a step of initialization to enable the DLL of the device. Load Extended Mode Register (LMR) is issued when BA0 is High, BA1 is Low, and A0-A11 are selected according to the Extended Mode Register Definition.

Read

The Read command is used to begin a burst read access. When the command is given to the device, the BA0 and BA1 inputs select the bank, and address bits A0-A7 (x32) select the block of columns and the starting column for the subsequent burst. The crossing of the CLK and $\overline{CLK}$ signals will cause the output values on the I/O pins to be valid. The Auto Pre-charge function is one option in the Read command. If the Auto Pre-charge is enabled, the currently selected row will be pre-charged following the Read burst. If the function is not enabled, the selected row will remain open for further accesses at the end of the Read burst.

Write

The Write command is used to begin a burst write access. When the command is given to the device, the BA0 and BA1 inputs select the bank, and address bits A0-A7 (x32) select the block of columns and the starting column for the subsequent burst. The rising edge on the Data Strobe input(s) will cause the input values on the Data Mask pin(s) and I/O pins to be sampled for the write operation. The Auto Pre-charge function is one option in the Write command. If the Auto Pre-charge is enabled, the currently selected row will be Pre-charged following the Write burst. If the function is not enabled, the selected row will remain open for further accesses at the end of the Write burst.

Pre-charge

A Pre-charge command will de-activate an open row in a bank. The input A8 (x32) is sampled at this time to determine whether Pre-charge is applied to a single bank or all banks. After tRP, the bank has been pre-charged. It is de-activated, and goes into the idle state and must be activated before any Read or Write command can be issued to it. A Pre-charge command is treated as a NOP if either (a) the specified bank is already undergoing Pre-charge, or (b) the specified bank has no open row.

Auto Pre-charge

Auto Pre-charge is a feature that can be enabled as an option in a Read or Write command. If the input value on A8 (x32) is High during a Read or Write command, an automatic Pre-charge will occur just after the memory burst is completed. If the input value on A8 (x32) is Low, no Pre-charge will occur. With Auto Pre-charge, a minimum time of tRP must pass before the next command is issued to the same bank.

Active

The Active command opens a row in preparation for a Read or Write burst. The row stays open for accesses until the bank receives a Pre-charge command. Other rows in the bank cannot be opened until the bank is de-activated with a Pre-charge command and another Active command is issued.

Burst Terminate

The Burst Terminate command truncates the burst of the most recently issued Read command (with Auto Pre-charge disabled). The open row being accessed in the Read burst remains open.

Auto Refresh

The DDR SDRAM is issued the Auto Refresh command during normal operation to maintain data in the memory array. All the banks must be idle for the command to be executed. The device has 4096 refresh cycles every 32ms.

Self Refresh

To issue the Self Refresh command, CKE must be Low. When the DDR SDRAM is in Self Refresh mode, it retains the data contents without external clocking, and ignores other input signals. The DLL is disabled upon entering the Self Refresh mode, and is enabled again upon leaving the mode. To exit Self Refresh, all inputs must be stable prior to CKE going High. Next, a NOP command command must be issued on each clock cycle for at least tXSNR to ensure that internal refresh operations are completed. To prepare for a memory access, the DDR SDRAM must receive a DLL reset followed by a NOP command for 200 clock cycles.

DEVICE OPERATION

Bank and Row Activation

An Active command must be issued to the DDR SDRAM to open a bank and row prior to an access. The row will be available for a Read or Write command once a time tRCD has occurred. The Active command is depicted in the figure. As CLK goes High, $\overline{\text{CS}}$ and $\overline{\text{RAS}}$ are Low, while CKE, $\overline{\text{WE}}$, and $\overline{\text{CAS}}$ are High. Upon issuing the Active command, the values on the address inputs specify the row, and BA0 and BA1 specify the bank. When an Active command is issued for a bank and row, another row in that same bank may be activated after a time tRC. When an Active command is issued for a bank and row, a row in a different bank may be activated after a time tRRD. (Note: to ensure that time requirement tRCD, tRC, or tRRD is met, NOP commands should be issued for a whole number of clock cycles that is greater than the time requirement (ie. tRCD) divided by the clock period.)

Read Operation

A Read command starts a burst from an activated row. The Read command is depicted in the figure. As CLK goes High, $\overline{\text{CS}}$ and $\overline{\text{CAS}}$ are Low, while $\overline{\text{RAS}}$, CKE, and $\overline{\text{WE}}$ are High. The values on the inputs BA0 and BA1 specify the bank to access, and the address inputs specify the starting column in the open row. If Auto Pre-charge is enabled in the Read command, the open row will be pre-charged after completion of the Read burst. Unless stated otherwise, all timing diagrams for Read operations have disabled Auto Pre-charge.

The Read command causes data to be retrieved and placed in the pipeline. The subsequent command can be NOP, Read, or Terminate Burst. The data from the starting column specified in the Read command appears on I/O pins following a CAS latency of after the Read command. On each CLK and $\overline{\text{CLK}}$ crossing, the data from the next column in the burst sequence is output from the pipeline until the burst is completed (see Read Burst, Non-consecutive Read Burst, and Consecutive Read Burst). There are two cases in which a full Read burst length is not completed. The first is when the data retrieved from a subsequent Read burst interrupts the previous burst (see Random Read Accesses). The second is when a subsequent Burst Terminate command truncates the burst (see Terminating a Read Burst and Read to Write). The Burst Terminate and Read commands obey the same CAS latency timing such that they should be issued x cycles after a previous Read command, where x is the number of pairs of columns to output. By following a desired command sequence, continuous data can be output with either whole Read bursts or truncated Read bursts. Whenever a Read burst finishes and no other commands have been initiated, the I/O returns to High-Z.

If Auto Pre-charge is not enabled in the Read burst, the Pre-charge command can be issued separately following the Read command. The Pre-charge command should be received by the device x cycles after the Read command, where x is the desired number of pairs of columns to output during the Read burst. After the Pre-charge command, it is necessary to wait until both tRAS and tRP have been met before issuing a new command to the same bank.

Data Strobe output is driven synchronously with the output data on the I/O pins. The Low portion of the Data Strobe just prior to the first output data is the Read Pre-amble; and the Low portion coinciding with the last output data is the Read Post-amble. Before any Write command can be executed, any previous Read burst must have been completed normally or truncated by a Burst Terminate command. In the diagram Read to Write, a Burst Terminate command is issued to truncate a Read Burst early, and begin a Write operation. After the Write command, a time tDQSS is required prior to latching the data on the I/O.

Write Operation

A Write command starts a burst from an activated row. The Write command is depicted in the figure. As CLK goes High, $\overline{CS}$, $\overline{WE}$, and $\overline{CAS}$ are Low, while CKE and $\overline{RAS}$ are High. The values on the inputs BA0 and BA1 specify the bank to access, and the address inputs specify the starting column in the open row. If Auto Pre-charge is enabled in the Write command, the open row will be pre-charged after completion of the Write burst and time tWR. Unless stated otherwise, all timing diagrams for Write operations have disabled Auto Pre-charge.

The Write command in conjunction with Data Strobe inputs causes data to be latched and placed in the pipeline. The Low portion of the Data Strobe between the Write command and the first rising edge of the strobe is the Write Pre-amble; and the Low portion following the last input data is the Write Post-amble. A minimum time of tDQSS after the Write, the next command can be NOP or Write. The data that is to be written to the starting column specified in the Write command will be latched upon the first rising edge of Data Strobe input(s) DQS0-DQS3 (x32) after that Write command. On each Data Strobe transition from Low-to-High or High-to-Low, the input values on the I/O are sampled, and enter pipeline to be written in the pre-determined burst sequence (see Write Burst, Consecutive Write to Write, and Non-consecutive Write to Write). A new Write command can be issued x cycles after a previous Write command, where x is the number of pairs of columns to input. By following a desired command sequence, continuous data can be input with either whole Write bursts or truncated Write bursts. Whenever a Write burst finishes and no other commands have been initiated, the I/O returns to High-Z.

A Write burst may be followed by Read command, with or without truncating the Write burst. To avoid truncating the input data, the timing parameter tWTR should be obeyed before issuing the Read command (see Write to Read, Non-truncated). The period tWTR begins on the first positive clock edge after the last data input has been latched. The Write burst can be truncated deliberately by using the Data Mask feature and a Read command with an earlier timing (see Write to Read, Truncated).

If Auto Pre-charge is not enabled in the Write burst, the Pre-charge command can be issued separately some time following the Write command. The procedure to execute it is similar to the procedure to transition from a Write burst to a Read burst. To avoid truncating the input data, the timing parameter tWR should be obeyed before issuing the Pre-charge command (see Write to Pre-charge, Non-truncated). The period tWR begins on the first positive clock edge after the last data input has been latched. The Write burst can be truncated deliberately by using the Data Mask feature and a Pre-charge command with an earlier timing (see Write to Pre-charge, Truncated). After the Pre-charge command, it is necessary to wait until tRP has been met before issuing a new command to the same bank.

Power Down Operation

When the DDR SDRAM enters Power Down mode, power consumption is greatly reduced. To enter the mode, several conditions must be met. There must be neither a Read operation, nor a Write operation underway in the device at CLK positive edge n – 1, with CKE stable High. Prior to CLK positive edge n, CKE should go Low. A Power Down mode is entered if the appropriate command is issued as CLK n goes High. (If the command at CLK n is Auto Refresh, the SDRAM enters Self Refresh mode.) If the command at CLK n is NOP or Deselect, the device will enter Pre-charge Power Down mode or Active Power Down mode. While in a Power Down mode, CKE must be stable Low, and CLK and $\overline{CLK}$ signals maintained, while other inputs are ignored. Pre-charge Power Down mode conserves additional power by freezing the DLL. To exit the Power Down mode, normal voltages and clock frequency are applied. Prior to CLK positive edge n, CKE should go High. A NOP or Deselect command at CLK n, allows a valid command to be issued at CLK positive edge n + 1. (If exiting Self Refresh mode, the DLL is automatically enabled, and the device must be prepared according to the section describing Self Refresh.)

Pre-charge Operation

When this command is issued, either a particular bank, or all four banks will be de-activated after a time period of tRP. The bank(s) will be available for a row access until that time has occurred. The Pre-charge command is depicted in the figure. As CLK goes High, $\overline{CS}$, $\overline{RAS}$, and $\overline{WE}$ are Low, while CKE and $\overline{CAS}$ are High. The values on the address inputs are Don't Care, except for the input A8 (x32), which determines whether a single bank is selected for Pre-charge, or all four banks. If A8 is Low, the inputs BA0 and BA1 select the single bank; however, if A8 is High, BA0 and BA1 are Don't Care. Once any bank has been pre-charged, it becomes idle. Before any row can have a Read or Write access, it must be activated.

Timing Waveforms

Figure 1. AC Parameters for Read Timing (Burst Length =4)

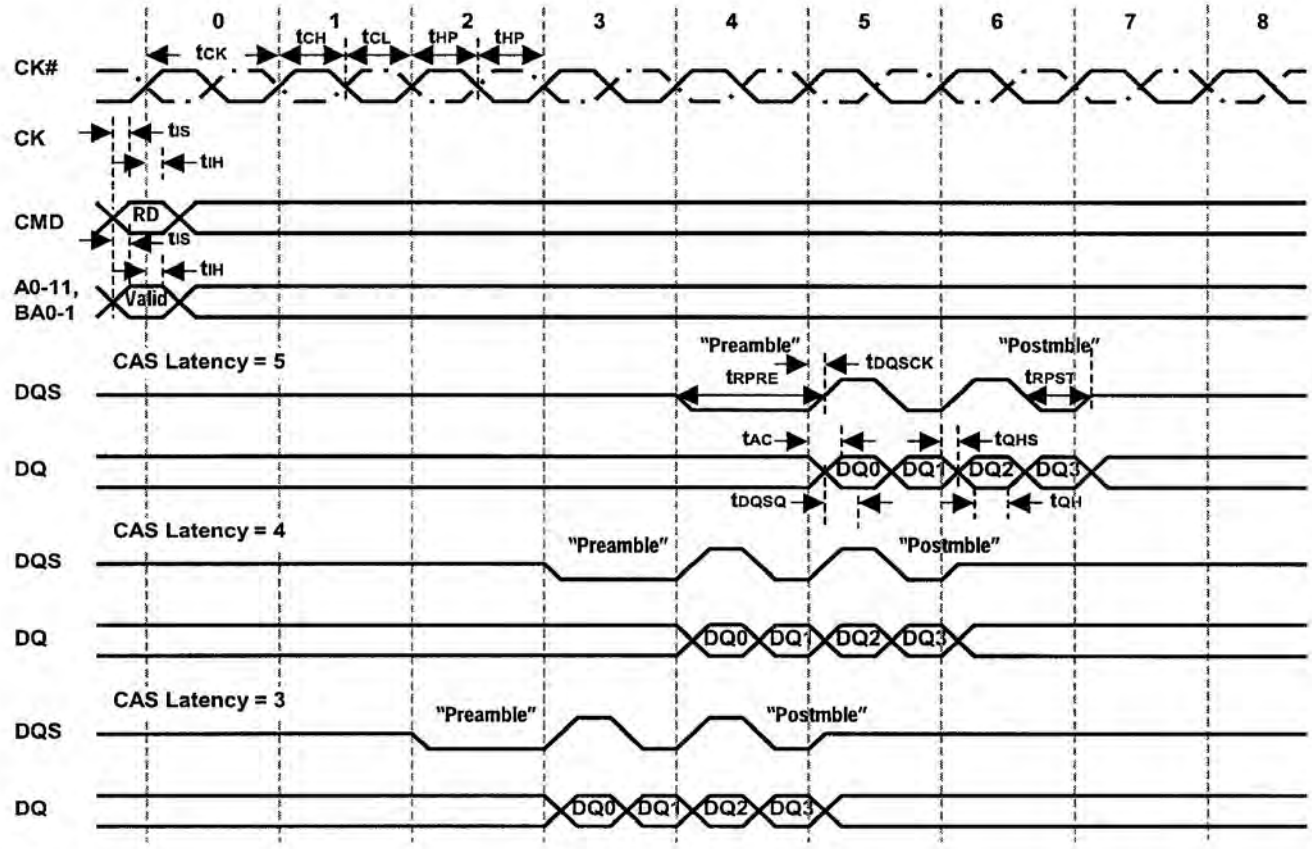


Figure 2. AC Parameters for Write Timing (Burst Length=4)

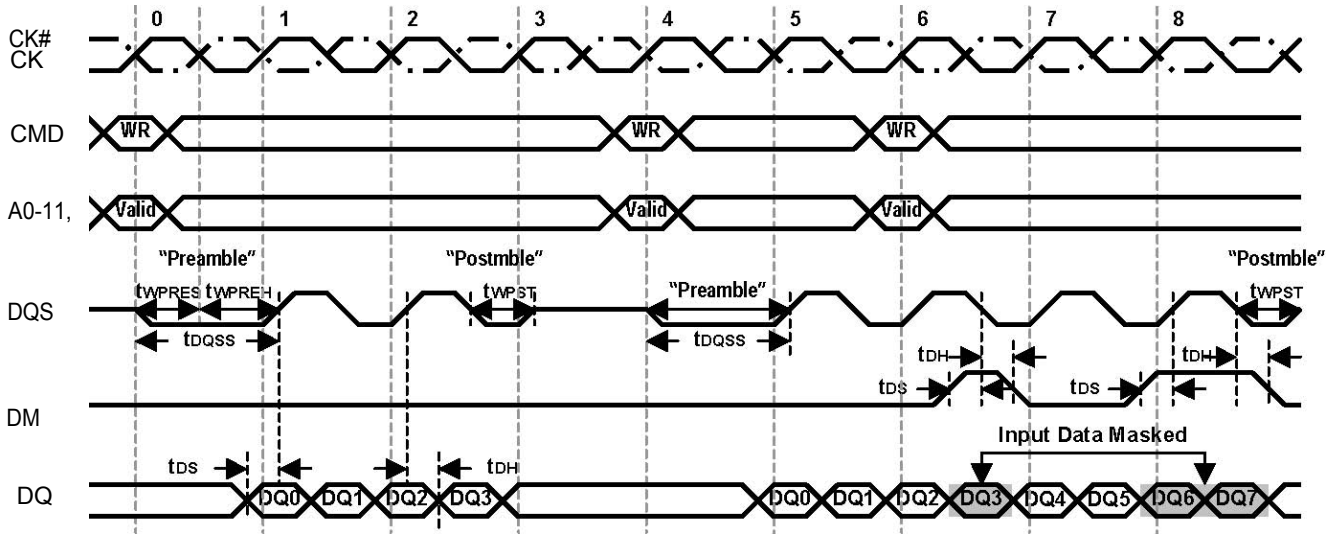


Figure 3. Bank Activate Read or Write Command Timing

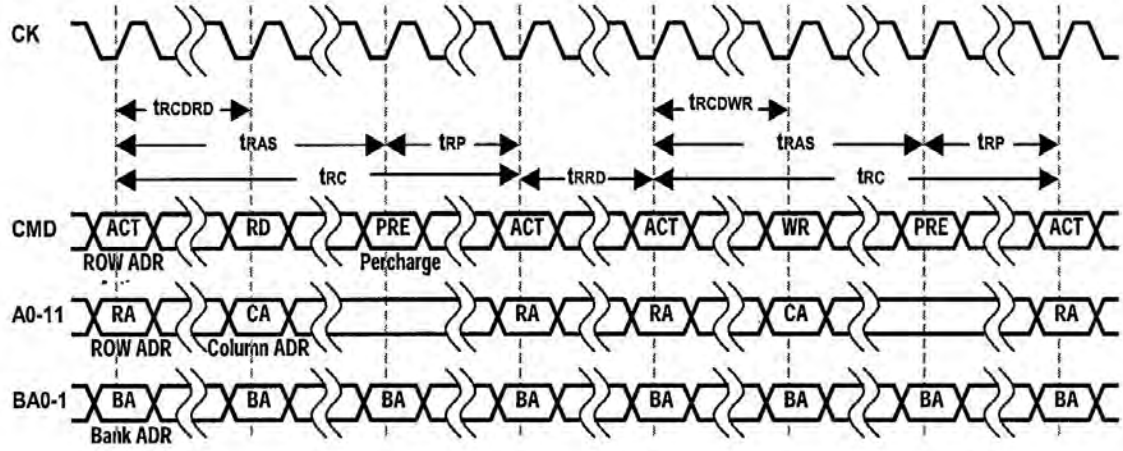


Figure 4. Burst Stop for Read (CAS Letancy = 5, Burst Length = 4)

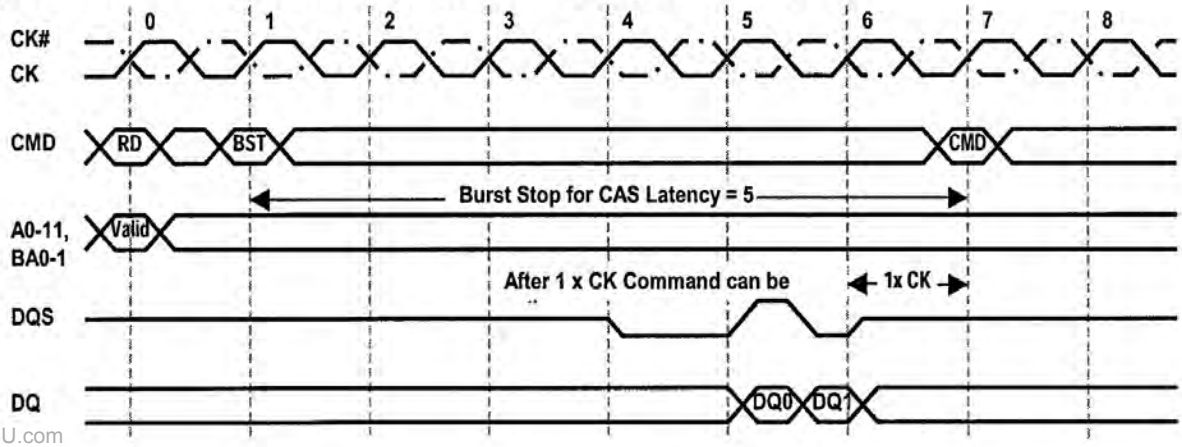


Figure 5. Read with Auto Precharge (CAS Letancy = 5, Burst Length = 4)

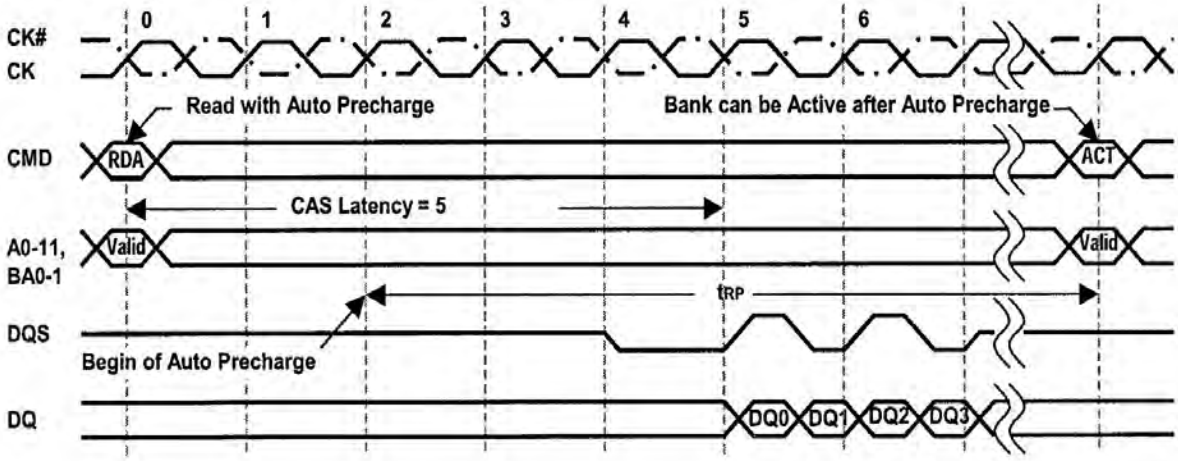


Figure 6. Write with Auto Precharge (Burst Length = 4)

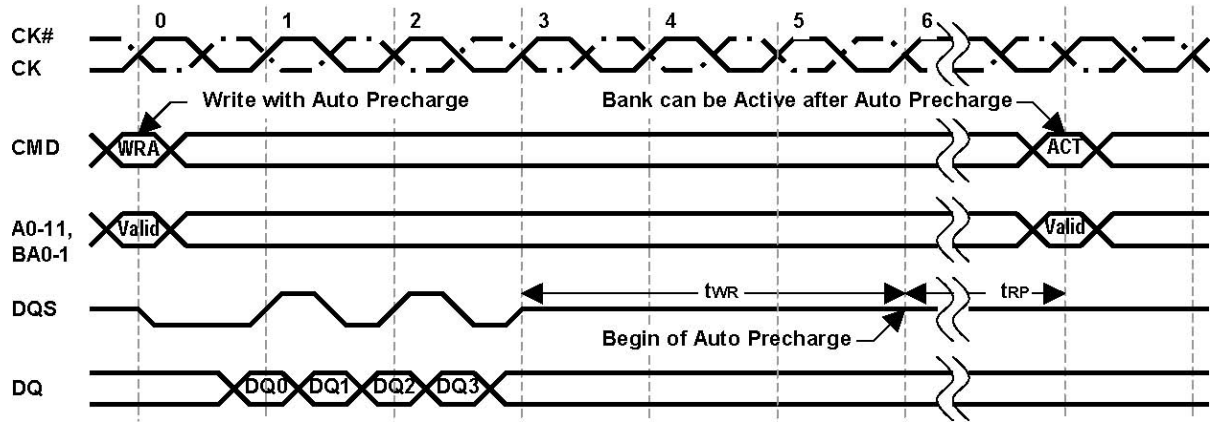


Figure 7. Read Burst Interrupt by Read (CAS Letancy =5, Burst Length = 4)

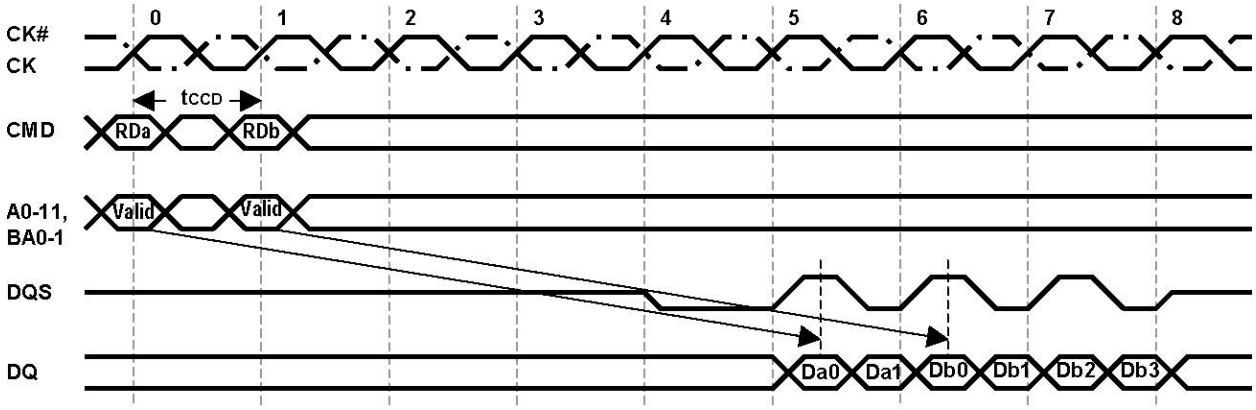


Figure 8. Write Interrupted by Write (Burst Length =4)

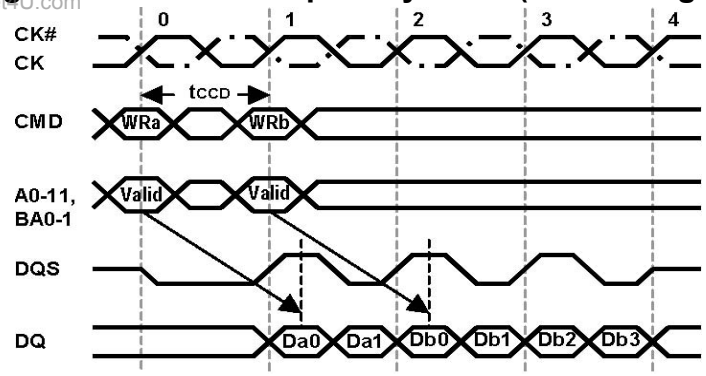


Figure 9. Auto Refresh Timing

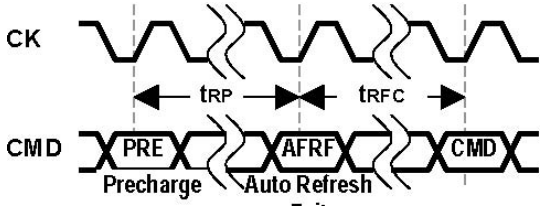


Figure 10. Self Refresh Timimg

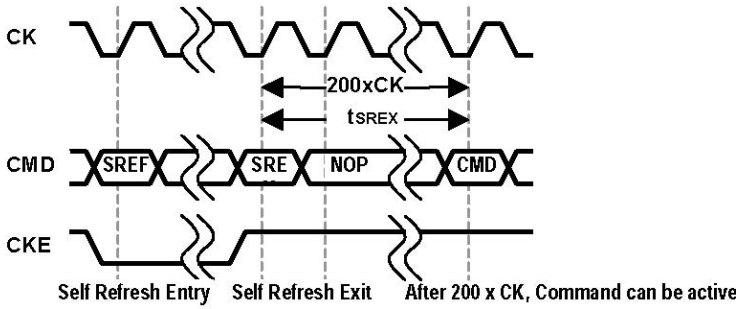


Figure 11. Precharge Command

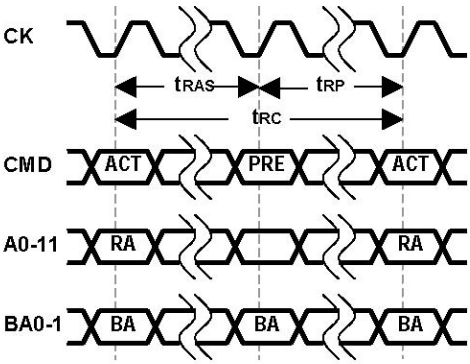


Figure 12. Power Up Sequence

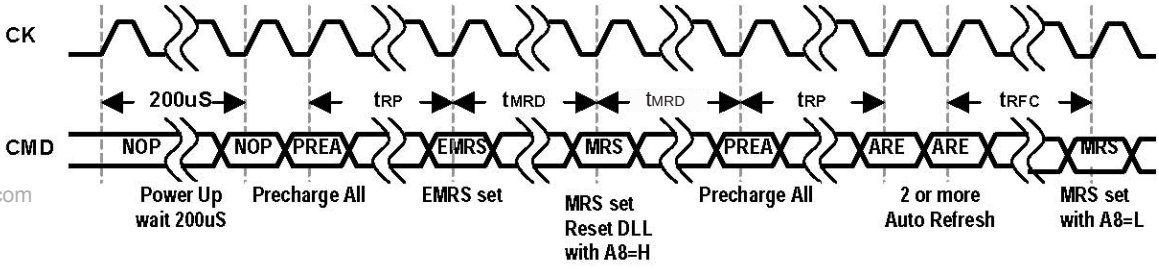


Figure 13. Mode Register Set Timing

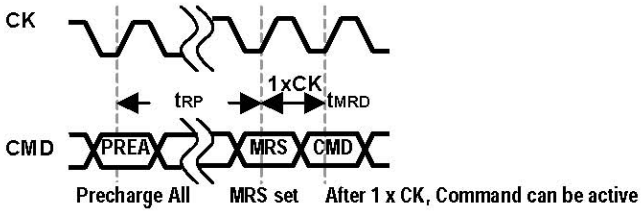
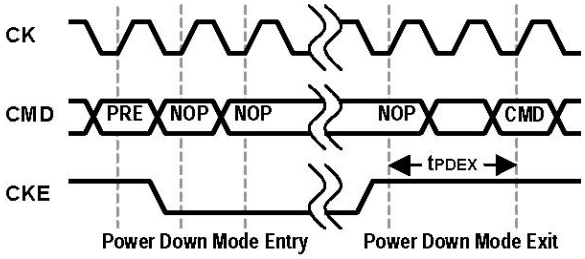


Figure 14. Power Down Mode



ORDERING INFORMATION

Commercial Range: 0°C to +70°C

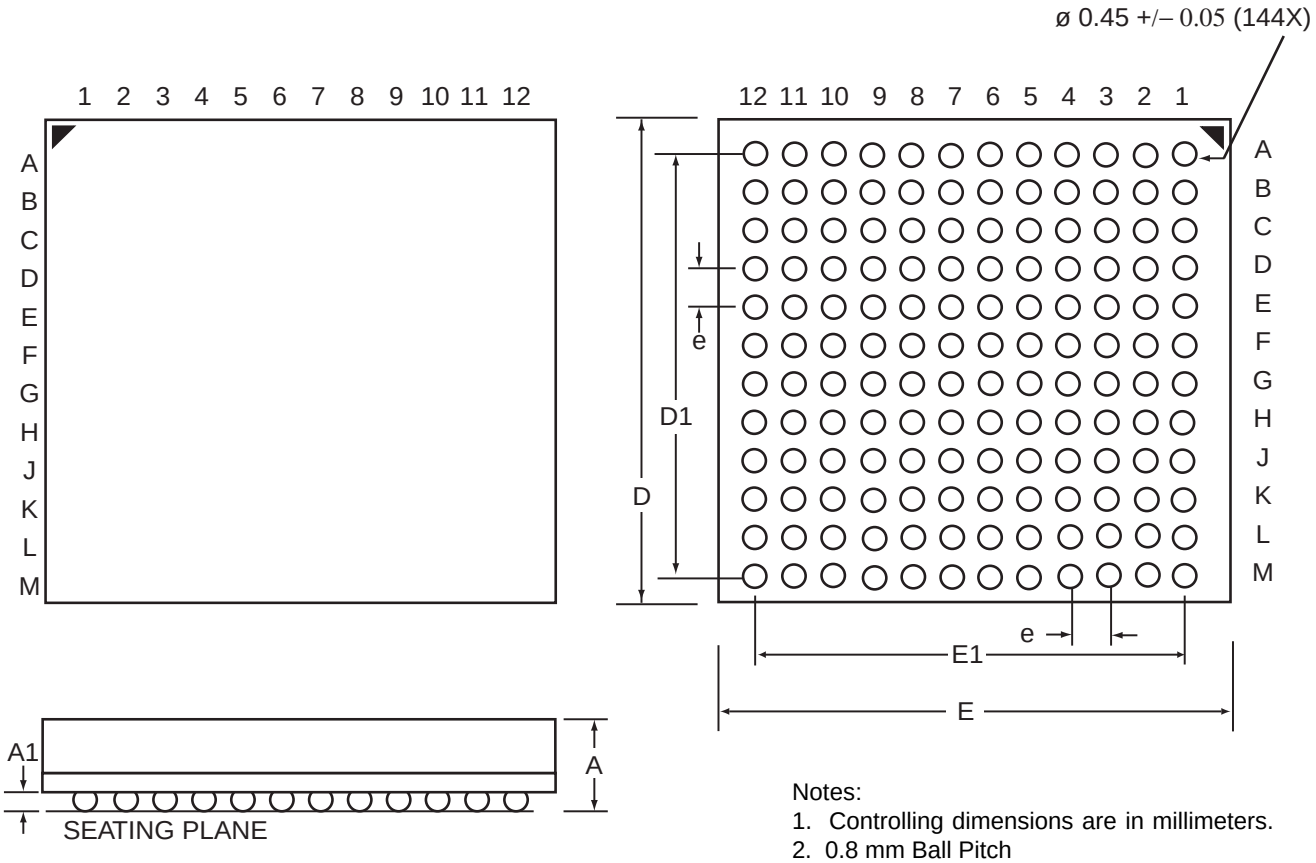
Frequency	Speed (ns)	Order Part No.	Package
200 MHz	5	IS43R32400A-5B	144-ball FBGA
200 MHz	5	IS43R32400A-5BL	144-ball FBGA, Lead-free
166 MHz	6	IS43R32400A-6B	144-ball FBGA
166 MHz	6	IS43R32400A-6BL	144-ball FBGA, Lead-free

Industrial Range: -40°C to +85°C

Frequency	Speed (ns)	Order Part No.	Package
166 MHz	6	IS43R32400A-6BI	144-ball FBGA
166 MHz	6	IS43R32400A-6BLI	144-ball FBGA, Lead-free

PACKAGING INFORMATION

Mini Ball Grid Array
Package Code: B (144-Ball)



Notes:
1. Controlling dimensions are in millimeters.
2. 0.8 mm Ball Pitch

mBGA - 12mm x 12mm

	MILLIMETERS			INCHES		
Sym.	**Min.**	**Typ.**	**Max.**	**Min.**	**Typ.**	**Max.**
N0. Leads		**144**				
A	1.17	1.25	1.40	0.046	0.049	0.055
A1	0.32	0.35	0.38	0.013	0.014	0.015
D	11.95	12.00	12.05	0.470	0.472	0.474
D1	—	8.80	—	—	0.346	—
E	11.95	12.00	12.05	0.470	0.472	0.474
E1	—	8.80	—	—	0.346	—
e	—	0.80	—	—	0.031	—