IS45LV44002B

4M x 4 (16-MBIT) DYNAMIC RAM WITH EDO PAGE MODE

SEPTEMBER 2005

FEATURES

- Extended Data-Out (EDO) Page Mode access cycle
- TTL compatible inputs and outputs
- Refresh Interval:
  – 2,048 cycles/32 ms
- Refresh Mode: $\overline{\text{RAS}}$-Only, $\overline{\text{CAS}}$-before-$\overline{\text{RAS}}$ (CBR), and Hidden
- Single power supply: 3.3V ± 10%
- Byte Write and Byte Read operation via two $\overline{\text{CAS}}$
- Automotive Temperature Range
  Option A1: -40°C to +85°C
- Lead-free available

DESCRIPTION

The *ISSI* IS45LV44002B is 4,194,304 x 4-bit high-performance CMOS Dynamic Random Access Memory. These devices offer an accelerated cycle access called EDO Page Mode. EDO Page Mode allows 2,048 random accesses within a single row with access cycle time as short as 20 ns per 4-bit word.

These features make the IS45LV44002B ideally suited for high-bandwidth graphics, digital signal processing, high-performance computing systems, and peripheral applications.

The IS45LV44002B is packaged in a 24-pin 300-mil SOJ with JEDEC standard pinouts.

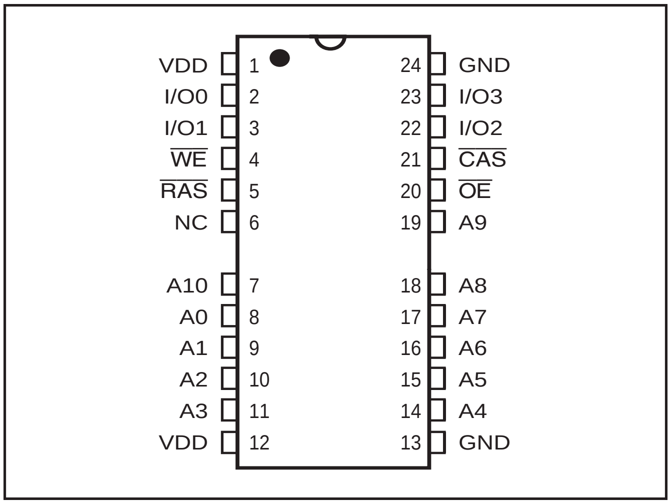
PRODUCT SERIES OVERVIEW

Part No.	Refresh	Voltage
IS45LV44002B	2K	3.3V ± 10%

KEY TIMING PARAMETERS

Parameter	-50	Unit
$\overline{\text{RAS}}$ Access Time (t_{RAC})	50	ns
$\overline{\text{CAS}}$ Access Time (t_{CAC})	13	ns
Column Address Access Time (t_{AA})	25	ns
EDO Page Mode Cycle Time (t_{PC})	20	ns
Read/Write Cycle Time (t_{RC})	84	ns

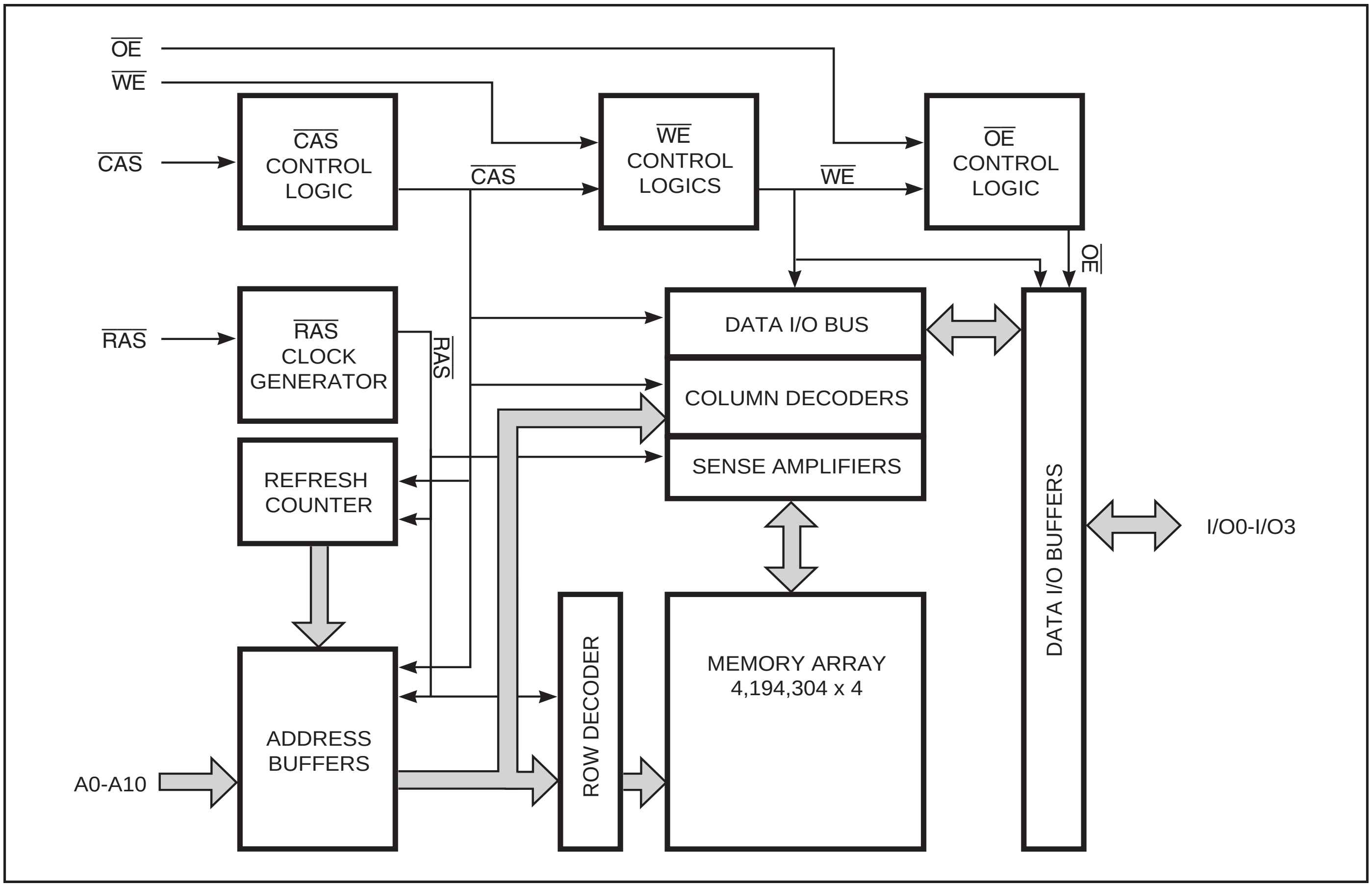
PIN CONFIGURATION: 24-pin SOJ



PIN DESCRIPTIONS

A0-A10	Address Inputs
I/O0-3	Data Inputs/Outputs
$\overline{\text{WE}}$	Write Enable
$\overline{\text{OE}}$	Output Enable
$\overline{\text{RAS}}$	Row Address Strobe
$\overline{\text{CAS}}$	Column Address Strobe
V_{DD}	Power
GND	Ground
NC	No Connection

FUNCTIONAL BLOCK DIAGRAM



TRUTH TABLE

Function		$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	$\overline{OE}$	Address tR/tC	I/O
Standby		H	H	X	X	X	High-Z
Read		L	L	H	L	ROW/COL	DOUT
Write: Word (Early Write)		L	L	L	X	ROW/COL	DIN
Read-Write		L	L	H→L	L→H	ROW/COL	DOUT, DIN
EDO Page-Mode Read	1st Cycle:	L	H→L	H	L	ROW/COL	DOUT
	2nd Cycle:	L	H→L	H	L	NA/COL	DOUT
EDO Page-Mode Write	1st Cycle:	L	H→L	L	X	ROW/COL	DIN
	2nd Cycle:	L	H→L	L	X	NA/COL	DIN
EDO Page-Mode	1st Cycle:	L	H→L	H→L	L→H	ROW/COL	DOUT, DIN
Read-Write	2nd Cycle:	L	H→L	H→L	L→H	NA/COL	DOUT, DIN
Hidden Refresh	Read	L→H→L	L	H	L	ROW/COL	DOUT
	Write(1)	L→H→L	L	L	X	ROW/COL	DOUT
$\overline{RAS}$-Only Refresh		L	H	X	X	ROW/NA	High-Z
CBR Refresh		H→L	L	X	X	X	High-Z

Note:
1. EARLY WRITE only.

Functional Description

The IS45LV44002B is a CMOS DRAMs optimized for high-speed bandwidth, low power applications. During READ or WRITE cycles, each bit is uniquely addressed through the 11 address bits. These are entered 11 bits (A0-A10) at a time for the 2K refresh device. The row address is latched by the Row Address Strobe ($\overline{\text{RAS}}$). The column address is latched by the Column Address Strobe ($\overline{\text{CAS}}$). $\overline{\text{RAS}}$ is used to latch the first nine bits and $\overline{\text{CAS}}$ is used the latter ten bits.

Memory Cycle

A memory cycle is initiated by bringing $\overline{\text{RAS}}$ LOW and it is terminated by returning both $\overline{\text{RAS}}$ and $\overline{\text{CAS}}$ HIGH. To ensures proper device operation and data integrity any memory cycle, once initiated, must not be ended or aborted before the minimum t_{RAS} time has expired. A new cycle must not be initiated until the minimum precharge time t_{RP}, t_{CP} has elapsed.

Read Cycle

A read cycle is initiated by the falling edge of $\overline{\text{CAS}}$ or $\overline{\text{OE}}$, whichever occurs last, while holding $\overline{\text{WE}}$ HIGH. The column address must be held for a minimum time specified by t_{AR}. Data Out becomes valid only when t_{RAC}, t_{AA}, t_{CAC} and t_{OEA} are all satisfied. As a result, the access time is dependent on the timing relationships between these parameters.

Write Cycle

A write cycle is initiated by the falling edge of $\overline{\text{CAS}}$ and $\overline{\text{WE}}$, whichever occurs last. The input data must be valid at or before the falling edge of $\overline{\text{CAS}}$ or $\overline{\text{WE}}$, whichever occurs last.

Auto Refresh Cycle

To retain data, 2,048 refresh cycles are required in each 32 ms period. There are two ways to refresh the memory:

1. By clocking each of the 2,048 row addresses (A0 through A10) with RAS at least once every 32 ms. Any read, write, read-modify-write or RAS-only cycle refreshes the addressed row.
2. Using a $\overline{\text{CAS}}$-before-$\overline{\text{RAS}}$ refresh cycle. $\overline{\text{CAS}}$-before-$\overline{\text{RAS}}$ refresh is activated by the falling edge of $\overline{\text{RAS}}$, while holding $\overline{\text{CAS}}$ LOW. In $\overline{\text{CAS}}$-before-$\overline{\text{RAS}}$ refresh cycle, an internal 9-bit counter provides the row addresses and the external address inputs are ignored.

$\overline{\text{CAS}}$-before-$\overline{\text{RAS}}$ is a refresh-only mode and no data access or device selection is allowed. Thus, the output remains in the High-Z state during the cycle.

Power-On

After application of the V_{DD} supply, an initial pause of 200 µs is required followed by a minimum of eight initialization cycles (any combination of cycles containing a $\overline{\text{RAS}}$ signal).

During power-on, it is recommended that $\overline{\text{RAS}}$ track with V_{DD} or be held at a valid V_{IH} to avoid current surges.

ABSOLUTE MAXIMUM RATINGS(1)

Symbol	Parameters	Rating	Unit
V_T	Voltage on Any Pin Relative to GND	–0.5 to +4.6	V
V_{DD}	Supply Voltage	–0.5 to +4.6	V
I_{OUT}	Output Current	50	mA
P_D	Power Dissipation	1	W
T_A	Operating Temperature	-40 to +85	°C
T_{STG}	Storage Temperature	–55 to +125	°C

Note:

1. Stress greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

RECOMMENDED OPERATING CONDITIONS (Voltages are referenced to GND.)

Symbol	Parameter	Min.	Typ.	Max.	Unit
V_{DD}	Supply Voltage	3.0	3.3	3.6	V
V_{IH}	Input High Voltage	2.0	—	V_{DD} + 0.3	V
V_{IL}	Input Low Voltage	–0.3	—	0.8	V
T_A	Automotive Ambient Temperature (A1)	-40	—	+85	°C

CAPACITANCE(1,2)

Symbol	Parameter	Max.	Unit
C_{IN1}	Input Capacitance: A0-A10	5	pF
C_{IN2}	Input Capacitance: $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$, $\overline{OE}$	7	pF
C_{IO}	Data Input/Output Capacitance: I/O0-I/O3	7	pF

Notes:

1. Tested initially and after any design or process changes that may affect these parameters.
2. Test conditions: T_A = 25°C, f = 1 MHz.

ELECTRICAL CHARACTERISTICS[1]

(Recommended Operating Conditions unless otherwise noted.)

Symbol	Parameter	Test Condition	Speed	Min.	Max.	Unit
I_{IL}	Input Leakage Current	Any input 0V $\leq V_{IN} \leq V_{DD}$ Other inputs not under test = 0V		–5	5	µA
I_{IO}	Output Leakage Current	Output is disabled (Hi-Z) $0V \leq V_{OUT} \leq V_{DD}$		–5	5	µA
V_{OH}	Output High Voltage Level	$I_{OH} = -2.0$ mA, $V_{DD} = 3.3V$		2.4	—	V
V_{OL}	Output Low Voltage Level	$I_{OL} = 2$ mA, $V_{DD} = 3.3V$		—	0.4	V
$I_{CC}1$	Standby Current: TTL	$\overline{RAS}$, $\overline{CAS} \geq V_{IH}$		—	2	mA
$I_{CC}2$	Standby Current: CMOS	$\overline{RAS}$, $\overline{CAS} \geq V_{DD} - 0.2V$		—	0.5	mA
$I_{CC}3$	Operating Current: Random Read/Write[2,3,4] Average Power Supply Current	$\overline{RAS}$, $\overline{CAS}$, Address Cycling, $t_{RC} = t_{RC}$ (min.)	-50	—	120	mA
$I_{CC}4$	Operating Current: EDO Page Mode[2,3,4] Average Power Supply Current	$\overline{RAS} = V_{IL}$, $\overline{CAS}$, Cycling $t_{PC} = t_{PC}$ (min.)	-50	—	90	mA
$I_{CC}5$	Refresh Current: $\overline{RAS}$-Only[2,3] Average Power Supply Current	$\overline{RAS}$ Cycling, $\overline{CAS} \geq V_{IH}$ $t_{RC} = t_{RC}$ (min.)	-50	—	120	mA
$I_{CC}6$	Refresh Current: CBR[2,3,5] Average Power Supply Current	$\overline{RAS}$, $\overline{CAS}$ Cycling $t_{RC} = t_{RC}$ (min.)	-50	—	120	mA

Notes:

1. An initial pause of 200 µs is required after power-up followed by eight $\overline{RAS}$ refresh cycles ($\overline{RAS}$-Only or CBR) before proper device operation is assured. The eight $\overline{RAS}$ cycles wake-up should be repeated any time the t_{REF} refresh requirement is exceeded.
2. Dependent on cycle rates.
3. Specified values are obtained with minimum cycle time and the output open.
4. Column-address is changed once each EDO page cycle.
5. Enables on-chip refresh and address counters.

AC CHARACTERISTICS(1,2,3,4,5,6)

(Recommended Operating Conditions unless otherwise noted.)

		-50		
Symbol	**Parameter**	**Min.**	**Max.**	**Units**
t_{RC}	Random READ or WRITE Cycle Time	84	—	ns
t_{RAC}	Access Time from $\overline{RAS}$(6, 7)	—	50	ns
t_{CAC}	Access Time from $\overline{CAS}$(6, 8, 15)	—	13	ns
t_{AA}	Access Time from Column-Address(6)	—	25	ns
t_{RAS}	$\overline{RAS}$ Pulse Width	50	10K	ns
t_{RP}	$\overline{RAS}$ Precharge Time	30	—	ns
t_{CAS}	$\overline{CAS}$ Pulse Width(23)	8	10K	ns
t_{CP}	$\overline{CAS}$ Precharge Time(9)	9	—	ns
t_{CSH}	$\overline{CAS}$ Hold Time (21)	38	—	ns
t_{RCD}	$\overline{RAS}$ to $\overline{CAS}$ Delay Time(10, 20)	12	37	ns
t_{ASR}	Row-Address Setup Time	0	—	ns
t_{RAH}	Row-Address Hold Time	8	—	ns
t_{ASC}	Column-Address Setup Time(20)	0	—	ns
t_{CAH}	Column-Address Hold Time(20)	8	—	ns
t_{AR}	Column-Address Hold Time (referenced to $\overline{RAS}$)	30	—	ns
t_{RAD}	$\overline{RAS}$ to Column-Address Delay Time(11)	10	25	ns
t_{RAL}	Column-Address to $\overline{RAS}$ Lead Time	25	—	ns
t_{RPC}	$\overline{RAS}$ to $\overline{CAS}$ Precharge Time	5	—	ns
t_{RSH}	$\overline{RAS}$ Hold Time	8	—	ns
t_{RHCP}	$\overline{RAS}$ Hold Time from $\overline{CAS}$ Precharge	30	—	ns
t_{CLZ}	$\overline{CAS}$ to Output in Low-Z(15, 24)	0	—	ns
t_{CRP}	$\overline{CAS}$ to $\overline{RAS}$ Precharge Time(21)	5	—	ns
t_{OD}	Output Disable Time(19, 24)	3	15	ns
t_{OE}	Output Enable Time(15, 16)	—	12	ns
t_{OED}	Output Enable Data Delay (Write)	12	—	ns
t_{OEHC}	$\overline{OE}$ HIGH Hold Time from $\overline{CAS}$ HIGH	5	—	ns
t_{OEP}	$\overline{OE}$ HIGH Pulse Width	10	—	ns
t_{OES}	$\overline{OE}$ LOW to $\overline{CAS}$ HIGH Setup Time	5	—	ns
t_{RCS}	Read Command Setup Time(17, 20)	0	—	ns
t_{RRH}	Read Command Hold Time (referenced to $\overline{RAS}$)(12)	0	—	ns
t_{RCH}	Read Command Hold Time (referenced to $\overline{CAS}$)(12, 17, 21)	0	—	ns
t_{WCH}	Write Command Hold Time(17)	8	—	ns
t_{WCR}	Write Command Hold Time (referenced to $\overline{RAS}$)(17)	40	—	ns
t_{WP}	Write Command Pulse Width(17)	8	—	ns
t_{WPZ}	$\overline{WE}$ Pulse Widths to Disable Outputs	7	—	ns

AC CHARACTERISTICS (Continued)(1,2,3,4,5,6)

(Recommended Operating Conditions unless otherwise noted.)

		-50		
Symbol	**Parameter**	**Min.**	**Max.**	**Units**
t_{RWL}	Write Command to $\overline{\text{RAS}}$ Lead Time(17)	13	—	ns
t_{CWL}	Write Command to $\overline{\text{CAS}}$ Lead Time(17, 21)	8	—	ns
t_{WCS}	Write Command Setup Time(14, 17, 20)	0	—	ns
t_{DHR}	Data-in Hold Time (referenced to $\overline{\text{RAS}}$)	39	—	ns
t_{ACH}	Column-Address Setup Time to $\overline{\text{CAS}}$ Precharge during WRITE Cycle	15	—	ns
t_{OEH}	$\overline{\text{OE}}$ Hold Time from $\overline{\text{WE}}$ during READ-MODIFY-WRITE cycle(18)	8	—	ns
t_{DS}	Data-In Setup Time(15, 22)	0	—	ns
t_{DH}	Data-In Hold Time(15, 22)	8	—	ns
t_{RWC}	READ-MODIFY-WRITE Cycle Time	108	—	ns
t_{RWD}	$\overline{\text{RAS}}$ to $\overline{\text{WE}}$ Delay Time during READ-MODIFY-WRITE Cycle(14)	64	—	ns
t_{CWD}	$\overline{\text{CAS}}$ to $\overline{\text{WE}}$ Delay Time(14, 20)	26	—	ns
t_{AWD}	Column-Address to $\overline{\text{WE}}$ Delay Time(14)	39	—	ns
t_{PC}	EDO Page Mode READ or WRITE Cycle Time	20	—	ns
t_{RASP}	$\overline{\text{RAS}}$ Pulse Width in EDO Page Mode	50	100K	ns
t_{CPA}	Access Time from $\overline{\text{CAS}}$ Precharge(15)	—	30	ns
t_{PRWC}	EDO Page Mode READ-WRITE Cycle Time	56	—	ns
t_{COH}	Data Output Hold after $\overline{\text{CAS}}$ LOW	5	—	ns
t_{OFF}	Output Buffer Turn-Off Delay from $\overline{\text{CAS}}$ or $\overline{\text{RAS}}$(13,15,19, 24)	0	12	ns
t_{WHZ}	Output Disable Delay from $\overline{\text{WE}}$	3	10	ns
t_{CSR}	$\overline{\text{CAS}}$ Setup Time (CBR REFRESH)(20, 25)	5	—	ns
t_{CHR}	$\overline{\text{CAS}}$ Hold Time (CBR REFRESH)(21, 25)	8	—	ns
t_{ORD}	$\overline{\text{OE}}$ Setup Time prior to $\overline{\text{RAS}}$ during HIDDEN REFRESH Cycle	0	—	ns
t_{REF}	Auto Refresh Period 2,048 Cycles	—	32	ms
t_{T}	Transition Time (Rise or Fall)(2, 3)	1	50	ns

AC TEST CONDITIONS

Output load: Two TTL Loads and 50 pF

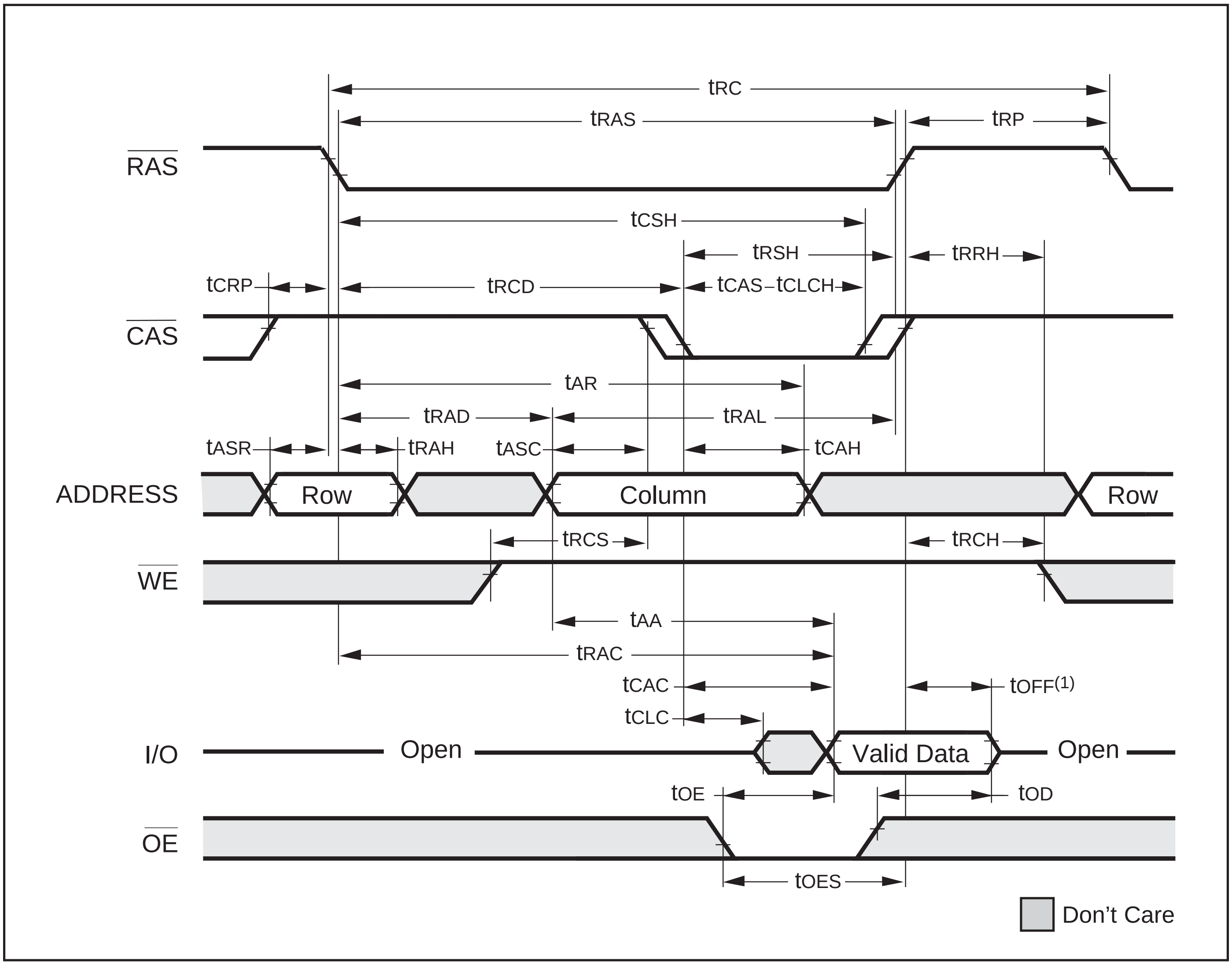
Input timing reference levels: $V_{IH} = 2.4V$, $V_{IL} = 0.8V$

Output timing reference levels: $V_{OH} = 2.0V$, $V_{OL} = 0.8V$

Notes:

1. An initial pause of 200 µs is required after power-up followed by eight $\overline{\text{RAS}}$ refresh cycle ($\overline{\text{RAS}}$-Only or CBR) before proper device operation is assured. The eight $\overline{\text{RAS}}$ cycles wake-up should be repeated any time the t_{REF} refresh requirement is exceeded.
2. V_{IH} (MIN) and V_{IL} (MAX) are reference levels for measuring timing of input signals. Transition times, are measured between V_{IH} and V_{IL} (or between V_{IL} and V_{IH}) and assume to be 1 ns for all inputs.
3. In addition to meeting the transition rate specification, all input signals must transit between V_{IH} and V_{IL} (or between V_{IL} and V_{IH}) in a monotonic manner.
4. If $\overline{\text{CAS}}$ and $\overline{\text{RAS}}$ = V_{IH}, data output is High-Z.
5. If $\overline{\text{CAS}}$ = V_{IL}, data output may contain data from the last valid READ cycle.
6. Measured with a load equivalent to one TTL gate and 50 pF.
7. Assumes that $t_{RCD} \leq t_{RCD}$ (MAX). If t_{RCD} is greater than the maximum recommended value shown in this table, t_{RAC} will increase by the amount that t_{RCD} exceeds the value shown.
8. Assumes that $t_{RCD} \geq t_{RCD}$ (MAX).
9. If $\overline{\text{CAS}}$ is LOW at the falling edge of $\overline{\text{RAS}}$, data out will be maintained from the previous cycle. To initiate a new cycle and clear the data output buffer, $\overline{\text{CAS}}$ and $\overline{\text{RAS}}$ must be pulsed for t_{CP}.
10. Operation with the t_{RCD} (MAX) limit ensures that t_{RAC} (MAX) can be met. t_{RCD} (MAX) is specified as a reference point only; if t_{RCD} is greater than the specified t_{RCD} (MAX) limit, access time is controlled exclusively by t_{CAC}.
11. Operation within the t_{RAD} (MAX) limit ensures that t_{RCD} (MAX) can be met. t_{RAD} (MAX) is specified as a reference point only; if t_{RAD} is greater than the specified t_{RAD} (MAX) limit, access time is controlled exclusively by t_{AA}.
12. Either t_{RCH} or t_{RRH} must be satisfied for a READ cycle.
13. t_{OFF} (MAX) defines the time at which the output achieves the open circuit condition; it is not a reference to V_{OH} or V_{OL}.
14. t_{WCS}, t_{RWD}, t_{AWD} and t_{CWD} are restrictive operating parameters in LATE WRITE and READ-MODIFY-WRITE cycle only. If $t_{WCS} \geq t_{WCS}$ (MIN), the cycle is an EARLY WRITE cycle and the data output will remain open circuit throughout the entire cycle. If $t_{RWD} \geq t_{RWD}$ (MIN), $t_{AWD} \geq t_{AWD}$ (MIN) and $t_{CWD} \geq t_{CWD}$ (MIN), the cycle is a READ-WRITE cycle and the data output will contain data read from the selected cell. If neither of the above conditions is met, the state of I/O (at access time and until $\overline{\text{CAS}}$ and $\overline{\text{RAS}}$ or $\overline{\text{OE}}$ go back to V_{IH}) is indeterminate. $\overline{\text{OE}}$ held HIGH and $\overline{\text{WE}}$ taken LOW after $\overline{\text{CAS}}$ goes LOW result in a LATE WRITE ($\overline{\text{OE}}$-controlled) cycle.
15. Output parameter (I/O) is referenced to corresponding $\overline{\text{CAS}}$ input.
16. During a READ cycle, if $\overline{\text{OE}}$ is LOW then taken HIGH before $\overline{\text{CAS}}$ goes HIGH, I/O goes open. If $\overline{\text{OE}}$ is tied permanently LOW, a LATE WRITE or READ-MODIFY-WRITE is not possible.
17. Write command is defined as $\overline{\text{WE}}$ going low.
18. LATE WRITE and READ-MODIFY-WRITE cycles must have both t_{OD} and t_{OEH} met ($\overline{\text{OE}}$ HIGH during WRITE cycle) in order to ensure that the output buffers will be open during the WRITE cycle. The I/Os will provide the previously written data if $\overline{\text{CAS}}$ remains LOW and $\overline{\text{OE}}$ is taken back to LOW after t_{OEH} is met.
19. The I/Os are in open during READ cycles once t_{OD} or t_{OFF} occur.
20. Determined by falling edge of $\overline{\text{CAS}}$.
21. Determined by rising edge of $\overline{\text{CAS}}$.
22. These parameters are referenced to $\overline{\text{CAS}}$ leading edge in EARLY WRITE cycles and $\overline{\text{WE}}$ leading edge in LATE WRITE or READ-MODIFY-WRITE cycles.
23. $\overline{\text{CAS}}$ must meet minimum pulse width.
24. The 3 ns minimum is a parameter guaranteed by design.
25. Enables on-chip refresh and address counters.

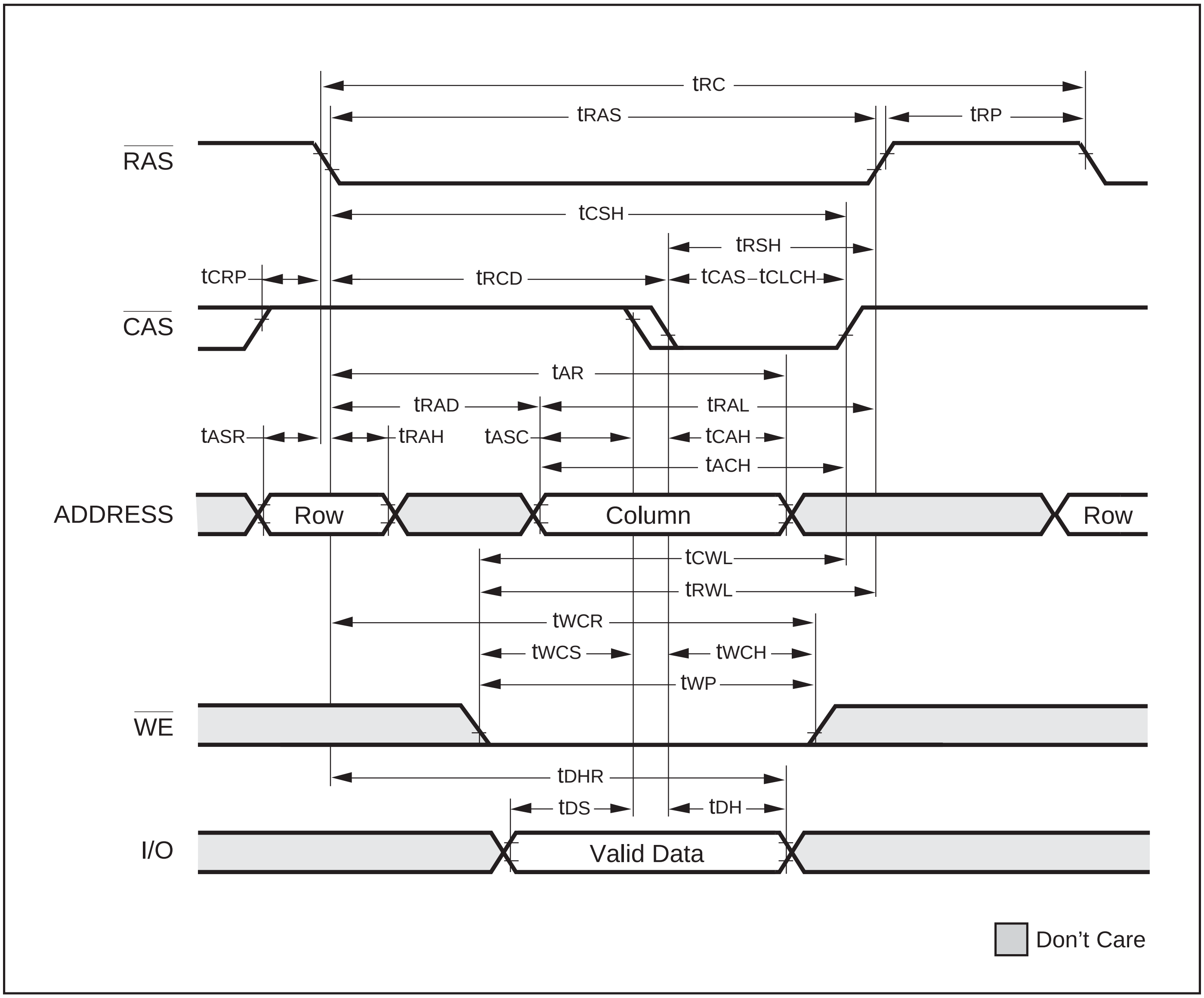
READ CYCLE



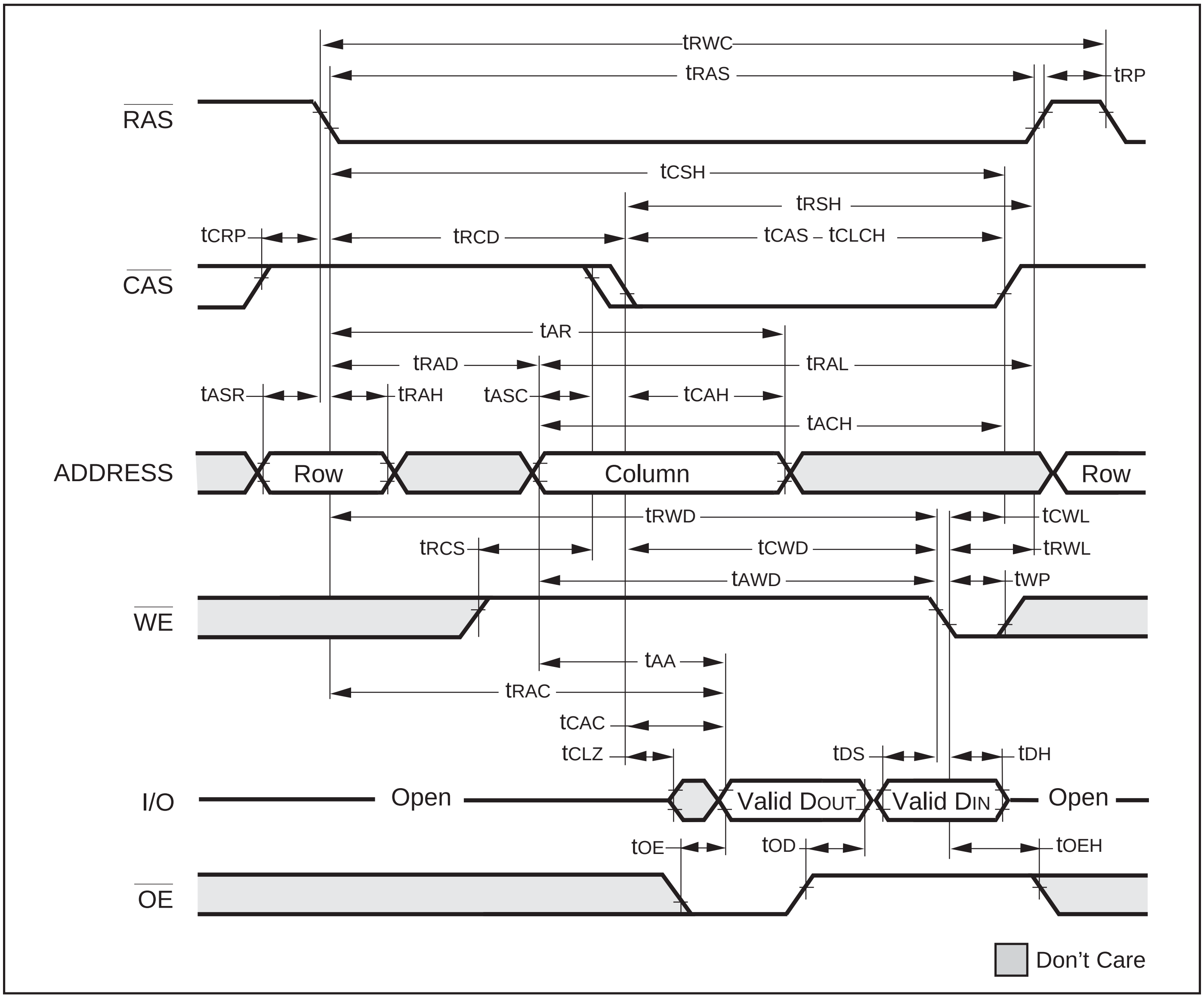
Note:

1. tOFF is referenced from rising edge of **RAS** or **CAS**, whichever occurs last.

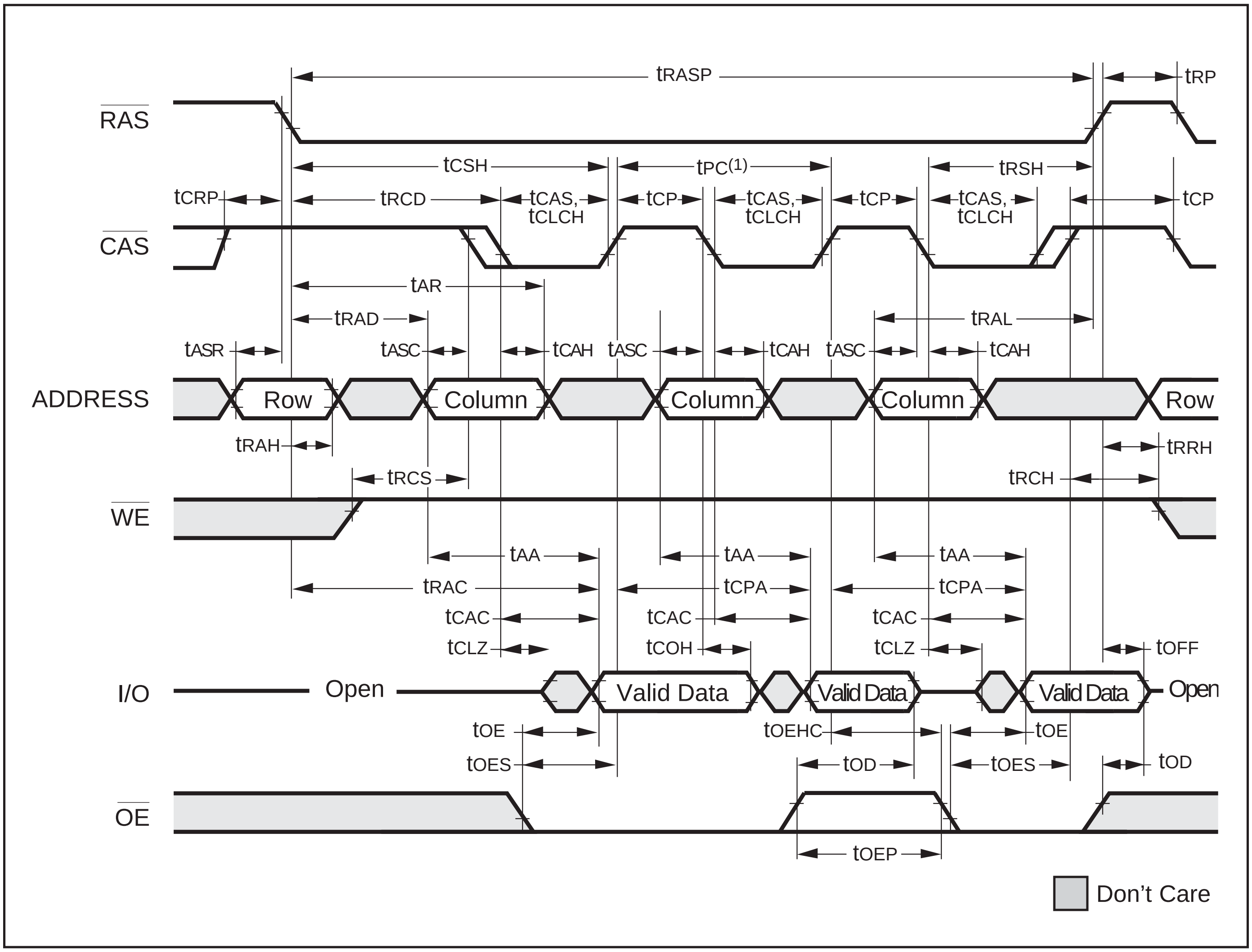
EARLY WRITE CYCLE ($\overline{\text{OE}}$ = DON'T CARE)



READ WRITE CYCLE (LATE WRITE and READ-MODIFY-WRITE Cycles)



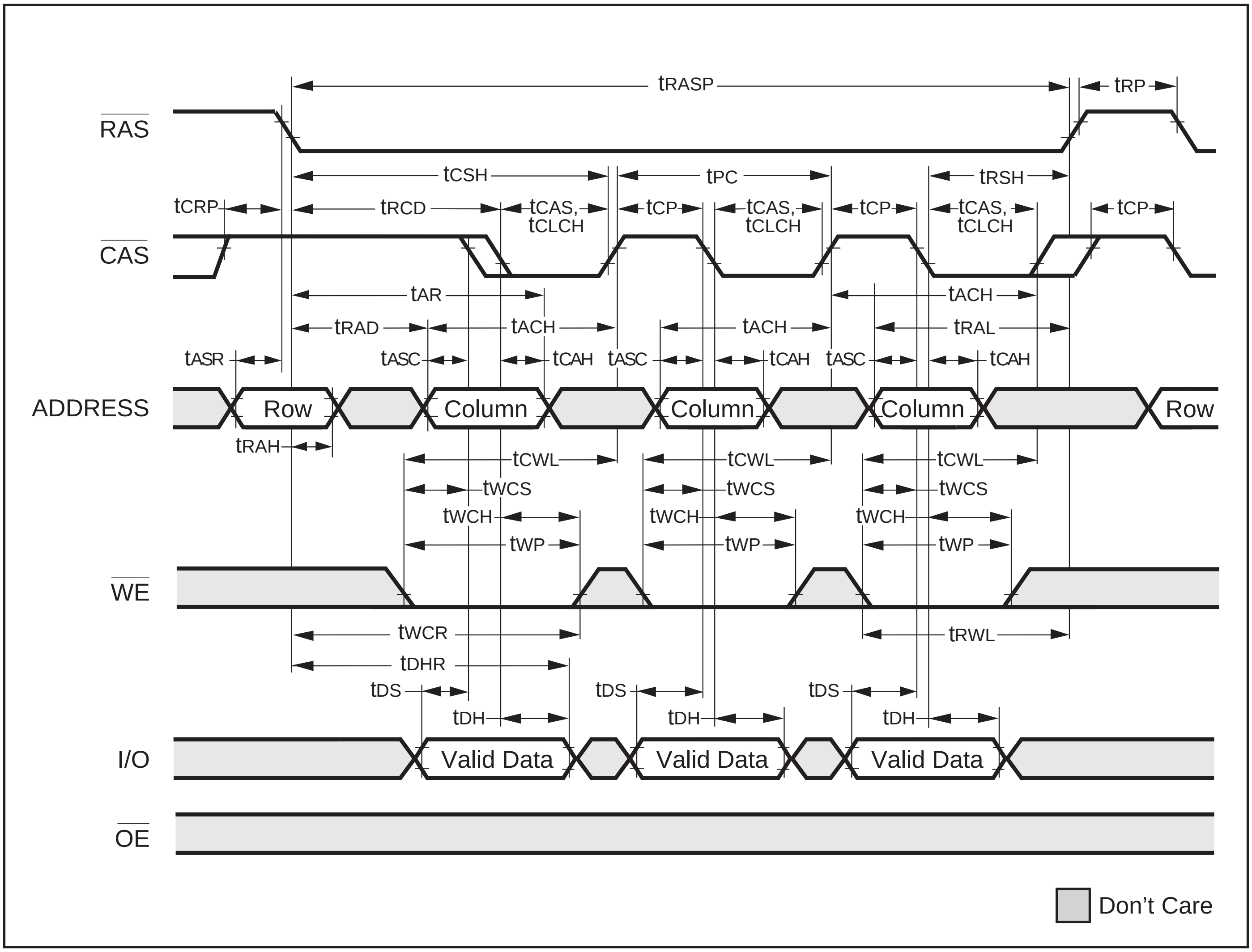
EDO-PAGE-MODE READ CYCLE



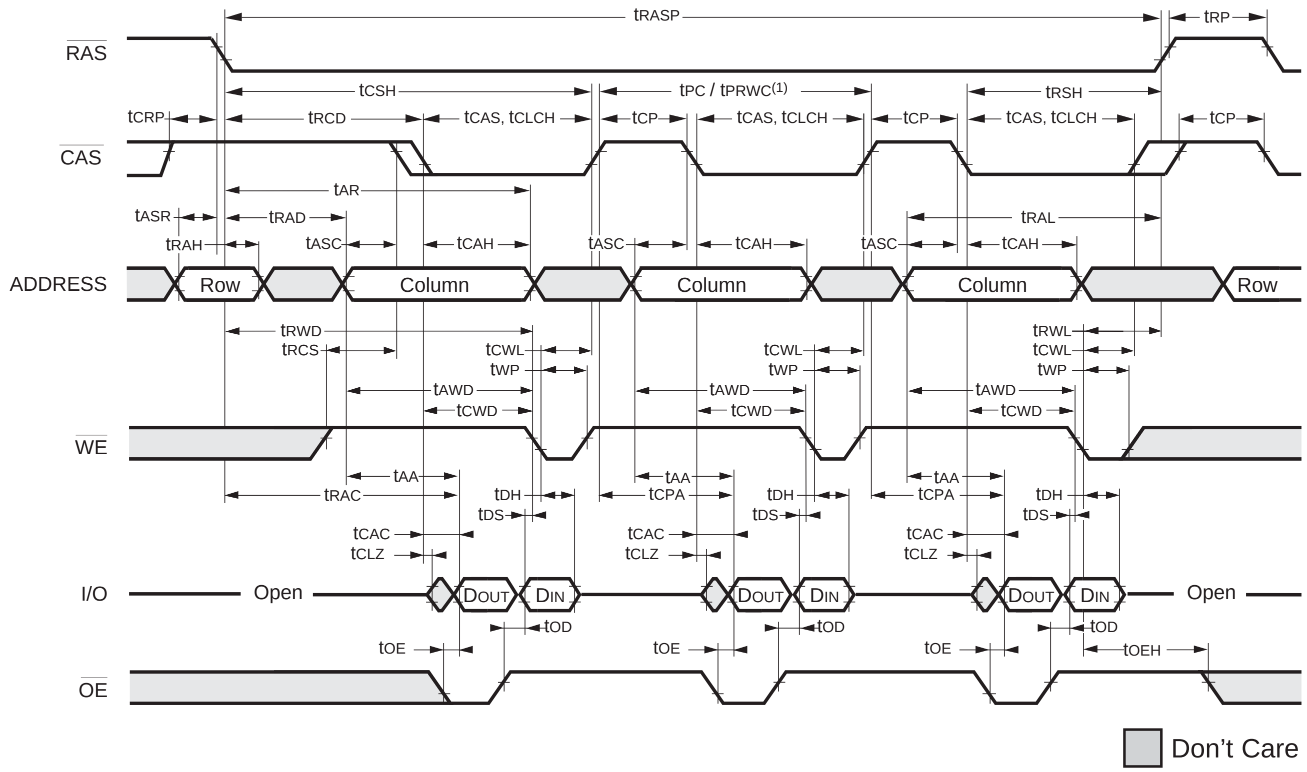
Note:

1. t_{PC} can be measured from falling edge of $\overline{\mathbf{CAS}}$ to falling edge of $\overline{\mathbf{CAS}}$, or from rising edge of $\overline{\mathbf{CAS}}$ to rising edge of $\overline{\mathbf{CAS}}$. Both measurements must meet the t_{PC} specifications.

EDO-PAGE-MODE EARLY-WRITE CYCLE



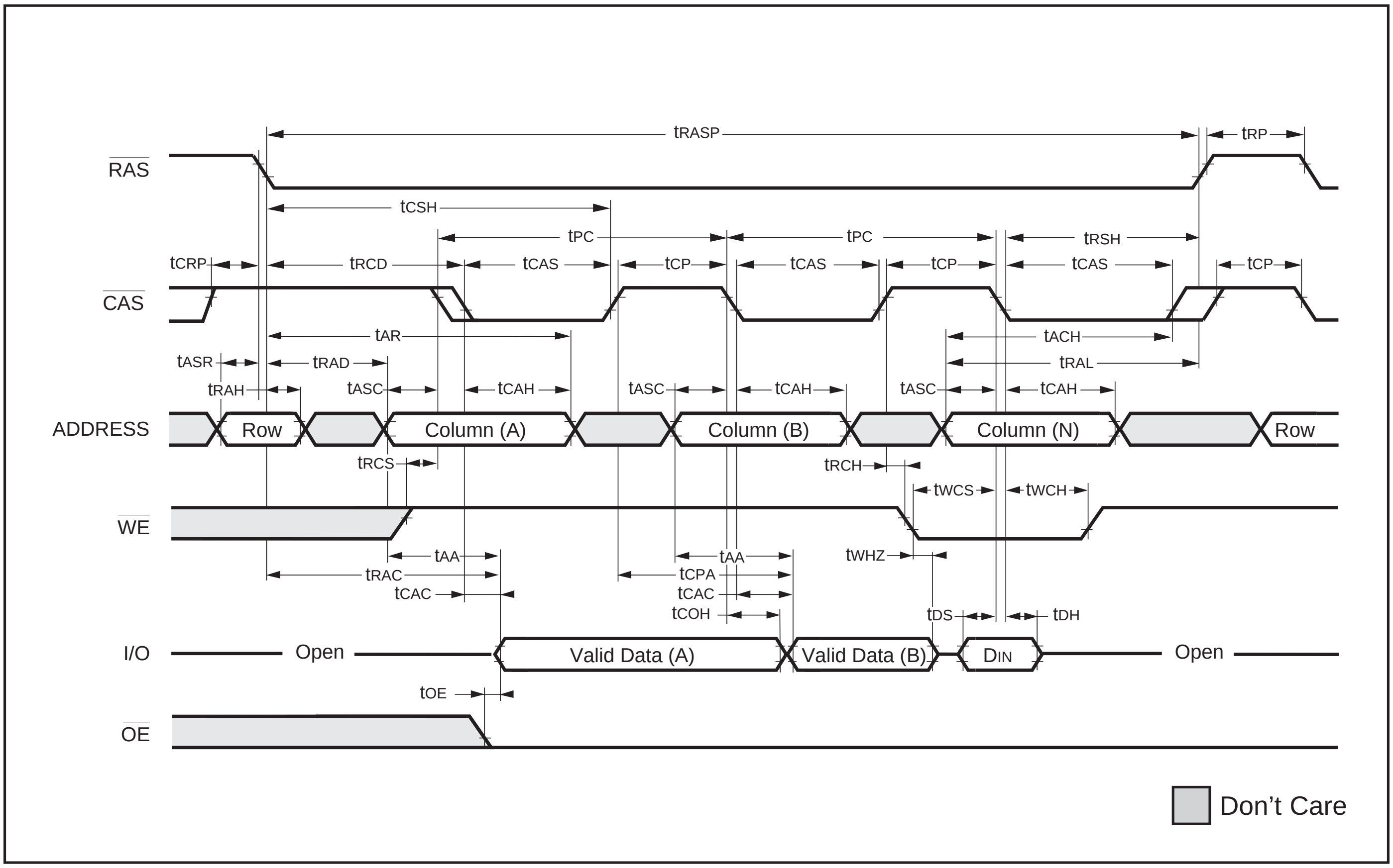
EDO-PAGE-MODE READ-WRITE CYCLE (LATE WRITE and READ-MODIFY WRITE Cycles)



Note:

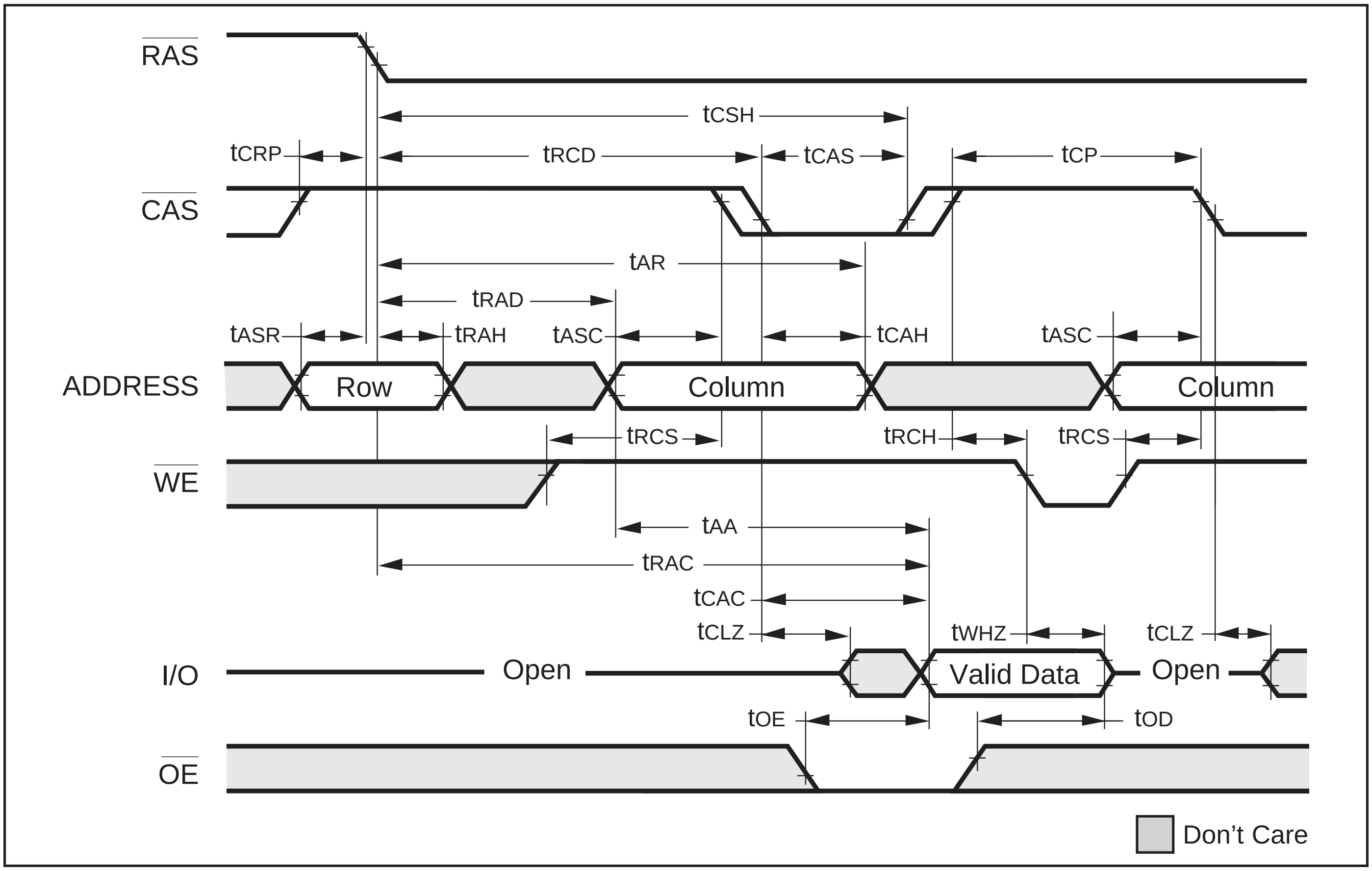
1. t_{PC} can be measured from falling edge of $\overline{\textbf{CAS}}$ to falling edge of $\overline{\textbf{CAS}}$, or from rising edge of $\overline{\textbf{CAS}}$ to rising edge of $\overline{\textbf{CAS}}$. Both measurements must meet the t_{PC} specifications.

EDO-PAGE-MODE READ-EARLY-WRITE CYCLE (Pseudo READ-MODIFY WRITE)

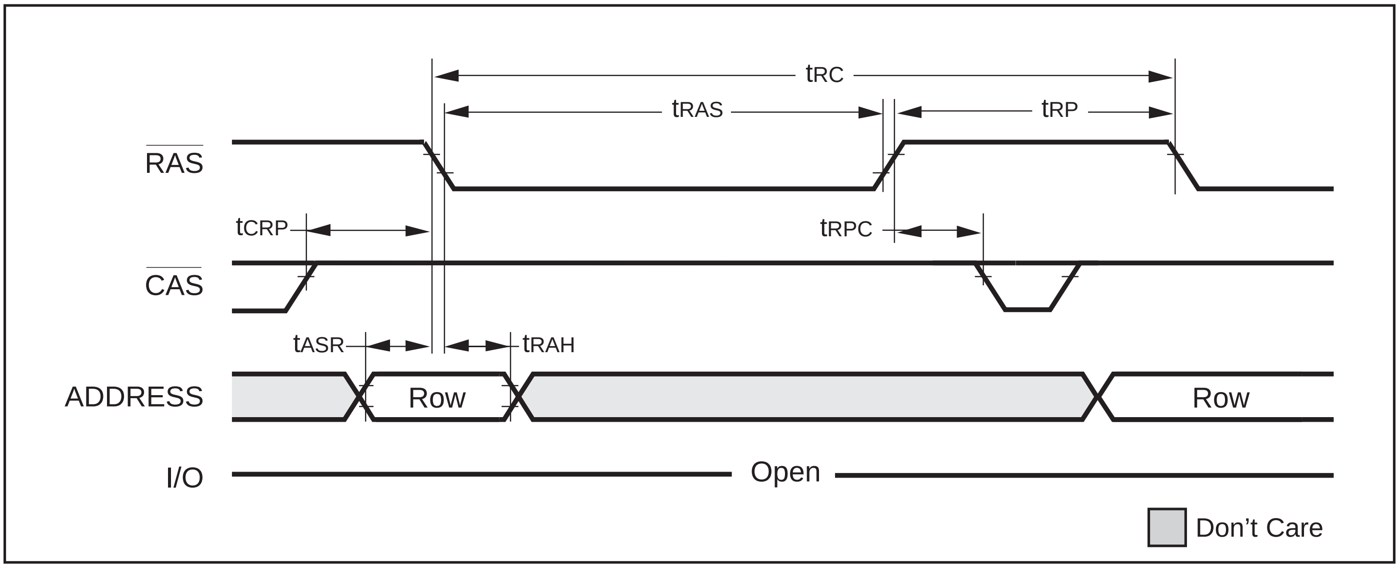


AC WAVEFORMS

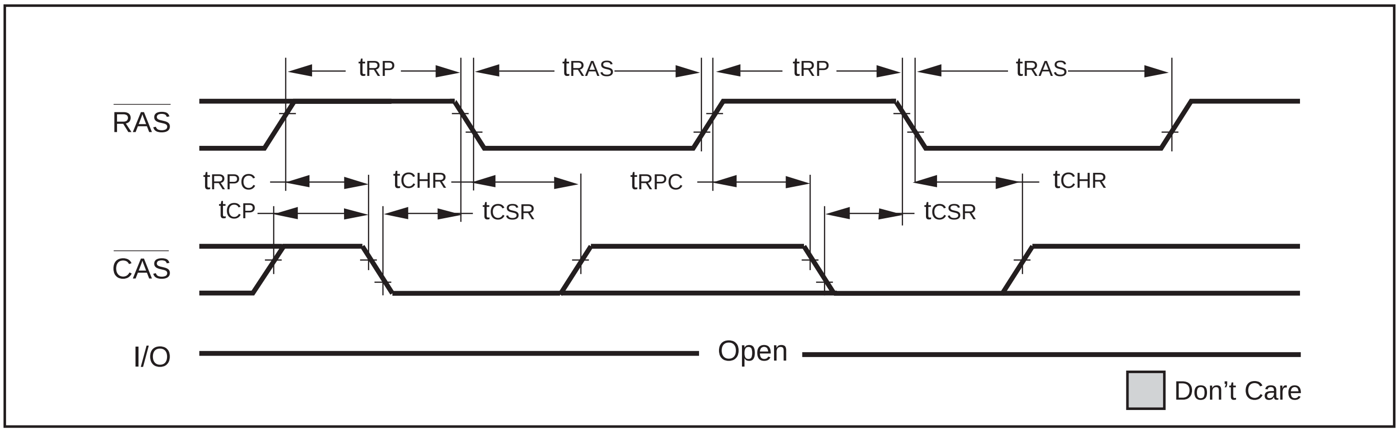
READ CYCLE (With WE-Controlled Disable)



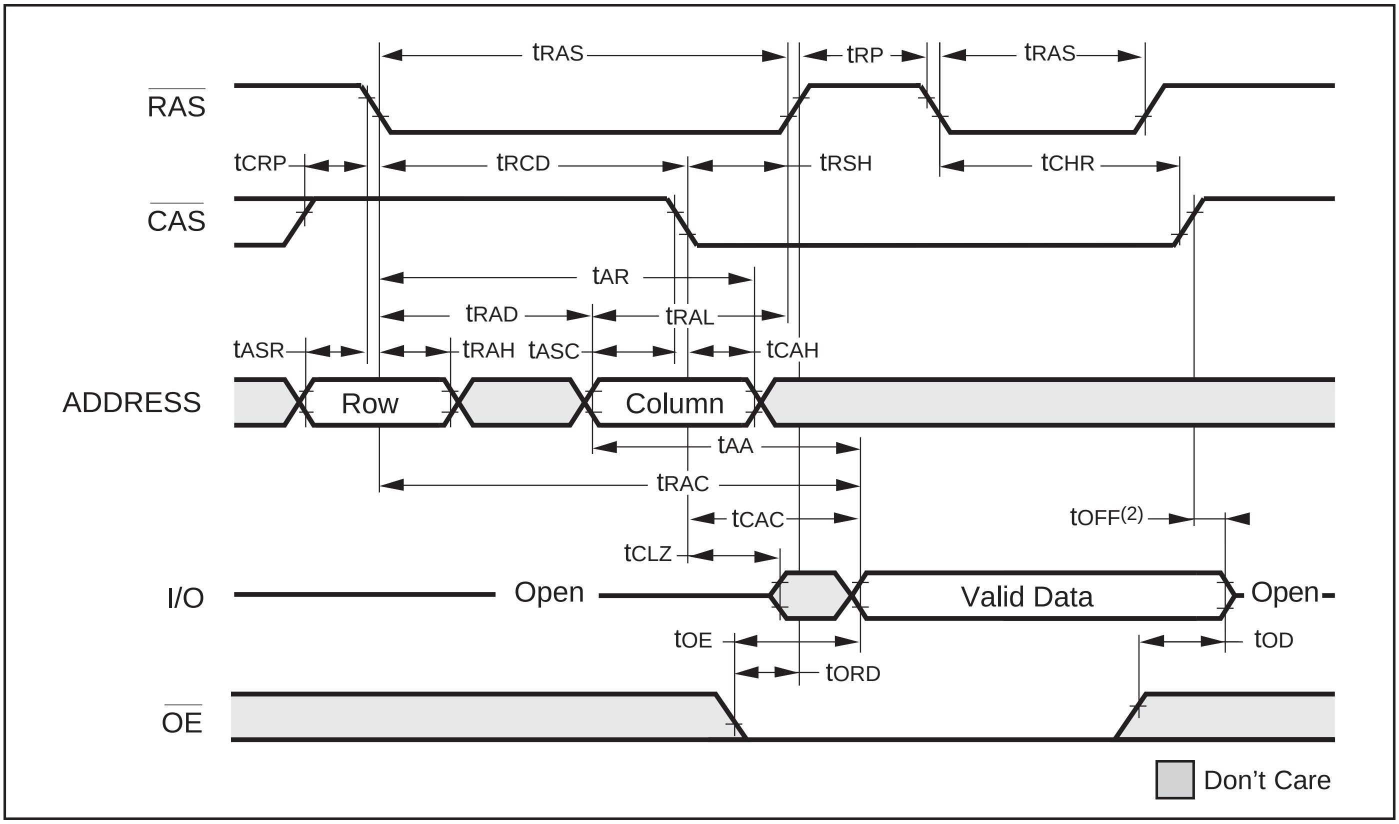
RAS-ONLY REFRESH CYCLE (OE, WE = DON'T CARE)



CBR REFRESH CYCLE (Addresses; WE, OE = DON'T CARE)



HIDDEN REFRESH CYCLE(1) (WE = HIGH; OE = LOW)



Notes:

1. A Hidden Refresh may also be performed after a Write Cycle. In this case, **WE** = LOW and **OE** = HIGH.
2. tOFF is referenced from rising edge of **RAS** or **CAS**, whichever occurs last.

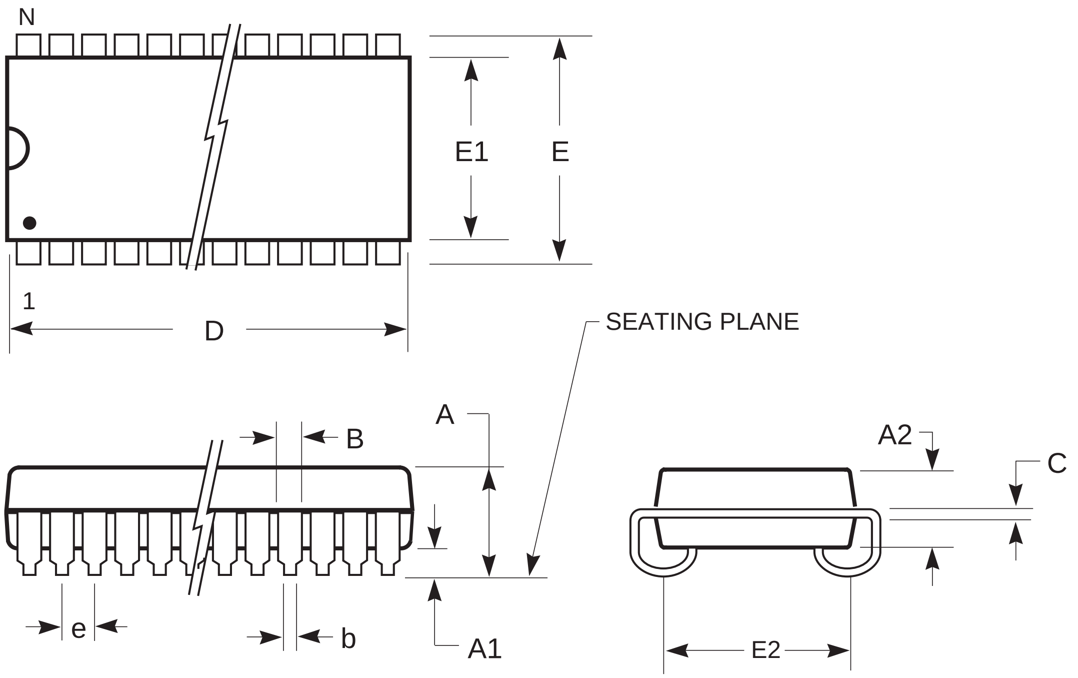
ORDERING INFORMATION

Automotive Range: -40°C to 85°C

Speed (ns)	Order Part No.	Refresh	Package
50	IS45LV44002B-50JA1	2K	300-mil SOJ
50	IS45LV44002B-50JLA1	2K	300-mil SOJ, Lead-free

PACKAGING INFORMATION

300-mil Plastic SOJ
Package Code: J



	MILLIMETERS			INCHES		
Sym.	**Min.**	**Typ.**	**Max.**	**Min.**	**Typ.**	**Max.**
N0. Leads		**24/26**				
A	—	—	3.56	—	—	0.140
A1	0.64	—	—	0.025	—	—
A2	2.41	—	2.67	0.095	—	0.105
b	0.41	—	0.51	0.016	—	0.020
B	0.66	—	0.81	0.026	—	0.032
C	0.20	—	0.25	0.008	—	0.010
D	17.02	—	17.27	0.670	—	0.680
E	8.26	—	8.76	0.325	—	0.345
E1	7.49	—	7.75	0.295	—	0.305
E2	6.27	—	7.29	0.247	—	0.287
e		1.27 BSC			0.050 BSC	

Notes:

1. Controlling dimension: inches, unless otherwise specified.
2. BSC = Basic lead spacing between centers.
3. Dimensions D and E1 do not include mold flash protrusions and should be measured from the bottom of the package.
4. Formed leads shall be planar with respect to one another within 0.004 inches at the seating plane.

PACKAGING INFORMATION

300-mil Plastic SOJ
Package Code: J

	MILLIMETERS			INCHES		
Sym.	**Min.**	**Typ.**	**Max.**	**Min.**	**Typ.**	**Max.**
N0. Leads		**28**				
A	—	—	3.56	—	—	0.140
A1	0.64	—	—	0.025	—	—
A2	2.41	—	2.67	0.095	—	0.105
b	0.41	—	0.51	0.016	—	0.020
B	0.66	—	0.81	0.026	—	0.032
C	0.20	—	0.25	0.008	—	0.010
D	18.29	—	18.54	0.720	—	0.730
E	8.26	—	8.76	0.325	—	0.345
E1	7.49	—	7.75	0.295	—	0.305
E2	6.27	—	7.29	0.247	—	0.287
e		1.27 BSC			0.050 BSC	

	MILLIMETERS			INCHES		
Sym.	**Min.**	**Typ.**	**Max.**	**Min.**	**Typ.**	**Max.**
N0. Leads		**32**				
A	—	—	3.56	—	—	0.140
A1	0.64	—	—	0.025	—	—
A2	2.41	—	2.67	0.095	—	0.105
b	0.41	—	0.51	0.016	—	0.020
B	0.66	—	0.81	0.026	—	0.032
C	0.20	—	0.25	0.008	—	0.010
D	20.83	—	21.08	0.820	—	0.830
E	8.26	—	8.76	0.325	—	0.345
E1	7.49	—	7.75	0.295	—	0.305
E2	6.27	—	7.29	0.247	—	0.287
e		1.27 BSC			0.050 BSC	