

72 Mb (2M x 36 & 4M x 18) DDR-IIP (Burst of 2) CIO Synchronous SRAMs



(2.5 Cycle Read Latency)

Advanced Information
May 2009

Features

- 2M x 36 or 4M x 18.
- On-chip delay-locked loop (DLL) for wide data valid window.
- Common data input/output bus.
- Synchronous pipeline read with self-timed late write operation.
- Double data rate (DDR-IIP) interface for read and write input ports.
- Fixed 2-bit burst for read and write operations.
- Clock stop support.
- Two input clocks (K and $\bar{K}$) for address and control registering at rising edges only.
- Industrial temperature available upon request.
- Two echo clocks (CQ and $\overline{CQ}$) that are delivered simultaneously with data.
- +1.8V core power supply and 1.5, 1.8V V_{DDQ} , used with 0.75, 0.9V V_{REF} .
- HSTL input and output levels.
- Registered addresses, write and read controls, byte writes, data in, and data outputs.
- Full data coherency.
- Boundary scan using limited set of JTAG 1149.1 functions.
- Byte write capability.
- Fine ball grid array (FBGA) package
 - 15mm x 17mm body size
 - 1mm pitch
 - 165-ball (11 x 15) array
- Programmable impedance output drivers via 5x user-supplied precision resistor.

Description

The 72Mb IS61DDPB22M36 and IS61DDPB24M18 are synchronous, high-performance CMOS static random access memory (SRAM) devices. These SRAMs have a common I/O bus. The rising edge of K clock initiates the read/write operation, and all internal operations are self-timed.

Refer to the *Timing Reference Diagram for Truth Table* on page 8 for a description of the basic operations of these DDR-IIP (Burst of 2) CIO SRAMs.

The input addresses are registered on all rising edges of the K clock. The DQ bus operates at double data rate for reads and writes. The following are registered internally on the rising edge of the K clock:

- Read and write addresses
- Address load
- Read/write enable
- Byte writes
- Data-in
- Data-out

The following are registered on the rising edge of the $\bar{K}$ clock:

- Byte writes
- Data-in for second burst addresses
- Data-out

Byte writes can change with the corresponding data-in to enable or disable writes on a per-byte basis. An internal write buffer enables the data-ins to be registered one cycle later than the write address. The first data-in burst is clocked with the rising edge of the next K clock, and the second burst is timed to the following rising edge of the $\bar{K}$ clock.

During the burst read operation, at the first burst the data-outs are updated from output registers off the second rising edge of the $\bar{K}$ clock (2.5 cycles later). At the second burst, the data-outs are updated with the fourth rising edge of the corresponding K clock (see page 8).

The device is operated with a single +1.8V power supply and is compatible with HSTL I/O interfaces.

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x36 FBGA Pinout (Top View)

	1	2	3	4	5	6	7	8	9	10	11
A	$\overline{\text{CQ}}$	NC/SA*	SA	R/ $\overline{\text{W}}$	$\overline{\text{BW}}_2$	$\overline{\text{K}}$	$\overline{\text{BW}}_1$	$\overline{\text{LD}}$	SA	SA	CQ
B	NC	DQ27	DQ18	SA	$\overline{\text{BW}}_3$	K	$\overline{\text{BW}}_0$	SA	NC	NC	DQ8
C	NC	NC	DQ28	V _{SS}	SA	NC	SA	V _{SS}	NC	DQ17	DQ7
D	NC	DQ29	DQ19	V _{SS}	V _{SS}	V _{SS}	V _{SS}	V _{SS}	NC	NC	DQ16
E	NC	NC	DQ20	V _{DDQ}	V _{SS}	V _{SS}	V _{SS}	V _{DDQ}	NC	DQ15	DQ6
F	NC	DQ30	DQ21	V _{DDQ}	V _{DD}	V _{SS}	V _{DD}	V _{DDQ}	NC	NC	DQ5
G	NC	DQ31	DQ22	V _{DDQ}	V _{DD}	V _{SS}	V _{DD}	V _{DDQ}	NC	NC	DQ14
H	$\overline{\text{Do}}\overline{\text{ff}}$	V _{REF}	V _{DDQ}	V _{DDQ}	V _{DD}	V _{SS}	V _{DD}	V _{DDQ}	V _{DDQ}	V _{REF}	ZQ
J	NC	NC	DQ32	V _{DDQ}	V _{DD}	V _{SS}	V _{DD}	V _{DDQ}	NC	DQ13	DQ4
K	NC	NC	DQ23	V _{DDQ}	V _{DD}	V _{SS}	V _{DD}	V _{DDQ}	NC	DQ12	DQ3
L	NC	DQ33	DQ24	V _{DDQ}	V _{SS}	V _{SS}	V _{SS}	V _{DDQ}	NC	NC	DQ2
M	NC	NC	DQ34	V _{SS}	V _{SS}	V _{SS}	V _{SS}	V _{SS}	NC	DQ11	DQ1
N	NC	DQ35	DQ25	V _{SS}	SA	SA	SA	V _{SS}	NC	NC	DQ10
P	NC	NC	DQ26	SA	SA	NC	SA	SA	NC	DQ9	DQ0
R	TDO	TCK	SA	SA	SA	NC	SA	SA	SA	TMS	TDI

* The following pins are reserved for higher densities: 2A for 144Mb

- $\overline{\text{BW}}_0$ controls writes to DQ0–DQ8; $\overline{\text{BW}}_1$ controls writes to DQ9–DQ17; $\overline{\text{BW}}_2$ controls writes to DQ18–DQ26; $\overline{\text{BW}}_3$ controls writes to DQ27–DQ35.

x18 FBGA Pinout (Top View)

	1	2	3	4	5	6	7	8	9	10	11
A	$\overline{\text{CQ}}$	SA	SA	R/ $\overline{\text{W}}$	$\overline{\text{BW}}_1$	$\overline{\text{K}}$	NC/SA*	$\overline{\text{LD}}$	SA	SA	CQ
B	NC	DQ9	NC	SA	NC/SA*	K	$\overline{\text{BW}}_0$	SA	NC	NC	DQ8
C	NC	NC	NC	V _{SS}	SA	NC	SA	V _{SS}	NC	DQ7	NC
D	NC	NC	DQ10	V _{SS}	V _{SS}	V _{SS}	V _{SS}	V _{SS}	NC	NC	NC
E	NC	NC	DQ11	V _{DDQ}	V _{SS}	V _{SS}	V _{SS}	V _{DDQ}	NC	NC	DQ6
F	NC	DQ12	NC	V _{DDQ}	V _{DD}	V _{SS}	V _{DD}	V _{DDQ}	NC	NC	DQ5
G	NC	NC	DQ13	V _{DDQ}	V _{DD}	V _{SS}	V _{DD}	V _{DDQ}	NC	NC	NC
H	$\overline{\text{Do}}\overline{\text{ff}}$	V _{REF}	V _{DDQ}	V _{DDQ}	V _{DD}	V _{SS}	V _{DD}	V _{DDQ}	V _{DDQ}	V _{REF}	ZQ
J	NC	NC	NC	V _{DDQ}	V _{DD}	V _{SS}	V _{DD}	V _{DDQ}	NC	DQ4	NC
K	NC	NC	DQ14	V _{DDQ}	V _{DD}	V _{SS}	V _{DD}	V _{DDQ}	NC	NC	DQ3
L	NC	DQ15	NC	V _{DDQ}	V _{SS}	V _{SS}	V _{SS}	V _{DDQ}	NC	NC	DQ2
M	NC	NC	NC	V _{SS}	V _{SS}	V _{SS}	V _{SS}	V _{SS}	NC	DQ1	NC
N	NC	NC	DQ16	V _{SS}	SA	SA	SA	V _{SS}	NC	NC	NC
P	NC	NC	DQ17	SA	SA	NC	SA	SA	NC	NC	DQ0
R	TDO	TCK	SA	SA	SA	NC	SA	SA	SA	TMS	TDI

* The following pin is reserved for higher densities: 7A for 144Mb, 5B for 288Mb.

- $\overline{\text{BW}}_0$ controls writes to DQ0–DQ8; $\overline{\text{BW}}_1$ controls writes to DQ9–DQ17

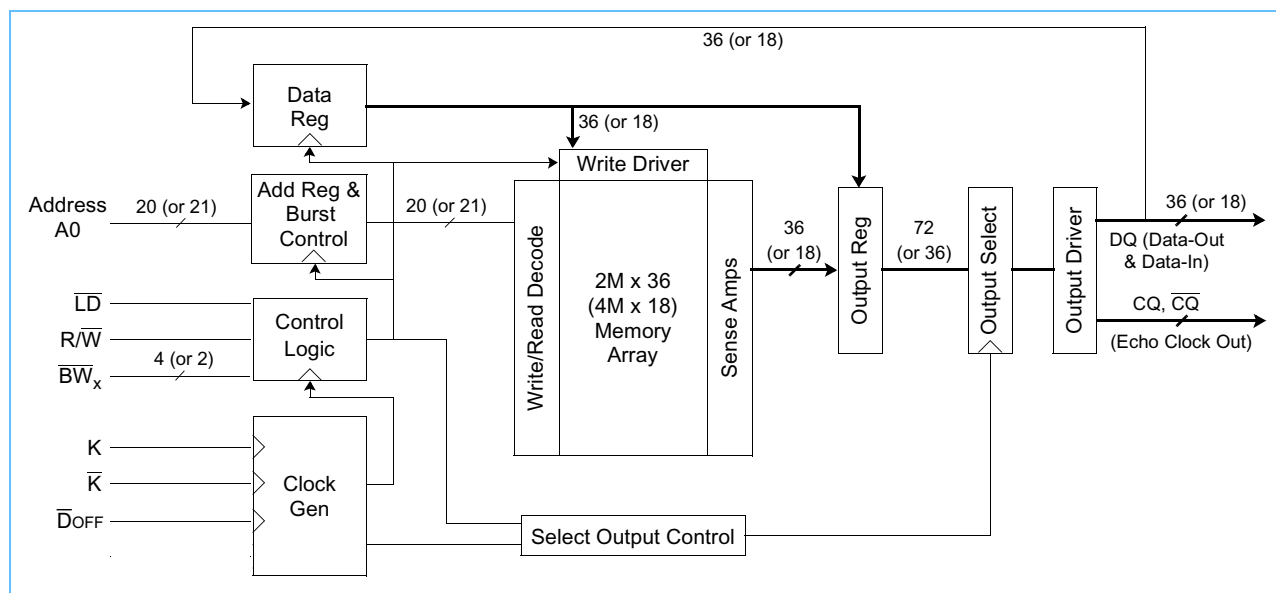
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Pin Description

Symbol	Pin Number	Description
K, $\overline{K}$	6B, 6A	Input clock.
CQ, $\overline{CQ}$	11A, 1A	Output echo clock.
$\overline{Doff}$	1H	DLL disable when low.
SA	3A, 9A, 10A, 4B, 8B, 5C, 7C, 5N, 6N, 7N, 4P, 5P, 7P, 8P, 3R, 4R, 5R, 7R, 8R, 9R	2M x 36 address inputs.
SA	2A, 3A, 9A, 10A, 4B, 8B, 5C, 7C, 5N, 6N, 7N, 4P, 5P, 7P, 8P, 3R, 4R, 5R, 7R, 8R, 9R	4M x 18 address inputs.
DQ0–DQ8 DQ9–DQ17 DQ18–DQ26 DQ27–DQ35	11P, 11M, 11L, 11K, 11J, 11F, 11E, 11C, 11B 10P, 11N, 10M, 10K, 10J, 11G, 10E, 11D, 10C 3B, 3D, 3E, 3F, 3G, 3K, 3L, 3N, 3P 2B, 3C, 2D, 2F, 2G, 3J, 2L, 3M, 2N	2M x 36 DQ pins
DQ0–DQ8 DQ9–DQ17	11P, 10M, 11L, 11K, 10J, 11F, 11E, 10C, 11B 2B, 3D, 3E, 2F, 3G, 3K, 2L, 3N, 3P	4M x 18 DQ pins
R/ $\overline{W}$	4A	Read/write control. Read when active high.
$\overline{LD}$	8A	Synchronizes load. Loads new address when low.
$\overline{BW}_0, \overline{BW}_1, \overline{BW}_2, \overline{BW}_3$	7B, 7A, 5A, 5B	2M x 36 byte write control, active low.
$\overline{BW}_0, \overline{BW}_1$	7B, 5A	4M x 18 byte write control, active low.
V _{REF}	2H, 10H	Input reference level.
V _{DD}	5F, 7F, 5G, 7G, 5H, 7H, 5J, 7J, 5K, 7K	Power supply.
V _{DDQ}	4E, 8E, 4F, 8F, 4G, 8G, 3H, 4H, 8H, 9H, 4J, 8J, 4K, 8K, 4L, 8L	Output power supply.
V _{SS}	4C, 8C, 4D, 5D, 6D, 7D, 8D, 5E, 6E, 7E, 6F, 6G, 6H, 6J, 6K, 5L, 6L, 7L, 4M, 5M, 6M, 7M, 8M, 4N, 8N	Ground
ZQ	11H	Output driver impedance control.
TMS, TDI, TCK	10R, 11R, 2R	IEEE 1149.1 test inputs (1.8V LVTTTL levels).
TDO	1R	IEEE 1149.1 test output (1.8V LVTTTL level).
NC	2A, 1B, 9B, 10B, 1C, 2C, 9C, 1D, 9D, 10D, 1E, 2E, 9E, 1F, 9F, 10F, 1G, 9G, 10G, 1J, 2J, 9J, 1K, 2K, 9K, 1L, 9L, 10L, 1M, 2M, 9M, 1N, 9N, 10N, 1P, 2P, 9P, 6R, 6P, 6C	x36 Configuration
NC	7A, 1B, 3B, 5B, 9B, 10B, 1C, 2C, 3C, 9C, 11C, 1D, 2D, 9D, 10D, 11D, 1E, 2E, 9E, 10E, 1F, 3F, 9F, 10F, 1G, 2G, 9G, 10G, 11G, 1J, 2J, 3J, 9J, 11J, 1K, 2K, 9K, 10K, 1L, 3L, 9L, 10L, 1M, 2M, 3M, 9M, 11M, 1N, 2N, 9N, 10N, 11N, 1P, 2P, 9P, 10P, 6R, 6P, 6C	x18 Configuration

Block Diagram



SRAM Features

Read Operations

The SRAM operates continuously in a burst-of-two mode. Read cycles are started by registering $\overline{R/W}$ in active high state at the rising edge of the K clock. The K and $\overline{K}$ clocks are also used to control the timing to the outputs. The data corresponding to the first address is clocked 2.5 cycles later by the rising edge of the $\overline{K}$ clock. The data corresponding to the second burst is clocked 3 cycles later by the following rising edge of the K clock. A set of free-running echo clocks, CQ and $\overline{CQ}$, are produced internally with timings identical to the data-outs. The echo clocks can be used as data capture clocks by the receiver device.

Whenever $\overline{LD}$ is low, a new address is registered at the rising edge of the K clock. A NOP operation ($\overline{LD}$ is high) does not terminate the previous read. The output drivers disable automatically to a high state.

Write Operations

Write operations can also be initiated at every rising edge of the K clock whenever $\overline{R/W}$ is low. The write address is also registered at that time. When the address needs to change, $\overline{LD}$ needs to be low simultaneously to be registered by the rising edge of K. Again, the write always occurs in bursts of two.

Because of its common I/O architecture, the data bus must be tri-stated at least one cycle before the new data-in is presented at the DQ bus.

The write data is provided in a 'late write' mode; that is, the data-in corresponding to the first address of the burst, is presented one cycle later or at the rising edge of the next K clock. The data-in corresponding to the second write burst address follows next, registered by the rising edge of $\overline{K}$.

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The data-in provided for writing is initially kept in write buffers. The information on these buffers is written into the array on the following write cycle. A read cycle to the last write address produces data from the write buffers. Similarly, a read address followed by the same write address produces the latest write data. The SRAM maintains data coherency.

During a write, the byte writes independently control which byte of any of the two burst addresses is written (see *X18/X36 Write Truth Tables* on page 9 and *Timing Reference Diagram for Truth Table* on page 8).

Whenever a write is disabled ($R/\overline{W}$ is high at the rising edge of K), data is not written into the memory.

RQ Programmable Impedance

An external resistor, RQ, must be connected between the ZQ pin on the SRAM and V_{SS} to enable the SRAM to adjust its output driver impedance. The value of RQ must be 5x the value of the intended line impedance driven by the SRAM. For example, an RQ of 250 Ω results in a driver impedance of 50 Ω . The allowable range of RQ to guarantee impedance matching is between 175 Ω and 350 Ω , with the tolerance described in *Programmable Impedance Output Driver DC Electrical Characteristics* on page 13. The RQ resistor should be placed less than two inches away from the ZQ ball on the SRAM module. The capacitance of the loaded ZQ trace must be less than 3 pF.

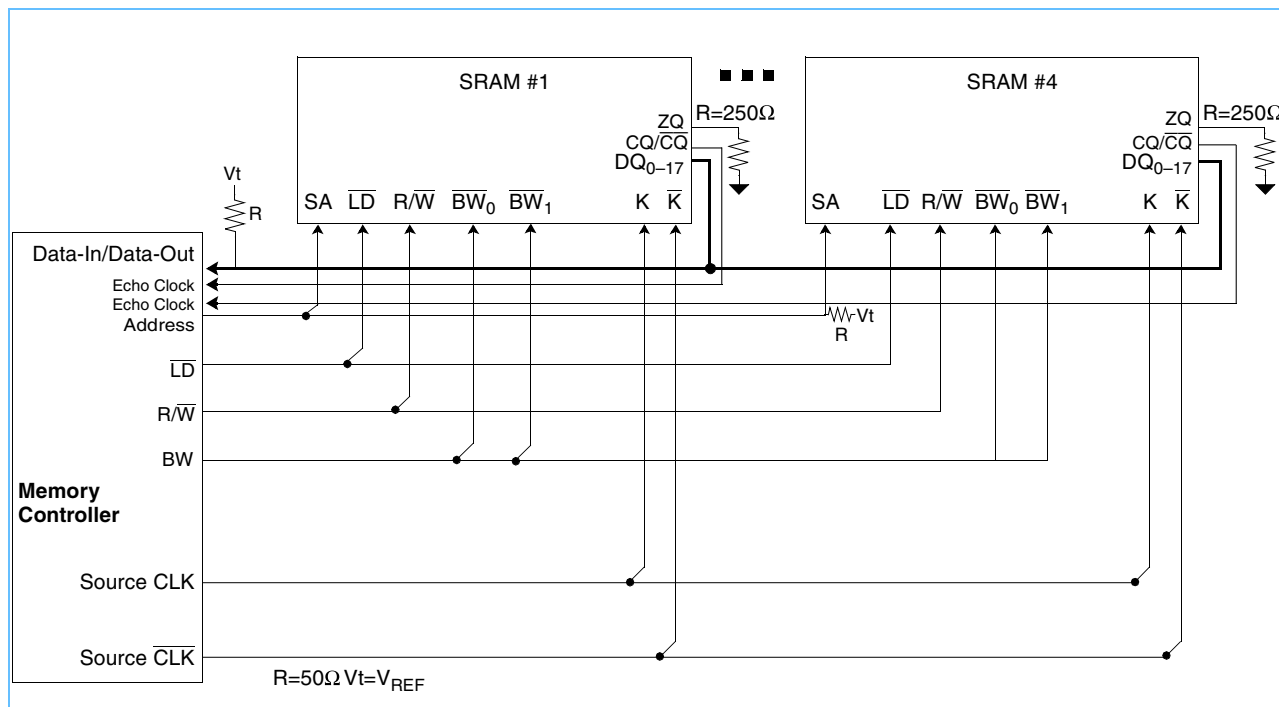
The ZQ pin can also be directly connected to V_{DDQ} to obtain a minimum impedance setting. ZQ must never be connected to V_{SS} .

Programmable Impedance and Power-Up Requirements

Periodic readjustment of the output driver impedance is necessary as the impedance is greatly affected by drifts in supply voltage and temperature. At power-up, the driver impedance is in the middle of allowable impedances values. The final impedance value is achieved within 2048 clock cycles.

Application Example

The following figure depicts an implementation of four 4M x 18 DDR-IIP SRAMs with common I/Os.



Power-Up and Power-Down Sequences

The following sequence is used for power-up:

1. The power supply inputs must be applied in the following order while keeping $\overline{\text{Doff}}$ in LOW logic state:

- 1) VDD
- 2) VDDQ
- 3) VREF

2. Start applying stable clock inputs (K, $\overline{\text{K}}$, C, and $\overline{\text{C}}$).

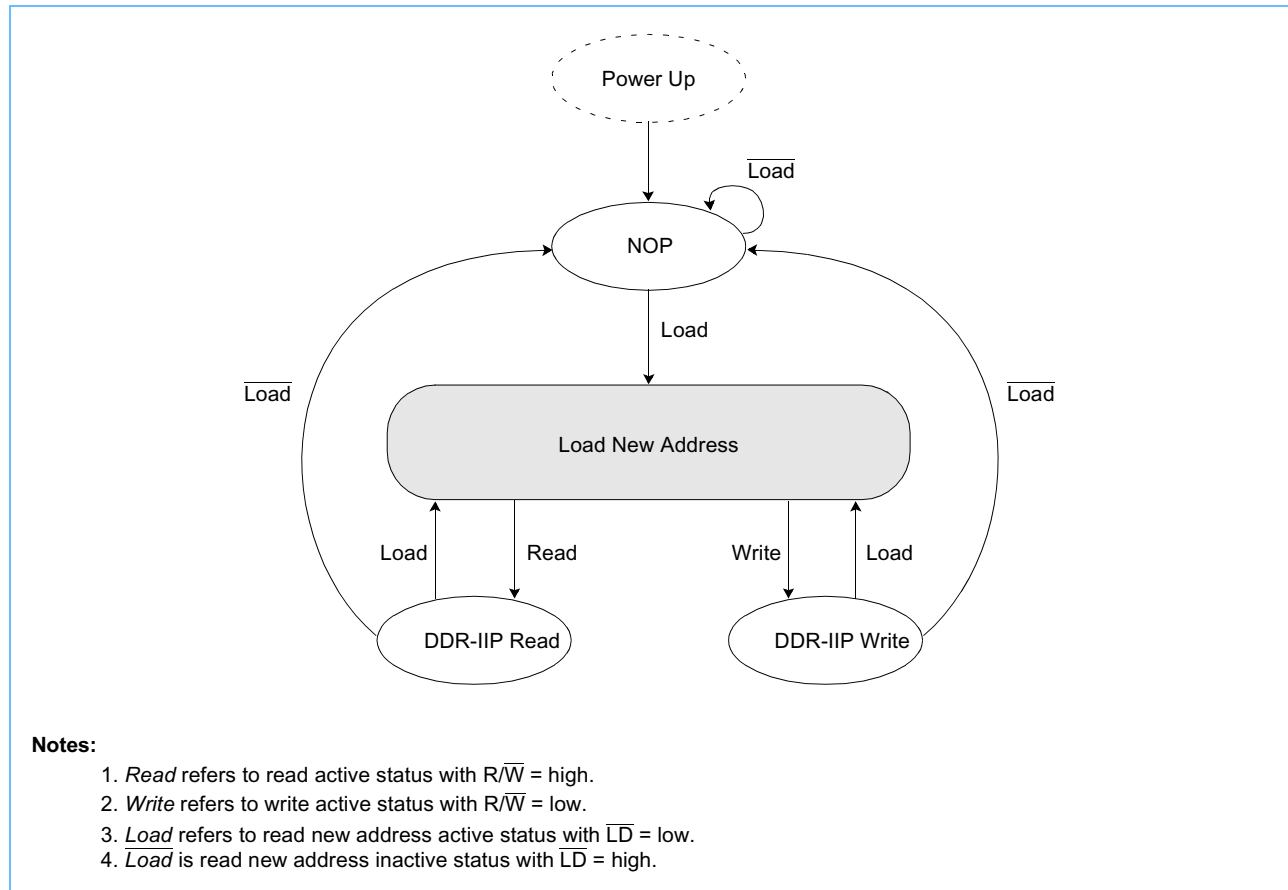
3. After clock signals have stabilized, change $\overline{\text{Doff}}$ to HIGH logic state.

4. Once the $\overline{\text{Doff}}$ is switched to HIGH logic state, wait an additional 1024 clock cycles to lock the DLL.

NOTES:

1. The power-down sequence must be done in reverse of the power-up sequence.
2. VDDQ can be allowed to exceed VDD by no more than 0.6V.
3. VREF can be applied concurrently with VDDQ.

State Diagram

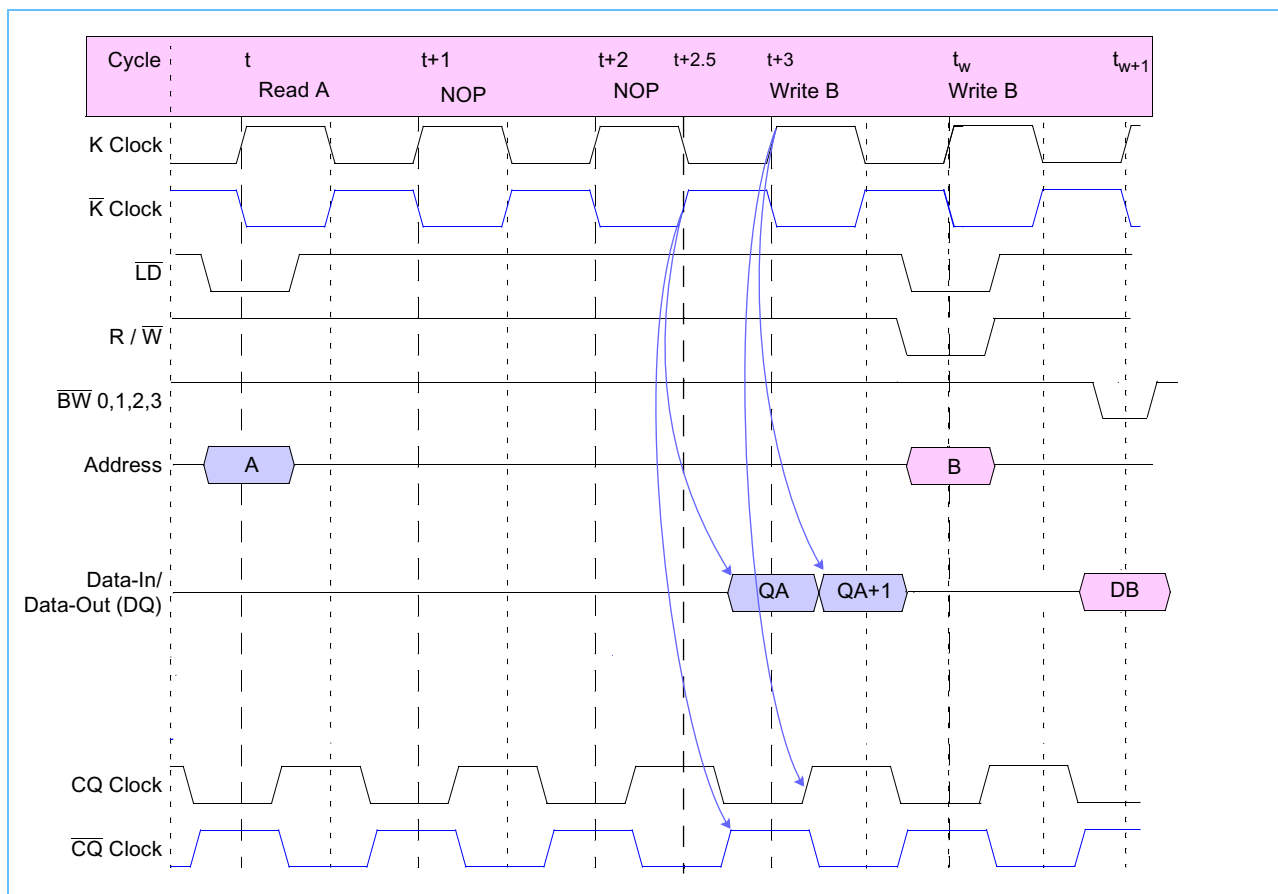


The *Timing Reference Diagram for Truth Table* on page 8 is helpful in understanding the clock and write truth tables, as it shows the cycle relationship between clocks, address, data in, data out, and controls. All read and write commands are issued at the beginning of cycle "t".

Linear Burst Sequence Table

Burst Sequence	SA ₀
First Address	1
Second Address	0

Timing Reference Diagram for Truth Table



Clock Truth Table (Use the following table with the *Timing Reference Diagram for Truth Table*.)

Mode	Clock	Controls		Data-Out/Data-In	
	K	$\bar{LD}$	R/ $\bar{W}$	Q_A / D_B	Q_{A+1} / D_{B+1}
Stop Clock	Stop	X	X	Previous state	Previous state
No Operation (NOP)	L H	H	H	High-Z	High-Z
Read A	L H	L	X	D out at $\bar{K}(t + 2.5)$	D out at $K(t + 3)$
Write B	L H	X	L	$D_B(t_W + 1)$	$D_B(t_W + 1.5)$

Notes:

1. The internal burst counter is always fixed as two-bit.
2. X = don't care; H = logic "1"; L = logic "0".
3. A read operation is started when control signal $R/\bar{W}$ is active high.
4. A write operation is started when control signal $R/\bar{W}$ is active low.
5. Before entering into the stop clock, all pending read and write commands must be completed.
6. For timing definitions, refer to the *AC Characteristics* on page 15. Signals must have AC specifications at timings indicated in parenthesis with respect to switching clocks K and $\bar{K}$.

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X36 Write Truth Table Use the following table with the *Timing Reference Diagram for Truth Table* on page 8.

Operation	K (t_w)	$\bar{K}$ ($t_w + 0.5$)	$\overline{BW}_0$	$\overline{BW}_1$	$\overline{BW}_2$	$\overline{BW}_3$	D_B	D_{B+1}
Write Byte 0	L→H		L	H	H	H	D0-8 ($t_w + 1$)	
Write Byte 1	L→H		H	L	H	H	D9-17 ($t_w + 1$)	
Write Byte 2	L→H		H	H	L	H	D18-26 ($t_w + 1$)	
Write Byte 3	L→H		H	H	H	L	D27-35 ($t_w + 1$)	
Write All Bytes	L→H		L	L	L	L	D0-35 ($t_w + 1$)	
Abort Write	L→H		H	H	H	H	Don't care	
Write Byte 0		L→H	L	H	H	H		D0-8 ($t_w + 1.5$)
Write Byte 1		L→H	H	L	H	H		D9-17 ($t_w + 1.5$)
Write Byte 2		L→H	H	H	L	H		D18-26 ($t_w + 1.5$)
Write Byte 3		L→H	H	H	H	L		D27-35 ($t_w + 1.5$)
Write All Bytes		L→H	L	L	L	L		D0-35 ($t_w + 1.5$)
Abort Write		L→H	H	H	H	H		Don't care

Notes;

1. For all cases, $\overline{R/\overline{W}}$ must be active low during the rising edge of K occurring at time t_w .
2. For timing definitions, refer to the *AC Characteristics* on page 15. Signals must have AC specifications with respect to switching clocks K and $\bar{K}$.

X18 Write Truth Table (Use this table with the *Timing Reference Diagram for Truth Table* on page 8.)

Operation	K (t_w)	$\bar{K}$ ($t_w + 0.5$)	$\overline{BW}_0$	$\overline{BW}_1$	D_B	D_{B+1}
Write Byte 0 on B	L→H		L	H	D0-8 ($t_w + 1$)	
Write Byte 1 on B	L→H		H	L	D9-17 ($t_w + 1$)	
Write All Bytes on B	L→H		L	L	D0-17 ($t_w + 1$)	
Abort Write on B	L→H		H	H	Don't care	
Write Byte 1 on B+1		L→H	L	H		D0-8 ($t_w + 1.5$)
Write Byte 2 on B+1		L→H	H	L		D9-17 ($t_w + 1.5$)
Write All Bytes on B+1		L→H	L	L		D0-17 ($t_w + 1.5$)
Abort Write on B+1		L→H	H	H		Don't care

Notes;

1. Refer to *Timing Reference Diagram for Truth Table* on page 8. Cycle time starts at n and is referenced to the K clock.
2. For all cases, $\overline{R/\overline{W}}$ must be active low during the rising edge of K occurring at t_w .
3. For timing definitions, refer to the *AC Characteristics* on page 15. Signals must have AC specs with respect to switching clocks K and $\bar{K}$.

Absolute Maximum Ratings

Item	Symbol	Rating	Units
Power supply voltage	V_{DD}	-0.5 to 2.9	V
Output power supply voltage	V_{DDQ}	-0.5 to 2.9	V
Input voltage	V_{IN}	-0.5 to $V_{DD}+0.3$	V
Data out voltage	V_{DOUT}	-0.5 to 2.6	V
Operating temperature	T_A	0 to 70	°C
Junction temperature	T_J	110	°C
Storage temperature	T_{STG}	-55 to +125	°C

Note: Stresses greater than those listed in this table can cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this datasheet is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

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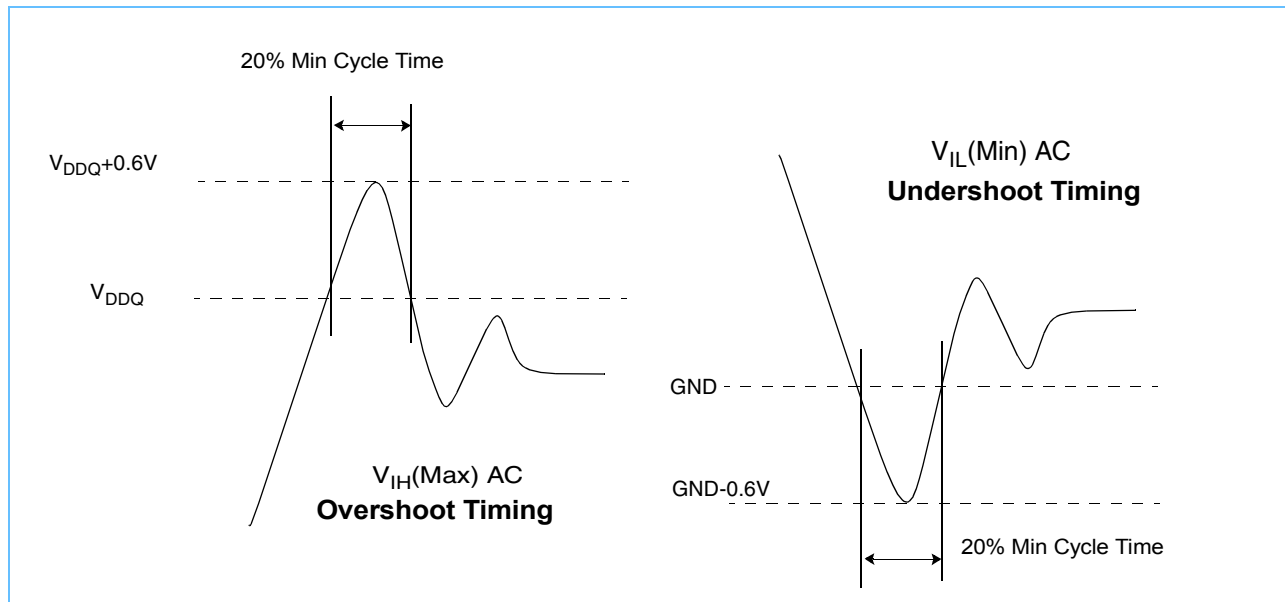


Recommended DC Operating Conditions ($T_A = 0$ to $+70^\circ\text{C}$)

Parameter	Symbol	Minimum	Typical	Maximum	Units	Notes
Supply voltage	V_{DD}	1.8 - 5%		1.8 + 5%	V	1
Output driver supply voltage	V_{DDQ}	1.4		1.9	V	1
Input high voltage	V_{IH}	$V_{REF} + 0.1$		$V_{DDQ} + 0.2$	V	1, 2
Input low voltage	V_{IL}	-0.2		$V_{REF} - 0.1$	V	1, 3
Input reference voltage	V_{REF}	0.68		0.95	V	1, 5
Clocks signal voltage	V_{IN-CLK}	-0.2		$V_{DDQ} + 0.2$	V	1, 4

1. All voltages are referenced to V_{SS} . All V_{DD} , V_{DDQ} , and V_{SS} pins must be connected.
2. $V_{IH}(\text{Max})$ AC = See *Overshoot and Undershoot Timings*.
3. $V_{IL}(\text{Min})$ AC = See *Overshoot and Undershoot Timings*.
4. V_{IN-CLK} specifies the maximum allowable DC excursions of each clock (K and $\bar{K}$).
5. Peak-to-peak AC component superimposed on V_{REF} may not exceed 5% of V_{REF} .

Overshoot and Undershoot Timings



PBGA Thermal Characteristics

Item	Symbol	Rating	Units
Thermal resistance junction to ambient (airflow = 1m/s)	R _{ΘJA}	TBD	°C/W
Thermal resistance junction to case	R _{ΘJC}	TBD	°C/W
Thermal resistance junction to pins	R _{ΘJB}	TBD	°C/W

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Capacitance ($T_A = 0$ to $+70^\circ\text{C}$, $V_{DD} = 1.8\text{V} -5\%, +5\%$, $f = 1\text{MHz}$)

Parameter	Symbol	Test Condition	Maximum	Units
Input capacitance	C_{IN}	$V_{IN} = 0\text{V}$	4	pF
Data-in/Out capacitance (DQ0–DQ35)	C_{DQ}	$V_{DIN} = 0\text{V}$	4	pF
Clocks Capacitance (K and $\bar{K}$)	C_{CLK}	$V_{CLK} = 0\text{V}$	4	pF

DC Electrical Characteristics ($T_A = 0$ to $+70^\circ\text{C}$, $V_{DD} = 1.8\text{V} -5\%, +5\%$)

Parameter	Symbol	Minimum	Maximum	Units	Notes
x36 average power supply operating current ($I_{OUT} = 0$, $V_{IN} = V_{IH}$ or V_{IL})	I_{DD33} I_{DD40} I_{DD50}	— — —	600 550 500	mA	1, 3
x18 average power supply operating current ($I_{OUT} = 0$, $V_{IN} = V_{IH}$ or V_{IL})	I_{DD33} I_{DD40} I_{DD50}	— — —	600 550 500	mA	1, 3
Power supply standby current ($\bar{R} = V_{IH}$, $\bar{W} = V_{IH}$. All other inputs = V_{IH} or V_{IL} , $I_{IH} = 0$)	I_{SBSS}	—	200	mA	1
Input leakage current, any input (except JTAG) ($V_{IN} = V_{SS}$ or V_{DD})	I_{LI}	-2	+2	uA	
Output leakage current ($V_{OUT} = V_{SS}$ or V_{DDQ} , Q in High-Z)	I_{LO}	-2	+2	uA	
Output “high” level voltage ($I_{OH} = -6\text{mA}$)	V_{OH}	$V_{DDQ} - .4$	V_{DDQ}	V	2, 4
Output “low” level voltage ($I_{OL} = +6\text{mA}$)	V_{OL}	V_{SS}	$V_{SS} + .4$	V	2, 4
JTAG leakage current ($V_{IN} = V_{SS}$ or V_{DD})	I_{LIJTAG}	-100	+100	uA	5

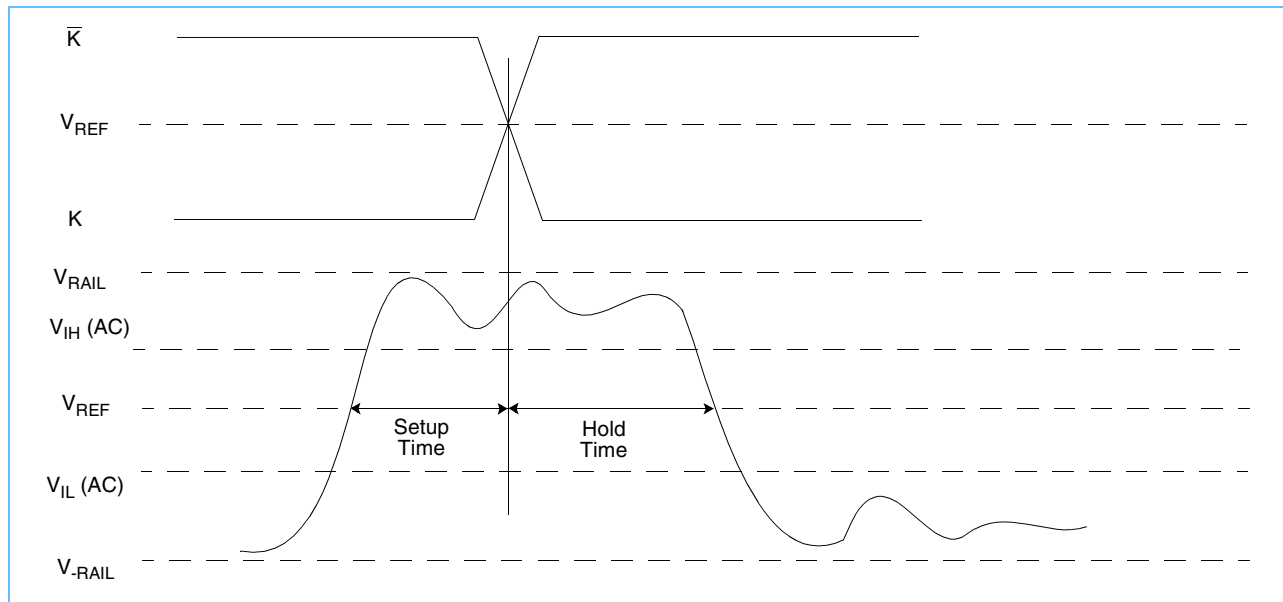
1. I_{OUT} = chip output current.
2. Minimum impedance output driver.
3. The numeric suffix indicates the part operating at speed, as indicated in *AC Characteristics* on page 15.
4. JEDEC Standard JESD8-6 Class 1 compatible.
5. For JTAG inputs only.
6. Currents are estimates only and need to be verified.

Typical AC Input Characteristics

Item	Symbol	Minimum	Maximum	Notes
AC input logic high	$V_{IH} (ac)$	$V_{REF} + 0.2$		1, 2, 3, 4
AC input logic low	$V_{IL} (ac)$		$V_{REF} - 0.2$	1, 2, 3, 4
Clock input logic high (K, $\bar{K}$)	$V_{IH-CLK} (ac)$	$V_{REF} + 0.2$		1, 2, 3
Clock input logic low (K, $\bar{K}$)	$V_{IL-CLK} (ac)$		$V_{REF} - 0.2$	1, 2, 3

1. The peak-to-peak AC component superimposed on V_{REF} may not exceed 5% of the DC component of V_{REF} .
2. Performance is a function of V_{IH} and V_{IL} levels to clock inputs.
3. See the *AC Input Definition* diagram.
4. See the *AC Input Definition* diagram. The signals should swing monotonically with no steps rail-to-rail with input signals never ringing back past $V_{IH} (AC)$ and $V_{IL} (AC)$ during the input setup and input hold window. $V_{IH} (AC)$ and $V_{IL} (AC)$ are used for timing purposes only.

AC Input Definition



Programmable Impedance Output Driver DC Electrical Characteristics

($T_A = 0$ to $+70^\circ C$, $V_{DD} = 1.8V \pm 5\%$, $+5\%$, $V_{DDQ} = 1.5, 1.8V$)

Parameter	Symbol	Minimum	Maximum	Units	Notes
Output "high" level voltage	V_{OH}	$V_{DDQ} / 2$	V_{DDQ}	V	1, 3
Output "low" level voltage	V_{OL}	V_{SS}	$V_{DDQ} / 2$	V	2, 3

1. $I_{OH} = \left(\frac{V_{DDQ}}{2} \right) / \left(\frac{RQ}{5} \right) \pm 15\%$ @ $V_{OH} = V_{DDQ} / 2$ For: $175\Omega \leq RQ \leq 350\Omega$
2. $I_{OL} = \left(\frac{V_{DDQ}}{2} \right) / \left(\frac{RQ}{5} \right) \pm 15\%$ @ $V_{OL} = V_{DDQ} / 2$ For: $175\Omega \leq RQ \leq 350\Omega$
3. Parameter tested with $RQ = 250\Omega$ and $V_{DDQ} = 1.5V$.

72 Mb (2M x 36 & 4M x 18) DDR-IIP (Burst of 2) CIO Synchronous SRAMs

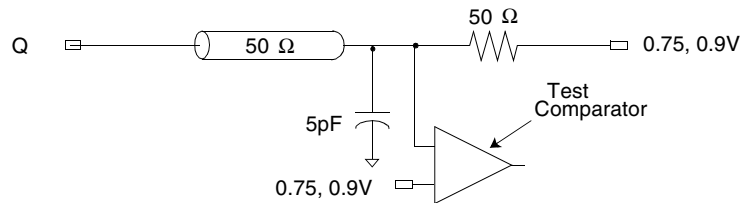


AC Test Conditions ($T_A = 0$ to $+70^\circ\text{C}$, $V_{DD} = 1.8\text{V} -5\%, +5\%$, $V_{DDQ} = 1.5, 1.8\text{V}$)

Parameter	Symbol	Conditions	Units	Notes
Output driver supply voltage	V_{DDQ}	1.5, 1.8	V	
Input high level	V_{IH}	$V_{REF}+0.5$	V	
Input Low Level	V_{IL}	$V_{REF}-0.5$	V	
Input reference voltage	V_{REF}	0.75, 0.9	V	
Input rise time	T_R	0.35	ns	
Input fall time	T_F	0.35	ns	
Output timing reference level		V_{REF}	V	
Clocks reference level		V_{REF}	V	
Output load conditions				1, 2

1. See AC Test Loading.
2. Parameter tested with $R_Q = 250\Omega$ and $V_{DDQ} = 1.5\text{V}$.

AC Test Loading



72 Mb (2M x 36 & 4M x 18) DDR-IIP (Burst of 2) CIO Synchronous SRAMs



AC CHARACTERISTICS (V_{dd} = 1.8V ± 0.1V, T_A = 0 °C to 70 °C)

ISSI Parameter	Description	DDR IIP										unit	notes
		400		375		333		300					
		min	max	min	max	min	max	min	max				
tKHKH	K Clock Cycle Time	2.50	7.50	2.66	7.50	3.00	7.50	3.30	7.50	ns			
tKHKL	Input Clock (K/K) HIGH	0.40		0.40		0.40		0.40		tKHKH			
tKLKH	Input Clock (K/K) LOW	0.40		0.40		0.40		0.40		tKHKH			
tKHKH	K Clock Rise to K Clock Rise (rising edge to rising edge)	1.06		1.13		1.28		1.40		ns			
Setup Times													
tAVKH	Address Setup to K Clock Rise	0.40		0.40		0.40		0.40		ns	2		
tIVKH	Control Setup to K Clock Rise (R, W)	0.40		0.40		0.40		0.40		ns	2		
tIVKH	Double Data Rate Control Setup to Clock (K, K) Rise (BWS ₀ , BWS ₁ , BWS ₂ , BWS ₃)	0.28		0.28		0.28		0.28		ns	2		
tDVKH	Data Input Setup to Clock (K/K) Rise	0.28		0.28		0.28		0.28		ns	2		
Hold Times													
tKHAX	Address Hold after K Clock Rise	0.40		0.40		0.40		0.40		ns			
tKHIX	Control Hold after K Clock Rise	0.40		0.40		0.40		0.40		ns			
tKHIX	Double Data Rate Control Hold after Clock (K/K) Rise (BWS ₀ , BWS ₁ , BWS ₂ , BWS ₃)	0.28		0.28		0.28		0.28		ns			
tKHDX	Data Input Hold after Clock (K/K) Rise	0.28		0.28		0.28		0.28		ns			
Output Times													
tCHQV	K/K Clock Rise to Data Valid		0.45		0.45		0.45		0.45	ns	1		
tCHQX	Data Output Hold after Output K/K Clock Rise (Active to Active)	-0.45		-0.45		-0.45		-0.45		ns	1		
tCHCQV	K/K Clock Rise to Echo Clock Valid		0.45		0.45		0.45		0.45	ns			
tCHCQX	Echo Clock Hold after K/K Clock Rise	-0.45		-0.45		-0.45		-0.45		ns			
tCQHQV	Echo Clock High to Data Valid		0.20		0.20		0.20		0.20	ns	1		
tCQHQX	Echo Clock High to Data Invalid	-0.20		-0.20		-0.20		-0.20		ns	1		
tCHQZ	Clock (K/K) Rise to High-Z (Active to High-Z)		0.45		0.45		0.45		0.45	ns	1		
tCHQX1	Clock (K/K) Rise to Low-Z	-0.45		-0.45		-0.45		-0.45		ns	1		
DLL Timing													
tKC Var	Clock Phase Jitter		0.20		0.20		0.20		0.20	ns			
tKC lock	DLL Lock Time (K)	2048		2048		2048				cycles			
tDoffLowToReset	Doff Low period to DLL Reset	5		5		5				ns			

Notes:

1. See AC Test Loading on page 14.
2. During normal operation, VIH, VIL, TRISE, and TFALL of inputs must be within 20% of VIH, VIL, TRISE, and TFALL of clock.

[illegible]

IEEE 1149.1 TAP and Boundary Scan

The SRAM provides a limited set of JTAG functions to test the interconnection between SRAM I/Os and printed circuit board traces or other components. There is no multiplexer in the path from I/O pins to the RAM core.

In conformance with IEEE Standard 1149.1, the SRAM contains a TAP controller, instruction register, boundary scan register, bypass register, and ID register.

The TAP controller has a standard 16-state machine that resets internally on power-up. Therefore, a TRST signal is not required.

Signal List

- TCK: test clock
- TMS: test mode select
- TDI: test data-in
- TDO: test data-out

JTAG DC Operating Characteristics ($T_A = 0$ to $+70^\circ\text{C}$)

Operates with JEDEC Standard 8-5 (1.8V) logic signal levels

Parameter	Symbol	Minimum	Typical	Maximum	Units	Notes
JTAG input high voltage	V_{IH1}	1.3	—	$V_{DD}+0.3$	V	1
JTAG input low voltage	V_{IL1}	-0.3	—	0.5	V	1
JTAG output high level	V_{OH1}	$V_{DD}-0.4$	—	V_{DD}	V	1, 2
JTAG output low level	V_{OL1}	V_{SS}	—	0.4	V	1, 3
1. All JTAG inputs and outputs are LVTTTL-compatible. 2. $I_{OH1} \geq -2\text{mA}$ 3. $I_{OL1} \geq +2\text{mA}$.						

JTAG AC Test Conditions ($T_A = 0$ to $+70^\circ\text{C}$, $V_{DD} = 1.8\text{V} -5\%, +5\%$)

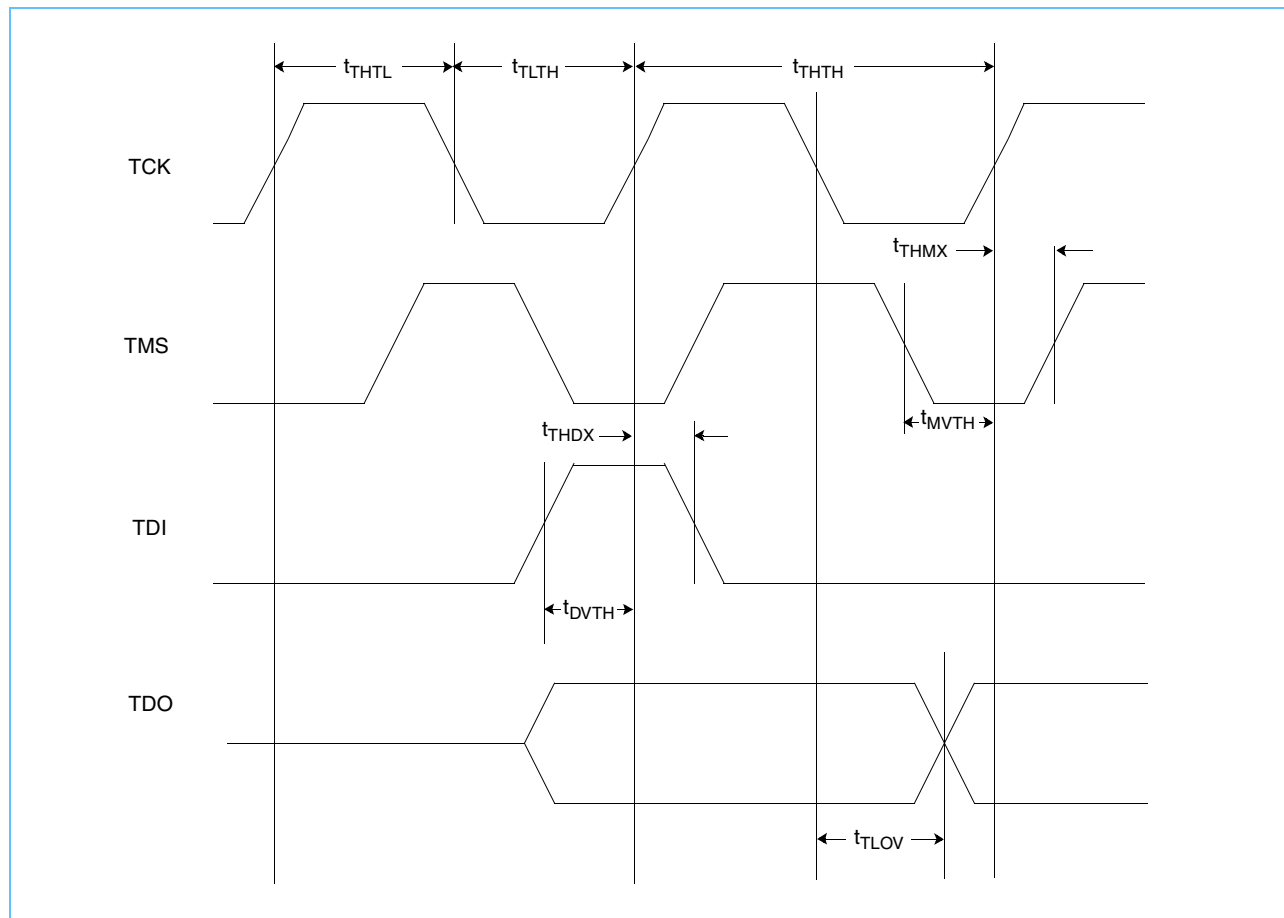
Parameter	Symbol	Conditions	Units
Input pulse high level	V_{IH1}	1.3	V
Input pulse low level	V_{IL1}	0.5	V
Input rise time	T_{R1}	1.0	ns
Input fall time	T_{F1}	1.0	ns
Input and output timing reference level		0.9	V

JTAG AC Characteristics ($T_A = 0$ to $+70^\circ\text{C}$, $V_{DD} = 1.8\text{V} -5\%, +5\%$)

Parameter	Symbol	Minimum	Maximum	Units	Notes
TCK cycle time	t_{THTH}	20	—	ns	
TCK high pulse width	t_{HTHL}	7	—	ns	
TCK low pulse width	t_{LTH}	7	—	ns	
TMS setup	t_{MVTH}	4	—	ns	
TMS hold	t_{THMX}	4	—	ns	
TDI setup	t_{DVTH}	4	—	ns	
TDI hold	t_{THDX}	4	—	ns	
TCK low to valid data	t_{TLOV}	—	7	ns	1

1. See AC Test Loading on page 14.

JTAG Timing Diagram



72 Mb (2M x 36 & 4M x 18) DDR-IIP (Burst of 2) CIO Synchronous SRAMs

Scan Register Definition

Register Name	Bit Size x18 or x36
Instruction	3
Bypass	1
ID	32
Boundary Scan	109

ID Register Definition

Part	Field Bit Number and Description			
	Revision Number (31:29)	Part Configuration (28:12)	JEDEC Code (11:1)	Start Bit (0)
4M x 18	000	00def0wx0t0q0b0s0	000 101 001 00	1
2M x 36	000	00def0wx0t0q0b0s0	000 101 001 00	1

Part Configuration Definition:

def = 011 for 72Mb
wx = 11 for x36, 10 for x18
t = 1 for DLL, 0 for non-DLL
q = 1 for QUADB2, 0 for DDR-II, DDR-IIP
b = 1 for burst of 4, 0 for burst of 2
s = 1 for separate I/O, 0 for common I/O

Instruction Set

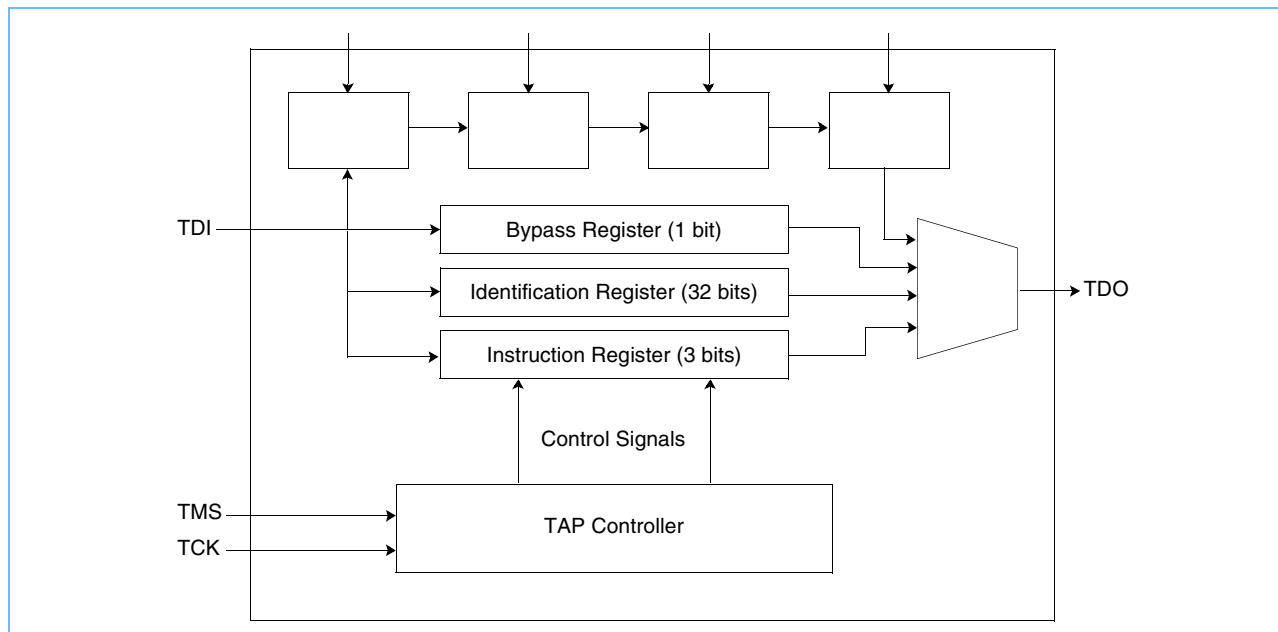
Code	Instruction	TDO Output	Notes
000	EXTEST	Boundary Scan Register	2,6
001	IDCODE	32-bit Identification Register	
010	SAMPLE-Z	Boundary Scan Register	1, 2
011	PRIVATE	Do not use	5
100	SAMPLE	Boundary Scan Register	4
101	PRIVATE	Do not use	5
110	PRIVATE	Do not use	5
111	BYPASS	Bypass Register	3

1. Places Qs in high-Z in order to sample all input data, regardless of other SRAM inputs.
2. TDI is sampled as an input to the first ID register to allow for the serial shift of the external TDI data.
3. BYPASS register is initiated to V_{SS} when BYPASS instruction is invoked. The BYPASS register also holds the last serially loaded TDI when exiting the shift-DR state.
4. SAMPLE instruction does not place DQs in high-Z.
5. This instruction is reserved. Invoking this instruction will cause improper SRAM functionality.
6. This EXTEST is not IEEE 1149.1-compliant. By default, it places Q in high-Z. If the internal register on the scan chain is set high, Q will be updated with information loaded via a previous SAMPLE instruction. The actual transfer occurs during the update IR state after EXTEST is loaded. The value of the internal register can be changed during SAMPLE and EXTEST only.

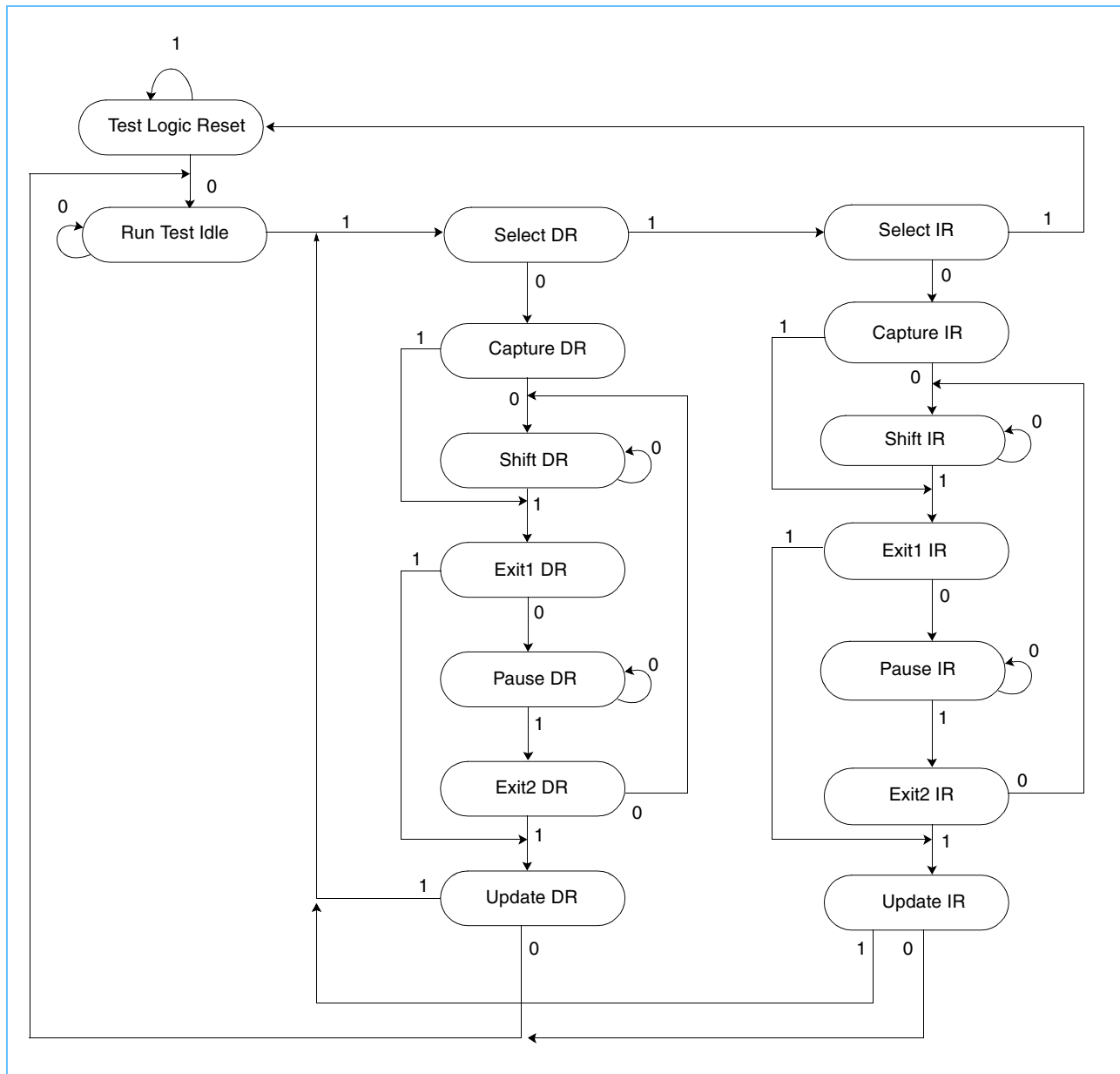
List of IEEE 1149.1 Standard Violations

- 7.2.1.b, e
- 7.7.1.a-f
- 10.1.1.b, e
- 10.7.1.a-d
- 6.1.1.d

JTAG Block Diagram



TAP Controller State Machine



72 Mb (2M x 36 & 4M x 18) DDR-IIP (Burst of 2) CIO Synchronous SRAMs



Boundary Scan Exit Order The same length is used for x18 and x36 I/O configuration.

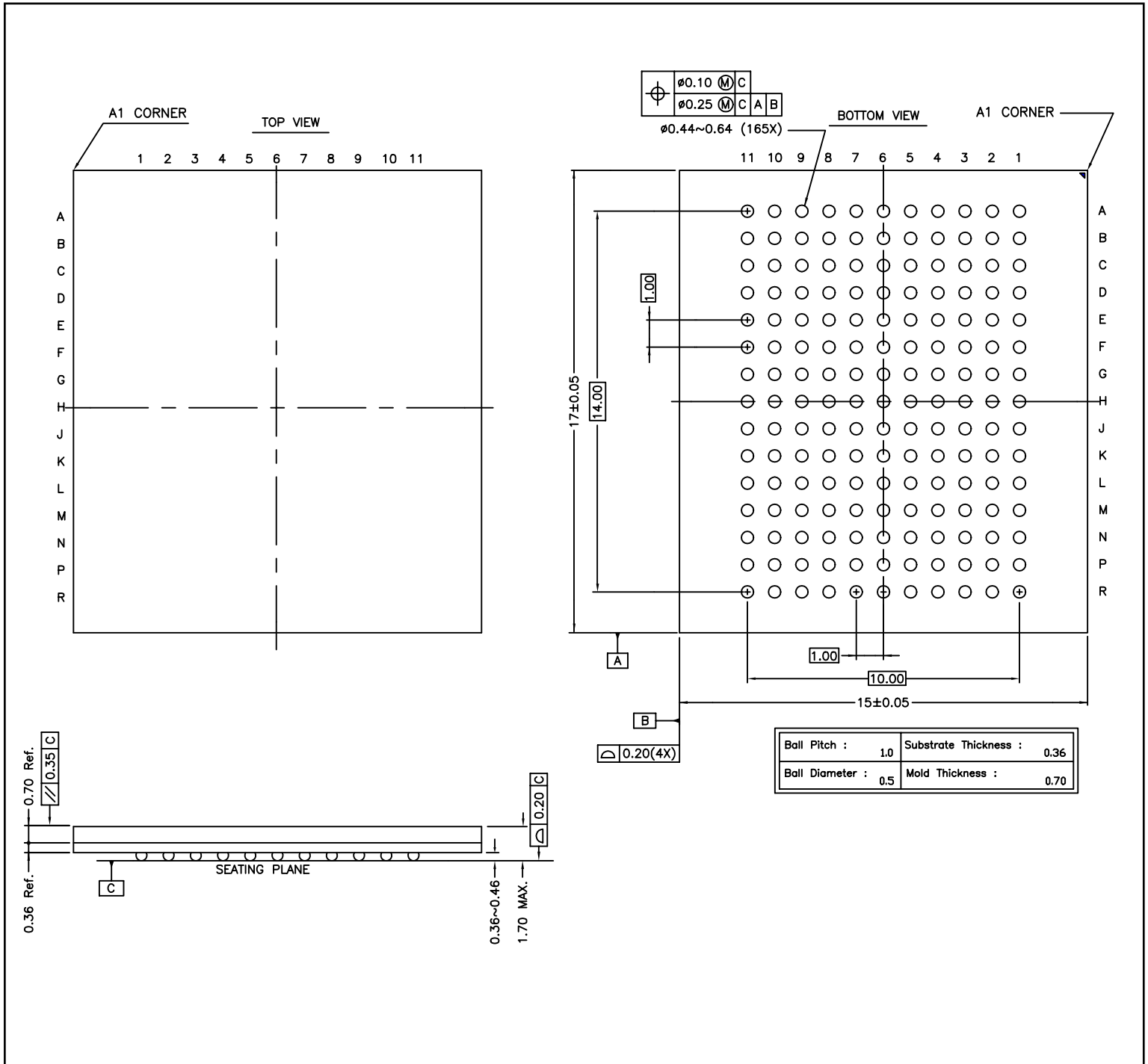
Order	Pin ID	Order	Pin ID	Order	Pin ID
1	6R	37	10D	73	2C
2	6P	37	9E	74	3E
3	6N	39	10C	75	2D
4	7P	40	11D	76	2E
5	7N	41	9C	77	1E
6	7R	42	9D	78	2F
7	8R	43	11B	79	3F
8	8P	44	11C	80	1G
9	9R	45	9B	81	1F
10	11P	46	10B	82	3G
11	10P	47	11A	83	2G
12	10N	48	10A	84	1H
13	9P	49	9A	85	1J
14	10M	50	8B	86	2J
15	11N	51	7C	87	3K
16	9M	52	6C	88	3J
17	9N	53	8A	89	2K
18	11L	54	7A	90	1K
19	11M	55	7B	91	2L
20	9L	56	6B	92	3L
21	10L	57	6A	93	1M
22	11K	58	5B	94	1L
23	10K	59	5A	95	3N
24	9J	60	4A	96	3M
25	9K	61	5C	97	1N
26	10J	62	4B	98	2M
27	11J	63	3A	99	3P
28	11H	64	2A	100	2N
29	10G	65	1A	101	2P
30	9G	66	2B	102	1P
31	11F	67	3B	103	3R
32	11G	68	1C	104	4R
33	9F	69	1B	105	4P
34	10F	70	3D	106	5P
35	11E	71	3C	107	5N
36	10E	72	1D	108	5R
				109	Internal

Notes:

- 1) NC pins as defined on *FBGA pinouts* on page 2 are read as "don't cares".
- 2) State of Internal pin (#109) is loaded via JTAG

72 Mb (2M x 36 & 4M x 18) DDR-IIP (Burst of 2) CIO Synchronous SRAMs

11 x 15 FBGA Dimensions



**72 Mb (2M x 36 & 4M x 18)
DDR-IIP (Burst of 2) CIO Synchronous SRAMs**



ORDERING INFORMATION

Commercial Range: 0°C to +70°C

Speed	Order Part No.	Organization	Package
400 MHz	IS61DDPB22M36-400M3	2Mx36	165 BGA
	IS61DDPB22M36-400M3L	2Mx36	165 BGA, Lead-free
	IS61DDPB24M18-400M3	4Mx18	165 BGA
	IS61DDPB24M18-400M3L	4Mx18	165 BGA, Lead-free
375 MHz	IS61DDPB22M36-375M3	2Mx36	165 BGA
	IS61DDPB22M36-375M3L	2Mx36	165 BGA, Lead-free
	IS61DDPB24M18-375M3	4Mx18	165 BGA
	IS61DDPB24M18-375M3L	4Mx18	165 BGA, Lead-free