IS93C56

ISSI

2048-BIT SERIAL ELECTRICALLY ERASABLE PROM WITH 2V READ CAPABILITY

PRELIMINARY

August 1990

FEATURES

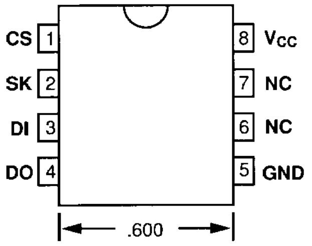
- **State-of-the-Art Architecture**
  - Non-volatile data storage
  - Single supply - 5V operation
  - Full TTL compatible inputs and outputs
  - 1MHz operation
- **Hardware and Software Write Protection**
  - Defaults to write-disabled state at power up
  - Software instructions for write-enable/disable
- **Low Power Consumption**
  - 1mA active (typical)
  - 1µA standby (typical)
- **Low Voltage Read Operations**
  - Reliable read operations down to 2.0 volts
- **Advanced Low Voltage CMOS E^{2}PROM Technology**
- **Versatile, easy-to-use Interface**
  - Self-timed programming cycle
  - Automatic erase-before-write
  - Programming Status Indicator
  - Word and chip erasable
  - Stop SK anytime for power savings
- **Durable and Reliable**
  - 10-year data retention after 10K write cycles
  - Minimum of 10,000 write cycles per word
  - Unlimited read cycles
  - ESD protection

OVERVIEW

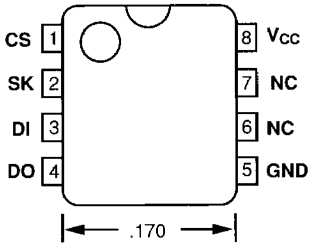
The IS93C56 is a low cost 2048-bit, non-volatile, serial E^{2}PROM. It is fabricated using ISSI's advanced CMOS E^{2}PROM technology. The IS93C56 provides efficient non-volatile read/write memory arranged as 128 registers of 16 bits each. Seven 11-bit instructions control the operation of the device, which includes read, write, and mode enable functions. The data out pin (DO) indicates the status of the device during in the self-timed non-volatile programming cycle.

PIN CONFIGURATIONS

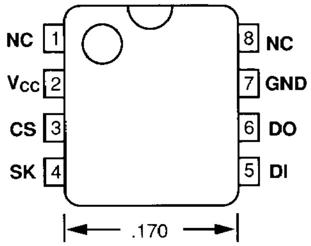
Plastic Dual-in-line "SP" Package



EIAJ Small Outline "JR" Package



EIAJ Small Outline "SJ" Package



PIN NAMES

CS	Chip Select
SK	Serial Data Clock
DI	Serial Data Input
DO	Serial Data Output
GND	Ground
Vcc	Power Supply
NC	Not Connected

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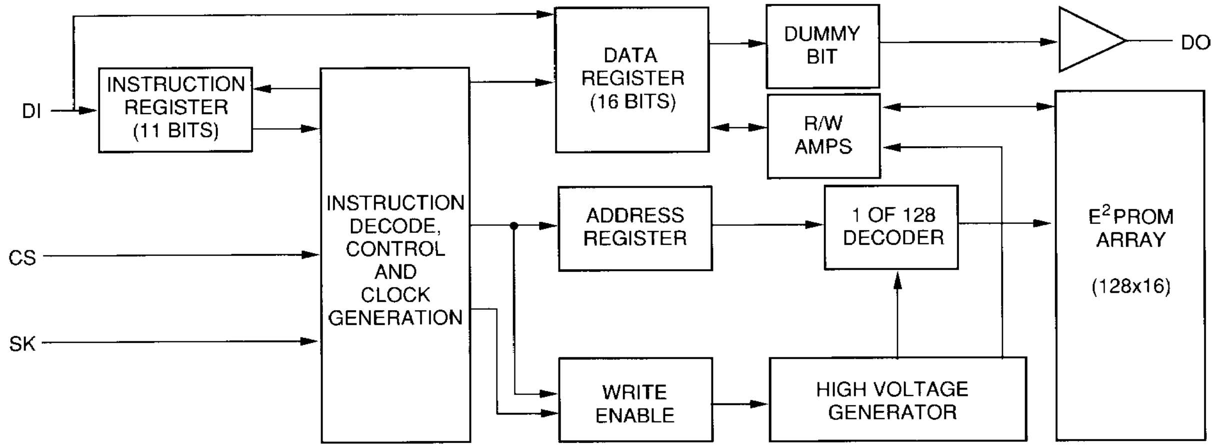
BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Temperature under bias: IS93C56............0°C to +70°C
IS93C56-I.....-40°C to +85°C
Storage Temperature...........................-65°C to +125°C
Voltage with Respect to Ground.................-0.3 to +6.5V

NOTE: These are STRESS ratings only. Appropriate conditions for operating these devices are given elsewhere in this specification. Stresses beyond those listed here may permanently damage the part. Prolonged exposure to maximum ratings may affect device reliability.

APPLICATIONS

The IS93C56 is ideal for high volume applications requiring low power and low density storage. This device uses a low cost, space saving 8-pin package. Candidate applications include robotics, alarm devices, electronic locks, meters and instrumentation settings.

ENDURANCE AND DATA RETENTION

The IS93C56 is designed for applications requiring up to 10,000 write cycles. It provides 10 years of secure data retention, without power after the execution of 10,000 write cycles.

DEVICE OPERATION

The IS93C56 is controlled by seven 11-bit instructions. Instructions are clocked in (serially) on the DI pin. Each instruction begins with a logical "1" (the start bit). This is followed by the opcode (2 bits), the address field (8 bits), and data, if appropriate. The clock signal (SK) may be halted at any time and the IS93C56 will remain in its last state. This allows full static flexability and maximum power conservation.

Read (READ)

The READ instruction is the only instruction that outputs serial data on the DO pin. After the read instruction and address have been decoded, data is transferred from the selected memory register into a 16-bit serial shift register. (Please note that one logical "0" bit precedes the actual 16-bit output data string.) The output on DO changes during the low-to-high transitions of SK. (See Figure 3.)

Low Voltage Read

The IS93C56 has been designed to ensure that data read operations are reliable in low voltage environments. The IS93C56 is guaranteed to provide accurate data during read operations with V_{CC} as low as 2.0V.

Write Enable (WEN)

The write enable (WEN) instruction must be executed before any device programming can be done. When V_{CC} is applied, this device powers up in the write disabled state. The device then remains in a write disabled state until a WEN instruction is executed. Thereafter the device remains enabled until a WDS instruction is executed or until V_{CC} is removed. (NOTE: Neither the WEN nor the WDS instruction has any effect on the READ instruction.) (See Figure 4.)

Write (WRITE)

The WRITE instruction includes 16 bits of data to be written into the specified register. After the last data bit has been applied to DI, and before the next rising edge of SK, CS must be brought LOW. The falling edge of CS initiates the self-timed programming cycle.

After a minimum wait of 250ns from the falling edge of CS (t_{CS}), if CS is brought HIGH, DO will indicate the READY/BUSY status of the chip: logical "0" means programming is still in progress; logical "1" means the selected register has been written, and the part is ready for another instruction. (See Figure 5.) (NOTE: The combination of CS HIGH, DI HIGH and the rising edge of the SK clock, resets the READY/BUSY flag. Therefore, it is important if you want to access the READY/BUSY flag , not to reset it through this combination of control signals.) Before a WRITE instruction can be executed, the device must be write enabled (see WEN).

Write All (WRALL)

The write all (WRALL) instruction programs all registers with the data pattern specified in the instruction. While the WRALL instruction is being loaded, the address field becomes a sequence of DON'T-CARE bits. (See Figure 6.) ERAL is required before WRAL operation.

As with the WRITE instruction, if CS is brought HIGH after a minimum wait of 250ns (t_{CS}), the DO pin indicates the READY/BUSY status of the chip. (See Figure 6.)

Write Disable (WDS)

The write disable (WDS) instruction disables all programming capabilities. This protects the entire part against accidental modification of data until a WEN instruction is executed. (When V_{CC} is applied, this part powers up in the write disabled state.) To protect data, a WDS instruction should be executed upon completion of each programming operation. (NOTE: Neither the WEN nor the WDS instruction has any effect on the READ instruction.) (See Figure 7.)

Erase Register

After the erase instruction is entered, CS must be brought low. The falling edge of CS initiates the self-timed internal programming cycle. Bringing CS HIGH after a minimum of t_{CS}, will cause DO to indicate the READ/BUSY status of the chip: a logical "0" indicates programming is still in progress; a logical "1" indicates the erase cycle is complete and the part is ready for another instruction. (See Figure 8.)

Erase All (ERAL)

Full chip erase is provided for ease of programming. Erasing the entire chip involves setting all bits in the entire memory array to a logical "1." (See Figure 9.)

INSTRUCTION SET

Instruction	Start Bit	OP Code	Address	Input Data
READ	1	10	X(A6-A0)	
WEN (Write Enable)	1	00	11XXXXXX	
WRITE	1	01	X(A6-A0)	D15-D0
WRALL (Write All Registers)	1	00	01XXXXXX	D15-D0
WDS (Write Disable)	1	00	00XXXXXX	
ERASE	1	11	X(A6-A0)	
ERAL (Erase All Registers)	1	00	10XXXXXX	

DC ELECTRICAL CHARACTERISTICS

T_A = 0°C to +70°C or -40°C to +85°C for IS93C56, V_{CC} = 5V ±10%

Symbol	Parameter	Conditions	IS93C56		IS93C56-I		Units
			Min	Max	Min	Max	
I_{CC1}	Operating Current CMOS Input Levels	CS = V_{IH}, SK = 1MHz		2		2	mA
I_{CC2}	Operating Current TTL Input Levels	CS = V_{IH}, SK = 1MHz		5		5	mA
I_{SB}	Standby Current	CS = DI = SK =0V		4		4	µA
I_{IL}	Input Leakage	V_{IN} = 0V to Vcc, CS, SK, DI	-1	1	-1	1	µA
I_{OL}	Output Leakage	V_{OUT} = 0V to Vcc, CS = 0V	-1	1	-1	1	µA
V_{IL}	Input Low Voltage		-0.1	0.8	-0.1	0.8	V
V_{IH}	Input High Voltage		2	Vcc	2	Vcc	V
V_{OL1}	Output Low Voltage	I_{OL} = 2.1mA TTL		0.4		0.4	V
V_{OH1}	Output High Voltage	I_{OH} = -400µA TTL	2.4		2.4		V
V_{OL2}	Output Low Voltage	I_{OL} = 10µA CMOS		0.2		0.2	V
V_{OH2}	Output High Voltage	I_{OH} = -10µA CMOS	Vcc-0.2		Vcc-0.2		V

AC ELECTRICAL CHARACTERISTICS

T_A = 0°C to +70°C or -40°C to +85°C for IS93C56, V_{CC} = 5V ±10%

Symbol	Parameter	Conditions	IS93C56		IS93C56-I		Units
			Min	Max	Min	Max	
f_{SK}	SK Clock Frequency		0	1	0	1	MHz
t_{SKH}	SK High Time		250		250		ns
t_{SKL}	SK Low Time		250		250		ns
t_{CS}	Minimum CS Low Time		250		250		ns
t_{CSS}	CS Setup Time	Relative to SK	50		50		ns
t_{DIS}	DI Setup Time	Relative to SK	100		100		ns
t_{CSH}	CS Hold Time	Relative to SK	0		0		ns
t_{DIH}	DI Hold Time	Relative to SK	100		100		ns
t_{PD1}	Output Delay to "1"	AC Test		500		500	ns
t_{PD0}	Output Delay to "0"	AC Test		500		500	ns
t_{SV}	CS to Status Valid	AC Test C_L = 100pF		500		500	ns
t_{DF}	CS to DO in 3-state	CS = V_{IL}		100		100	ns
t_{WP}	Write Cycle Time			10		10	ms

CAPACITANCE

$T_A = 25°C$, $f = 250KHz$

Symbol	Parameter	Max	Units
C_{OUT}	Output Capacitance	5	pF
C_{IN}	Input Capacitance	5	pF

FIGURE 1. AC TEST CONDITIONS

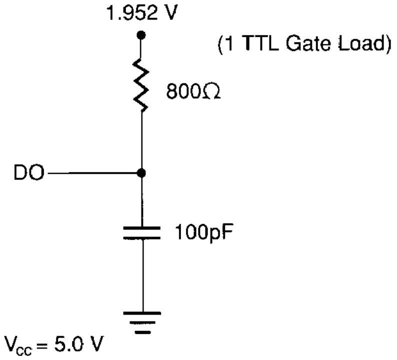


FIGURE 2. SYNCHRONOUS DATA TIMING

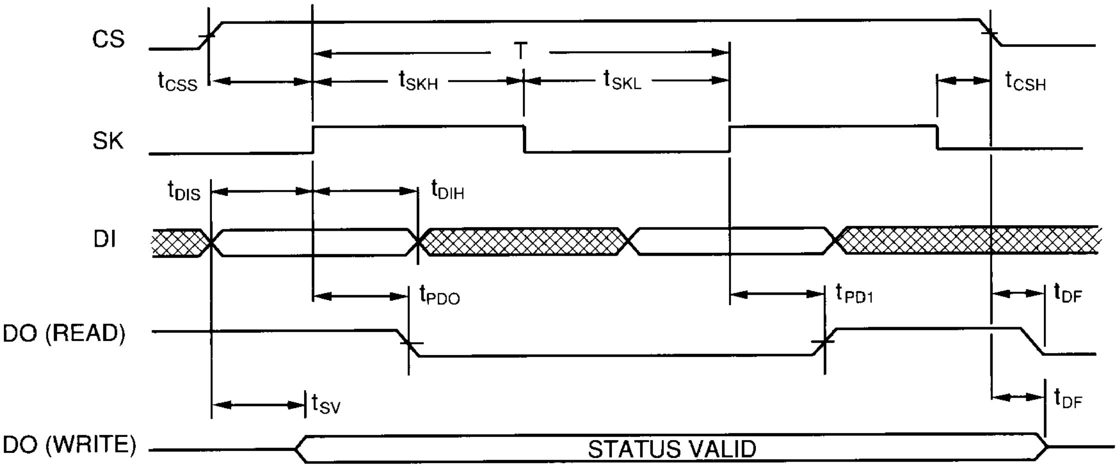


FIGURE 3. READ CYCLE TIMING

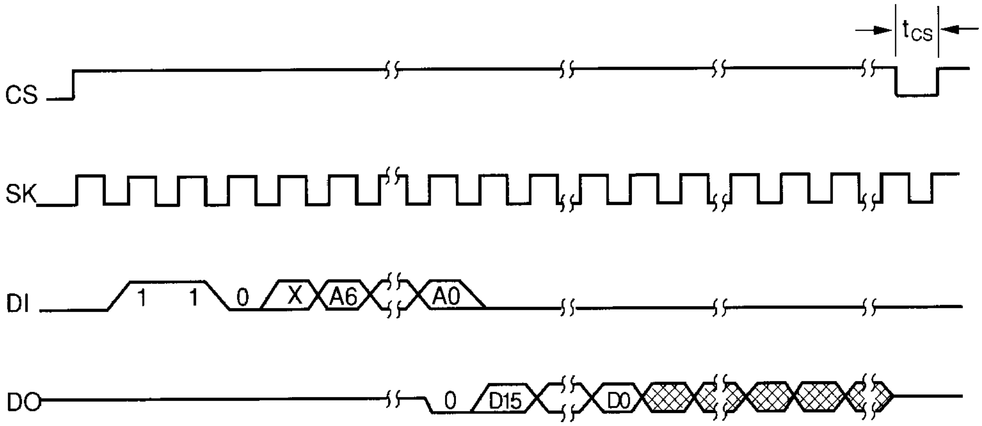
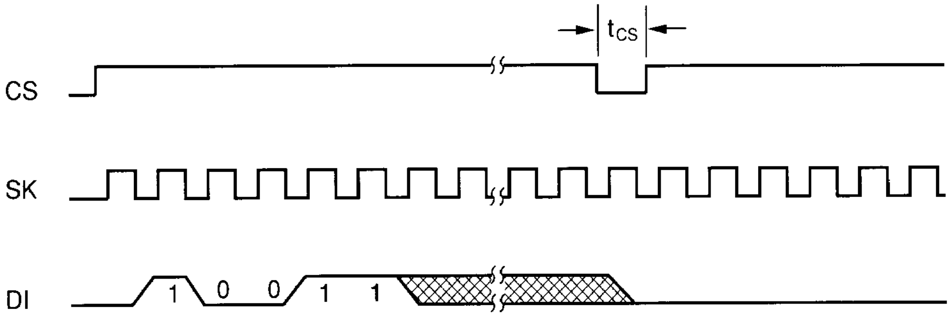


FIGURE 4. WRITE ENABLE (WEN) CYCLE TIMING



DO = 3-state

FIGURE 5. WRITE CYCLE TIMING

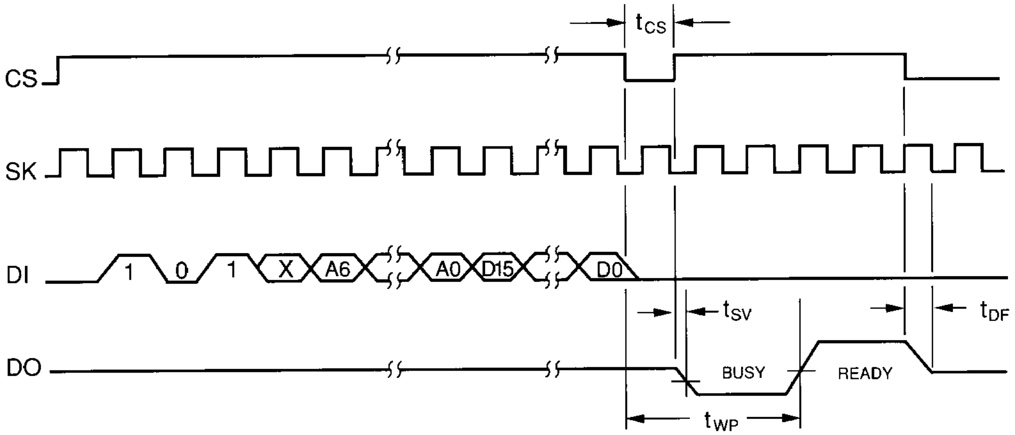


FIGURE 6. WRITE ALL (WRALL) CYCLE TIMING

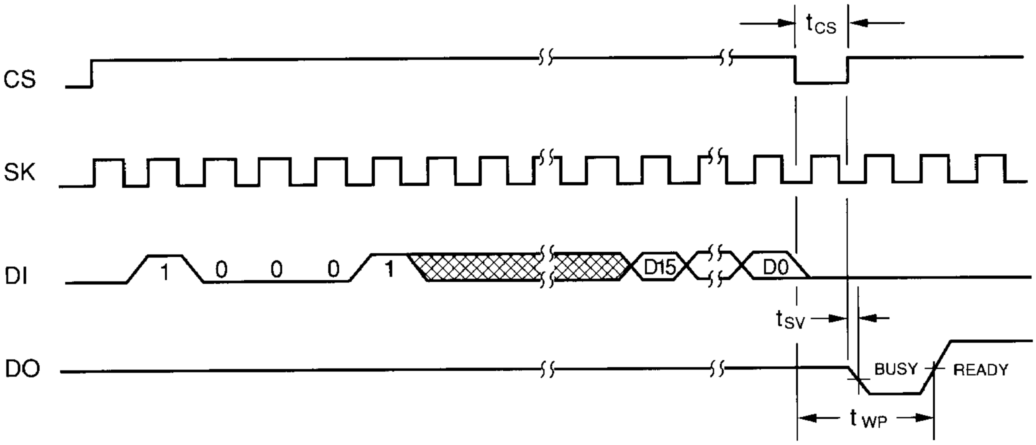


FIGURE 7. WRITE DISABLE (WDS) CYCLE TIMING

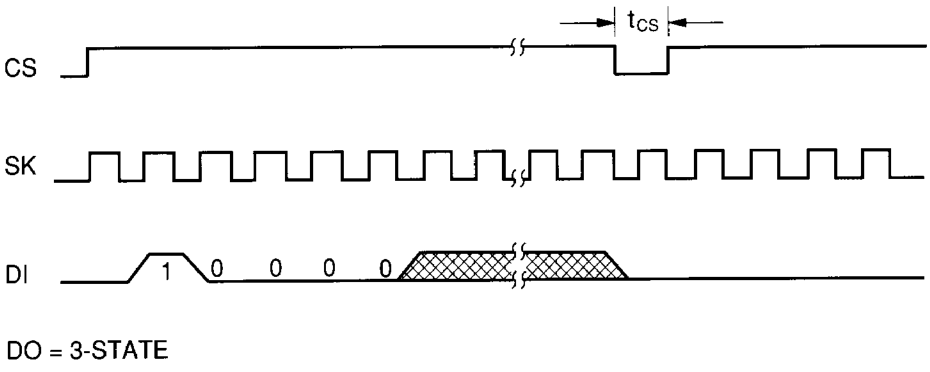


FIGURE 8. ERASE (REGISTER) CYCLE TIMING

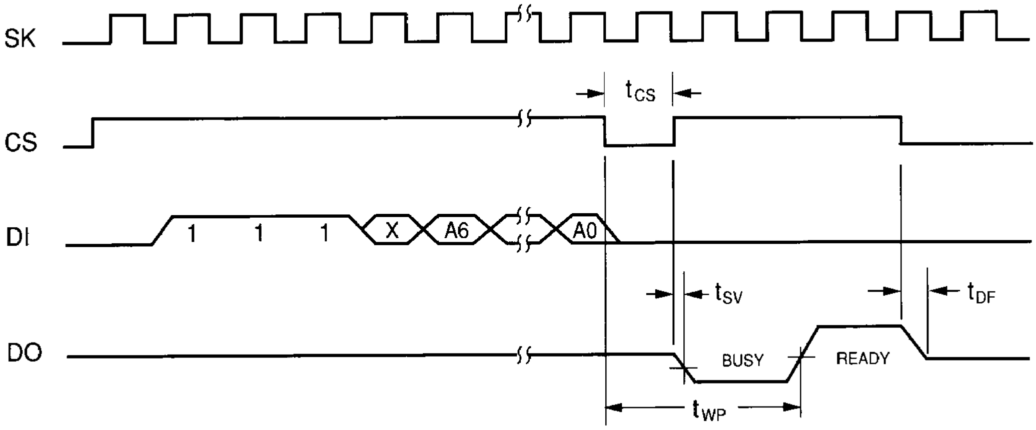
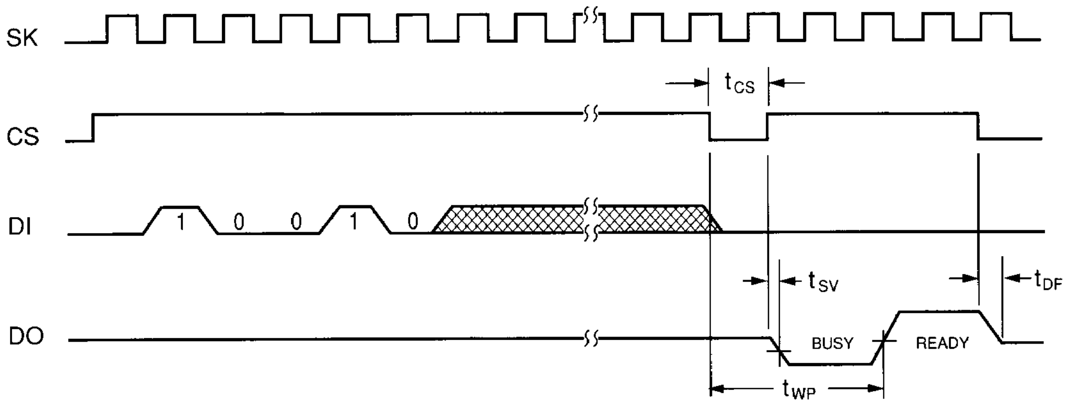
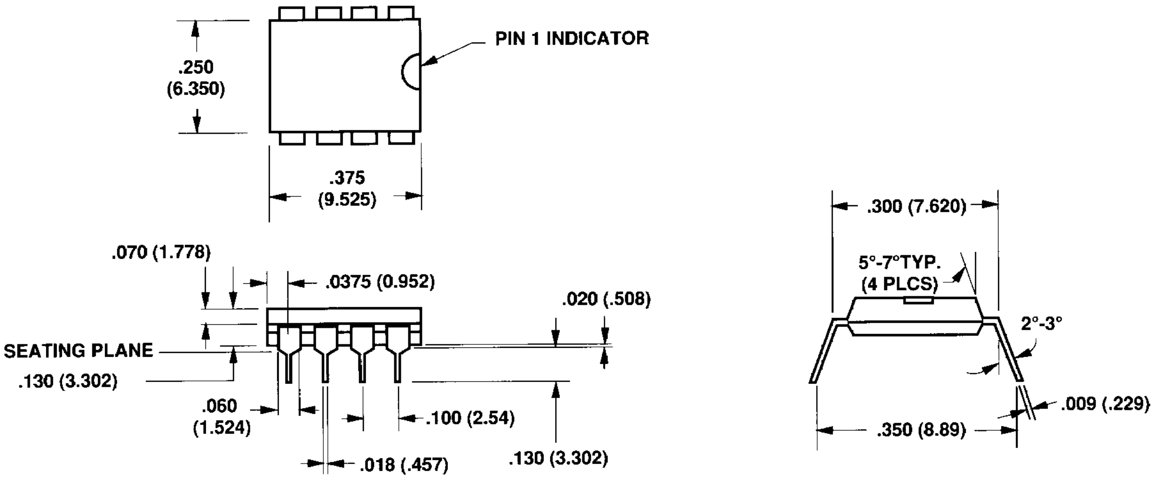


FIGURE 9. ERASE ALL (ERAL) CYCLE TIMING



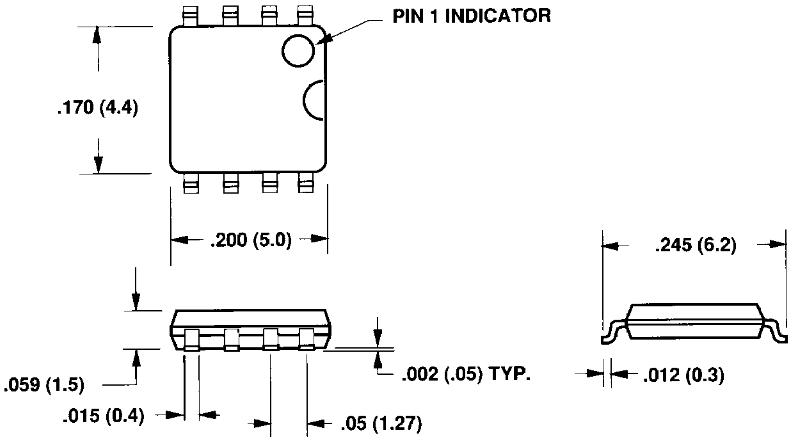
PACKAGE DIAGRAMS

Plastic Dual-in-line Package (PDIP)



EIAJ Small Outline Package

Package code "SJ" or "JR" specifies pinout*



* See cover page for pinout options

ORDERING INFORMATION

Standard Configurations

Prefix	Part Type	Package Type*	Temperature Range*
IS	93C56	SP, SJ, JR	Blank, I, M

*CONTACT ISSI FOR YOUR SPECIAL TEMPERATURE AND PACKAGING REQUIREMENTS

Part Numbers:

IS 93C56 SP I

Prefix

Temperature Range

No Designator — 0°C to +70°C
I — -40°C to +85°C
M — -55°C to +125°C

Package Type

SP — Plastic DIP
SJ — Small Outline (EIAJ STD)
JR — Small Outline (EIAJ STD)

Part Type
93C56

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