



# ISA04N60A

## N-Channel MOSFET

Lead Free Package and Finish

### Applications:

- Adaptor
- TV Main Power
- SMPS Power Supply
- LCD Panel Power

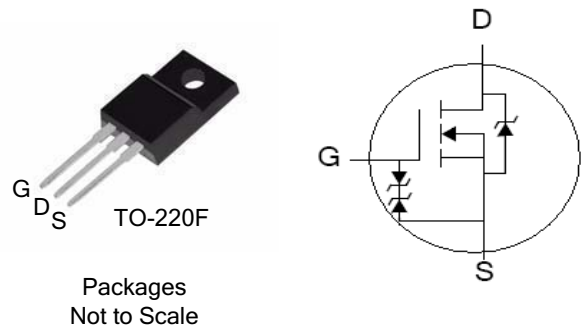
$V_{DSS}$	$R_{DS(ON)}$ (Max.)	$I_D$
600 V	2.3 $\Omega$	4 A

### Features:

- RoHS Compliant
- Low ON Resistance
- Low Gate Charge
- ESD improved Capability

### Ordering Information

PART NUMBER	PACKAGE	BRAND
ISA04N60A	TO-220F	ISA04N60A



### Absolute Maximum Ratings $T_C=25^\circ\text{C}$ unless otherwise specified

Symbol	Parameter	ISA04N60A	Units
$V_{DSS}$	Drain-to-Source Voltage (NOTE *1)	600	V
$I_D$	Continuous Drain Current	4*	A
$I_{D@ 100^\circ\text{C}}$	Continuous Drain Current	2.9	
$I_{DM}$	Pulsed Drain Current, $V_{GS}@ 10\text{V}$ (NOTE *2)	16	
$P_D$	Power Dissipation	30	W
	Derating Factor above $25^\circ\text{C}$	0.24	$\text{W}/^\circ\text{C}$
$V_{GS}$	Gate-to-Source Voltage	$\pm 20$	V
$E_{AS}$	Single Pulse Avalanche Energy $L=10\text{ mH}$	230	mJ
$I_{AS}$	Pulsed Avalanche Rating	Figure 16	A
$dv/dt$	Peak Diode Recovery $dv/dt$ (NOTE *3)	5.0	V/ns
$V_{ESD(G-S)}$	Gate to Source ESD (HBM-C=100pF, $R=1.5\text{K}\Omega$ )	3000	V
$T_L$ $T_{PKG}$	Maximum Temperature for Soldering Leads at 0.063 in (1.6 mm) from Case for 10 seconds	300	$^\circ\text{C}$
	Package Body for 10 seconds	260	
$T_J$ and $T_{STG}$	Operating Junction and Storage Temperature Range	-55 to 150	

\* Drain Current Limited by Maximum Junction Temperature

**Caution:** Stresses greater than those listed in the "Absolute Maximum Ratings" Table may cause permanent damage to the device.

### Thermal Resistance

Symbol	Parameter	ISA04N60A	Units	Test Conditions
$R_{\theta JC}$	Junction-to-Case	4.17	$^\circ\text{C}/\text{W}$	Drain lead soldered to water cooled heatsink, $P_D$ adjusted for a peak junction temperature of $+150^\circ\text{C}$ .
$R_{\theta JA}$	Junction-to-Ambient	62.5		1 cubic foot chamber, free air.

**OFF Characteristics**  $T_J=25^\circ\text{C}$  unless otherwise specified

Symbol	Parameter	Min.	Typ.	Max.	Units	Test Conditions
$BV_{DSS}$	Drain-to-Source Breakdown Voltage	600	--	--	V	$V_{GS}=0V, I_D=250\mu A$
$\Delta BV_{DSS}/\Delta T_J$	Breakdown Voltage Temperature Coefficient, Figure 11.	--	0.66	--	V/ $^\circ\text{C}$	Reference to $25^\circ\text{C}$ , $I_D=250\mu A$
$I_{DSS}$	Drain-to-Source Leakage Current	--	--	25	$\mu A$	$V_{DS}=600V, V_{GS}=0V$
		--	--	250		$V_{DS}=480V, V_{GS}=0V$ $T_J=125^\circ\text{C}$
$I_{GSS}$	Gate-to-Source Forward Leakage	--	--	10	$\mu A$	$V_{GS}=+20V$
	Gate-to-Source Reverse Leakage	--	--	-10		$V_{GS}=-20V$

**ON Characteristics**  $T_J=25^\circ\text{C}$  unless otherwise specified

Symbol	Parameter	Min.	Typ.	Max.	Units	Test Conditions
$R_{DS(ON)}$	Static Drain-to-Source On-Resistance Figure 9 and 10.	--	1.9	2.3	$\Omega$	$V_{GS}=10V, I_D=2.0A$ (NOTE *4)
$V_{GS(TH)}$	Gate Threshold Voltage, Figure 12.	2.0	--	4.0	V	$V_{DS}=V_{GS}, I_D=250\mu A$
gfs	Forward Transconductance	--	5.0	--	S	$V_{DS}=15V, I_D=2.0A$ (NOTE *4)

**Dynamic Characteristics** Essentially independent of operating temperature

Symbol	Parameter	Min.	Typ.	Max.	Units	Test Conditions
$C_{iss}$	Input Capacitance	--	530	--	$\mu F$	$V_{GS}=0V$ $V_{DS}=25V$ $f=1.0MHz$
$C_{oss}$	Output Capacitance	--	57	--		
$C_{rss}$	Reverse Transfer Capacitance	--	11	--		
$Q_g$	Total Gate Charge	--	15	--	nC	$V_{DD}=300V$ $I_D=4A, V_{GS}=10V$
$Q_{gs}$	Gate-to-Source Charge	--	3.0	--		
$Q_{gd}$	Gate-to-Drain ("Miller") Charge	--	7.0	--		

**Resistive Switching Characteristics** Essentially independent of operating temperature

Symbol	Parameter	Min.	Typ.	Max.	Units	Test Conditions
$t_{d(ON)}$	Turn-on Delay Time	--	9.0	--	ns	$V_{DD}=300V$ $I_D=4A$ $V_{GS}=10V$ $R_G=4.7\Omega$
$t_{rise}$	Rise Time	--	6.0	--		
$t_{d(OFF)}$	Turn-Off Delay Time	--	27	--		
$t_{fall}$	Fall Time	--	8.0	--		

**Source-Drain Diode Characteristics**  $T_C=25^\circ\text{C}$  unless otherwise specified

Symbol	Parameter	Min.	Typ.	Max.	Units	Test Conditions
$I_S$	Continuous Source Current (Body Diode)	--	--	4	A	Integral pn-diode in MOSFET
$I_{SM}$	Maximum Pulsed Current (Body Diode)	--	--	16	A	
$V_{SD}$	Diode Forward Voltage	--	--	1.5	V	$I_S=4\text{A}$ , $V_{GS}=0\text{V}$
$t_{rr}$	Reverse Recovery Time	--	450	--	ns	$V_{GS}=0\text{V}$
$Q_{rr}$	Reverse Recovery Charge	--	1.8	--	$\mu\text{C}$	$I_F=4\text{A}$ , $di/dt=100\text{A}/\mu\text{s}$

Notes:

---

\*1.  $T_J = +25^\circ\text{C}$  to  $+150^\circ\text{C}$ .

\*2. Repetitive rating; pulse width limited by maximum junction temperature.

\*3.  $I_{SD}=4\text{A}$ ,  $di/dt < 100\text{A}/\mu\text{s}$ ,  $V_{DD} < BV_{DSS}$ ,  $T_J=+150^\circ\text{C}$ .

\*4. Pulse width  $\leq 380\mu\text{s}$ ; duty cycle  $\leq 2\%$ .

### Characteristics Curve:

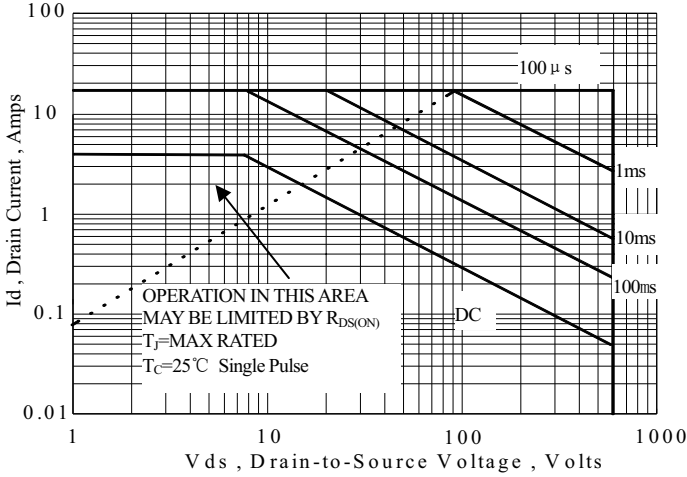


Figure 1 Maximum Forward Bias Safe Operating Area

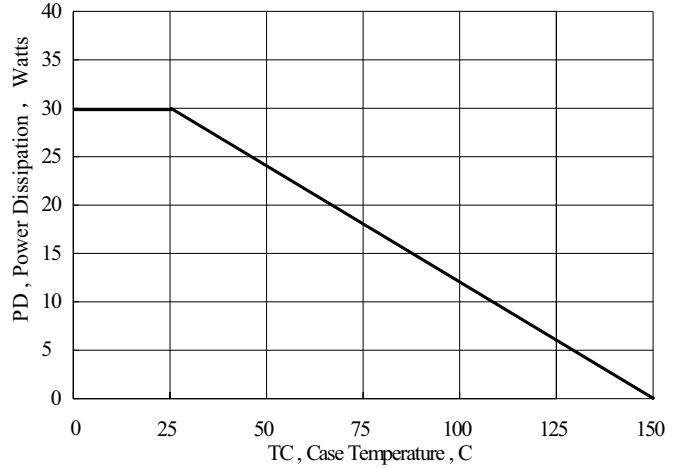


Figure 2 Maximum Power Dissipation vs Case Temperature

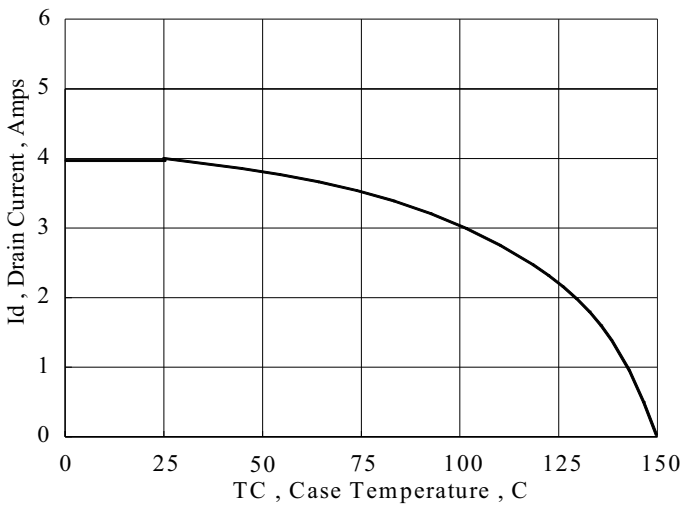


Figure 3 Maximum Continuous Drain Current vs Case Temperature

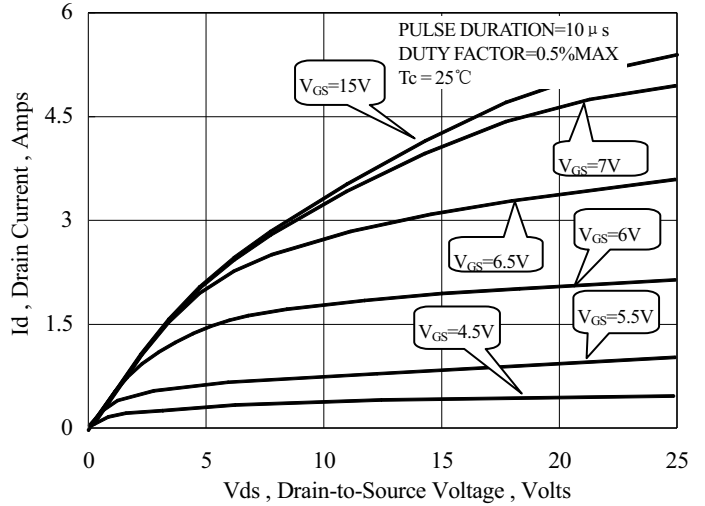


Figure 4 Typical Output Characteristics

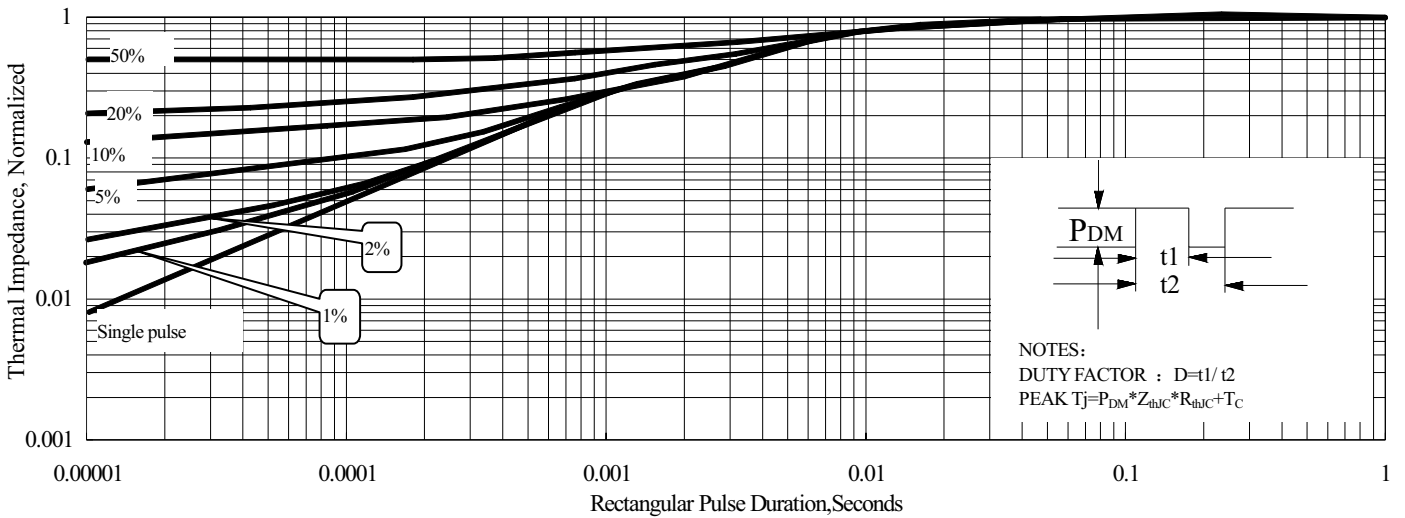


Figure 5 Maximum Effective Thermal Impedance , Junction to Case

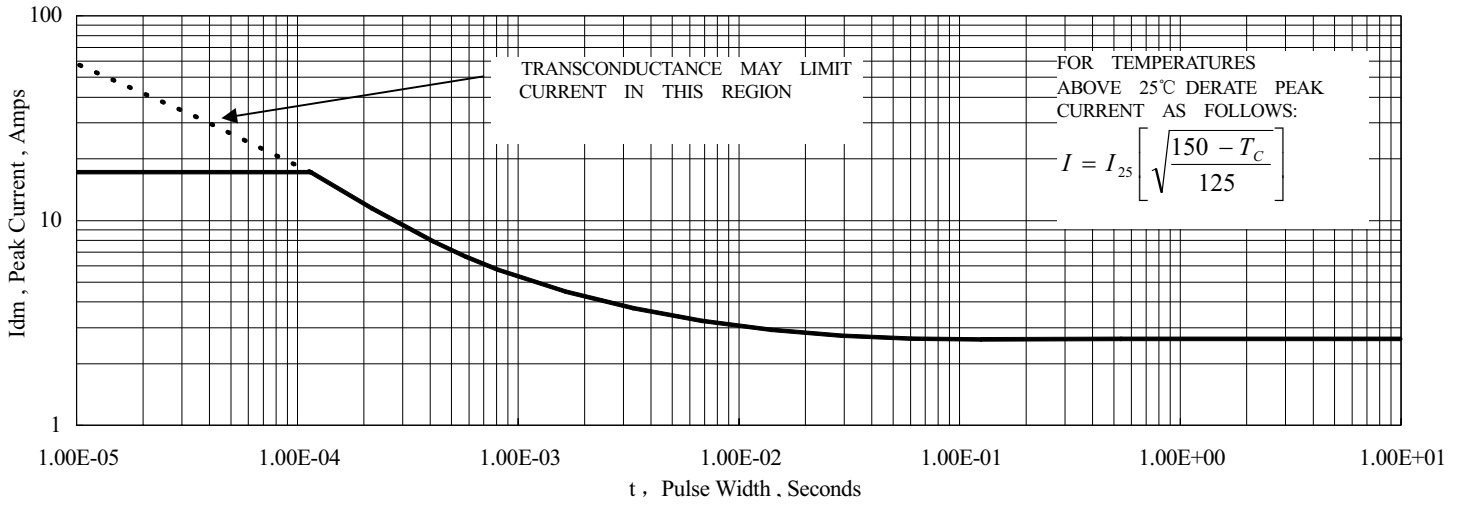


Figure 6 Maximum Peak Current Capability

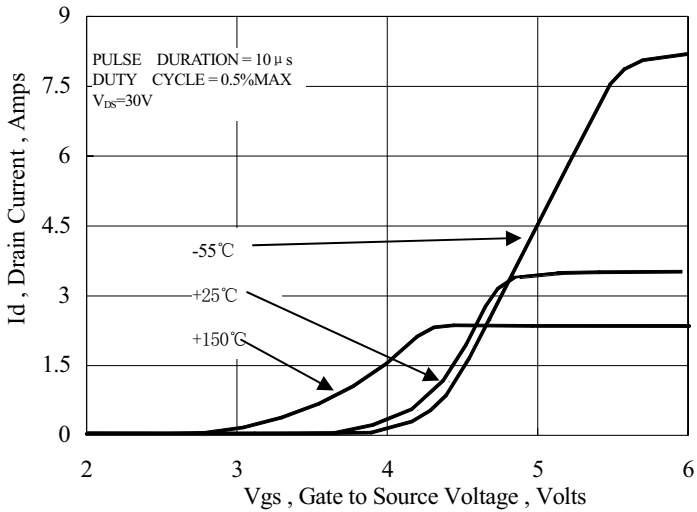


Figure 7 Typical Transfer Characteristics

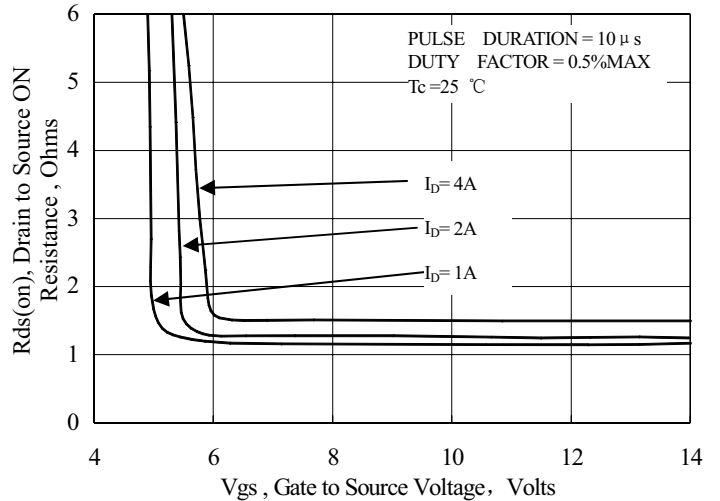


Figure 8 Typical Drain to Source ON Resistance vs Gate Voltage and Drain Current

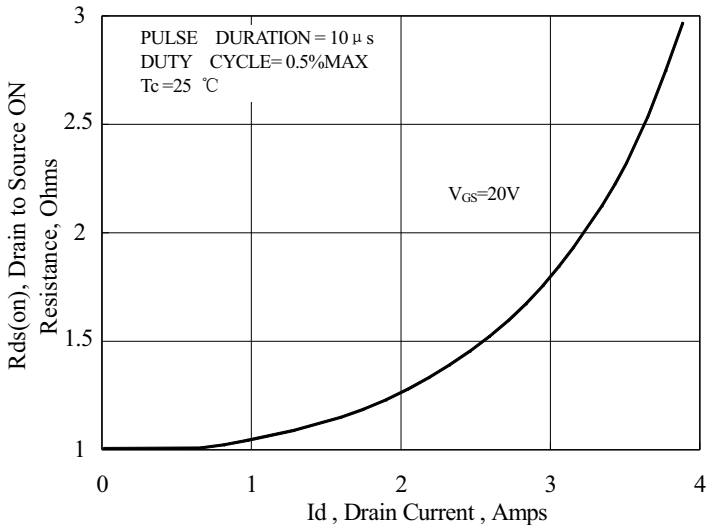


Figure 9 Typical Drain to Source ON Resistance vs Drain Current

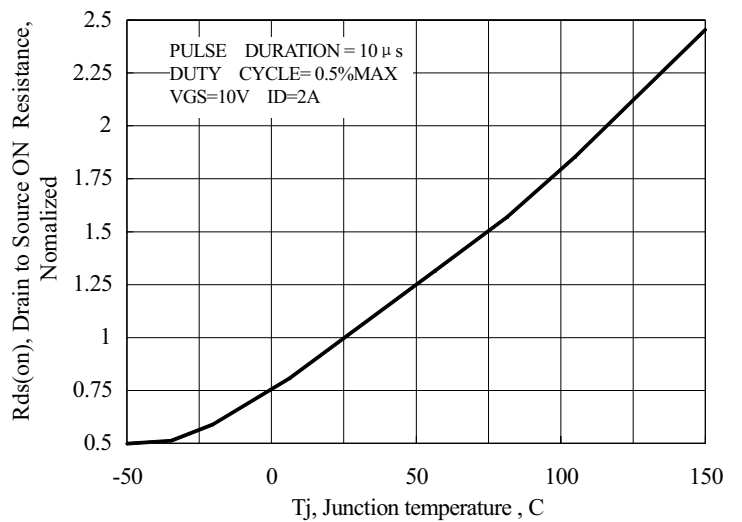


Figure 10 Typical Drain to Source on Resistance vs Junction Temperature

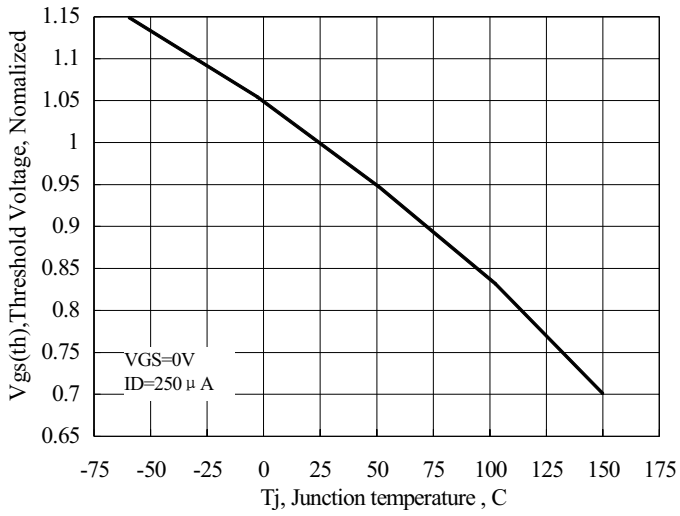


Figure 11 Typical Threshold Voltage vs Junction Temperature

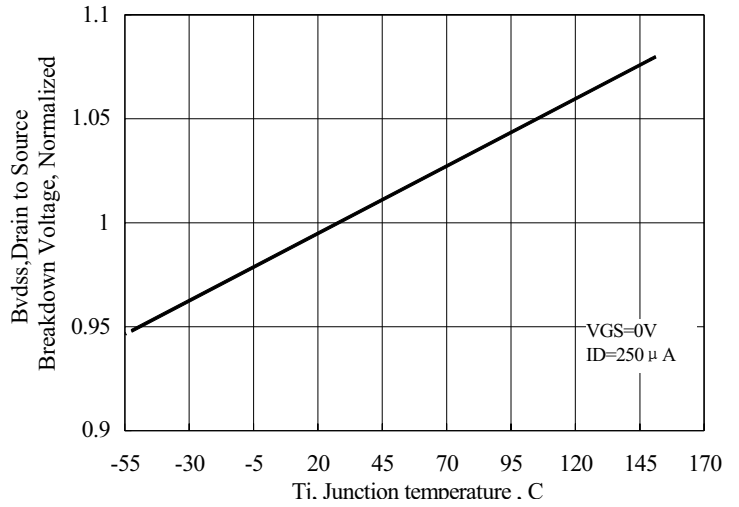


Figure 12 Typical Breakdown Voltage vs Junction Temperature

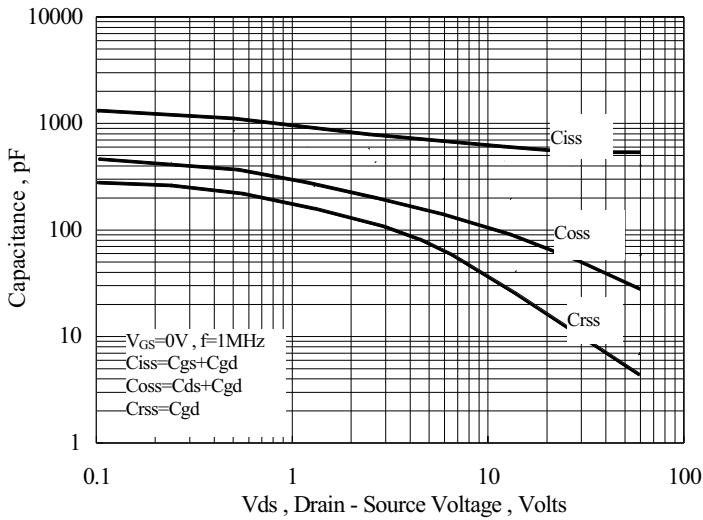


Figure 13 Typical Capacitance vs Drain to Source Voltage

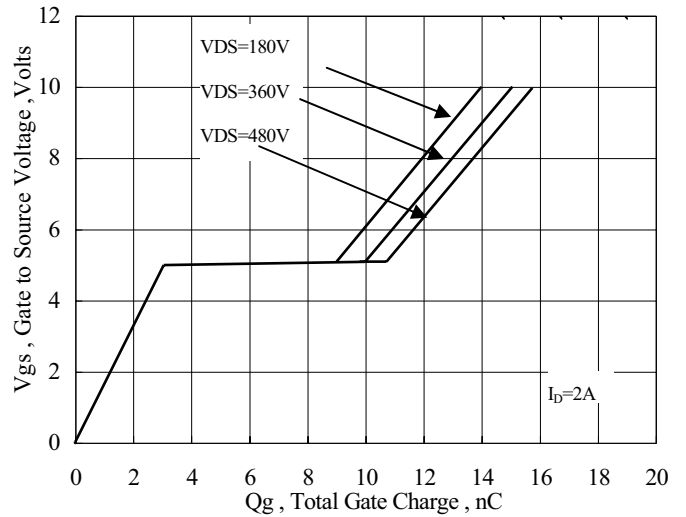


Figure 14 Typical Gate Charge vs Gate to Source Voltage

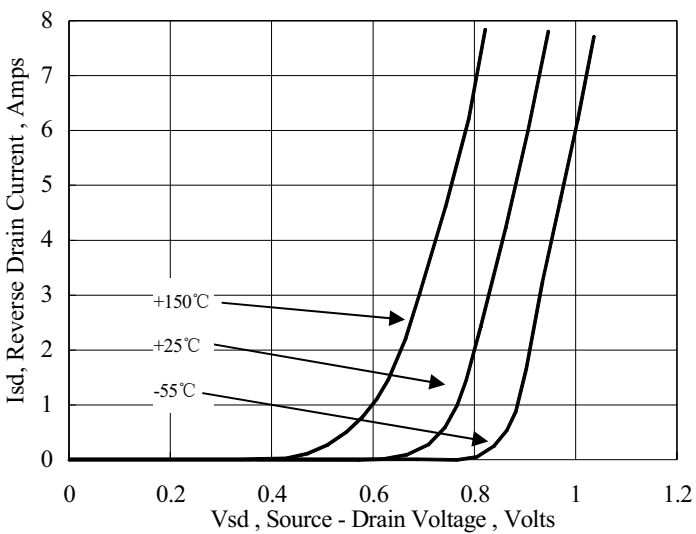


Figure 15 Typical Body Diode Transfer Characteristics

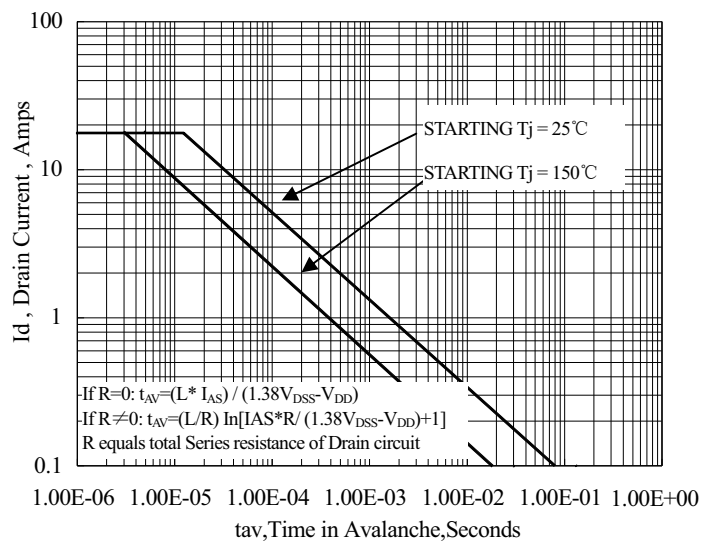


Figure 16 Unclamped Inductive Switching Capability

TEST CIRCUITS AND WAVEFORMS

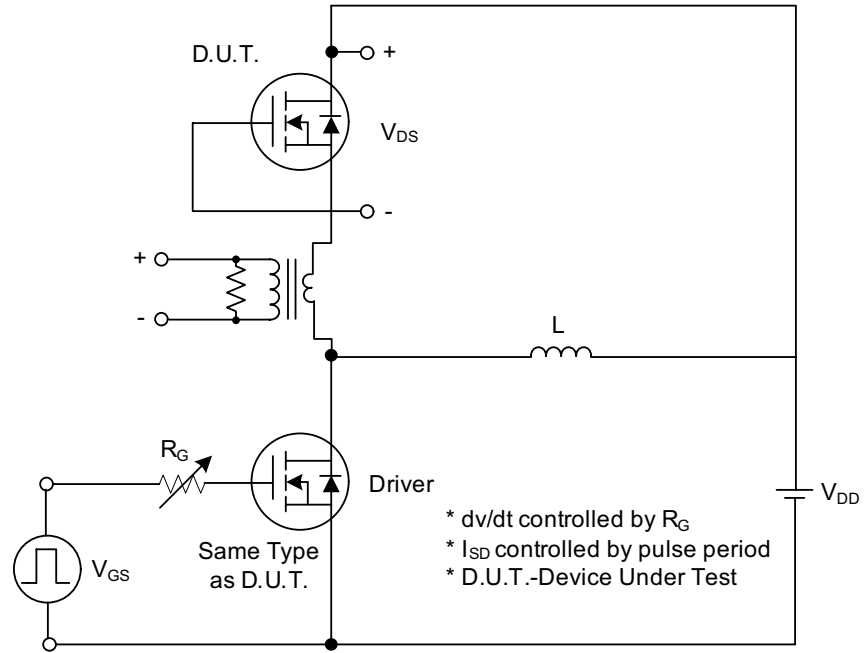


Fig. 1.1 Peak Diode Recovery  $dv/dt$  Test Circuit

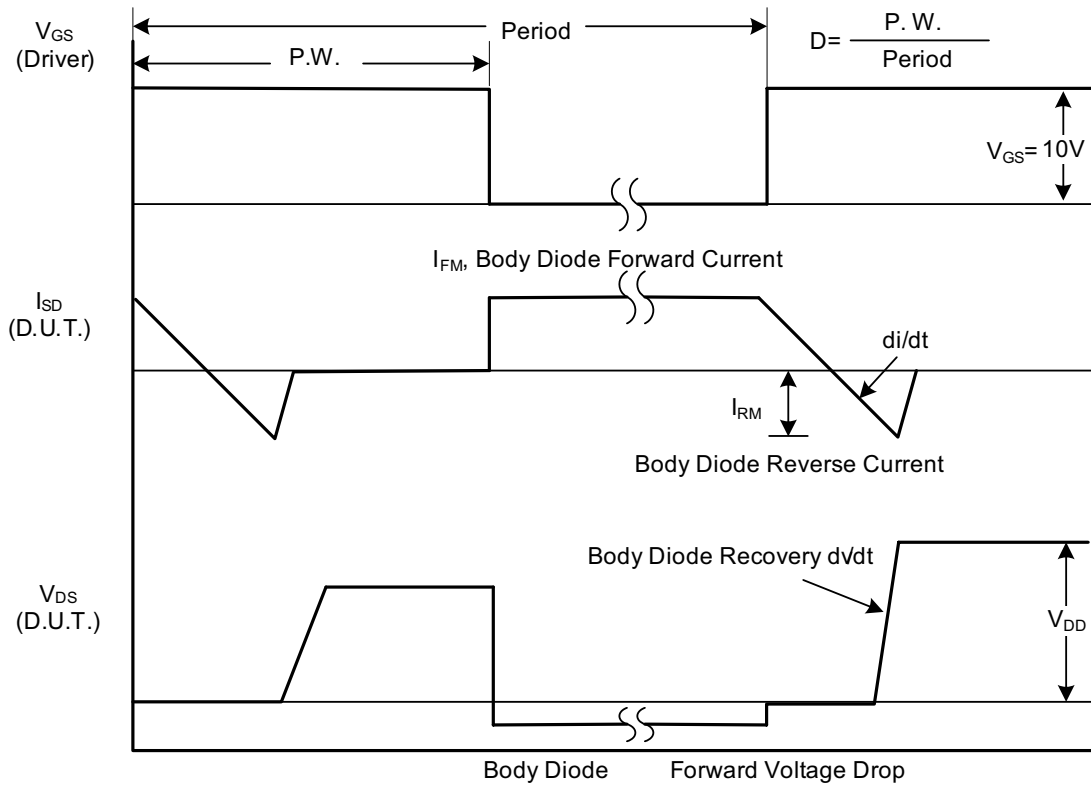


Fig. 1.2 Peak Diode Recovery  $dv/dt$  Waveforms

TEST CIRCUITS AND WAVEFORMS (Cont.)

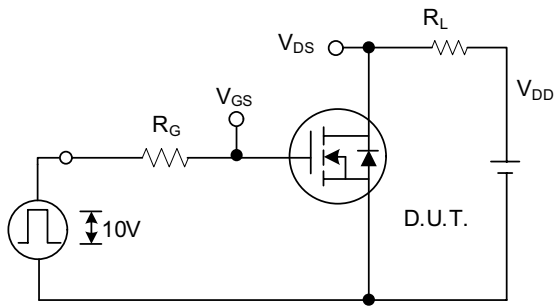


Fig. 2.1 Switching Test Circuit

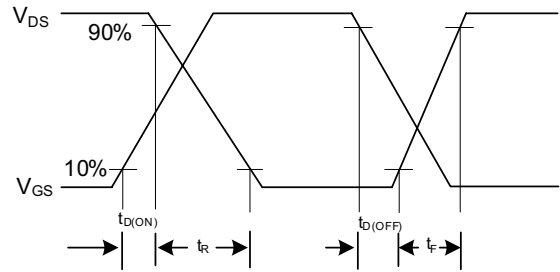


Fig. 2.2 Switching Waveforms

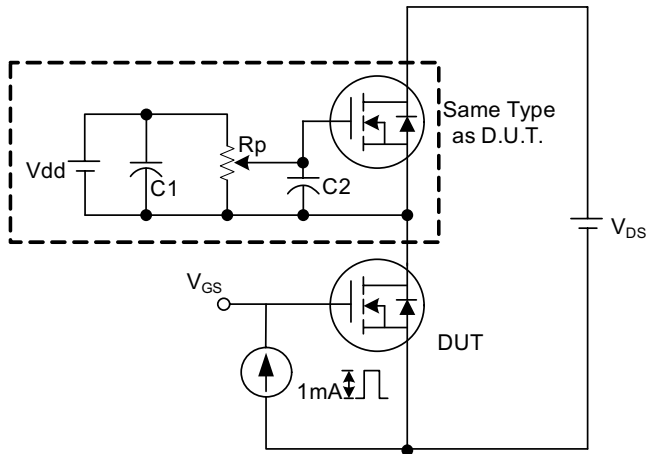


Fig. 3.1 Gate Charge Test Circuit

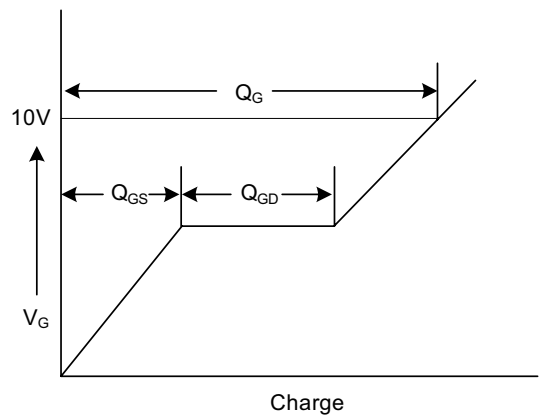


Fig. 3.2 Gate Charge Waveform

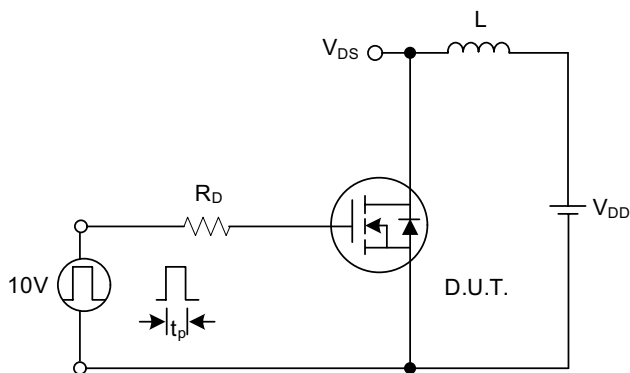


Fig. 4.1 Unclamped Inductive Switching Test Circuit

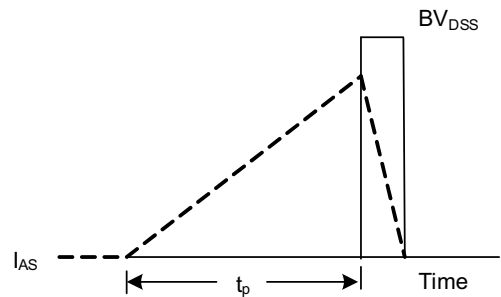


Fig. 4.2 Unclamped Inductive Switching Waveforms



---

## Disclaimers:

InPower Semiconductor Co., Ltd (IPS) reserves the right to make changes without notice in order to improve reliability, function or design and to discontinue any product or service without notice. Customers should obtain the latest relevant information before orders and should verify that such information is current and complete. All products are sold subject to IPS's terms and conditions supplied at the time of order acknowledgement.

InPower Semiconductor Co., Ltd warrants performance of its hardware products to the specifications at the time of sale, Testing, reliability and quality control are used to the extent IPS deems necessary to support this warrantee. Except where agreed upon by contractual agreement, testing of all parameters of each product is not necessarily performed.

InPower Semiconductor Co., Ltd does not assume any liability arising from the use of any product or circuit designs described herein. Customers are responsible for their products and applications using IPS's components. To minimize risk, customers must provide adequate design and operating safeguards.

InPower Semiconductor Co., Ltd does not warrant or convey any license either expressed or implied under its patent rights, nor the rights of others. Reproduction of information in IPS's data sheets or data books is permissible only if reproduction is without modification or alteration. Reproduction of this information with any alteration is an unfair and deceptive business practice. InPower Semiconductor Co., Ltd is not responsible or liable for such altered documentation.

Resale of IPS's products with statements different from or beyond the parameters stated by InPower Semiconductor Co., Ltd for that product or service voids all express or implied warranties for the associated IPS's product or service and is unfair and deceptive business practice. InPower Semiconductor Co., Ltd is not responsible or liable for any such statements.

---

## Life Support Policy:

InPower Semiconductor Co., Ltd's products are not authorized for use as critical components in life support devices or systems without the expressed written approval of InPower Semiconductor Co., Ltd.

As used herein:

1. Life support devices or systems are devices or systems which:
  - a. are intended for surgical implant into the human body,
  - b. support or sustain life,
  - c. whose failure to perform when properly used in accordance with instructions for used provided in the labeling, can be reasonably expected to result in significant injury to the user.
2. A critical component is any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.