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ISD1520

Single-Chip, Single-Message Voice Record/Playback Device
16- to 32-Second Durations

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ChipCorder®
TECHNOLOGY BY ISD

ISD1520

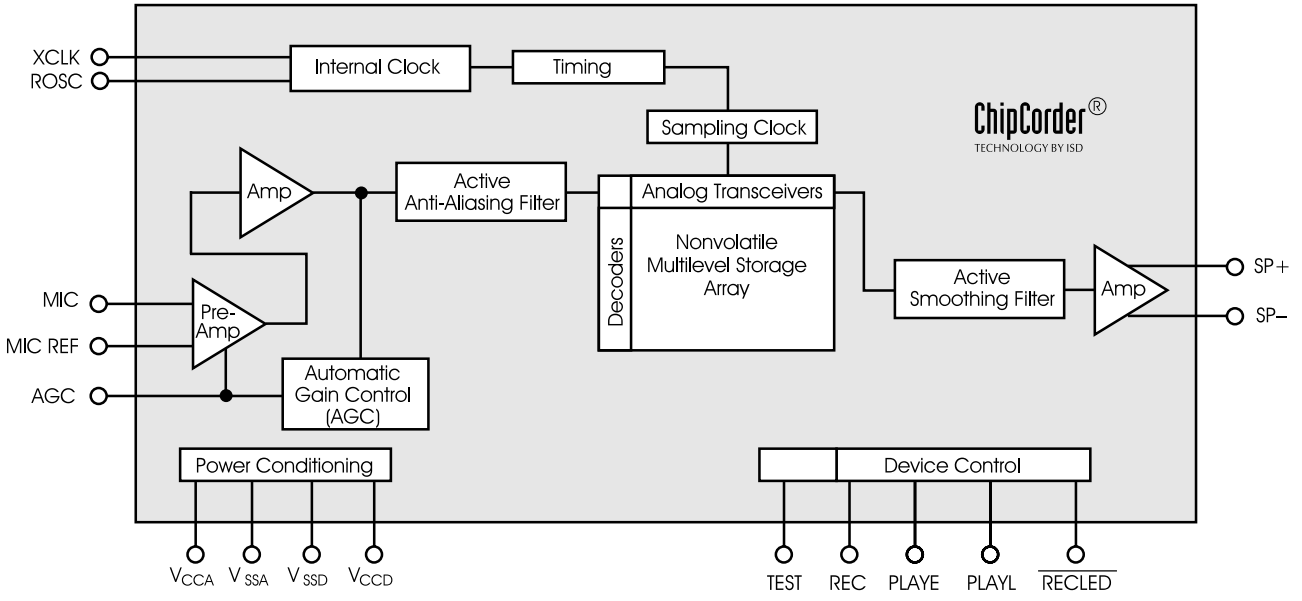
Single-Chip, Single-Message Voice Record/Playback Device 16- to 32-Second Durations

GENERAL DESCRIPTION

Information Storage Devices' ISD1520 ChipCorder® product provides a high-quality, single-chip, single-message, record/playback solution with user-selectable durations of 16 to 32 seconds. The CMOS devices include an on-chip oscillator (with external control), microphone preamplifier, automatic gain control, anti-aliasing filter, multilevel storage array, smoothing filter, and speaker amplifier. A minimum record/playback subsystem can be configured with a microphone, a speaker, several passive components, two push-buttons, and a power source.

Recordings are stored in on-chip, nonvolatile, memory cells, providing zero-power message storage. This unique, single-chip solution is made possible through ISD's patented multilevel storage technology. Voice and audio signals are stored directly into memory in their natural form, providing high-quality, solid-state voice reproduction.

Figure i: ISD1520 Block Diagram



FEATURES

- Easy-to-use single-chip, single-message voice record/playback solution
- High-quality, natural voice/audio reproduction
- Variable record/playback duration controlled by external resistor selection which sets sample rate.

  8 KHz sample rate = 16 seconds

  6.4 KHz sample rate = 20 seconds

  5.3 KHz sample rate = 24 seconds

  4.0 KHz sample rate = 32 seconds
- Push-button interface
  - Playback can be edge- or level-activated
- On-chip 8 Ω speaker driver
- Automatic power-down mode
  - Enters standby mode immediately following a record or playback cycle
  - 0.5 μA standby current (typical)
- Zero-power message storage
  - Eliminates battery backup circuits
- 100-year message retention (typical)
- 10,000 record cycles (typical)
- On-chip oscillator
- No algorithm development required
- Single +5 volt power supply
- 0°C to 50°C Operation
- Available in wafer form, die form, and 28-pin 600 mil. PDIP (for sampling only)

Table i: ISD1520 Summary

Part Number	Minimum Duration[1] (Seconds)	Maximum Input Sample Rate (KHz)[1]	Typical Filter Upper Pass Band (KHz)[1]
ISD1520	20	6.4	2.6

1. *Resistor value of 100 KΩ at the ROSC pin provides this specified duration. Only this duration is guaranteed and tested.*

DETAILED DESCRIPTION

SPEECH/SOUND QUALITY

ISD's patented ChipCorder technology provides natural record and playback. The input voice signals are stored directly in nonvolatile EEPROM cells and are reproduced without the synthetic effect often heard with digital solid-state speech solutions. A complete sample is stored in a single cell, minimizing the memory necessary to store a single message.

DURATION

The ISD1520 devices offer single-chip solutions with 16 to 32 seconds of record/playback duration capacity. Sampling rate and duration are determined by an external resistor connected to the ROSC pin. These specifications apply with the required resistor value for 20-second minimum playback duration.

NOTE *Only the 20 second duration is guaranteed and tested.*

EEPROM STORAGE

One of the benefits of ISD's ChipCorder technology is the use of on-chip non-volatile memory, providing zero-power message storage. The message is retained for up to 100 years without power. In addition, the device can be re-recorded typically over 10,000 times.

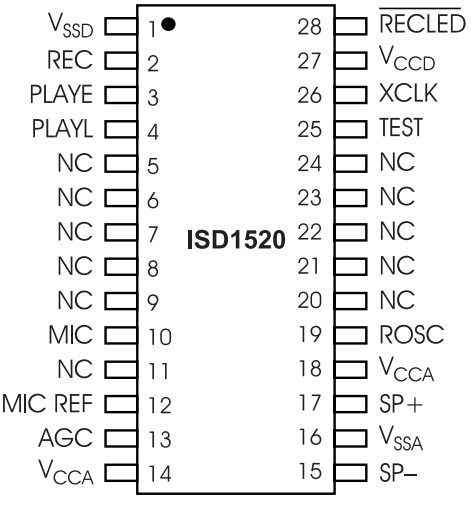
BASIC OPERATION

The ISD1520 ChipCorder device is controlled by the REC pin, and either of two playback pins, PLAYE (edge-activated playback) and PLAYL (level-activated playback). The ISD1520 parts are configured for design simplicity in a single-message application. Device operation is explained under "Functional Description Example" on page 6.

AUTOMATIC POWER-DOWN MODE

At the end of a playback or record cycle, the ISD1520 device automatically returns to a low-power standby mode, consuming typically 0.5 μA, provided that PLAYE, PLAYL, REC, XCLK, and TEST pins are LOW (see Table 3 on page 4). During a playback cycle, the device powers down automatically at the end of the message. During a record cycle, the device powers down immediately after REC is released LOW.

Figure 1: ISD1520 Pinouts—For Sampling Only



PDIP

NOTE: *NC means must Not Connect.*

PIN DESCRIPTIONS

VOLTAGE SUPPLIES (V_{CCA} , V_{CCD})

Analog and digital circuits internal to the ISD1520 device use separate power buses to minimize noise on the chip. These power buses are brought out to separate pins on the package and should be tied together as close to the supply as possible. It is important that the power supply be decoupled as close as possible to the package.

GROUND SUPPLIES (V_{SSA}, V_{SSD})

Similar to V_{CCA} and V_{CCD}, the analog and digital circuits internal to the ISD1520 device use separate ground buses to minimize noise. These pins should be tied together as close as possible to the device.

RECORD (REC)

The REC input is an active-HIGH record signal. The device records whenever REC is HIGH. This pin must remain HIGH for the duration of the recording. REC takes precedence over either playback (PLAYE or PLAYL) signal. If REC is pulled HIGH during a playback cycle, the playback immediately ceases and recording begins.

NOTE *The REC signal is internally debounced on the rising edge to prevent a false retriggering from a push-button switch.*

A record cycle is completed when REC is pulled LOW. An end-of-message (EOM) marker is internally recorded, enabling a subsequent playback cycle to terminate appropriately. The device automatically powers down to standby mode when REC goes LOW. This pin has an internal pull-down device. Holding this pin HIGH will increase standby current consumption.

PLAYBACK, EDGE-ACTIVATED (PLAYE)

When a HIGH-going transition is detected on this input pin, a playback cycle begins. Playback continues until an end-of-message marker is encountered or the end of the memory space is reached. Upon completion of the playback cycle, the device automatically powers down into standby mode. Taking PLAYE LOW during a playback cycle will not terminate the current cycle. This pin has an internal pull-down device. Holding this pin HIGH will increase standby current consumption.

PLAYBACK, LEVEL-ACTIVATED (PLAYL)

When this input pin transitions from LOW to HIGH, a playback cycle is initiated. Playback continues until PLAYL is pulled LOW, an end-of-message marker is detected, or the end of the memory space is reached. The device automatically powers down to standby mode upon completion of the playback cycle. This pin has an internal pull-down device. Holding this pin HIGH will increase standby current consumption.

RECORD LED OUTPUT ($\overline{\text{RECLED}}$)

The $\overline{\text{RECLED}}$ output is LOW during a record cycle. It can be used to drive a LED to provide feedback that a record cycle is in progress. In addition, $\overline{\text{RECLED}}$ pulses LOW momentarily when an end-of-message or end-of-memory marker is encountered in a playback cycle.

MICROPHONE INPUT (MIC)

The microphone input transfers its signal to the on-chip preamplifier. An on-chip Automatic Gain Control (AGC) circuit controls the gain of the preamplifier. An external microphone should be AC-coupled to this pin via a series capacitor. The capacitor value, together with the internal 10 KΩ resistance on this pin, determine the low-frequency cutoff for the ISD1520 passband. Internal AC-coupling connects the preamplifier to the amplifier.

MICROPHONE REFERENCE (MIC REF)

The MIC REF input is the inverting input to the microphone preamplifier. This provides input noise-cancellation, or common-mode rejection, when the microphone is connected differentially to the device.

AUTOMATIC GAIN CONTROL (AGC)

The AGC dynamically adjusts the gain of the preamplifier to compensate for the wide range of microphone input levels. The AGC allows the full range of sound, from whispers to loud sounds, to be recorded with minimal distortion. The "attack" time is determined by the time constant of a 5 KΩ internal resistance and an external capacitor (C6 on the schematic on Figure 2 on page 6) connected from the AGC pin to V_{SSA} analog ground. The "release" time is determined by the time constant of an external resistor (R5) and an external capacitor (C6) connected in parallel between the AGC pin and V_{SSA} analog ground. Nominal values of 470 KΩ and 4.7 μF give satisfactory results in most cases.

SPEAKER OUTPUTS (SP+, SP–)

The SP+ and SP– pins provide direct drive for loudspeakers with impedances as low as 8 Ω. A single output may be used, however, for direct-drive loudspeakers the two opposite-polarity outputs provide an improvement in output power of up to four times over a single-ended connection. Furthermore, when SP+ and SP– are used, a speaker coupling capacitor is not required. A single-ended connection will require an AC-coupling capacitor between the SP pin and the speaker.

The SP+ pin and the SP– pin are internally connected through a 50 KΩ resistance. When not in playback mode, they are floating.

EXTERNAL CLOCK (XCLK)

The external clock input for the ISD1520 device has an internal pull-down resistor. This pin is used for test purposes only. Do not bond this pad.

TEST (TEST)

The test input for the ISD1520 device has an internal pull-down resistor. This pin is used for test purposes only. Do not bond this pad.

RESISTOR CONTROLLED OSCILLATOR (ROSC)

The resistor-controlled oscillator input enables the user to vary the ISD1520 device record and playback duration. The resistor connected between the ROSC pin and V_{SS}, R2 (R_{OSC}), determines the sample frequency and the filter upper pass band for the ISD1520 device. ISD recommends an R_{OSC} resistor value of 100 KΩ.

SPECIFICATIONS

Table 1: Absolute Maximum Ratings[1]

Condition	Value
Junction temperature	150°C
Storage temperature range	–65°C to +150°C
Voltage applied to any pin	(V_{SS} – 0.3 V) to (V_{CC} + 0.3 V)
Lead temperature (soldering—10 seconds)	300°C
V_{CC} – V_{SS}	–0.3 V to +7.0 V

1. *Stresses above those listed may cause permanent damage to the device. Exposure to the absolute maximum ratings may affect device reliability. Functional operation is not implied at these conditions.*

Table 2: Operating Conditions

Condition	Value
Die operating temperature range(1)	0°C to +50°C
Supply voltage (V_{CC})(2)	+4.5 V to +6.5 V
Ground voltage (V_{SS})(3)	0 V

1. *Case Temperature*
2. $V_{CC} = V_{CCA} = V_{CCD}$.
3. $V_{SS} = V_{SSA} = V_{SSD}$.

Table 3: DC Parameters

Symbol	Parameters	Min[2]	Typ[1]	Max[2]	Units	Conditions
V_{IL}	Input Low Voltage			0.8	V	
V_{IH}	Input High Voltage	2.0			V	
V_{OL}	Output Low Voltage			0.4	V	I_{OL} = 4.0 mA(3)
V_{OH}	Output High Voltage	2.4			V	I_{OH} = –1.6 mA(3)
I_{CC}	V_{CC} Current (Operating)			30	mA	V_{CC} = 5.5 V(4), R_{EXT}∞
I_{SB}	V_{CC} Current (Standby)		0.5	10	µA	(4, 5)
I_{ILPD1}	Input Leakage Current			±1	µA	Force V_{SS}(6)
I_{ILPD2}	Input Current HIGH		200	400	µA	Force V_{CC}(7)
I_{ILPD3}	Input Current HIGH			130	µA	Force V_{CC}(8)
R_{EXT}	Output Load Impedance	8			Ω	Speaker Load, SP+ to SP–
R_{MIC}, R_{MICREF}	Preamp Input Resistance		10		KΩ	
A_{MSP}	MIC SP+/– Gain		45		dB	AGC = 0.0 V
R_{AGC}	AGC Output Resistance		5		KΩ	

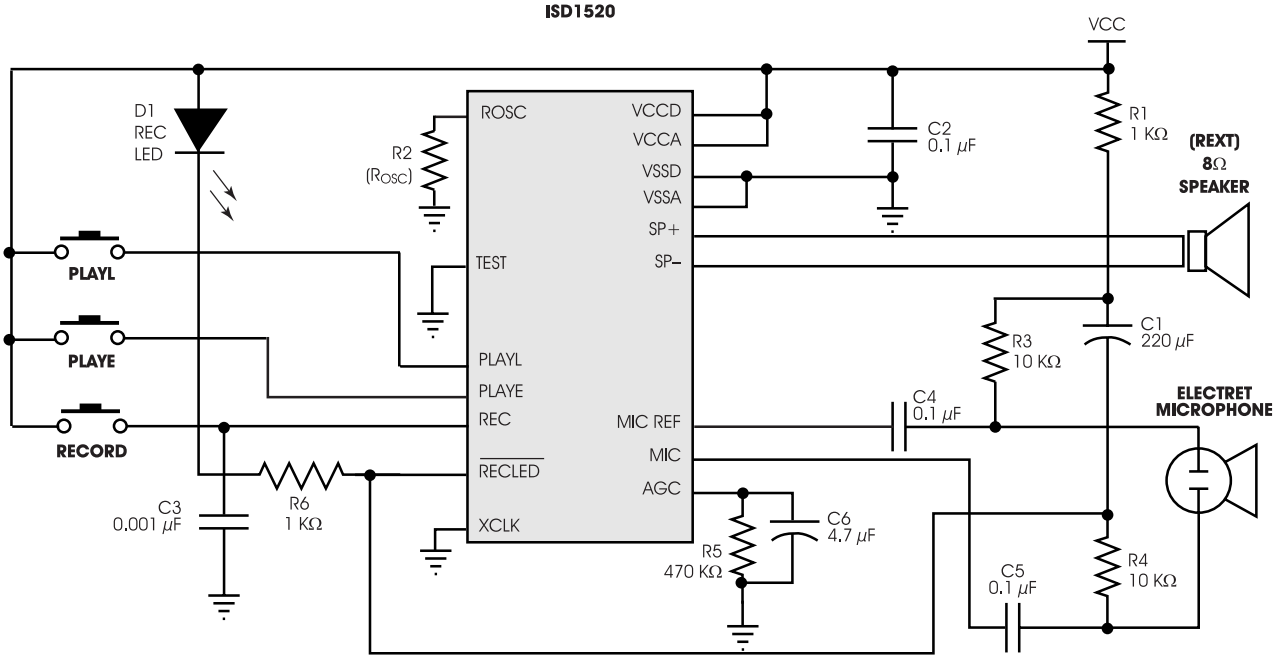
1. *Typical values: T_A = 25°C and 5.0 V.*
2. *All minimum and maximum limits are guaranteed by ISD via electrical testing or characterization. Not all specifications are 100 percent tested.*
3. *Record LED output, $\overline{RECLED}$.*
4. *V_{CCA} and V_{CCD} connected together.*
5. *REC, PLAYL, PLAYE, XCLK, and TEST must be at V_{SSD}.*
6. *REC, PLAYL, and PLAYE.*
7. *REC.*
8. *PLAYL and PLAYE.*

Table 4: AC Parameters[1]

Symbol	Characteristic	Min[3]	Typ[2]	Max[3]	Units	Conditions
						Ω
						Ω

1. *These specifications apply with R equaling 100 KΩ.*
2. *Typical values: T = 25°C and 5.0 V.*
3. *All minimum and maximum limits are guaranteed by ISD via electrical testing or characterization. Not all specifications are 100 percent tested.*
4. *Oscillator stability may vary as much as ±5 percent over the operating temperature and voltage ranges.*
5. *Low-frequency cutoff depends upon value of external capacitors (see Pin Descriptions)*
6. *Filter specification applies to the anti-aliasing filter and to the smoothing filter.*
7. *These specifications apply to usage of a 100 KΩ ideal resistor.*
8. *alanced input signal applied between IC and IC REF as shown in the application example. Single-ended IC or IC REF recommended to be less than 100 mV pea to pea .*

Figure 2: ISD1520 Application Example—Design Schematic



FUNCTIONAL DESCRIPTION EXAMPLE

The following example operating sequence demonstrates the functionality of the ISD1520 devices.

1. Record a message filling the memory.

   Pulling the REC pin HIGH initiates a record cycle from the beginning of the message space. The device will automatically power down after REC is released LOW. An EOM marker is written at the end of message. If REC is held HIGH, the recording continues until the message space has been filled. Once the message space is filled, recording ceases.

2. Edge-activated playback.

   Pulling the PLAYE pin HIGH initiates a playback cycle from the beginning of the message space. The falling edge of PLAYE has no effect on operation. When the device reaches the EOM marker, it automatically powers down. If a recording has filled the message space, the entire message is played. A subsequent rising edge on PLAYE initiates a new play cycle from the beginning of the memory.

3. Level-activated playback.

   Pulling the PLAYL pin HIGH initiates a playback cycle from the beginning of the message space. When the device reaches the EOM marker, it automatically powers down. If recording has filled the message space, the entire message is played. A subsequent rising edge on PLAYL initiates a new play cycle from the beginning of the memory.

4. Level-activated playback (truncated).

   If PLAYL is pulled LOW any time during the playback cycle, the device stops playing and enters the power-down mode. A subsequent rising edge on PLAYL initiates a new play cycle from the beginning of memory.

5. Record (interrupting playback).

   The REC pin takes precedence over other operations. Any HIGH-going transition on REC initiates a new record operation from the beginning of the memory, regardless of any current operation in progress.

6. Record a message, partially filling the memory.

   A record operation need not fill the entire memory. Releasing the REC pin LOW before filling the message space causes the recording to stop and an EOM marker to be placed. The device powers down automatically.

7. Play back a message that partially fills the memory.

   Pulling the PLAYE or PLAYL pin HIGH initiates a playback cycle. The playback cycle ceases when the EOM marker is encountered and the device powers down.

8. $\overline{\text{RECLED}}$ operation.

   The $\overline{\text{RECLED}}$ output pin provides an active-LOW signal which can be used to drive an LED as a "record-in-progress" indicator. It returns to a HIGH state when the REC pin is released LOW or when the recording is completed due to the memory being filled. This pin also pulses LOW to indicate the end of a message has been played.

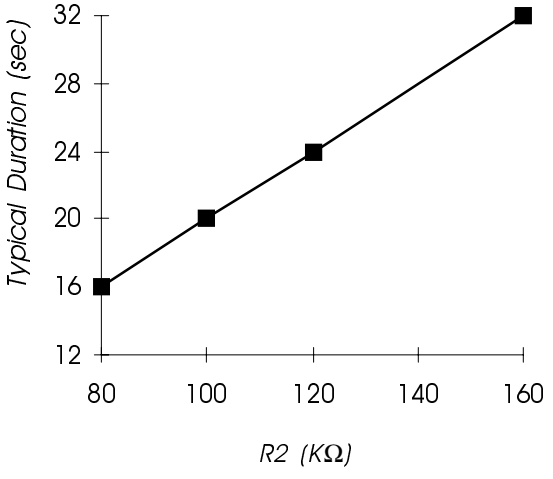
9. ROSC operation.

   The duration of the device can be varied by changing the value of R2 (R). This means the ISD1520 device can actually be between 16 to 32 seconds duration. See Graph 1 which charts typical durations when the R2 is varied from 80 KΩ to 160 KΩ.

   ROSC allows frequency shifting where a recorded voice or sound can be played back faster or slower than normal for special effects. For example, use a 100 KΩ resistor to make the recording and then playback with either an 80 KΩ resistor for faster "chipmunk" talk or a 120 KΩ resistor for a slower, lower voice.

   Another feature is a "pause" or interrupt function that can be done by taking the ROSC resistor to V to stop playback momentarily, resuming when the resistor is connected back to ground.

Chart 1: ISD1520 Duration versus R2 (R_{OSC}) at T_A = 25°C and 5.0 V



TIMING DIAGRAMS

Figure 3: Record Message Until Record Goes LOW

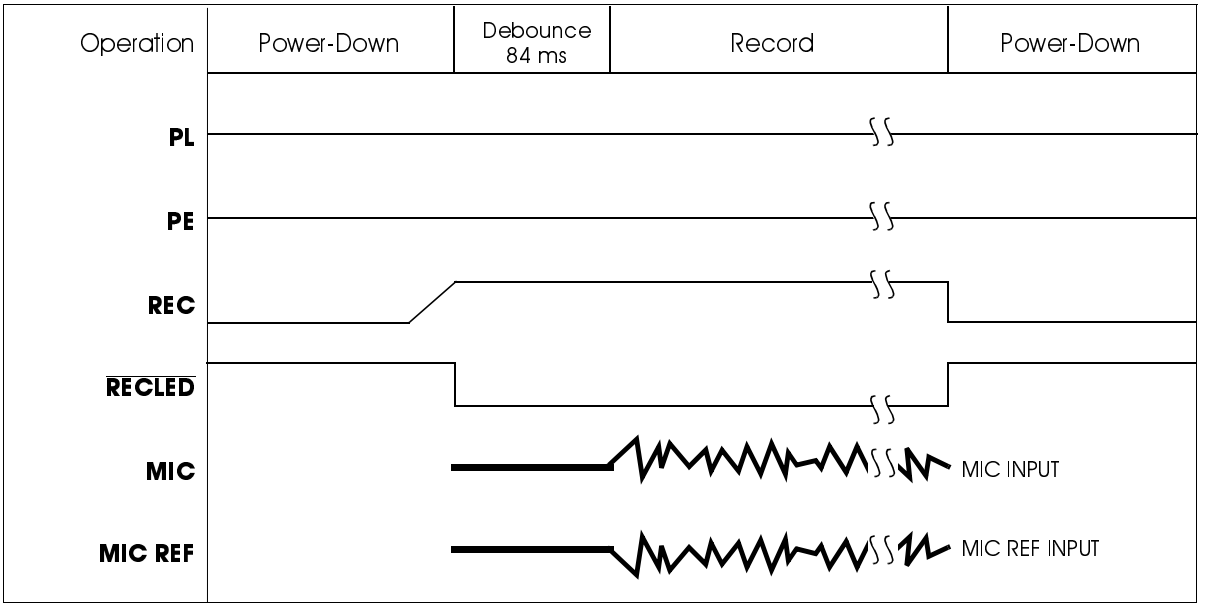


Figure 4: Record Message Until Array is Full

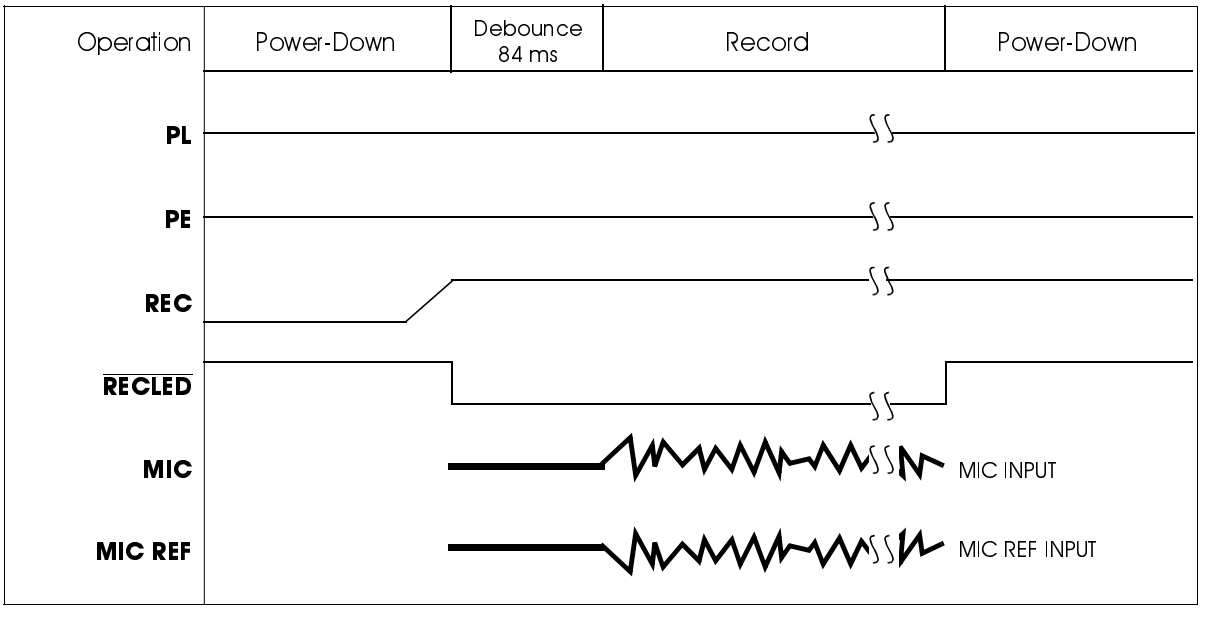


Figure 5: Play Edge (PE) Play Until End of Recording

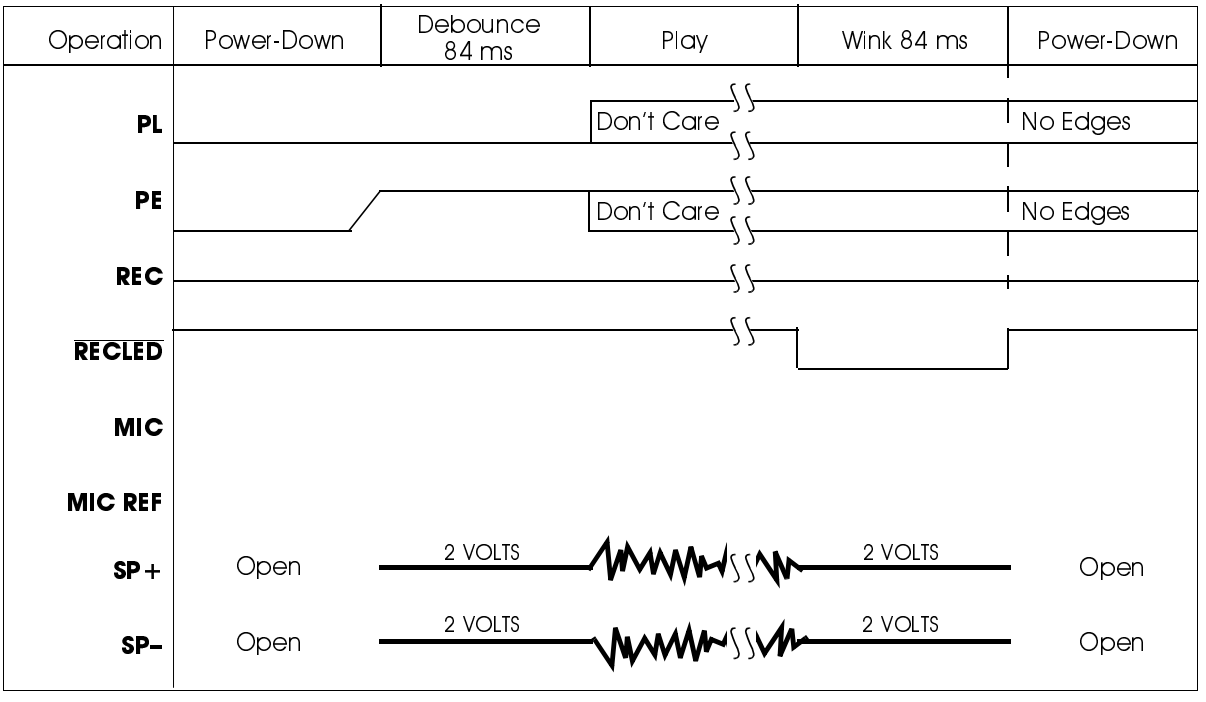
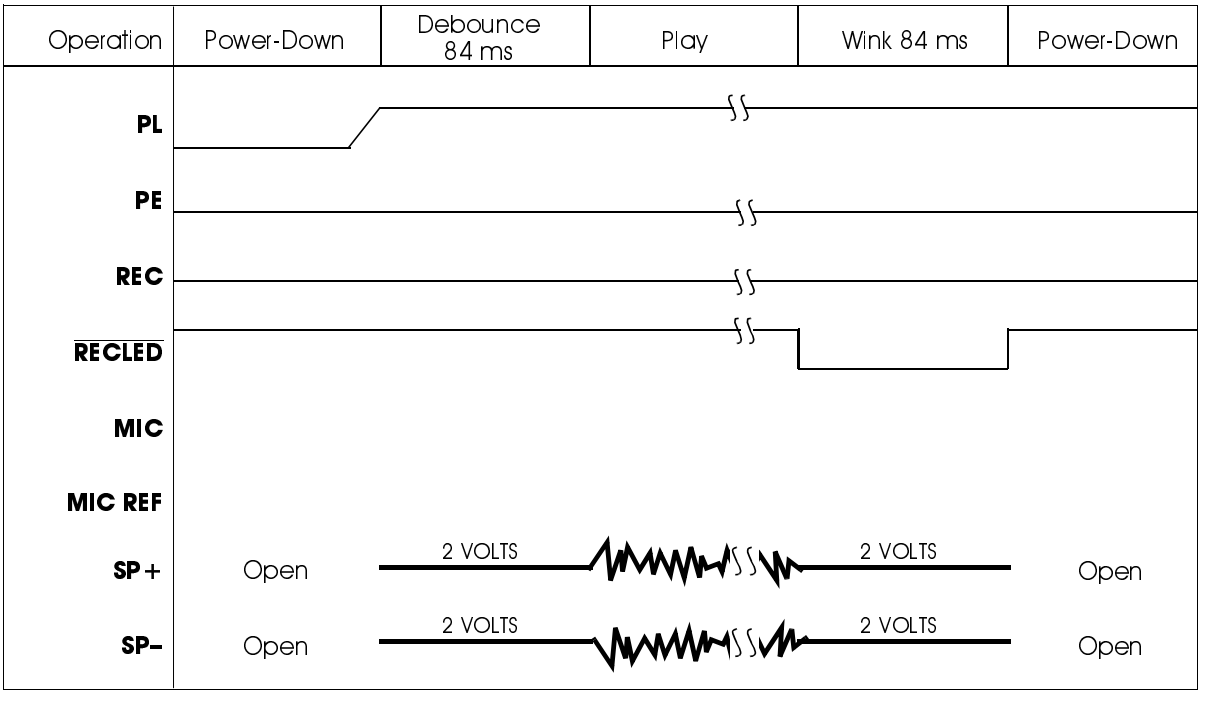


Figure 6: Play Level (PL) Play Until End of Recording



DEVICE PHYSICAL DIMENSIONS

Figure 9: ISD1520 Bonding Physical Layout[1] (Unpackaged Die)

ISD1520

I. Die Dimensions

X: 2710 ±25.4 microns
106.7 ±1 mil

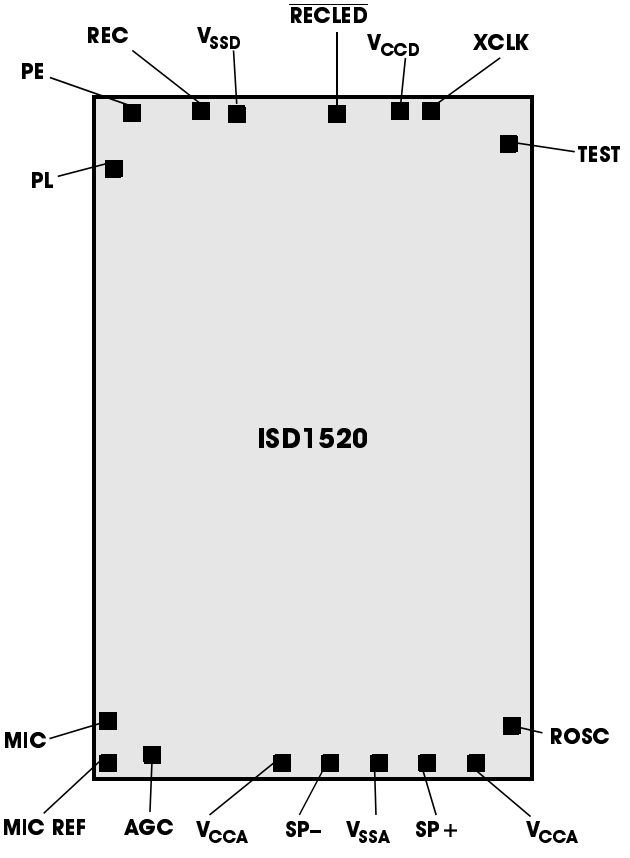
Y: 4210 ±25.4 microns
165.7 ±1 mil

II. Die Thickness[2]

16±1 mil (typ)

III. Pad Opening

100 microns
3.9 mils



1. *The backside of die is internally connected to V_{SS}. It **MUST NOT** be connected to any other potential or damage may occur.*
2. *Die thickness is subject to change, please contact ISD factory for status and availability.*

Table 5: ISD1520 Pin/Pad Designations with Respect to Die Center

Pin	Pin Name	X Axis (um)	Y Axis (um)	X Axis (mil)	Y Axis (mil)
1	VSSD	–342.40	1935.00	–13.48	76.18
2	REC	–579.80	1950.00	–22.83	76.77
3	PE	–1053.40	1950.00	–41.47	76.77
4	PL	–1201.80	1610.00	–47.31	63.39
5	N/C				
6	N/C				
7	N/C				
8	N/C				
9	N/C				
10	MIC	–1197.60	–1687.20	–47.15	–66.43
11	N/C				
12	MIC REF	–1190.40	–1948.00	–46.87	–76.69
13	AGC	–953.00	–1918.60	–37.52	–75.54
14	VCCA	–247.40	–1934.40	–9.74	–76.16
15	SP–	72.40	–1934.40	2.85	–76.16
16	VSSA	392.20	–1934.40	15.44	–76.16
17	SP+	712.00	–1934.40	28.03	–76.16
18	VCCA	1031.80	–1934.40	40.62	–76.16
19	ROSC	1198.00	–1682.20	47.17	–66.23
20	N/C				
21	N/C				
22	N/C				
23	N/C				
24	N/C				
25	TEST	1196.60	1765.60	47.11	69.51
26	XCLK	752.20	1946.40	29.61	76.63
27	VCCD	563.80	1946.40	22.20	76.63
28	$\overline{\text{RECLED}}$	150.80	1935.00	5.94	76.18

Figure 10: 28-Lead 0.600-Inch Plastic Dual Inline Package (PDIP) (P)—For Sampling Only

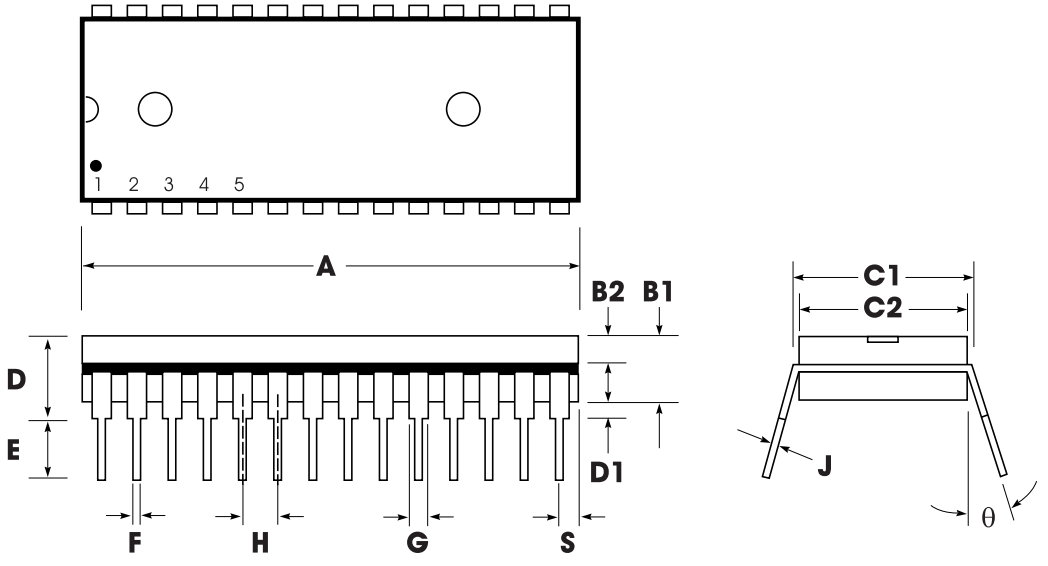


Table 6: Plastic Dual Inline Package (PDIP) (P) Dimensions—For Sampling Only

	INCHES			MILLIMETERS		
	Min	Nom	Max	Min	Nom	Max
A	1.445	1.450	1.455	36.70	36.83	36.96
B1		0.150			3.81	
B2	0.065	0.070	0.075	1.65	1.78	1.91
C1	0.600		0.625	15.24		15.88
C2	0.530	0.540	0.550	13.46	13.72	13.97
D			0.19			4.83
D1	0.015			0.38		
E	0.125		0.135	3.18		3.43
F	0.015	0.018	0.022	0.38	0.46	0.56
G	0.055	0.060	0.065	1.40	1.52	1.65
H		0.100			2.54	
J	0.008	0.010	0.012	0.20	0.25	0.30
S	0.070	0.075	0.080	1.78	1.91	2.03
q	0°		15°	0°		15°