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ADVANCED

Winbond Electronics Corp.

ISD1700A Series

Multi-Message

Single-Chip

Voice Record & Playback Devices

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1 GENERAL DESCRIPTION

The Winbond® ISD1700A ChipCorder® Series is a high quality, fully integrated, single-chip multi-message voice record and playback device ideally suited to a variety of electronic systems. The message duration is user selectable in ranges from 26 seconds to 120 seconds, depending on the specific device. The sampling frequency of each device can also be adjusted from 4 kHz to 12 kHz with an external resistor, giving the user greater flexibility in duration versus recording quality for each application. Operating voltage spans a range from 2.4 V to 5.5 V to ensure that the ISD1740A/50A/60A devices are optimized for a wide range of battery or line-powered applications.

The ISD1740A/50A/60A devices incorporate a proprietary message management system that allows the chip to self-manage address locations for multiple messages. This unique feature provides sophisticated messaging flexibility in a simple push-button environment. The devices include an on-chip oscillator (with external resistor control), microphone preamplifier with Automatic Gain Control (AGC), an auxiliary analog input, anti-aliasing filter, Multi-Level Storage (MLS) array, smoothing filter, volume control, Pulse Width Modulation (PWM) Class D speaker driver, and current output.

The ISD1740A/50A/60A devices also support an optional “vAlert” (voiceAlert) feature that can be used as a new message indicator. With vAlert, the IC strobes an external LED to indicate that a new message is present. Four special sound effect locations are reserved for audio confirmation of commands, such as “Start Record”, “Stop Record,” and “Erase.”

Recordings are stored in on-chip Flash memory cells, providing zero-power message storage. This unique single-chip solution is made possible through Winbond’s patented Multi-Level Storage (MLS) technology. Audio data are stored directly in solid-state memory without digital compression, providing superior quality voice and music reproduction.

Voice signals can be fed into the chip through two independent paths: a differential microphone input and a single-ended analog input. For outputs, the ISD1740A/50A/60A devices simultaneously provide a Pulse Width Modulation (PWM) Class D speaker driver and a separate current output. The PWM can directly drive a standard 8 Ω speaker or a typical buzzer, while the separate single-ended current output can drive an external amplifier.

The ISD1740A/50A/60A devices automatically enter into power down mode for power conservation when an operation is completed.

Notice: The specifications are subject to change without notice. Please contact Winbond Sales Offices or Representatives to verify current or future specifications.

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2 FEATURES

- Integrated message management systems for single-chip, push-button applications
  - **$\overline{\text{REC}}$** *:* level-trigger for recording
  - **$\overline{\text{PLAY}}$** *:* edge-trigger for individual message or level-trigger for sequential playback
  - **$\overline{\text{ERASE}}$** *:* edge-triggered erase for first or last message or level-triggered erase for all messages
  - **$\overline{\text{FWD}}$** *:* edge-trigger to advance to the next message or fast message scan during the playback
  - **$\overline{\text{VOL}}$** : 8 levels output volume control
  - RDY: ready or busy status indication
  - **$\overline{\text{RESET}}$** : bring back to the default state
  - Automatic power-down after each operation cycle
- Selectable sampling frequency controlled by an external oscillator resistor

Sampling Frequency	12 kHz	8 kHz	6.4 kHz	5.3 kHz	4 kHz
Rosc	60 kΩ	80 kΩ	100 kΩ	120 kΩ	160 kΩ

- Selectable message duration

Device	ISD1740A	ISD1750A	ISD1760A
Duration	26 ~ 80 sec	33 ~ 100 sec	40 ~ 120 sec

- Message and operation indicators
  - Four customizable Sound Effects (SE) for audible indications
  - Optional vAlert (voiceAlert) to indicate the presence of new messages
  - LED: stay on during recording, blink during playback, forward and erase operations
- Two individual input channels
  - MIC+/MIC-: differential microphone inputs with AGC (Automatic Gain Control)
  - AnaIn: single-ended auxiliary analog input for recording or feed-through
- Dual output channels
  - PWM Class D speaker amplifier to directly drive an 8 Ω speaker or a typical buzzer
  - AUD single-ended current output to drive external power amplifier
- ChipCorder standard features
  - High-quality, natural voice and audio reproduction
  - 2.4V to 5.5V operating voltage
  - 100-year message retention (typical)
  - 10,000 record cycles (typical)
- Commercial Temperature grade: 0°C to +50°C for die only
- Package options: available in die only

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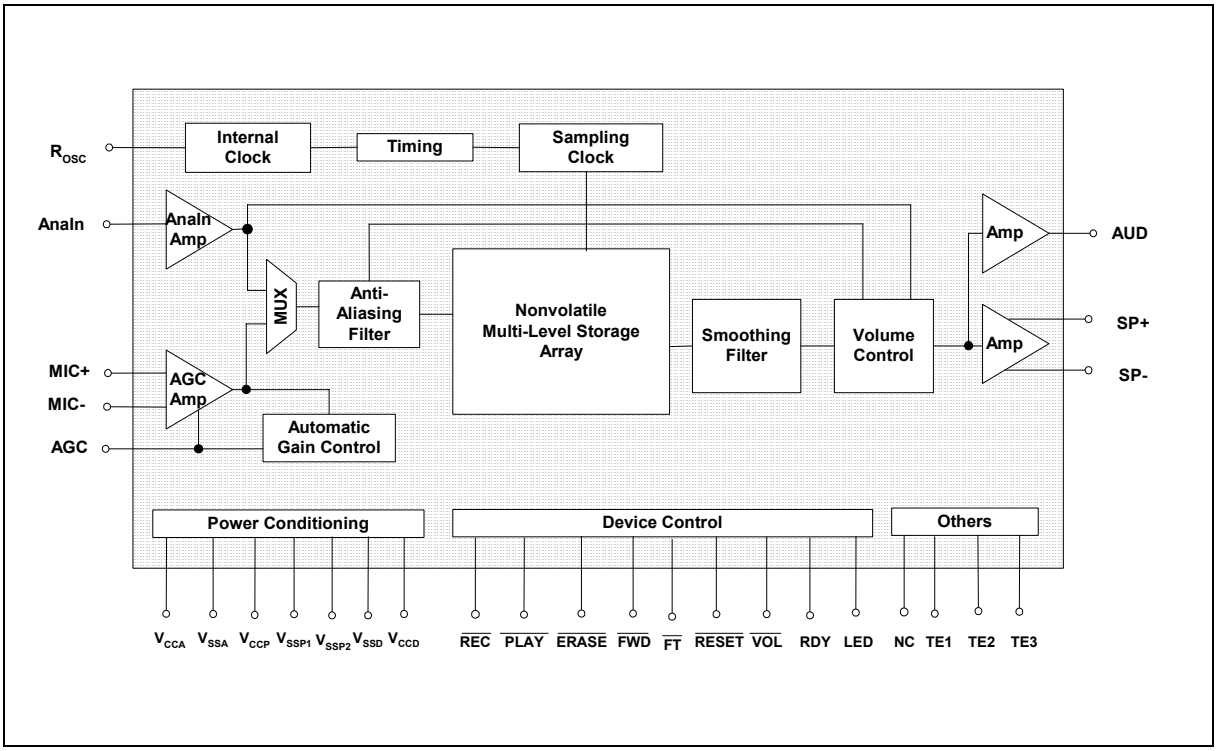
3 BLOCK DIAGRAM



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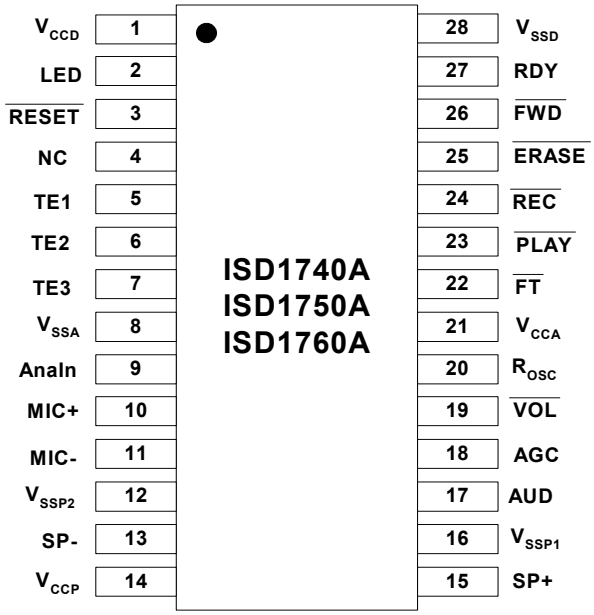
4 PINOUT CONFIGURATION



PDIP

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5 PIN DESCRIPTION

PIN NAME	PDIP PIN NO.	FUNCTIONS
V_{CCD}	1	**Digital Power Supply**: It is important to have a separate path for each power signal including V_{CCD}, V_{CCA} and V_{CCP} to minimize the noise coupling. Decoupling capacitors should be as close to the device as possible.
LED	2	**LED**: This output turns on a LED during a record cycle and blinks LED during playback, forward and erase operations.
$\overline{\text{RESET}}$	3	**RESET**: When Low, the device enters into a known state and initializes all pointers to the default state. This pin has an internal pull-up resistor [1].
NC	4	**NC:** No Connect.
TE1	5	**Test pin #1:** Connect to V_{CCD}.
TE2	6	**Test pin #2:** Connect to V_{CCD}.
TE3	7	**Test pin #3:** Connect to V_{CCD}.
V_{SSA}	8	**Analog Ground**: It is important to have a separate path for each ground signal including V_{SSA}, V_{SSD}, V_{SSP1} and V_{SSP2} to minimize the noise coupling.
AnaIn	9	**AnaIn:** Auxiliary analog input to the device for recording or feed-through. An AC-coupling capacitor (typical 0.1uF) is necessary and the amplitude of the input signal should not exceed 1.0 Vpp.
MIC+	10	**MIC+:** Non-inverting input of the differential microphone signal. The input signal should be AC-coupled to this pin via a series capacitor. The capacitor value, together with an internal 10 KΩ resistance on this pin, determines the low-frequency cutoff for the pass band filter.
MIC-	11	**MIC-**: Inverting input of the differential microphone signal. The input signal should be AC-coupled to the MIC+ pin. It provides input noise-cancellation, or common-mode rejection, when the microphone is connected differentially to the device.
V_{SSP2}	12	**Ground for Negative PWM Speaker Driver**: It is important to have a separate path for each ground signal including V_{SSA}, V_{SSD}, V_{SSP1} and V_{SSP2} to minimize the noise coupling.
SP-	13	**SP-**: The negative Class D PWM provides a differential output with SP+ pin to directly drive an 8 Ω speaker or typical buzzer. During power down or recording, this pin is tri-stated.
V_{CCP}	14	**Power Supply for PWM Speaker Driver**: It is important to have a separate path for each power signal including V_{CCD}, V_{CCA} and V_{CCP} to minimize the noise coupling. Decoupling capacitors to V_{SSP1} and V_{SSP2} should be as close to the device as possible. The V_{CCP} supply and V_{SSP} ground pins have large transient currents and need low impedance returns to the system supply and ground, respectively.
SP+	15	**SP+:** The positive Class D PWM provides a differential output with the SP- pin to directly drive an 8 Ω speaker or typical buzzer. During power down or recording, this pin is tri-stated.

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PIN NAME	PDIP PIN NO.	FUNCTIONS
V_{SSP1}	16	**Ground for Positive PWM Speaker Driver**: It is important to have a separate path for each ground signal including V_{SSA}, V_{SSD}, V_{SSP1} and V_{SSP2} to minimize the noise coupling.
AUD	17	**Auxiliary Output**: AUD is a single-ended current output. It can be used to drive an external amplifier.
AGC	18	**Automatic Gain Control (AGC)**: The AGC adjusts the gain of the preamplifier dynamically to compensate for the wide range of microphone input levels. The AGC allows the full range of signals to be recorded with minimal distortion. The AGC is designed to operate with a nominal capacitor of 4.7 µF connected to this pin. Connecting this pin to ground (V_{SSA}) provides maximum gain to the preamplifier circuitry. Conversely, connecting this pin to the power supply (V_{CCA}) provides minimum gain to the preamplifier circuitry.
$\overline{\text{VOL}}$	19	**Volume Control:** This control has 8 steps of volume adjustment. Each Low pulse decreases the volume by one level. Repeated pulses decrease the volume level from the current setting to the minimum then increase back to the maximum, and continue this loop. The factory default is set at maximum. This pin has an internal pull-up device [1] and an internal debounce (T_{Deb}) [2] for start and end, allowing the use of a push button switch.
R_{OSC}	20	**Oscillator Resistor**: A resistor connected from R_{OSC} pin to ground determines the sample frequency of the device, which sets the duration. Please refer to the Duration Section for details.
V_{CCA}	21	**Analog Power Supply**. It is important to have a separate path for each power signal including V_{CCD}, V_{CCA} and V_{CCP} to minimize the noise coupling. Decoupling capacitors to V_{SSA} should be as close to the device as possible.
$\overline{\text{FT}}$	22	**Feed-through:** When FT is engaged Low, the AnaIn feed-through path is activated. As a result, the AnaIn signal is transmitted directly from AnaIn to both the Speaker and AUD outputs, via the volume control circuit. This pin has an internal pull-up device [1] and an internal debounce (T_{Deb}) [2] for start and end, allowing the use of a push button switch.
$\overline{\text{PLAY}}$	23	**Playback:** Pulsing $\overline{\text{PLAY}}$ to Low once initiates a playback operation. Playback stops automatically when it reaches the end of the message. Pulsing it to Low again during playback stops the operation. Holding $\overline{\text{PLAY}}$ Low constantly functions as a sequential playback operation loop. This looping continues until $\overline{\text{PLAY}}$ returns to High. This pin has an internal pull-up device [1] and an internal debounce (T_{Deb}) [2] for start and end, allowing the use of a push button switch.

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PIN NAME	PDIP PIN NO.	FUNCTIONS
$\overline{\text{REC}}$	24	**Record:** The device starts recording whenever $\overline{\text{REC}}$ switches from High to Low and stays at Low. Recording stops when the signal returns to High. This pin has an internal pull-up device [1] and an internal debounce (T_{Deb}) [2] for start and end, allowing the use of a push button switch.
$\overline{\text{ERASE}}$	25	**Erase:** When active, it starts an erase operation. Erase operation will take place only when the playback pointer is positioned at either the first or last message. Pulsing this pin to Low enables erase operation and deletes the current message. Holding this pin Low for more than 3 sec. initiates a global erase operation, and will delete all the messages. This pin has an internal pull-up device [1] and an internal debounce (T_{Deb}) [2] for start and end, allowing the use of a push button switch.
$\overline{\text{FWD}}$	26	**Forward:** When triggered, it advances to the next message from the current location, when the device is in power down status. During playback cycle, pulsing this pin Low stops the current playback operation and advances to the next message, and then re-starts the playback operation of the new message. This pin has an internal pull-up device [1] and an internal debounce (T_{Deb}) [2] for start and end, allowing the use of a push button switch.
RDY	27	**Ready**: An open drain output. This pin stays Low during record, play, erase and forward operations and stays High in power down state.
V_{SSD}	28	**Digital Ground**: It is important to have a separate path for each ground signal including V_{SSA}, V_{SSD}, V_{SSP1} and V_{SSP2} to minimize the noise coupling..

Note: [1] 600 kΩ [2] TDeb = Refer to AC Timing

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6 FUNCTIONAL DESCRIPTION

6.1 DETAILED DESCRIPTION

6.1.1 Audio Quality

Winbond's patented ChipCorder® Multi-Level Storage (MLS) technology provides a natural, high-quality record and playback solution on a single chip. The input voice signals are stored directly in the Flash memory and are reproduced in their natural form without any of the compression artifacts caused by digital speech solutions.

6.1.2 Message Duration

The ISD1740A/50A/60A devices offer record and playback duration from 26 seconds to 120 seconds. Sampling rate and message duration are determined by an external resistor connected to the R_{OSC} pin.

Table 6.1 Duration vs. Sampling Frequency

Sample Rate	ISD1740A	ISD1750A	ISD1760A
12 kHz	26 sec	33 sec	40 sec
8 kHz	40 sec	50 sec	60 sec
6.4 kHz	50 sec	62 sec	75 sec
5.3 kHz	60 sec	75 sec	90 sec
4 kHz	80 sec	100 sec	120 sec

6.1.3 Flash Storage

The ISD1740A/50A/60A devices utilize embedded Flash memory to provide non-volatile storage. A message can be retained for a minimum of 100 years without power. Additionally, each device can be re-recorded over 10,000 times (typical).

6.2 MEMORY ARRAY ARCHITECTURE

The memory array provides storage for four special Sound Effects (SE) and the audio data. The memory array is addressed by rows. A row is the minimum storage resolution by which the memory can be addressed. The memory assignment is handled automatically by the internal message management system.

The four sound effects occupy four rows of the first sixteen rows in the memory array. The minimum storage resolution varies with the sampling frequency, as shown in **Table 6.2**.

Table 6.2 Minimum Storage Resolution vs. Sampling Frequency

Sampling Frequency	12 kHz	8 kHz	6.4 kHz	5.3 kHz	4 kHz
Minimum Storage Resolution	83.3 msec	125 msec	156 msec	187 msec	250 msec

For example, at 8 kHz sampling frequency, the minimum storage resolution is 125 msec, so, each Sound Effect (SE) is approximately 0.5 seconds long. The remaining memory is dedicated to audio data storage.

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6.3 MODES OF OPERATIONS

The ISD1740A/50A/60A devices are designed to operate in push-button operation only.

Push-button operation entails use of the **REC** , **PLAY** , **FT** , **FWD** , **ERASE** , **VOL** and **RESET** pins to trigger operations. The internal state machine automatically configures the signal path according to the operation requested. In this mode of operation, the internal state machine takes full control of message management. This allows the user to record, playback, erase, and forward messages without the needs to know the exact addresses of the messages storage inside the memory. For additional information, please refer to Section 7.

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7 PUSH-BUTTON OPERATIONS

The user utilizes the **REC**, **PLAY**, **FT**, **FWD**, **ERASE**, **VOL** or **RESET** pin to initiate an operation. The device automatically enters the power-down state at the end of a PLAY, REC, ERASE, FWD, VOL, or RESET operation.

7.1 OPERATION OVERVIEW

After power-on-reset (POR), the device is in the factory default state and two internal record and playback pointers are initialized. (Detailed information about these two pointers is provided later in this Section.) Then, the active analog path configuration is determined by the state of the **FT**, and by the operation requested (e.g. record, playback, or power down).

Up to four optional sound effects (SE1-4) can be programmed into the device to provide audible feedback to alert the user about the operating status. Separately, the LED output provides visual feedback on the operating state even if no sound effects are programmed.

A circular message management technique is implemented. Recorded messages are stored sequentially into the memory from the beginning to the end in a circular manner.

Two internal pointers, the record pointer and playback pointer, determine the point at which an operation starts. After power-on or **RESET**, these pointers are initialized as follows:

- If no messages are present, both point to the beginning.
- If messages are present, the record pointer points to the next available memory location after the last message and the playback pointer points to the beginning of the last recorded message.

The playback pointer is affected primarily by the **FWD** operation. The record pointer is updated to the next available memory location after each **REC** operation.

7.1.1 Record Operation

Recording is controlled by the **REC**. Setting this pin Low starts a record operation. The device will start recording from the next available location in memory and will continue recording until either the **REC** is returned High or the memory becomes full. The source of the recording is from either MIC or AnaIn, whereas the active analog configuration path is determined by the desired operation and the state of the **FT**. The **REC** is debounced internally. After recording, the record pointer will move from the last recorded message to the next available address and the playback pointer will be positioned at the beginning of the newly recorded message.

It is important for an Erase operation to be performed on the desired location before any recording proceeds. Also, the power supply must remain On during the entire process of recording. If power is interrupted during recording, the LED will blink seven times, which indicates that something unusual has occurred. In this event, performing a Global Erase will reset the chip back to its proper state.

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Message record indicators:

a) When **REC** goes Low:

- If present, SE1 is played and LED flashes once.
- Then, the LED stays On to indicate that a recording is in progress.

b) When **REC** goes High or when the memory is full:

- If present, SE2 is played and the LED flashes twice, and then remains Off to alert the user that the recording process has been completed.

Triggering of **REC** during a play, erase or forward operation is an illegal operation and will be ignored.

7.1.2 Playback Operation

Two playback modes are executed by **PLAY** , which is internally debounced.

a) ***Edge-trigger mode***: Pulsing **PLAY** Low once initiates a playback operation of the current message. Playback automatically stops at the end of the message. Pulsing **PLAY** again will re-play the message. During playback, the LED flashes and goes Off when the operation stops. Pulsing **PLAY** to Low again during playback stops the operation. Under these circumstances, the playback pointer remains at the start of the played message after the operation is completed.

b) ***Sequential Playback mode***: If **PLAY** is held Low constantly, all messages will be played and looped from the current message to its previous message. This looping continues until **PLAY** is released. After each message, SE1 is played. After the last message has been played, SE2 is played, and then device plays the first message again. During the entire playback operation, the LED flashes. When playback stops, the playback pointer will be placed at the start of the halted message.

Triggering **PLAY** during a record, erase, or forward operation is an illegal operation and will be ignored.

7.1.3 Forward Operation

The **FWD** allows the user to move the playback pointer to the next message in a forward direction. When the pointer reaches the last message, it will jump back to the first message. Hence, the movement is in a circular fashion among the messages. The **FWD** is debounced internally. The effect of a Low-going pulse on the **FWD** depends on the current state of the device:

a) If the device is in power-down state and the current location of the playback pointer is *not* the last message: the pointer will advance one message and, if present, SE1 is played. The LED flashes once.

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b) If the device is in power-down state and the current location of the play pointer is the last message: the pointer will advance to the first message and, if present, SE2 is played. The LED will flash twice.

c) If the device is currently playing a message that is not the last one:

- Playback is halted.
- The playback pointer is advanced one message.
- If present, SE1 is played.
- Playback of the next message begins.
- The LED flashes during this entire process.

d)If the device is currently playing a message that is the last one:

- Playback is halted.
- The playback pointer is advanced to the first message.
- If present, SE2 is played.
- Playback of the first message begins.
- The LED flashes during this entire process.

Triggering of the **$\overline{\text{FWD}}$** operation during an erase or record operation is an illegal operation and will be ignored.

7.1.4 Erase Operation

Erasing individual message takes place only if the playback pointer is at either the first or the last message. Erasing individual messages other than the first or last message is not possible. However, global erase can be executed at any message location and will erase all messages. These two erase modes are characterized as follows:

a) ***Individual Erase***: Only the first or last messages can be individually erased. Pulsing **$\overline{\text{ERASE}}$** Low performs actions dependent upon the current location of the playback pointer:

- If the device is idle and the playback pointer is currently pointing to the first message:
  - First message is erased.
  - SE2, if present, will be played and the LED will flash twice.
  - Playback pointer will be updated to point to the new first message (previously, the second message).
- If the device is idle and the playback pointer is currently pointing to the last message:
  - Last message is erased.
  - SE2, if present, will be played and the LED will flash twice.
  - Playback pointer will be updated to point to the new last message (previously, the second to last message).

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- If the device is idle and the playback pointer is *not* currently pointing to the first or last message:
  - No message is erased.
  - SE3, if present, will be played and the LED will flash twice.
  - Play pointer will be unchanged.
- If the device is currently playing the first or last message, pressing **$\overline{\text{ERASE}}$** will delete the current message, as in the related cases described above.

b) ***Global Erase***: Level-triggering this pin at Low for more than 2.5 seconds initiates the Global Erase operation and deletes all messages, except the SEs. If SEs are present, the device will play SE1 three times after **$\overline{\text{ERASE}}$** is held for 2.5 seconds. If **$\overline{\text{ERASE}}$** is not released during the playback of SE1, all messages will be erased, and the chip will play SE4. See Figure 7.1 for the operation details. The **$\overline{\text{ERASE}}$** is debounced internally.

Triggering **$\overline{\text{ERASE}}$** for individual erase during a record or forward operation is an illegal operation and will be ignored. However, triggering **$\overline{\text{ERASE}}$** for an individual erase operation during playback will delete the current played message, if it is the first or last one.

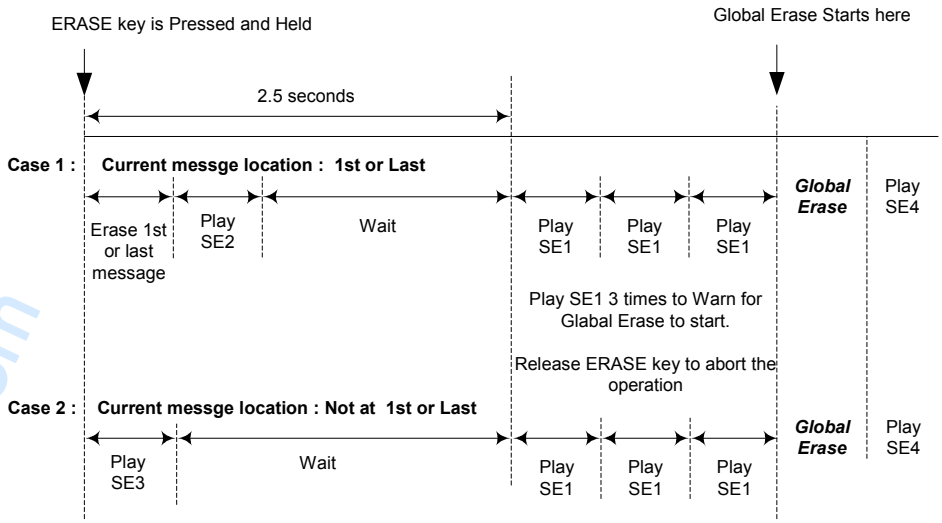

Figure 7.1: Global Erase Operation

7.1.5 Reset Operation

A 0.1 μF capacitor is recommended to connect **$\overline{\text{RESET}}$** to ground if a push button switch is used on this pin. When **$\overline{\text{RESET}}$** is triggered, the device will place both the record and the playback pointers at the last message. When a microcontroller is used for a power-on-Reset,

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RESET must stay active for at least 1 μsec after all supply rails reach their proper specifications.

7.1.6 VOL Operation

Pulsing **VOL** Low changes the volume output. Each pulse on **VOL** will decrease the volume until the minimum setting is reached. Subsequent pulses will increase the volume until the maximum level is reached and the cycle will start again. There are 8 steps of volume control. Each step changes the volume by 4 dB. The **VOL** is debounced internally. A **RESET** operation will re-initialize the volume level to the default state, which is the maximum level.

7.1.7 FT (Feed-Through) Operation

The **FT** controls the feed-through path from the input to the output of the chip. When **FT** is held Low, FT mode is enabled. By factory default, FT mode will pass AnaIn to SPK and AUD outputs if the device is idle. It will record AnaIn to the memory during a record operation.

7.2 vALERT FEATURE (OPTIONAL)

If this optional feature is enabled, after a recording operation, the LED output will blink once every few seconds to indicate the presence of a new message. After a subsequent playback operation, the vAlert will stop flashing.

7.3 SOUND EFFECT (SE) EDITING

SE editing can be accessed via push buttons. The first sixteen addresses are shared equally by four Sound Effects (SE1, SE2, SE3, and SE4).

7.3.1 Sound Effects

The functions of SEs are as follows:

- SE1: Beginning of recording, forward or global erase warning
- SE2: End of recording, single erase or forward from last message
- SE3: Invalid operation
- SE4: Global erase

Whether or not the SEs are programmed, the LED will flash accordingly. The LED flashes once for SE1, twice for SE2, and so on. The frequency of flashing depends upon the sampling frequency selected and the power supply level used.

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7.3.2 Entering SE Mode

- First press and hold **FWD** Low for more than 3 seconds. This action on **FWD** will play SE1 and cause the LED to blink once (if at the last message location, the chip will play SE2 and the LED will blink twice).
- While holding **FWD** Low, press and hold the **REC** Low until the LED blinks once. The device is now in SE editing mode.
- The LED flashing once indicates that SE1 is accessible.

7.3.3 SE Editing

- When in SE editing mode, one can perform record, play, or erase operation on each SE by pressing the appropriate button. For example, to record SE, simply press and hold **REC**. Similarly for play and erase functions, press and hold **PLAY** or **ERASE**, respectively.
- A **FWD** operation moves the record and playback pointers to the next SE sequentially. The LED will blink 1~4 times after such operations to indicate which SE is active. If **FWD** is pressed while accessing SE4, the LED will flash once to indicate that SE1 is again active.
- While the LED is blinking, the device will ignore any input commands. The User must wait until the LED stops blinking before any record, play or erase command can be sent.

7.3.4 Exiting SE Mode

- First press and hold **FWD** until the LED stops blinking. Then, simultaneously press and hold the **REC** Low until the LED blinks twice and SE2 (if present) is played. The device has now exited from SE editing mode.

7.3.5 Sound Effect Duration

The duration of sound effects is determined by the sampling frequency selected. All sound effects with the same sampling frequency have the same duration.

Table 8.1 Sound Effect Duration vs. Sampling Frequency

Sampling Frequency	12 kHz	8 kHz	6.4 kHz	5.3 kHz	4 kHz
Duration of SE	0.33 sec	0.5 sec	0.625 sec	0.75 sec	1 sec

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7.4 ANALOG INPUTS

7.4.1 Microphone Input

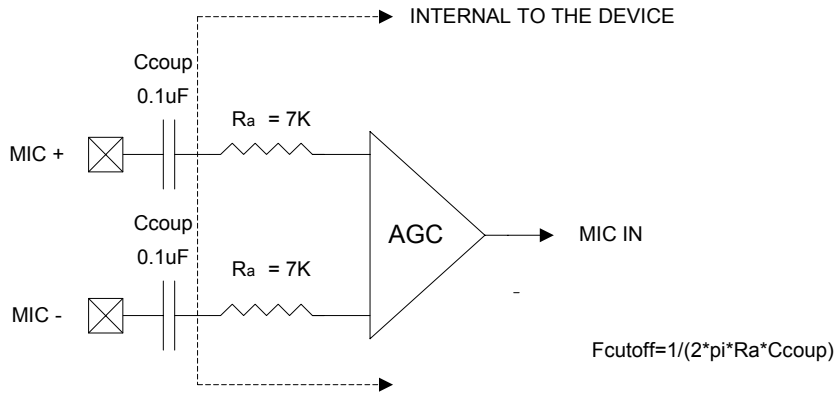

Figure 7.2: MIC input impedance (When this path is active)

7.4.2 AnaIn Input

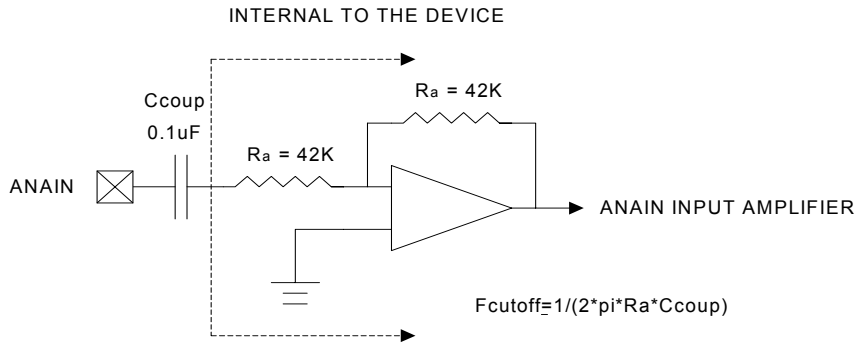

Figure 7.3: AnaIn input impedance (When the device is powered-up)

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8 TIMING DIAGRAMS

8.1 RECORD, PLAY AND ERASE

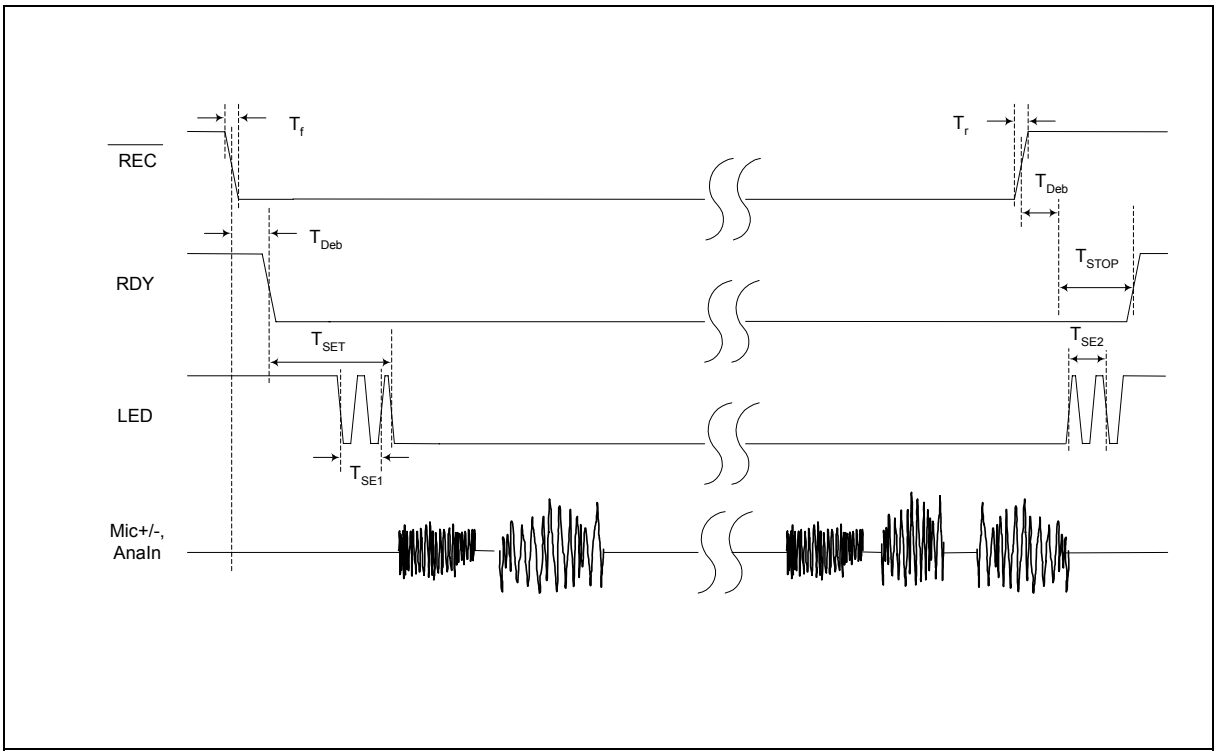

Figure 8.1: Record Operation

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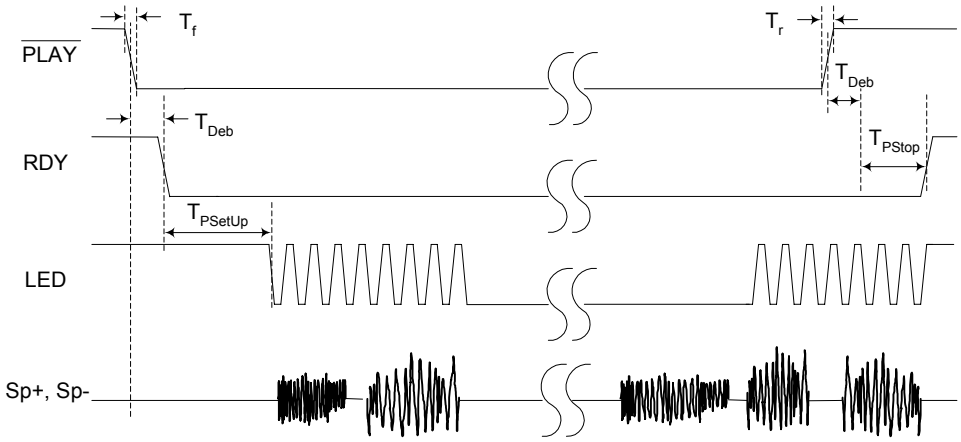
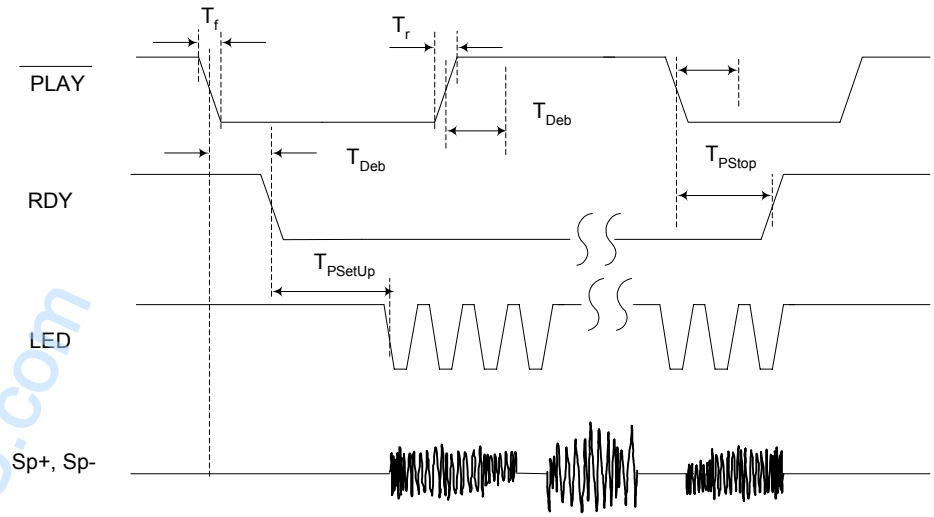


Playback the Entire Message



Start Playback and Stop Playback

Figure 8.2: Playback Operation

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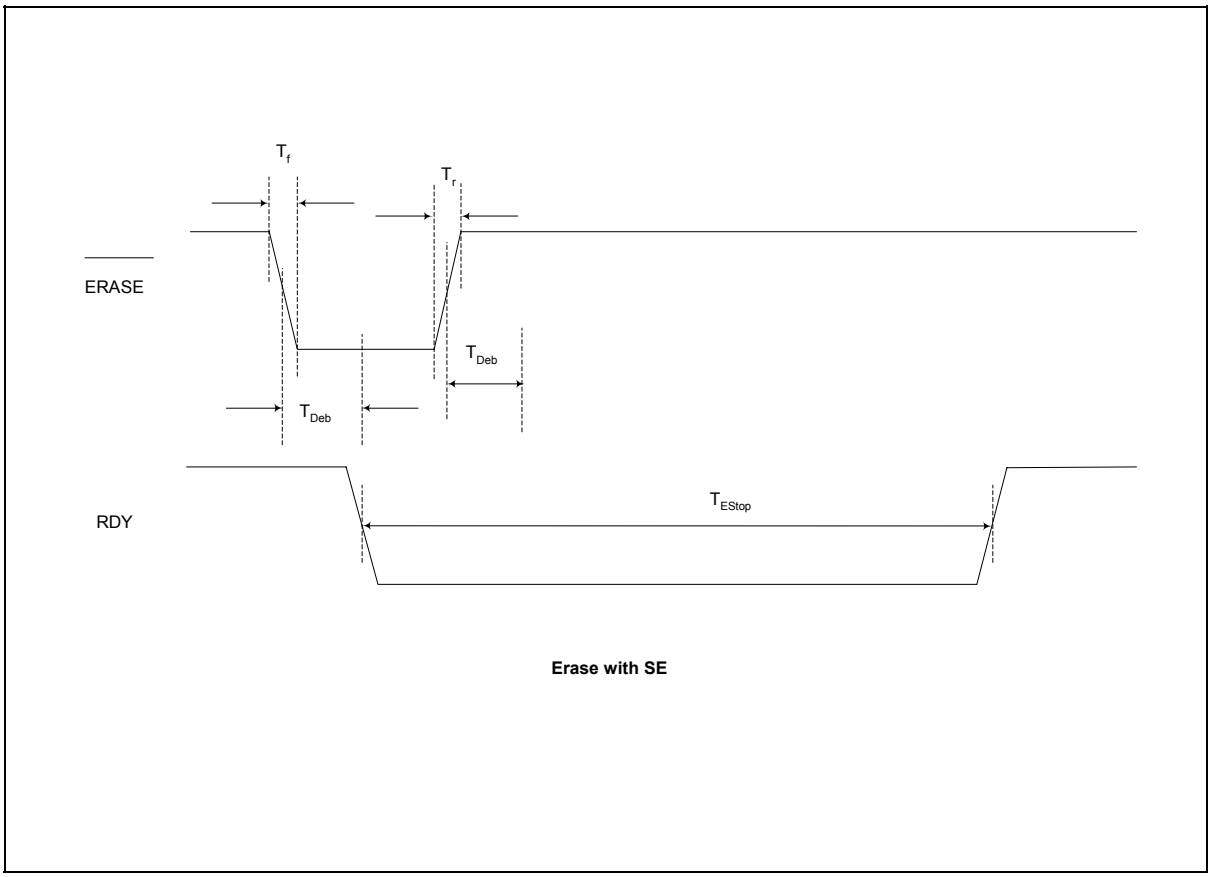

Figure 8.3: Erase Operation

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9 ABSOLUTE MAXIMUM RATINGS

ABSOLUTE MAXIMUM RATINGS

CONDITIONS	VALUES
Junction temperature	150°C
Storage temperature range	-65°C to +150°C
Voltage applied to any pins	(V_{SS} –0.3 V) to (V_{CC} +0.3 V)
Power supply voltage to ground potential	-0.3 V to +7.0 V

Note: Stresses above those listed may cause permanent damage to the device. Exposure to the absolute maximum ratings may affect device reliability and performance. Functional operation is not implied at these conditions.

9.1 OPERATING CONDITIONS

OPERATING CONDITIONS

CONDITIONS	VALUES
Operating temperature range	0°C to +50°C
Supply voltage (V_{CC}) [1]	+2.4 V to +5.5 V
Ground voltage (V_{SS}) [2]	0 V
Input voltage (V_{CC}) [1]	0 V to 5.5 V
Voltage applied to any pins	(V_{SS} –0.3 V) to (V_{DD} +0.3 V)

[1] $V_{CC} = V_{CCA} = V_{CCD} = V_{CCP}$

[2] $V_{SS} = V_{SSA} = V_{SSD} = V_{SSP1}$ V_{SSP2}

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10 ELECTRICAL CHARACTERISTICS

10.1 DC PARAMETERS

PARAMETER	SYMBOL	MIN	TYP [1]	MAX	UNITS	CONDITIONS
Supply Voltage	V_{DD}	2.4		5.5	V	
Input Low Voltage	V_{IL}	V_{SS}-0.3		0.3xV_{DD}	V	
Input High Voltage	V_{IH}	0.7xV_{DD}		V_{DD}	V	
Output Low Voltage	V_{OL}	V_{SS}-0.3		0.3xV_{DD}	V	I_{OL} = 4.0 mA[2]
Output High Voltage	V_{OH}	0.7xV_{DD}		V_{DD}	V	I_{OH} = -1.6 mA[2]
Record Current	I_{DD_Record}			20	mA	V_{DD} = 5.5 V, No load, Sampling freq = 12 kHz
Playback Current	$I_{DD\_Playback}$			20	mA	
Erase Current	I_{DD_Erase}			20	mA	
Standby Current	I_{SB}		0.5	1	µA	V_{DD} = 5.5 V, T=25°C [3] [4]
Input Leakage Current	I_{ILPD1}			±1	µA	Force V_{DD}
Input Current Low	I_{ILPD2}	-3		-10	µA	Force V_{SS} , others at Vcc
Preamp Input Impedance	R_{MIC+},R_{MIC-}		7		kΩ	Power-up AGC
AnaIn Input Impedance	R_{AnaIn}		42		kΩ	Power-up
MIC Differential Input	V_{IN1}		15	300	mV	Peak-to-Peak[5]
AnaIn Input Voltage	V_{IN2}			1	V	Peak-to-Peak
Gain from MIC to SP+/-	A_{MSP}	6		40	dB	V_{IN} = 15~300 mV, AGC = 4.7 µF, V_{CC} = 2.4V~5.5V
Speaker Output Load	R_{SPK}	8			Ω	Across both Speaker pins
Speaker Output Power	Pout		670		mW	V_{DD} = 5.5 V; 1Vp-p, 1 kHz sine wave at AnaIn. R_{SPK} = 8 Ω.
			313		mW	V_{DD} = 4.4 V
			117		mW	V_{DD}= 3 V
			49		mW	V_{DD}= 2.4 V
Speaker Output Voltage	V_{OUT1}		V_{DD}		V	R_{SPK} = 8Ω (Speaker), Typical buzzer
AUD	I_{AUD}		-3.0		mA	V_{DD} =4.5 V, R_{EXT}= 390 Ω
Total Harmonic Distortion	THD		1		%	15 mV p-p 1 kHz sine wave, Cmessage weighted

Notes:
[1] Conditions: V_{CC} = 4.5V, 8 kHz sampling frequency and T_A = 25°C, unless otherwise stated.
[2] LED output during Record operation.
[3] V_{CCA}, V_{CCD} and V_{CCP} are connected together. V_{SSA}, V_{SSP1}, V_{SSP2} and V_{SSD} are connected together.
[4] **REC** , **PLAY** , **FT** , **FWD** , **ERASE** , **VOL** and **RESET** must be at V_{CCD}.
[5] Balanced input signal applied between MIC+ and MIC- as shown in the applications example. Single-ended MIC+ or MIC- input is recommended to be less than 100 mV p-p.

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10.2 AC PARAMETERS

CHARACTERISTIC	SYMBOL	MIN	TYP [1]	MAX	UNITS	CONDITIONS	
Sampling Frequency [2]	F_S	4		12	kHz	Vcc=2.4 V~5.5V	
Duration [3]	T_{Dur}		Section 6.1.2		sec	Vcc=2.4 V~5.5V, all Fs	
Rising time	T_r	0		100	nsec		
Falling Time	T_f	0		100	nsec		
Debounce Time (REC, PLAY, ERASE, FWD, VOL)	T_{Deb}		16		msec	F_S =12 kHz	Vcc=2.4 V~5.5 V
			24		msec	F_S =8 kHz	
			30		msec	F_S =6.4 kHz	
			37		msec	F_S =5.3 kHz	
			48		msec	F_S =4 kHz	
RESET Pulse	T_{RESET}	1			µsec	Vcc=2.4 V~5.5 V	
Record SetUp Time	T_{RSetUp}		0.37		sec	F_S =12 kHz	Vcc=2.4 V~5.5 V, with SEs played
			0.54		sec	F_S =8 kHz	
			0.67		sec	F_S =6.4 kHz	
			0.80		sec	F_S =5.3 kHz	
			1.05		sec	F_S =4 kHz	
Record Stop Time	T_{RStop}		0.35		sec	F_S =12 kHz	Vcc=2.4 V~5.5 V, with SEs played
			0.52		sec	F_S =8 kHz	
			0.65		sec	F_S =6.4 kHz	
			0.77		sec	F_S =5.3 kHz	
			1.03		sec	F_S =4 kHz	
Play SetUp Time	T_{PSetUp}		100		msec	Vcc=2.4 V~5.5 V, all Fs	
Play Stop Time	T_{PStop}		33		msec	Vcc=2.4 V~5.5 V, all Fs	
Erase Stop Time	T_{EStop}		0.34		sec	F_S =12 kHz	Vcc=2.4 V~5.5 V, with SEs played
			0.51		sec	F_S =8 kHz	
			0.64		sec	F_S =6.4 kHz	
			0.77		sec	F_S =5.3 kHz	
			1.02		sec	F_S =4 kHz	
AUD Ramp Up Time	T_{RU}		4		msec	Vcc=2.4 V~5.5 V	
AUD Ramp down Time	T_{RD}		4		msec	Vcc=2.4 V~5.5 V	
LED Cycle frequency	T_{Cyc}	1		6	Hz	Playback at any F_S	

Notes: [1] Typical values: V_{CC} = 4.5 V, SF = 8 kHz and @ T_A = 25°C, unless otherwise stated.

[2] Sampling Frequency can vary as much as ±2.25 percent over the temperature and voltage ranges.

[3] Duration can vary as much as ±2.25 percent over the commercial temperature and voltage ranges.

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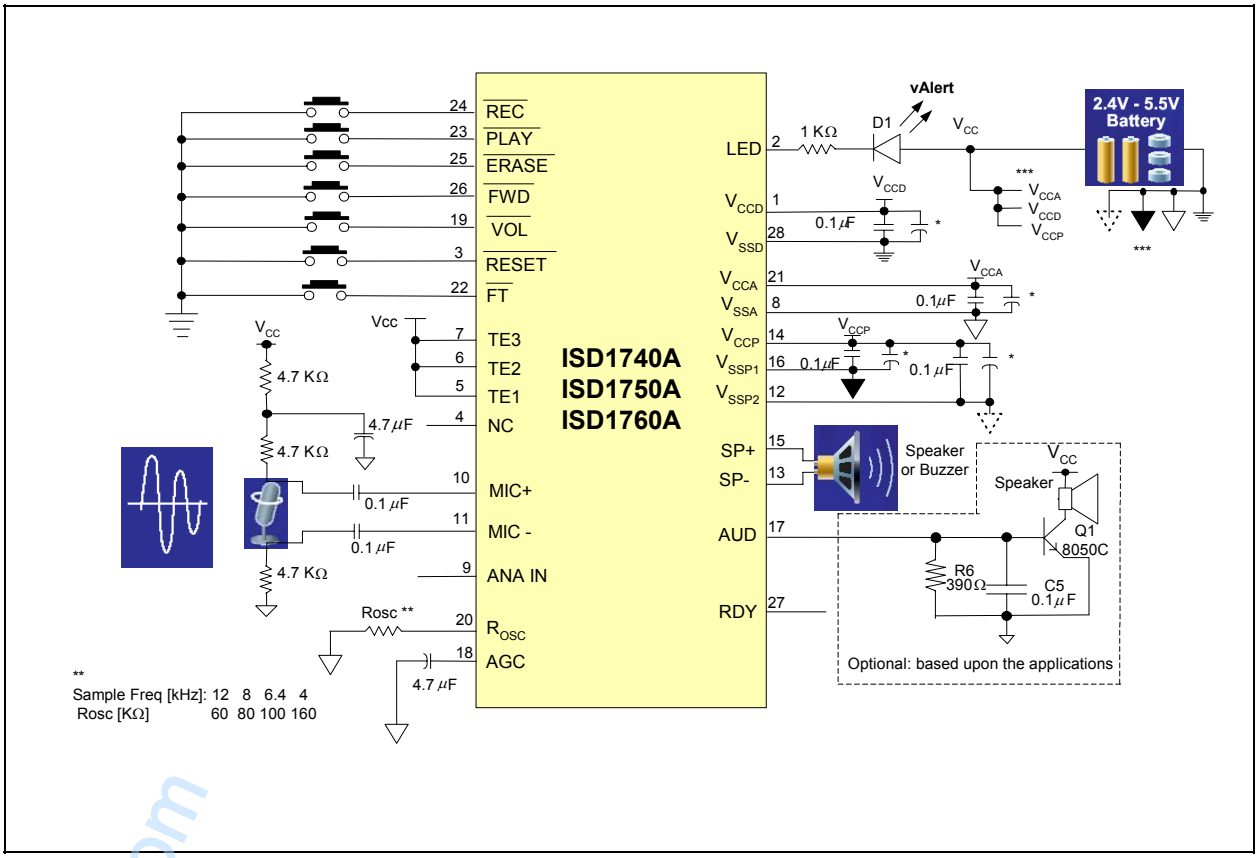
11 TYPICAL APPLICATION CIRCUITS

Two example circuits illustrate recording via MIC and AnaIn inputs, respectively. These examples show typical implementations of ISD1740A/50A/60A devices. .

Example #1:



Recording via MIC input

Notes:

* These capacitors may be needed in order to optimize for the best voice quality, which is also dependent upon the layout of the PCB. Depending on system requirements, they can be 10 μF, 4.7 μF or other values. Please refer to the ChipCorder Applications section or consult Winbond for layout advice.

** For Sampling Freq at 8 kHz, Rosc = 80 KΩ

*** It is important to have a separate path for each ground and power back to each terminal to minimize the noise. Also, the power supplies should be decoupled as close to the device as possible.

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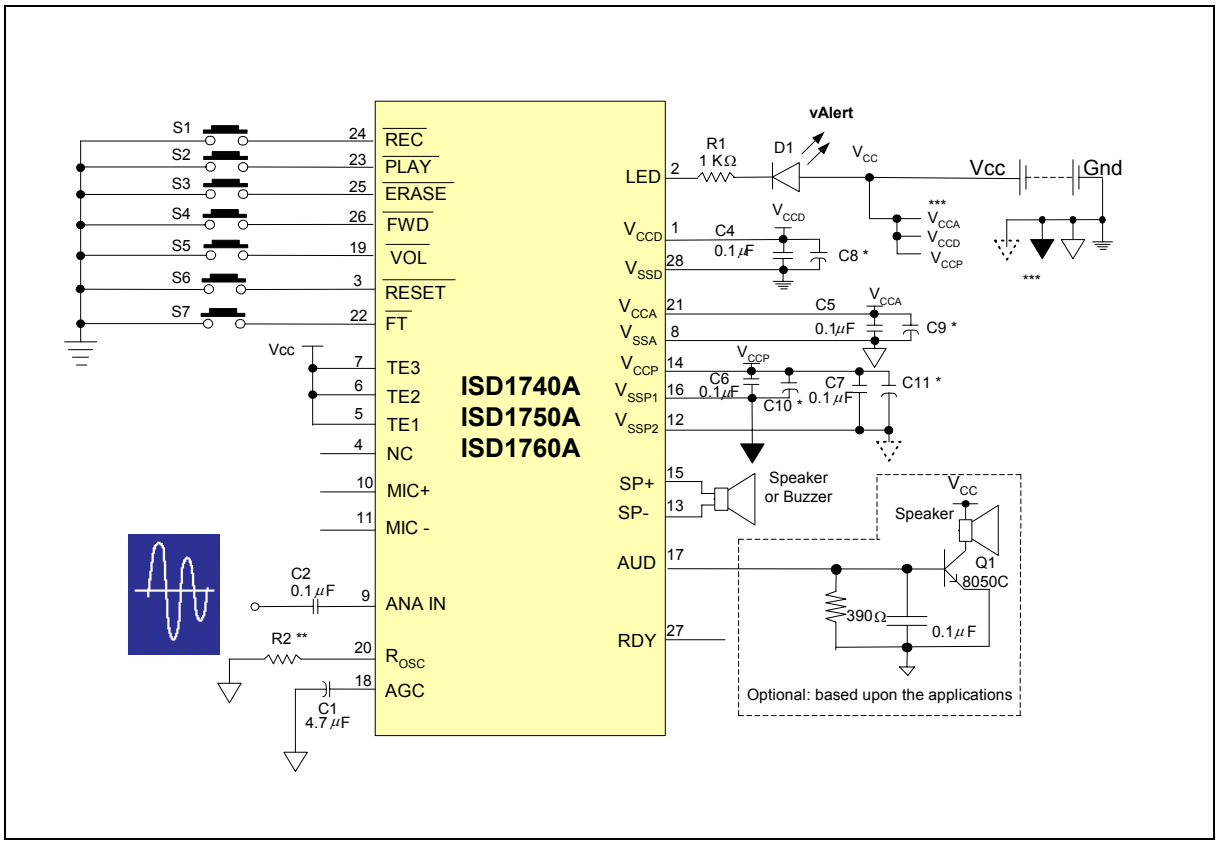
Example #2:



Recording via AnaIn input

Notes:

* These capacitors may be needed in order to optimize for the best voice quality, which is also dependent upon the layout of the PCB. Depending on system requirement, they can be 10 μF, 4.7 μF or other values. Please refer to ChipCorder Applications section or consult Winbond for layout advice.

** For Sampling Freq at 8 kHz, R2 = 80 KΩ

*** It is important to have a separate path for each ground and power back to the related terminal to minimize the noise. Also, the power supplies should be decoupled as close to the device as possible.

11.1 Good Audio Design Practices

To ensure the highest quality of voice reproduction, it is important to follow good audio design practices in layout and power supply decoupling. See Application Information or links below for details.

Good Audio Design Practices

http://www.winbond-usa.com/products/isd_products/chipcorder/applicationinfo/apin11.pdf

Single-Chip Board Layout Diagrams

http://www.winbond-usa.com/products/isd_products/chipcorder/applicationinfo/apin12.pdf

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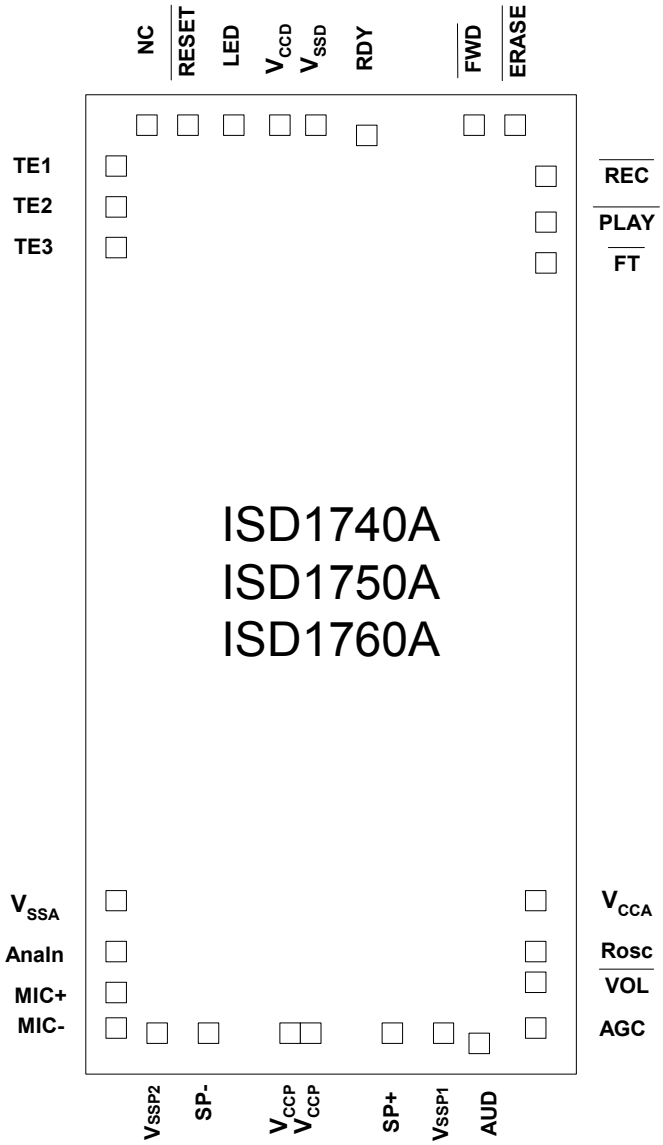
12 DIE PHYSICAL LAYOUT

12.1 ISD1740A/50A/60A[1][2]



Notes:

[1] The backside of the die is internally connected to V_{SSA}. It **MUST NOT** be connected to any other potential or damage may occur.

[2] Please contact the local Winbond Sales Offices or Representatives for details on (x,y) coordinates.

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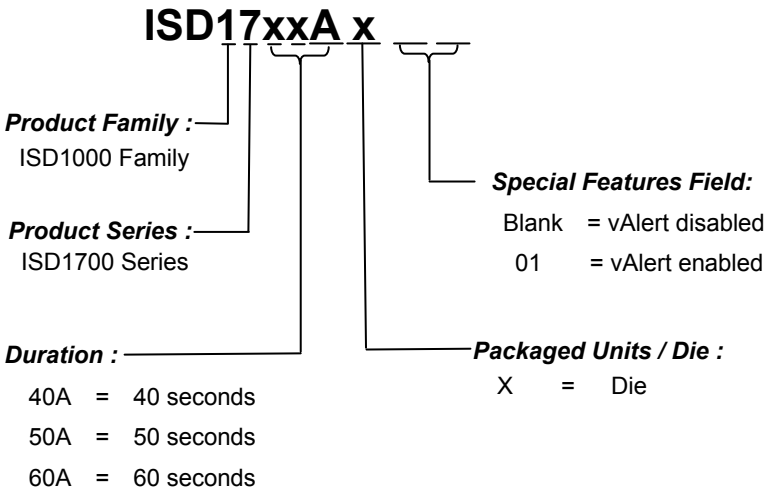
13 ORDERING INFORMATION

Product Number Descriptor Key



When ordering ISD1740A/ISD1750A/ISD1760A, please refer to the following valid ordering numbers, which are planned to be supported in volume for this product series. Please consult the local Winbond Sales Representatives for availability information.

Part Number	Ordering Number	
	No vAlert	*With* vAlert
ISD1740A	I1740AX	I1740AX01
ISD1750A	I1750AX	I1750AX01
ISD1760A	I1760AX	I1760AX01

For the latest product information, please access Winbond's worldwide web site at
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14 VERSION HISTORY

VERSION	DATE	DESCRIPTION
A0	March 2005	Initial version

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Headquarters
No. 4, Creation Rd. III
Science-Based Industrial Park,
Hsinchu, Taiwan
TEL: 886-3-5770066
FAX: 886-3-5665577
http://www.winbond.com.tw/

Winbond Electronics Corporation America
2727 North First Street, San Jose,
CA 95134, U.S.A.
TEL: 1-408-9436666
FAX: 1-408-5441797
http://www.winbond-usa.com/

Winbond Electronics (Shanghai) Ltd.
27F, 299 Yan An W. Rd. Shanghai,
200336 China
TEL: 86-21-62365999
FAX: 86-21-62356998

Taipei Office
9F, No. 480, Pueiguang Rd.
Neihu District
Taipei, 114 Taiwan
TEL: 886-2-81777168
FAX: 886-2-87153579

Winbond Electronics Corporation Japan
7F Daini-ueno BLDG. 3-7-18
Shinyokohama Kohokuku,
Yokohama, 222-0033
TEL: 81-45-4781881
FAX: 81-45-4781800

Winbond Electronics (H.K.) Ltd.
Unit 9-15, 22F, Millennium City,
No. 378 Kwun Tong Rd.,
Kowloon, Hong Kong
TEL: 852-27513100
FAX: 852-27552064

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