ISD ChipCorder®
ISD2361
DataSheet

For additional information or questions, please contact: Nuvoton Technology Corporation.

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1 GENERAL DESCRIPTION

ISD2361 is a playback only Digital ChipCorder® family product based on flash storage. The device features both internal and external flash support, digital de-compression, comprehensive memory management, integrated audio signal path with up to 3 channel concurrent playback and a Class D speaker driver capable of delivering 1W power output.

ISD2361 requires no external clock sources or components to operate. It can operate under SPI mode, or operate in stand-alone by detecting on level transition on its GPIO pins.

ISD2361YYI has 2Mbit non-volatile flash built-in, and can support external NOR serial flash up to 2G bit.

ISD2361SYI has 2Mbit non-volatile flash built-in only and cannot support external NOR serial flash.

2 FEATURES

- Performance Enhancements
  - Support external flash **(ISD2361YYI)**
  - GPIO trigger reliability
  - Better DPWM output SNR
  - Audio output power efficiency
- Duration
  - 64 seconds based on 8kHz/4bit ADPCM in 2Mbit of internal flash storage
  - **ISD2361YYI with external memory** – total addressable space is 2Gbit (1092minutes)
- Audio Management
  - Store pre-recorded audio (Voice Prompts) using high quality digital compression
  - Use simple index-based commands for playback – no address needed
  - Execute pre-programmed macro scripts (Voice Macros) designed to control the configuration of the device and playback Voice Prompts sequences
- Path and Playback Control
  - Audio streaming for up to 3 channels can be mixed and played back concurrently
  - Each channel has independent counter which enables user micro-management on VM execution
  - Mask Jump for branch execution; based on internal register or external GPIO pin
- Chip Control
  - Serial Peripheral Interface (SPI) for microprocessor control and programming
  - Standalone control when customized Voice Macro scripts are assigned to GPIO trigger pins
- Sample Rates
  - 8 sampling frequencies available: 4, 5.3, 6.4, 8, 10.67, 12.8, 16 and 32 kHz
  - Each Voice Prompt can have its own optimal sample rate
- Compression Algorithms
  - µ-Law: 6, 7 or 8 bits per sample
  - Differential µ-Law: 6, 7 or 8 bits per sample
  - PCM: 8, 10, 12 or 16 bits per sample
  - Enhanced ADPCM: 2, 3, 4 or 5 bits per sample
  - Variable bit-rate optimized compression allows best possible compression given a metric of Signal-to-Noise Ratios (SNR) and background noise levels
- Clock Source: Internal oscillator, ±1% deviation at room temperature

- Output
  - PWM: Class D speaker driver to direct drive speaker or buzzer
  - Delivers:
    - 4Ω load: 440mW@3.3V; 1.2W@5V; 1.5W@5.5V
    - 8Ω load: 330mW@3.3V; 800mW@5V; 1W@5.5V
- I/O
  - Total 10 General Purpose I/O (GPIO) pins
  - 6 out of the 10 GPIO pins multiplexed with SPI interface and capable of trigger play
  - 4 GPIO pins available when no external flash connected
  - SPI interface: MISO, MOSI, SCLK, SSB for commands and digital audio data
- Internal Flash Storage
  - Built-in 2Mbit of storage
  - Fast programming time (20µs/byte)
  - Erase sector size 512-byte, sector erase time 5ms
  - Integrated memory checksum calculation for fast verification
  - Endurance >100K cycles; retention >10 years
- External Flash Storage
  - **ISD2361YYI can support external flash**
  - **ISD2361SYI cannot support external flash**
  - Supports NOR serial flash command set (ISD2361YYI)
  - Addressable space up to 2Gbit (ISD2361YYI)
- Operating Voltage: 2.4V-5.5V
- Packages:
  - QFN-32 / SOP-16
  - Package is Halogen-free, RoHS-compliant and TSCA-compliant
- Temperature Options:
  - Industrial: -40°C to 105°C

3 BLOCK DIAGRAM

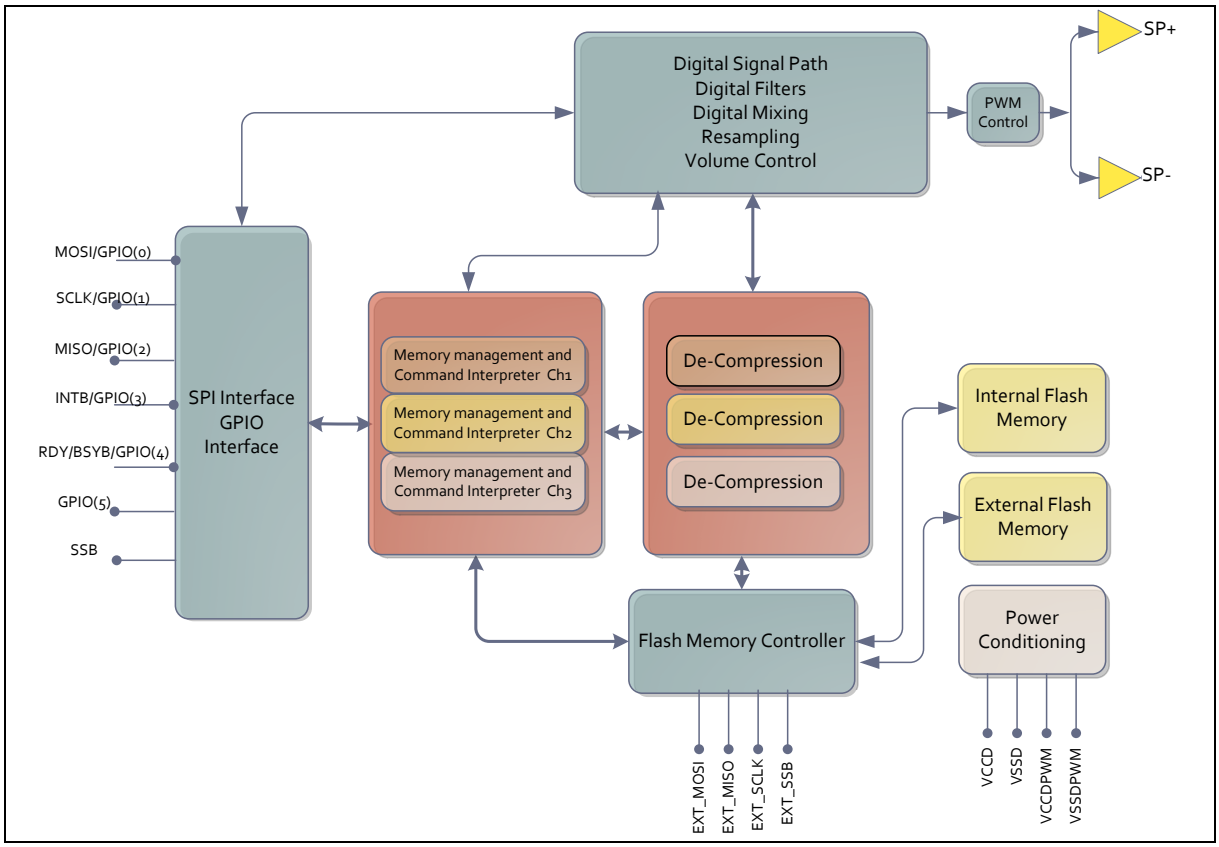


Figure 3-1 ISD2361YYI Block Diagram

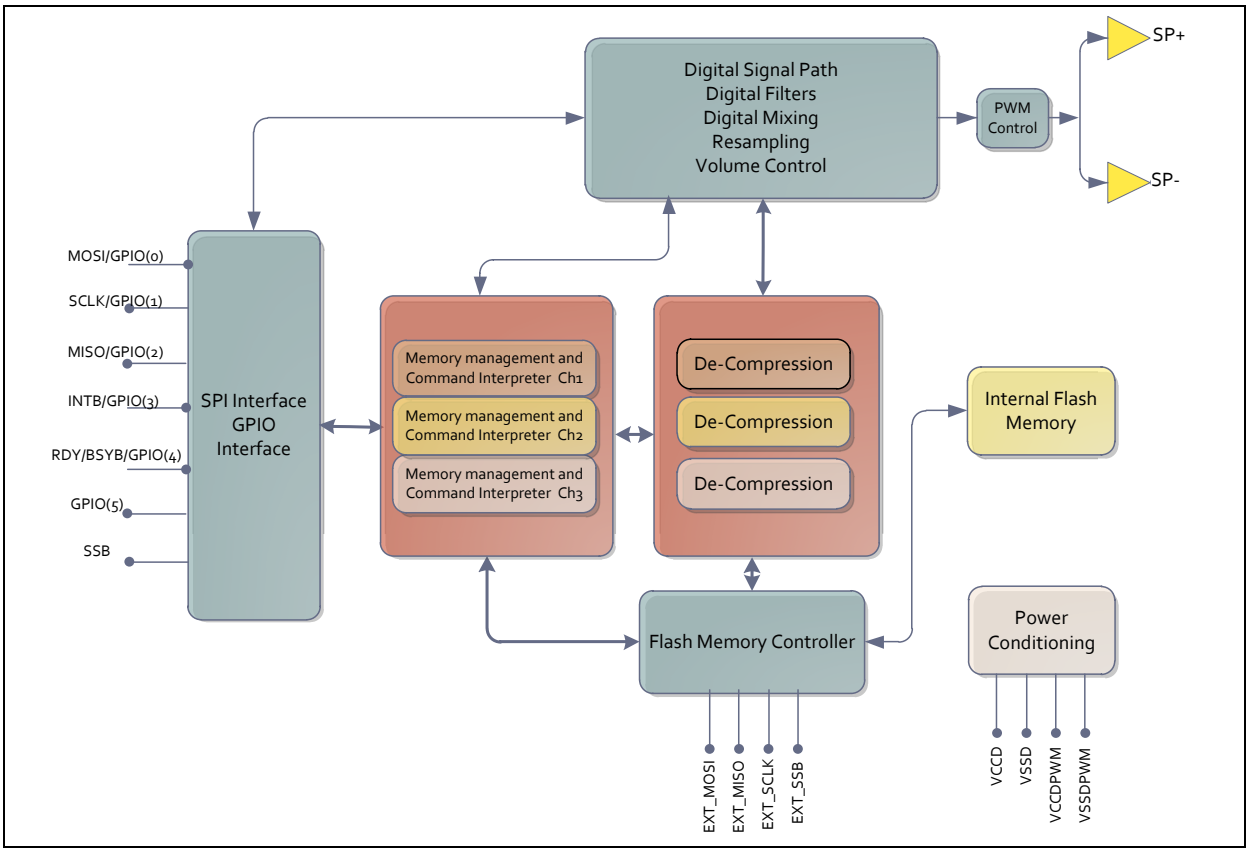


Figure 3-2 ISD2361SYI Block Diagram

4 PINOUT CONFIGURATION

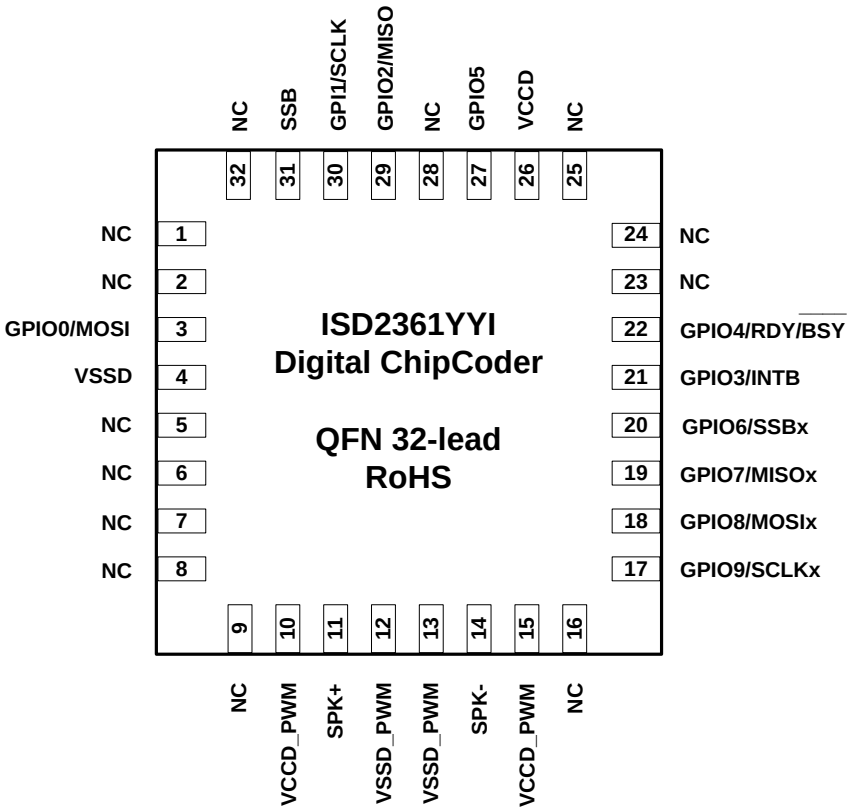


Figure 4-1 ISD2361 QFN 32-Lead Package

Note: The large center exposed pad under the QFN 32-Lead package should be connected to VSSD on the board to ensure good heat dissipation and mechanical stability.

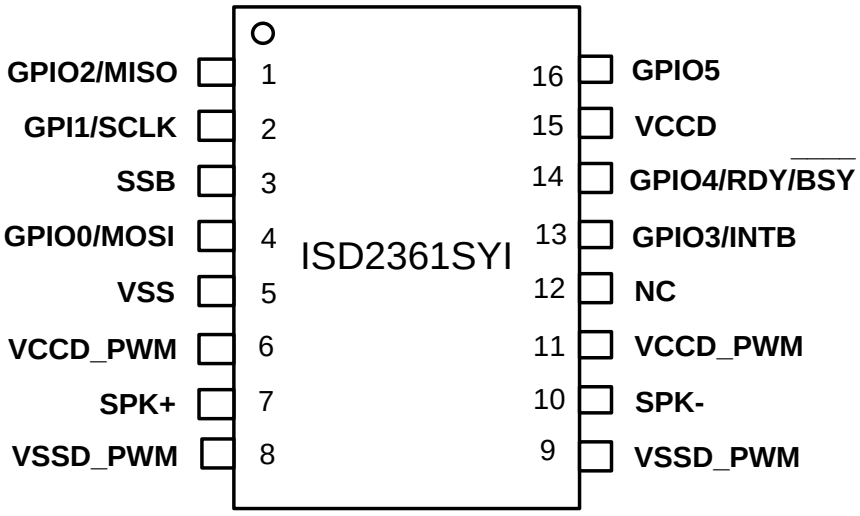


Figure 4-2 ISD2361 SOP 16-Lead 300 mil Package

5 PIN DESCRIPTION

QFN Pin #	SOP Pin #	Pin Name	I/O	Function
1		NC		This pin should be left unconnected.
2		NC		This pin should be left unconnected.
3	4	GPIO0/MOSI	I/O	Master-Out-Slave-In. Serial input to the ISD2361 from the host. Can be configured as a general purpose I/O pin.
4	5	VSSD		Digital Ground.
5		NC		This pin should be left unconnected.
6		NC		This pin should be left unconnected.
7		NC		This pin should be left unconnected.
8		NC		This pin should be left unconnected.
9		NC		This pin should be left unconnected.
10	6	VCCD_PWM	I	Digital Power for the PWM Driver.
11	7	SPK+	O	PWM driver positive output. This SPK+ output, together with SPK- pin, provide a differential output to drive 8Ω speaker or buzzer. During power down this pin is in tristate.
12	8	VSSD_PWM	I	Digital Ground for the PWM Driver.
13	9	VSSD_PWM	I	Digital Ground for the PWM Driver.
14	10	SPK-	O	PWM driver negative output. This SPK- output, together with SPK+ pin, provides a differential output to drive 8Ω speaker or buzzer. During power down this pin is tristate.
15	11	VCCD_PWM	I	Digital Power for the PWM Driver.
16		NC		This pin should be left unconnected.
17		GPIO9/SCLKx	I/O	- External SPI interface SCLK pin if external flash is connected. I2361 is the master. - Can be configured as general purpose I/O pin if external flash is not connected.
18		GPIO8/MOSIx	I/O	- External SPI interface MOSI (DOUT) pin if external flash is connected. I2361 is the master. - Can be configured as general purpose I/O pin if external flash is not connected.
19		GPIO7/MISOx	I/O	- External SPI interface MISO (DIN) pin if external flash is connected. I2361 is the master. - Can be configured as a general purpose I/O pin if external flash is not connected.
20		GPIO6/SSBx	I/O	- External SPI interface Slave Select pin if external flash is connected. I2361 is the master. - Can be configured as general purpose I/O pin if external flash is not connected.
21	13	GPIO3/INTB	I/O	Active low interrupt request pin. This pin is an open-drain output.

QFN Pin #	SOP Pin #	Pin Name	I/O	Function
				Can be configured as a general purpose I/O pin.
22	14	GPIO4/RDY/$\overline{BSY}$	I/O	An output pin to report the status of data transfer on the SPI interface. “High” indicates that ISD2361 is ready to accept new SPI commands or data. Can be configured as a general purpose I/O pin.
23		NC		This pin should be left unconnected.
24		NC		This pin should be left unconnected.
25		NC		This pin should be left unconnected.
26	15	VCCD	I	Digital Power.
27	16	GPIO5	I/O	Can be configured as a general purpose I/O pin.
28		NC		This pin should be left unconnected.
29	1	GPIO2/MISO	I/O	Master-In-Slave-Out. Serial output from the ISD2361 to the host. This pin is in tristate when SSB=1. Can be configured as a general purpose I/O pin.
30	2	GPI1/SCLK	I	Serial Clock input to the ISD2361 from the host. Can be configured as a general purpose input-only pin.
31	3	SSB	I	Slave Select input to the ISD2361 from the host. When SSB is low device is selected and responds to commands on the SPI interface. When asserted, GPIO0/1/2 automatically configure to MOSI/SCLK and MISO respectively. SSB has an internal pull-up to VCCD.
32		NC		This pin should be left unconnected.

*note: for QFN-32 package center pad underneath should connect to VSSD.

6 DEVICE OPERATION

6.1 APPLICATION DEVELOPMENT FLOW

Typical steps to build an ISD2361 application:

- Create an application image
  - Launch ISD-VPE2361, create a project.
  - Import 16bit PCM wave files into the project.
  - Edit project if needed. Compile to generate an application image.
- Program the application image into system memory
  - only internal flash if image size is less or equal to 2Mbit.
  - or both internal and external flash when the image size exceeds 2Mbit.
- Audio Playback
  - By sending SPI command,
  - Or by GPIO trigger.

6.2 AUDIO STORAGE

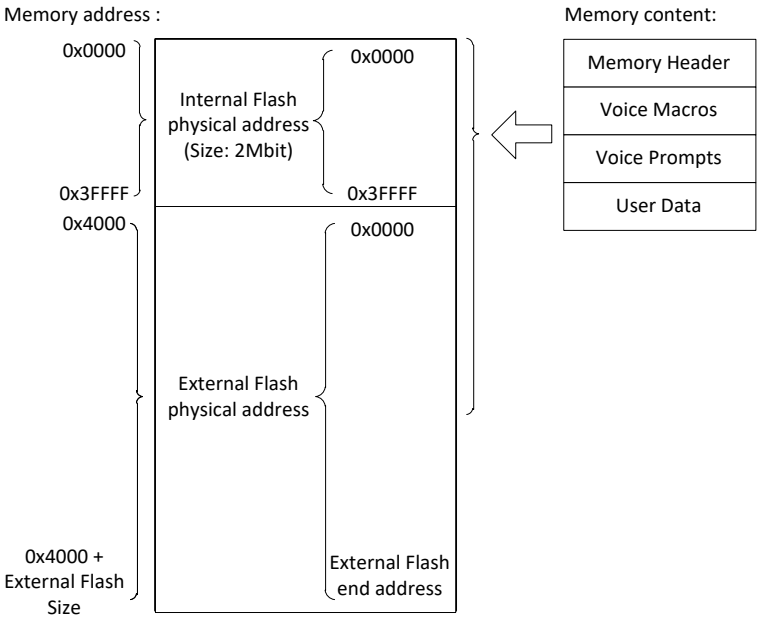


Figure 6-1 ISD2361 Memory Organization

Depends on the application requirement, user can choose not to populate external flash if the application image size is less than or equal to 2Mbit.

When external flash is presented, the internal and external flash together construct the system memory addressing space. The ISD2361 continuously addresses the memory into external flash starting once the address is greater than 0x3FFFF; see Figure 6-1.

User can use SPI Digital Read/Write command to access internal flash. And user can use OP_EXT opcode, followed by NOR serial flash SPI command to operate on external flash.

Memory content consists of the following:

- **Memory Header**: mainly consists of index table for Voice Macros and Voice Prompts, and also contains project configuration info.
- **Voice Macros**: data section for command scripts.
- **Voice Prompts**: audio data for all the sound effects.
- **User Data**: optional user reserved section for application data.

6.3 AUDIO ELEMENTS

An ISD2361 VPE project mainly consists of two basic audio elements, Voice Prompts and Voice Macros.

6.3.1 Voice Prompt

Voice Prompt, or VP in short, is the basic audio clip which can be played in ISD2316 system. VP is generated after a 16bit PCM wave file is imported into a VPE project, and after re-sampled and compressed in that project.

Each VP is assigned with an index. VP index and its audio data are linked into application image during VPE project compilation.

6.3.2 Voice Macro

Voice Macro, or VM in short, is audio command script which allows device to do a sequence of operations at once, for example configuring multiple registers and play one more multiple VPs afterwards.

User can execute a VM by either send SPI command or by GPIO trigger. A VM can be invoked by other VM as well.

6.4 DEVICE OPERATION

6.4.1 Operation Mode

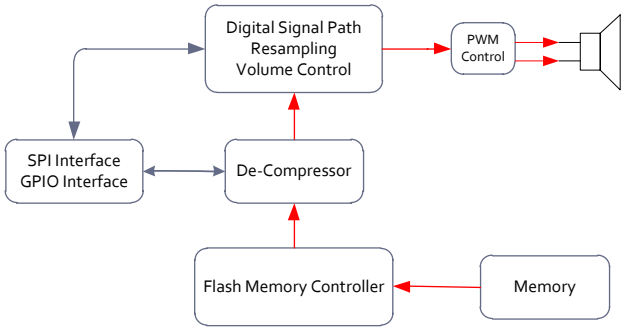
The ISD2361 device operates under SPI mode or GPIO trigger mode.

- The ISD2361 SPI interface supports SPI mode 3.
- GPIO trigger feature allows standalone application. GPIO0-5 six pins can be configured as GPIO trigger pins.

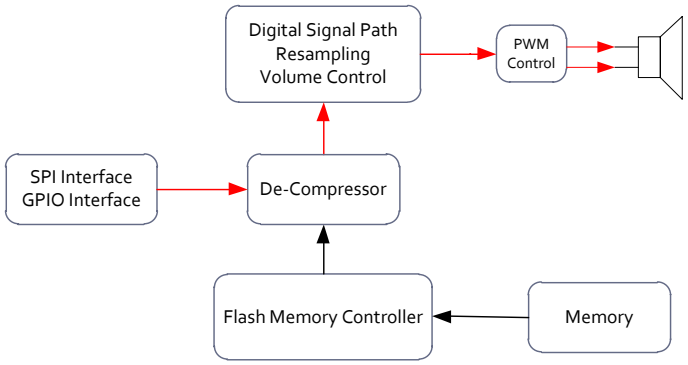
6.4.2 Signal Path

Two playback paths are supported: Playback from Memory and SPI-Decode. Also, memory content can be played back to SPI output, i.e. receiving de-compressed 16 bit PCM audio data from memory through SPI interface.

- Playback from Memory: configure register 0x02 to setup the simple playback path.



- SPI Decode: configure register 0x02 and use SPI_SND_DEC command to directly playback from SPI interface. The streaming data should be pre-compressed data by VPE.



6.4.3 Memory Protection

The ISD2361 device supports Read protection, Write protection and Chip_Erase protection. Combined with Protection Memory Pointer, flexible protection scheme can be achieved.

6.4.4 3-byte vs 4-byte Addressing Mode

The ISD2361 device supports both 3-byte and 4-byte addressing mode. When external flash size is 256Mbit or up, 4-byte addressing mode should be used otherwise the addressing space is limited to within 128Mbit.

Addressing mode can be chosen by SPI command or in standalone mode by POI VM – Power On Initialization Voice Macro.

In 4-Byte mode, the addressing space is up to 2Gbit.

6.4.5 Channel Control

The ISD2361 device integrates 3 channels each having its own memory management and de-compressor. Channel mixing can be achieved in SPI mode or trigger mode.

6.4.6 Flexible VM Control

Enriched Voice Macro commands support:

- Play Silence with configurable silence duration.
- VM command execution branch. The execution can be branched to;
  - o other VM;
  - o or an absolute address, e.g. a labelled address;
- Conditional branch. The VM execution can be branched when
  - o device is busy
  - o or a GPIO level condition is detected.
- Time Counter. Thus made possible the execution delay/pause fit for application needs.

6.4.7 Other Miscellaneous Functions

- Volume control: volume control can be done either by writing into register 0x03, or by GPIO trigger. 256 volume steps are available for register 0x03 control, and 8 volume steps for GPIO trigger volume control.
- Over Heat prevention: temperature alarm can be set at configurable temperature threshold. The ISD2361 device operates following an inertia pattern, that is the device will stop

playback when temperature exceeds the threshold, and will resume playback when temperature dropped to a certain level below threshold.

- Fast De-bounce: GPIO trigger pin de-bounce time can be set as either normal button press de-bounce or fast de-bounce. Fast de-bounce is especially suitable for MCU GPIO control, thus made possible one pin-control for multiple-message random playback.
- Internal memory hardware checksum.

7 ELECTRICAL CHARACTERISTICS

7.1 ABSOLUTE MAXIMUM RATINGS

DESCRIPTION	SYMBOL	CONDITION	MIN	MAX	UNITS
DC Power Supply	V_{CCD}	$V_{CCD} – V_{SSD}$	-0.3	+6.0	V
	V_{CCPWM}	$V_{CCPWM} – V_{SSPWM}$	-0.3	+6.0	V
Digital Input Voltage	DV_{IN}	DVIN - VSSD	$V_{SSD} – 0.3$	$V_{CCD} + 0.3$	V
Junction Temperature	TJ	-	-40	+125	°C
Storage Temperature	Tst	-	-65	+150	°C

CAUTION: Do not operate at or near the maximum ratings listed for extended period of time. Exposure to such conditions may adversely influence product reliability and result in failures not covered by warranty. These devices are sensitive to electrostatic discharge; follow proper IC Handling Procedures.

7.2 OPERATING CONDITIONS

OPERATING CONDITIONS (INDUSTRIAL PACKAGED PARTS)

CONDITIONS	VALUES
Operating temperature range (Case temperature)	-40°C to +105°C[1]
Supply voltage (V_{DD}) [2]	+2.4V to +5.5V
Ground voltage (V_{SS}) [3]	0V
Digital input voltage (DV_{IN})	0V to 5.5V
Voltage applied to any pins	(V_{SS} –0.3V) to (V_{DD} +0.3V)

NOTES: [1] TBD: maximum operating temperature to be further characterized.

[2] $V_{DD} = V_{CCD} = V_{CCPWM}$

[3] $V_{SS} = V_{SSD} = V_{SSPWM}$

7.3 AC PARAMETERS

7.3.1 Internal Oscillator

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	CONDITIONS
Sample rate with Internal Oscillator	Fsmax	-1%	32kHz	+1%	kHz	Vdd = 3V. At room temperature

7.3.2 Speaker Outputs

PARAMETER	SYMBOL	MIN	TYP[1]	MAX	UNITS	CONDITION
Output Power	P_{OUT_SPK}			440	mW	@ 3.3V, Load 4Ω [1][2]
				1.2	W	@ 5.0V, Load 4Ω [1][2]
				1.5	W	@ 5.5V, Load 4Ω [1][2]
				330	mW	@ 3.3V, Load 8Ω [1]
				800	mW	@ 5.0V, Load 8Ω [1]
				1.0	W	@ 5.5V, Load 8Ω [1]
THD, Memory to SPK+/SPK-	THD %		<0.1%			w/o load [1] [3]
Minimum Load Impedance	$R_{L(SPK)}$	4	8		Ω	

Notes: [1] T_A=25°C , 0dB FS, 12-bit PCM, 8K SR.
[2] Reg0x0B is configured as 0x5C.
[2] All measurements are C-message weighted.

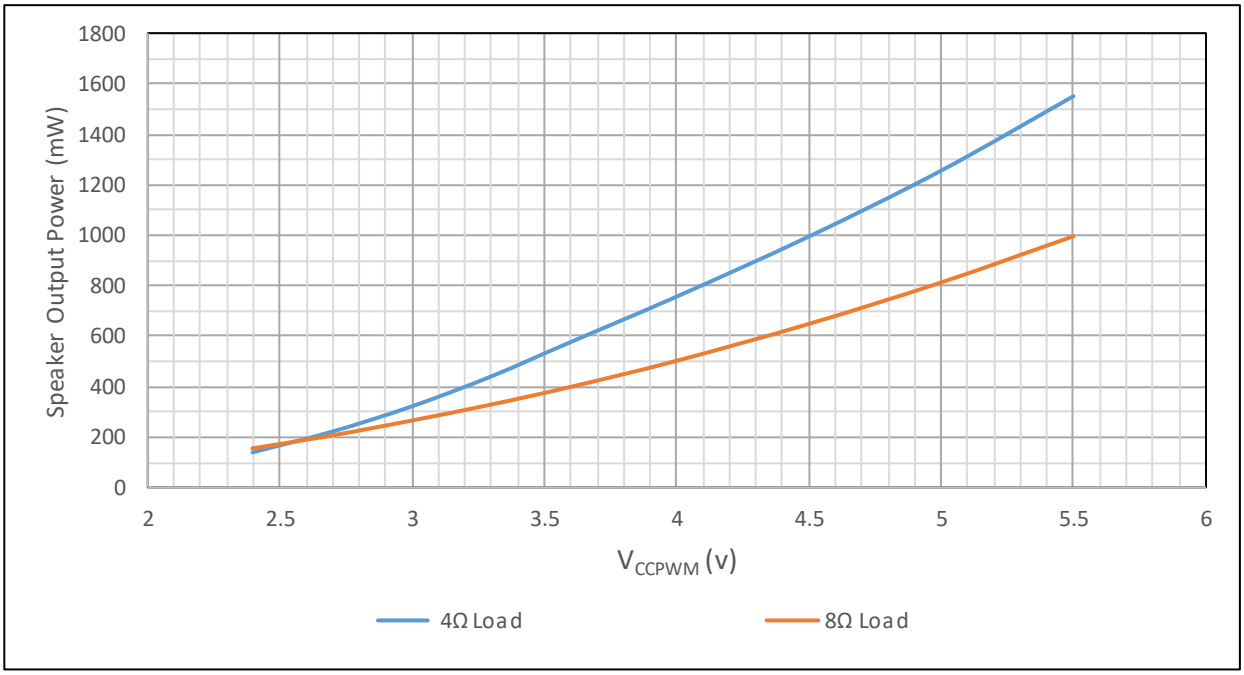


Figure 7-1 Speaker output power

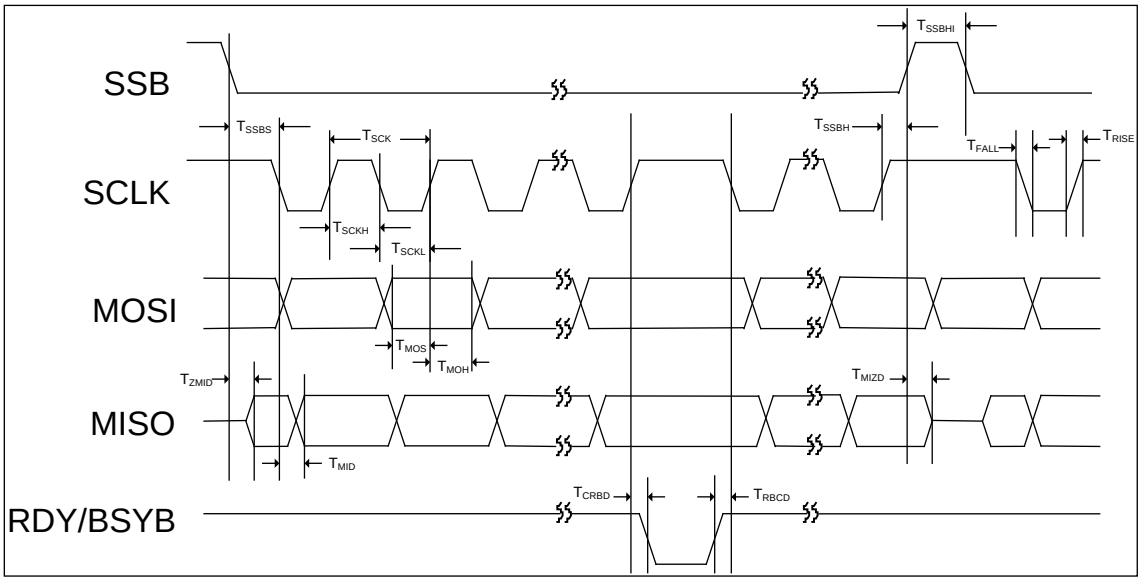
7.4 DC PARAMETERS

PARAMETER	SYMBOL	MIN	TYP [1]	MAX	UNITS	CONDITIONS
Supply Voltage	V_{DD}	2.4		5.5	V	
Input Low Voltage	V_{IL}	V_{SS}-0.3		0.3xV_{DD}	V	
Input High Voltage	V_{IH}	0.7xV_{DD}		V_{DD}	V	
Output Low Voltage	V_{OL}	V_{SS}-0.3		0.4	V	I_{OL} = 1mA
Output High Voltage	V_{OH}	2.4			V	I_{OH} = -1mA
Pull-up Resistance	R_{PU}		50		kΩ	
Pull-down Resistance	R_{PD}		10		kΩ	
INTB Output Low Voltage	V_{OH1}			0.4	V	
Maximum Operating Current	I_{DD_MAX}		8			V_{DD}= 5.5V, No load, Sampling freq. 8 kHz, all blocks enabled.
Playback Current	$I_{DD\_Playback}$		4		mA	No Load, V_{DD}=3V
Standby Current	I_{SB}		2.5	10	µA	V_{DD}= 5.5V
Input Leakage Current	I_{IL}			±10	µA	Force V_{DD}

Notes: [1] Conditions V_{DD}=3V, T_A=25°C unless otherwise stated

[2] To calculate total current, add load dissipation into application specific load.

7.5 SPI TIMING



SYMBOL	DESCRIPTION	MIN	TYP	MAX	UNIT
T_{SCK}	SCLK Cycle Time	60	---	---	ns
T_{SCKH}	SCLK High Pulse Width	25	---	---	ns
T_{SCKL}	SCLK Low Pulse Width	25	---	---	ns
T_{RISE}	Rise Time for All Digital Signals	---	---	10	ns
T_{FALL}	Fall Time for All Digital Signals	---	---	10	ns
T_{SSBS}	SSB Falling Edge to 1st SCLK Falling Edge Setup Time	30	---	---	ns
T_{SSBH}	Last SCLK Rising Edge to SSB Rising Edge Hold Time	30ns	---	50us	---
T_{SSBHI}	SSB High Time between SSB Lows	20	---	---	ns
T_{MOS}	MOSI to SCLK Rising Edge Setup Time	15	---	---	ns
T_{MOH}	SCLK Rising Edge to MOSI Hold Time	15	---	---	ns
T_{ZMID}	Delay Time from SSB Falling Edge to MISO Active	---	---	25	ns
T_{MIZD}	Delay Time from SSB Rising Edge to MISO Tri-state	---	---	12	ns
T_{MID}	Delay Time from SCLK Falling Edge to MISO	---	---	25	ns
T_{CRBD}	Delay Time: SCLK Rising Edge to RDY/BSYB Falling Edge	---	---	12	ns
T_{RBCD}	Delay Time: RDY/BSYB Rising Edge to SCLK Falling Edge	0	---	---	ns

8 APPLICATION DIAGRAM

The following application examples are provided for reference only. Nuvoton makes no representation or warranty that such applications are suitable for the use specified. Each design must be optimized in its own system for the best performance in voice quality, current consumption, functionality etc.

The ISD2361 can be controlled and programmed through a Serial Peripheral Interface (SPI) or can operate in standalone mode by triggers applied to the device's six General Purpose Input/Output (GPIO) pins.

8.1 SPI MODE APPLICATION UNDER MCU CONTROL

The ISD2361 has two SPI interfaces. One SPI interface is for the communication with host microcontroller. The other SPI interface is for external flash control.

For the SPI interface with host microcontroller, a RDY/BSYB signal (pin) is available for digital read/write data flow control.

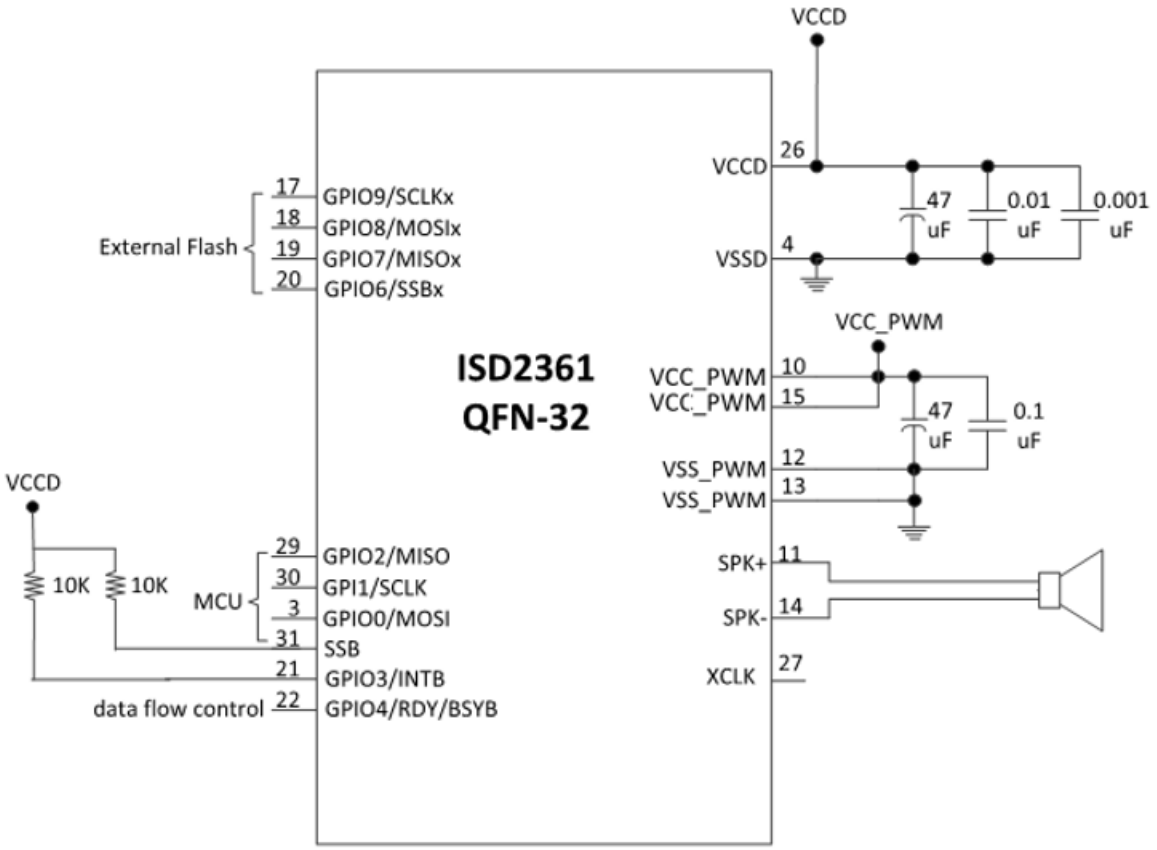


Figure 8-1 SPI Mode Application under MCU Control

8.2 GPIO Trigger Standalone Application

The ISD2361 can operate in standalone mode by triggers applied to the device's six General Purpose Input/output (GPIO) pins. Once Trigger mode is activated, a button press event will trigger the associated VM to run.

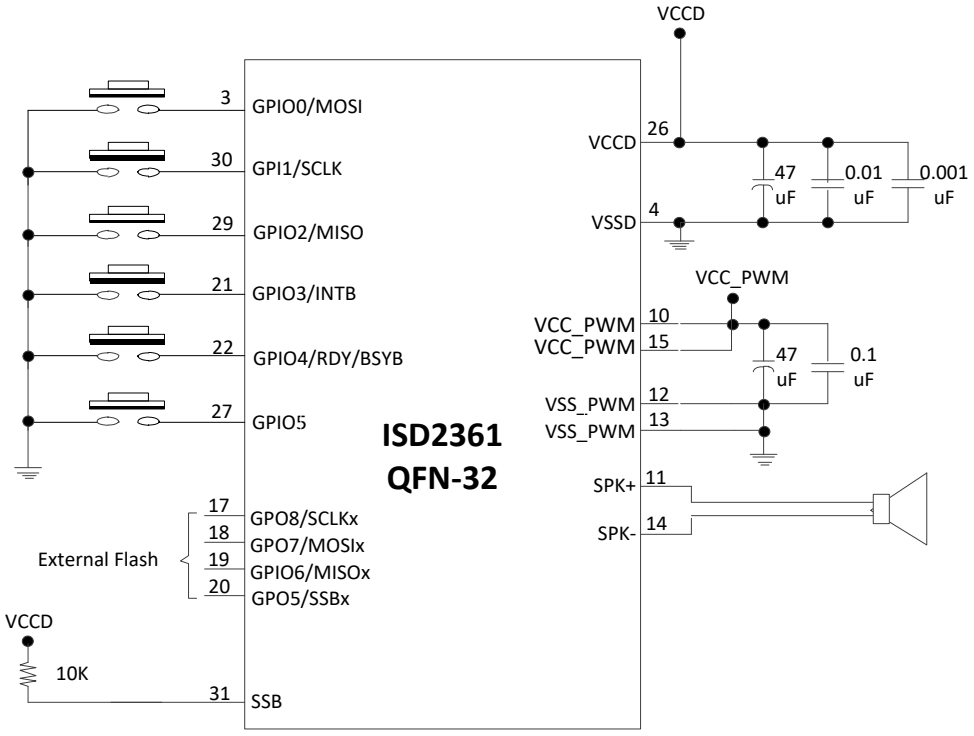
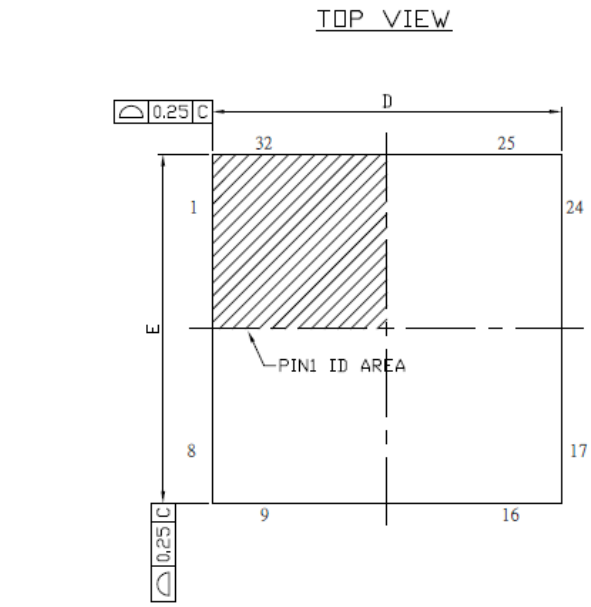


Figure 8-2 GPIO Trigger Standalone Application

9 PACKAGE SPECIFICATION

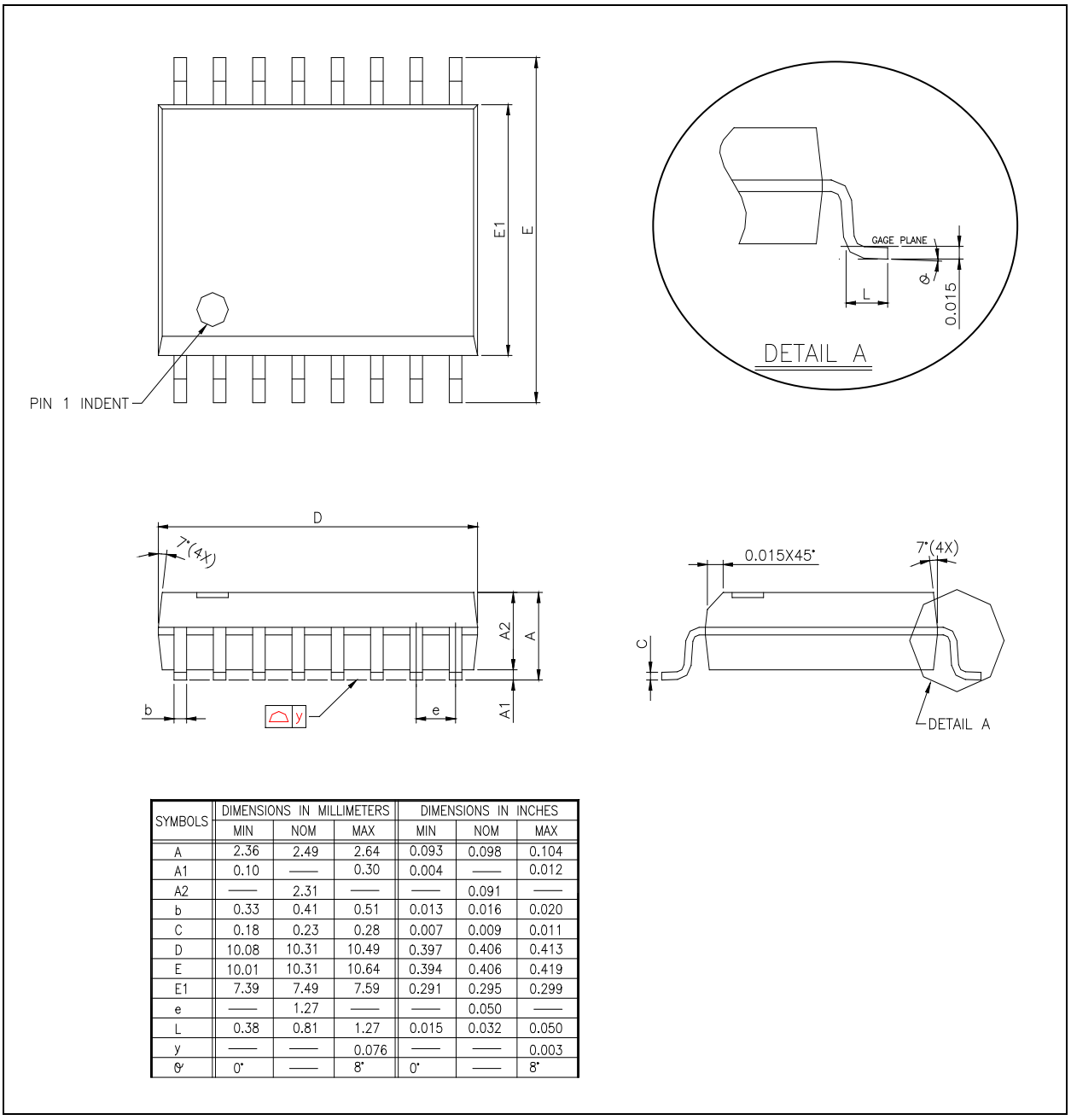
The ISD2361 is available in two kinds of packages: QFN-32 and SOP-16, as shown in Figure 9-1 and Figure 9-2.

QFN 32L 5X5 mm², Thickness 0.8 mm(Max), Pitch 0.5 mm (Saw Type) TICP EP SIZE 3.5X3.5 mm²



SYMBOL	DIMENSION (MM)			DIMENSION (MIL)		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	0.70	0.75	0.80	27.5	29.5	31.5
A1	0	0.02	0.05	0	0.8	2.0
A3	0.203 REF			8 REF		
b	0.20	0.25	0.30	7.8	9.8	11.8
D	4.90	5.00	5.10	192.9	196.8	200.7
D2	3.40	3.50	3.60	133.8	137.8	141.7
E	4.90	5.00	5.10	192.9	196.8	200.7
E2	3.40	3.50	3.60	133.8	137.8	141.7
e	0.50 BSC			19.7 BSC		
L	0.35	0.40	0.45	13.7	15.7	17.7

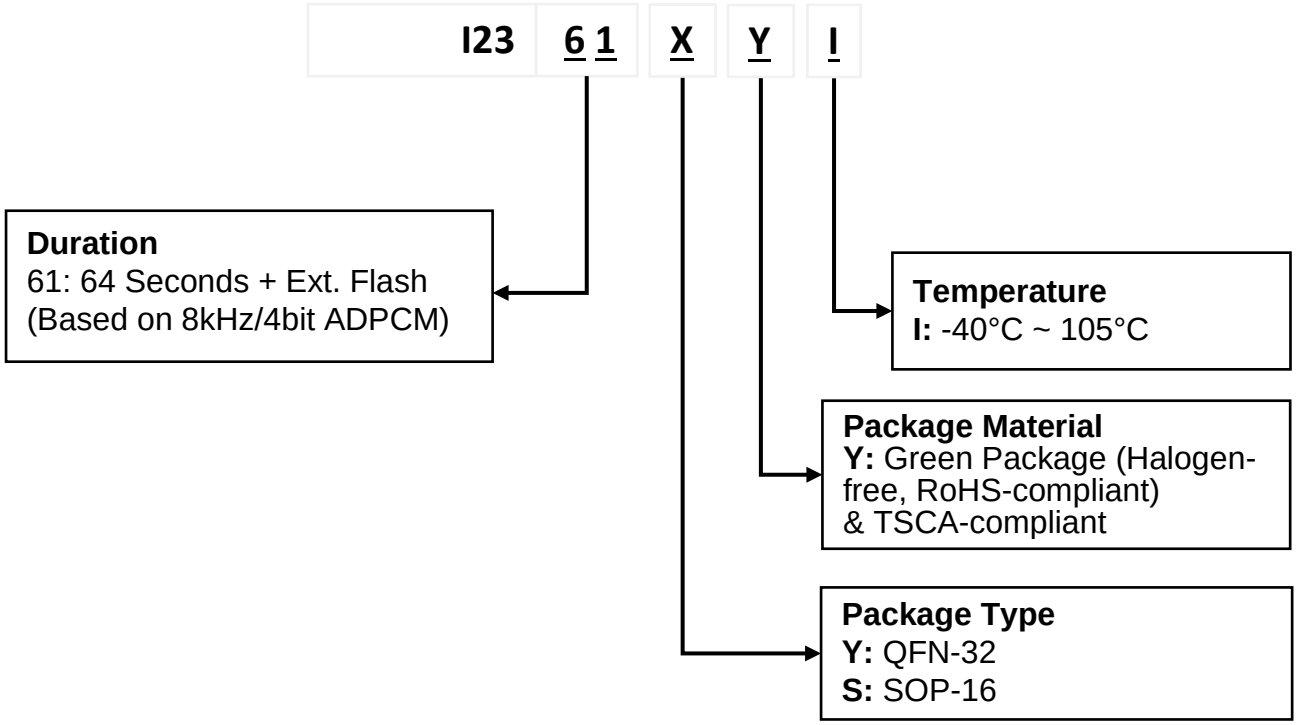
Figure 9-1 QFN 32-Lead Package



SYMBOLS	DIMENSIONS IN MILLIMETERS			DIMENSIONS IN INCHES		
	MIN	NOM	MAX	MIN	NOM	MAX
A	2.36	2.49	2.64	0.093	0.098	0.104
A1	0.10	——	0.30	0.004	——	0.012
A2	——	2.31	——	——	0.091	——
b	0.33	0.41	0.51	0.013	0.016	0.020
C	0.18	0.23	0.28	0.007	0.009	0.011
D	10.08	10.31	10.49	0.397	0.406	0.413
E	10.01	10.31	10.64	0.394	0.406	0.419
E1	7.39	7.49	7.59	0.291	0.295	0.299
e	——	1.27	——	——	0.050	——
L	0.38	0.81	1.27	0.015	0.032	0.050
y	——	——	0.076	——	——	0.003
θ°	0°	——	8°	0°	——	8°

Figure 9-2 SOP 16-Lead Package

10 ORDERING INFORMATION



Package Number	Part Number	Ordering Number	Duration	Package	Temperature	Notes
ISD2361SYI	ISD2361SYI	I2361SYI	64sec	SOP-16	-40°C ~ 105°C	
ISD2361SYI TR	ISD2361SYI	I2361SYI	64sec	SOP-16 Tape & Reel	-40°C ~ 105°C	
ISD2361YYI	ISD2361YYI	I2361YYI	64sec + Ext. Flash	QFN-32	-40°C ~ 105°C	
ISD2361YYI TR	ISD2361YYI	I2361YYI	64sec + Ext. Flash	QFN-32 Tape & Reel	-40°C ~ 105°C	

11 REVISION HISTORY

REVISION	DATE	DESCRIPTION
1.0	Nov 11, 2021	Initial release
1.1	Apr 6, 2021	Simplified description
1.2	May 6, 2021	Update output power data
1.3	Feb 28, 2022	Update ISD2361YYI and ISD2361SYI difference
1.4	Mar 28, 2022	Update ordering package information
1.5	May 18, 2022	Update feature description Update GPIO[9:6] description
1.6	Sep 20, 2022	Update SPI parameters
1.7	Feb 1, 2023	Update Halogen-free, RoHS-compliant and TSCA-compliant description

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