ISD91500

Datasheet

Multi-Algorithm Voice Processor

With Headphone Driver

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1 GENERAL DESCRIPTION

ISD91500 series is an audio system-on-chip (SoC) integrated with high-quality audio features optimized for low power, audio record and playback.

ISD91500 can run up to 49 MHz with embedded ARM® Cortex®-M0 32-bit microcontroller core and 64K-byte non-volatile flash memory which has additional 6KB boot loader flash and 20K-byte embedded SRAM. The audio features include microphone input ADC and stereo DAC with headphone ouput driver. ISD91500 also comes with a wide variety of peripherals, such as Timers, Watchdog Timer (WDT), Peripheral Direct Memory Access (PDMA), Serial interfaces (UART, SPI, I2C and I2S), USB, PWM modulators, GPIO, SDADC, SARADC, DAC and Low Voltage Detector.

ISD91500 series supports a rich set of power saving modes including Deep Power Down (DPD) mode drawing less than 2uA. A micro-power 10KHz oscillator enables the device to periodically wake up from deep power down to check other events.

Typical applications include USB headsets, Gaming controllers, USB/I2S audio bridge and voice communication systems.

2 FEATURES

- **Core**
  - ARM® Cortex®-M0 core running up to 49 MHz
  - One 24-bit system tick timer for operating system support
  - Single-cycle 32-bit hardware multiplier
  - NVIC (Nested Vetctor Interrupt Controller) for the interrupt inputs, each with 4-levels of priority
  - Serial Wire Debug (SWD) supports with 2 watchpoints/4 breakpoints
- **Power Management**
  - Wide operating voltage range from 1.7V to 3.6V (VCCD voltage level equal to VCCA)
  - Power Management Unit (PMU) providing different levels of power control
  - Deep Power Down (DPD) mode with specific register retention for lowest power state (typically <2uA)
  - Wake-up from DPD via LIRC timed operation
  - Standby Power Down(STOP) mode with RAM retention for lowest power state (typically <15uA)
  - Wake-up from STOP via any GPIOs or WDT interrupts
  - Fast wake-up mechanism with 20us CPU running instruction
- **Flash EPROM Memory**
  - 64KB Flash EPROM for program code and data storage
  - Additional 6KB of flash configured as boot sector for ISP loader
  - Support ISP and ICP code update
  - 512B page erase for embedded flash
  - Configurable boundary to delineate code and data flash
  - Support 2-wire In-circuit Programming (ICP) update from SWD ICE interface
- **SRAM Memory**
  - 20KB embedded SRAM
- **Clock Control**
  - 48 MHz/49.152MHz configurable internal high speed RC oscillator (HIRC) for system operation
  - 10 kHz internal low speed RC oscillator (LIRC) for Watchdog Timer and wake-up operation
  - 4~24.576 MHz external high speed crystal oscillator (HXT) for precise timing operation
  - One PLL sourced from HIRC, HXT, and XCLK input
  - Clock Doubler(XCLK) minimum input frequency 512KHz
  - Clock failure detection for high speed external crystal oscillator

- **GPIO**
  - Up to 50 GPIOs individually configurable as three I/O modes
    - Input with pull-up option
    - Push-Pull output
    - Open-Drain output
  - Schmitt trigger and slew rate selectable by quad
  - GPIO configureable as interrupt/wake-up source with edge/level setting
  - GPA group power level follow VCCD level and GPB/GPC/GPD group follow VCCPST level
  - Support 5V tolerance
- **Companding**
  - Compatible with CCITT G.726 and G.726 AnnexA
  - 8-bit PCM or 16-bit linear interfacing
  - 4 kinds ADPCM rates : 40, 32, 24, 16 kbps
  - 8-bit PCM u-law or A-law
  - Support full-duplex for encoding and decoding with different sampling rates
  - 8-level FIFO with interrupt
- **SARADC**
  - 12-bit SAR ADC with 12-bit output
  - 10-bits accuracy guaranteed
  - 12-ch external single-ended input
  - 200K SPS under VCCA (2.5V~3.6V)
  - DMA support for min CPU intervention
- **Audio Analog to Digital Converter**
  - Mono Sigma-Delta ADC with configurable decimation filter and 16 bit output
  - 16-level word FIFO data buffer with mono 32/24/16/8 bits data width
  - Programmable gain amplifier with 32 steps from -12 to 34.5dB in 1.5dB steps
  - Boost gain stage of 26dB, giving maximum total gain of 60.5dB
  - Input from optional gain dedicated from MIC pin
  - Optional 8 level output voltage (50%, 60%, 75%, 90% of VCCA, 1.2V, 1.7V, 2.0V, 2.4V)
  - Support FIFO threshold setting for interrupt
  - Sample rate 8K-48KHz
  - DMA support for minimal CPU intervention
- **24bit Stereo Audio DAC with Headphone Output (Class-AB)**
  - -75dB Total Harmonic Distortion (THD+N) performance
  - 90dB Signal-to-Noise (SNR) performance
  - 20mW per channel drive capability into 32Ω load @3.3V
  - 16-level 2-word FIFO data buffer with stereo 32/24/16/8 bits data width
  - Programmable digital volume control from -80dB to 6dB
  - Programmable analog headphone output volume control from -57dB to 6dB
  - Support sample rates from 8 KHz – 48 KHz
  - DMA support for minimal CPU intervention
- **UART**
  - Two UART ports with flow control (TX, RX, CTS and RTS)
  - 16 byte FIFO for receive and transmit data payloads
  - Programmable baud-rate generator max up to 4M (additional 1000000/1843200/3250000)
  - Programmable receiver buffer trigger level
  - DMA support for minimal CPU intervention
- **I^2C**
  - Up to two I2C controllers
  - Master/Slave up to 1Mbit/s
  - Bidirectional data transfer between masters and slaves

- Multi-master bus (no central master)
- Arbitration between simultaneously transmitting masters without corruption of serial data on the bus
- Serial clock synchronization with different bit rates to communicate via one serial bus
- Serial clock synchronization configurable as handshake mechanism to suspend and resume serial transfer
- Programmable clock allowing versatile rate control
- Support multiple address recognition (four slave address with mask option)

- **PDMA**
  - 8-channel DMAs support data transfer between SRAM and peripherals of SARADC, SDADC, DAC, SPI0, I2S, UART0/1
- **Timers**
  - Three timers with 8-bit pre-scalar and 16-bit resolution
  - Counter auto reloaded
  - Timer1 can be IR carrier generator
- **Watch Dog Timer**
  - Multiple clock sources
  - 8 selectable time-out period from micro seconds ~ seconds (depends on clock source)
  - WDT can wake up power down/sleep
  - Interrupt or reset selectable on watchdog time-out
- **PWM/Capture Timer**
  - 2 sets supporting up to 8 individual PWM outputs
  - Built-in two sets of one 16-bit timer and four 16-bit comparators supporting up to 8 single-ended PWM outputs or 4 complementary paired PWM outputs
  - The PWM generator equipped with a clock source selector, a clock divider, an 8-bit pre-scalar for each
  - PWM set and Dead-Zone generator for complementary paired PWM
  - PWM interrupt synchronous to PWM period
  - 16-bit digital capture timers (shared with PWM timers) providing rising/falling capture inputs
  - Capture interrupt
- **SPI**
  - 2 sets of SPI interface
  - SPI Clock up to 25 MHz
  - SPI data rate in Quad mode of 100 Mbps
  - SPI master/slave mode
  - MSB or LSB first data transfer
  - 2 slave/device select lines when used in master mode
  - 8-level 32-bit FIFO
  - DMA support
  - Quad/Dual SPI support
- **I^2S**
  - 1 set of I2S interface
  - Master mode and Slave mode
  - Capable of handling 8, 16, 24 and 32 bits data sizes in each audio channel
  - Monaural and stereo audio data
  - I2S protocols: Philips standard, MSB-justified, and LSB-justified data format
  - PCM protocols: PCM standard, MSB-justified, and LSB-justified data format
  - Interrupt requests generated when buffer levels cross a programmable boundary
  - Support two 16-level FIFO data buffers, one for transmitting and the other for receiving
  - Support two PDMA requests, one for transmitting and the other for receiving
- **USB 2.0 Device Controller**

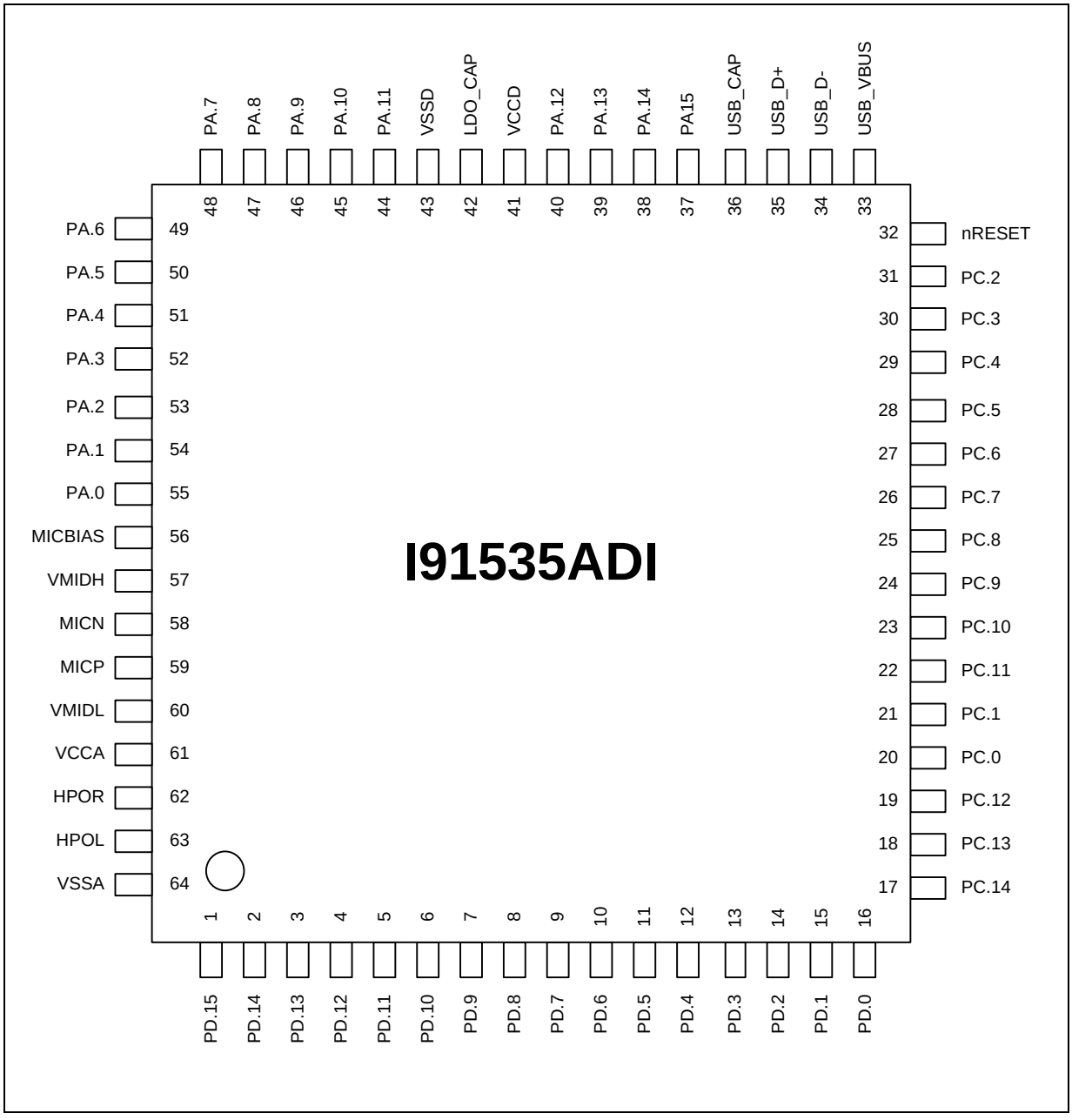
- Compliant with USB 2.0 full-speed specification
- 1 interrupt vector with 4 different interrupt events (NEVWK, VBUSDET, USB and BUS)
- Support Control/Bulk/Interrupt/Isochronous transfer type
- Support suspend function when no bus activity existing for 3 ms
- 12 endpoints for configurable Control/Bulk/Interrupt/Isochronous transfer types and maximum 1k bytes buffer size
- Remote wake-up capability

- **Brown-Out Detector (BOD)**
  - With 11 levels: 1.8/1.9/2.0/2.1/2.2/2.4/2.6/2.8/3.0/3.1/3.4V with VCCD detection
  - Support Brown-out Interrupt or Reset option
- **Low Voltage Reset**
  - Threshold voltage levels: 1.6V with VCCD detection
- **Operating Temperature: -40℃~85℃**
- **Package**
  - LQFP64
  - QFN48
  - Package is Halogen-free, RoHS-compliant and TSCA-compliant

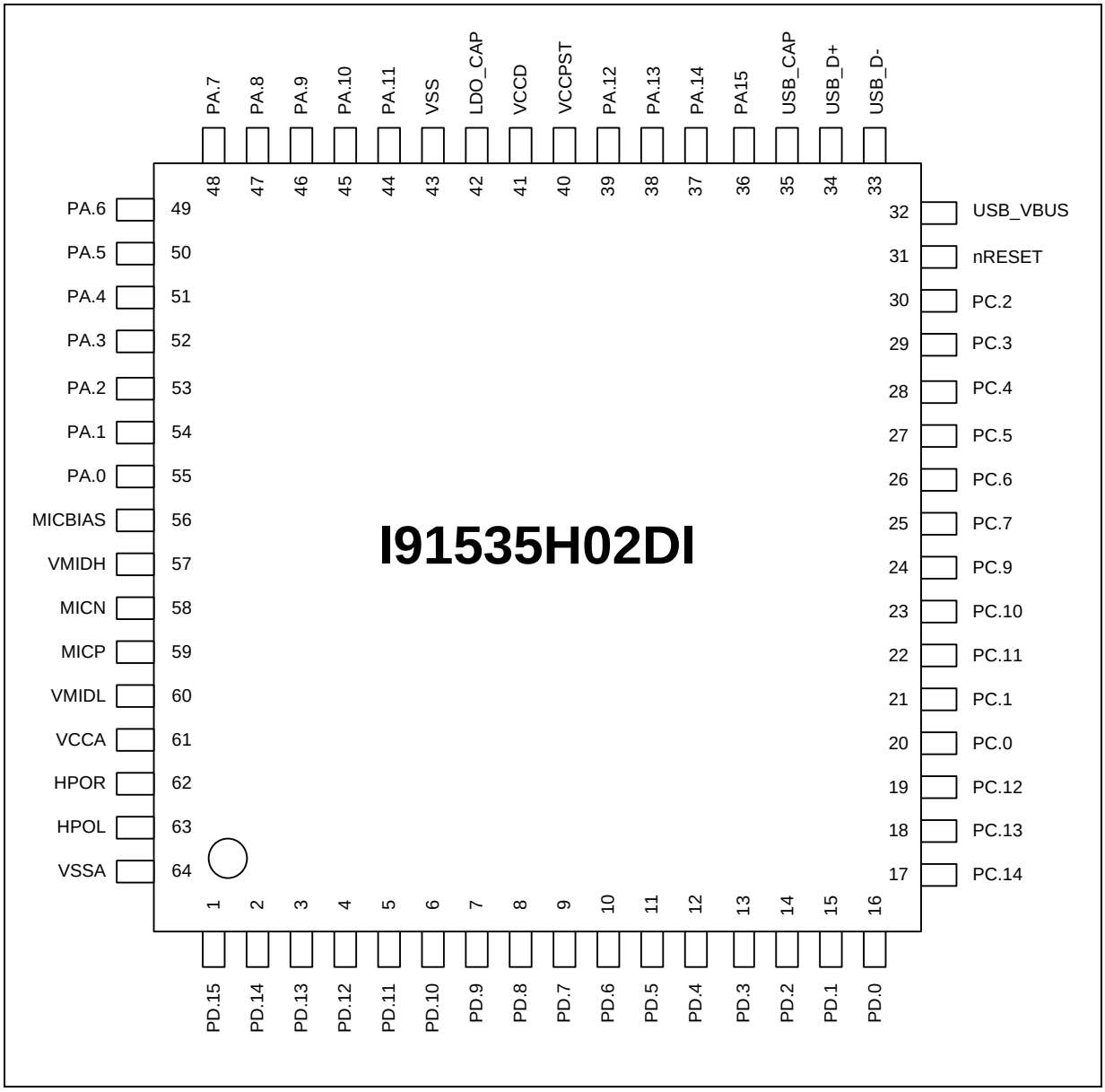
3 PART INFORMATION AND PIN CONFIGURATION

3.1 LQFP 64-Pin Diagram

3.1.1 I91535ADI

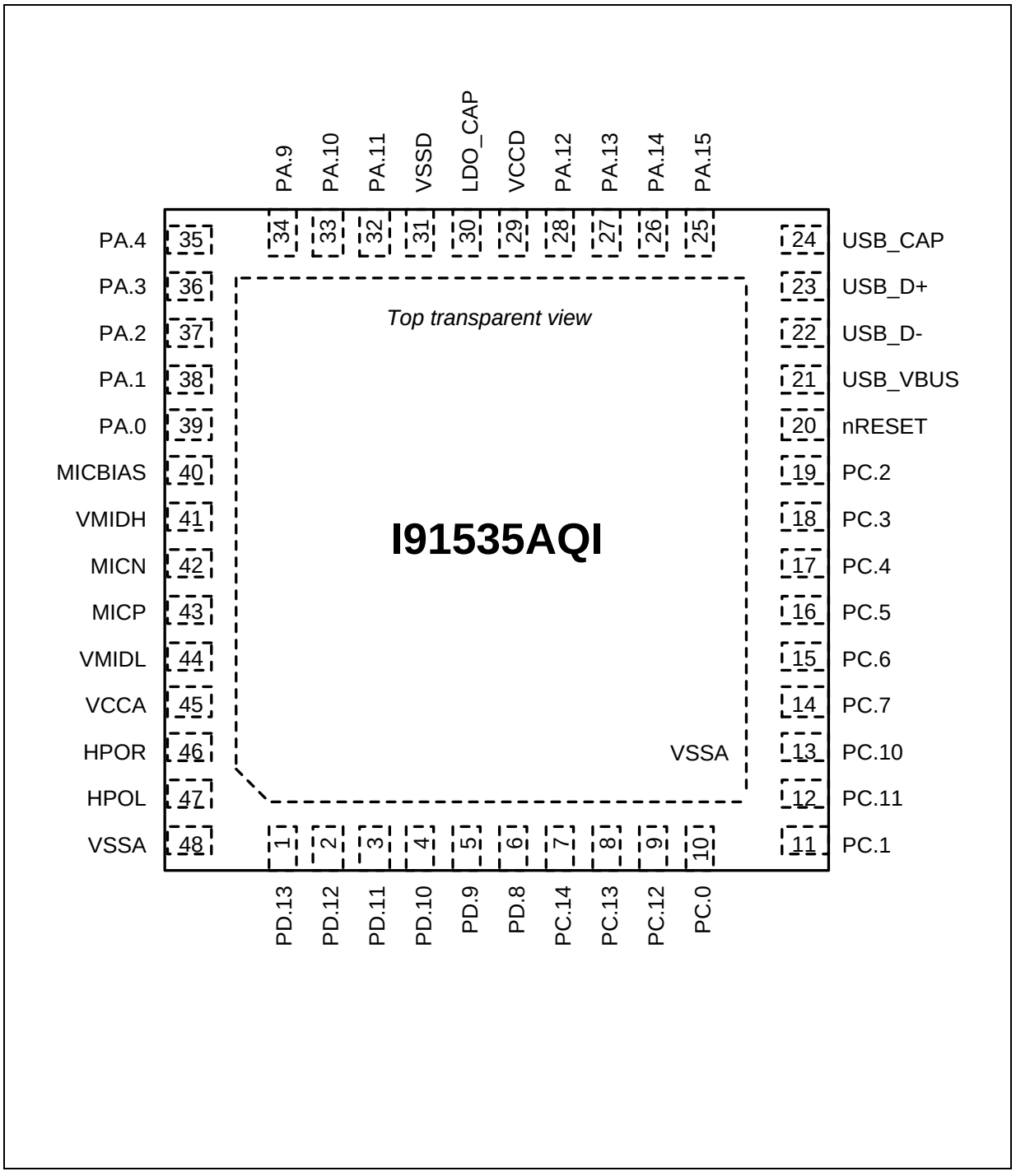


3.1.2 I91535H02DI

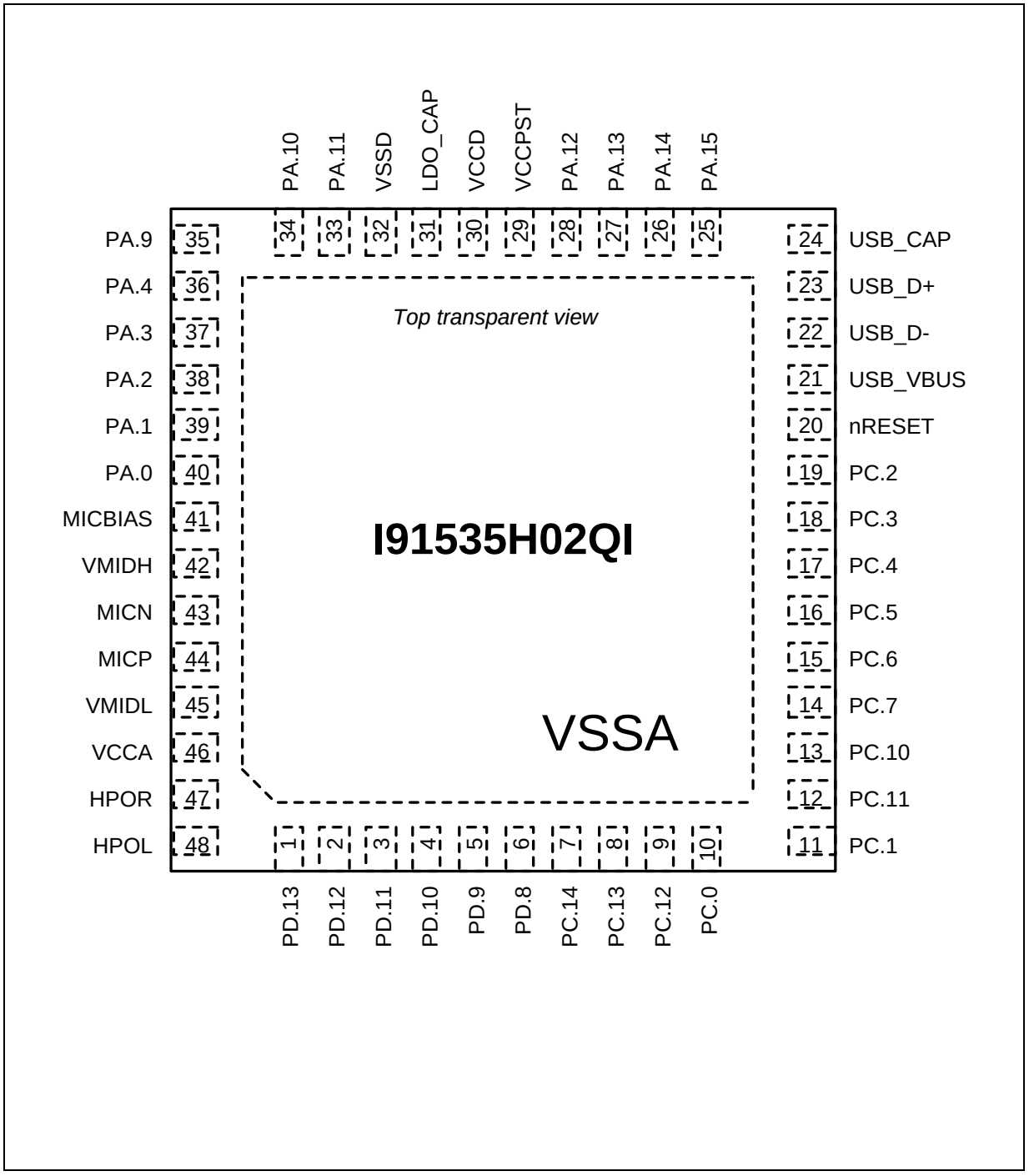


3.2 QFN 48-Pin Diagram

3.2.1 I91535AQI



3.2.2 I91535H02QI



3.3 Pin/Pad Description

3.3.1 LQFP64

I91535ADI Pin No.	I91535H02DI Pin No.	Name	Type	Alt CFG	Description
1	1	PD.15	**I/O**	0	General purpose input/output pin; port D, bit15
		I2C0_SDA	**O**	1	I2C0 data input/output pin
		SPI1_MOSI1	**O**	3	SPI1 Master Out Slave In 1
2	2	PD.14	**I/O**	0	General purpose input/output pin; port D, bit14
		I2C0_SCL	**I/O**	1	I2C0 clock pin
		SPI0_SS1	**O**	2	SPI0 Slave Select 1
		SPI1_MISO1	**I/O**	3	SPI1 Master In Slave Out 1
3	3	PD.13	**I/O**	0	General purpose input/output pin; port D, bit13
		I2C1_SDA	**I/O**	1	I2C1 data input/output pin
		SPI0_MISO1	**I/O**	2	SPI0 Master In Slave Out 1
		ICE_DAT	**I/O**	3	SWD Interface, Serial Data
4	4	PD.12	**I/O**	0	General purpose input/output pin, port D, bit12
		I2C1_SCL	**I/O**	1	I2C1 clock pin
		SPI0_MOSI1	**I/O**	2	SPI0 Master Out Slave In 1
		ICE_CLK	**I/O**	3	SWD Interface, Serial Clock
5	5	PD.11	**I/O**	0	General purpose input/output pin, port D, bit11
		PWM1_ch3	**I/O**	1	PWM1 channel 3 output
		SPI0_MOSI0	**I/O**	2	SPI0 Master Out Slave In 0
		I2C1_SDA	**I/O**	3	I2C1 data input/output pin
6	6	PD.10	**I/O**	0	General purpose input/output pin, port D, bit10
		PWM1_ch2	**I/O**	1	PWM1 channel 2 output
		SPI0_CLK	**I/O**	2	SPI0 Serial Clock
		I2C1_SCL	**I/O**	3	I2C1 clock pin
7	7	PD.9	**I/O**	0	General purpose input/output pin, port D, bit9
		PWM1_ch1	**I/O**	1	PWM1 channel 1 output
		SPI0_MISO0	**I/O**	2	SPI0 Master In Slave Out 0
		UART0_RX	**I**	3	UART0 Receiver Serial In

I91535ADI Pin No.	I91535H02DI Pin No.	Name	Type	Alt CFG	Description
8	8	PD.8	**I/O**	0	General purpose input/output pin, port D, bit8
		PWM1_ch0	**I/O**	1	PWM1 channel 0 output
		SPI0_SS0	**I/O**	2	SPI0 Slave Select 0
		UART0_TX	**O**	3	UART0 Transmitter Serial Out
9	9	PD.7	**I/O**	0	General purpose input/output pin, port D, bit7
		PWM0_ch3	**I/O**	1	PWM0 channel 3 output
		SPI1_MISO0	**I/O**	3	SPI1 Master In Slave Out 0
10	10	PD.6	**I/O**	0	General purpose input/output pin, port D, bit6
		PWM0_ch2	**I/O**	1	PWM0 channel 2 output
		SPI1_CLK	**I/O**	3	SPI1 Serial Clock
11	11	PD.5	**I/O**	0	General purpose input/output pin, port D, bit5
		PWM0_ch1	**I/O**	1	PWM0 channel 1 output
		SPI1_MOSI0	**I/O**	3	SPI1 Master Out Slave In 0
12	12	PD.4	**I/O**	0	General purpose input/output pin, port D, bit4
		PWM0_ch0	**I/O**	1	PWM0 channel 0 output
		CAP0	**I**	2	Capture input based on PWM0 timer
		I2S0_DI	**I**	3	I2S0 Data input pin
13	13	PD.3	**I/O**	0	General purpose input/output pin, port D, bit3
		UART1_RX	**I**	1	UART1 Receiver Serial In
		PWM0_ch3	**I**	2	PWM0 channel 3 output
		I2S0_DO	**O**	3	I2S0 Data output pin
14	14	PD.2	**I/O**	0	General purpose input/output pin, port D, bit2
		UART1_TX	**O**	1	UART1 Transmitter Serial Out
		PWM0_ch2	**I**	2	PWM0 channel 2 output
		I2S0_BCLK	**I/O**	3	I2S0 Bit Clock pin
15	15	PD.1	**I/O**	0	General purpose input/output pin, port D, bit1
		UART1_nRTS	**O**	1	UART1 Request To Send Output
		PWM0_ch1	**I**	2	PWM0 channel 1 output
		I2S0_LRCK	**I/O**	3	I2S0 left right channel clock pin

I91535ADI Pin No.	I91535H02DI Pin No.	Name	Type	Alt CFG	Description
16	16	PD.0	**I/O**	0	General purpose input/output pin, port D, bit0
		UART1_nCTS	**I**	1	UART1 Clear To Send Input
		PWM0_ch0	**I/O**	2	PWM0 channel 0 output
		I2S0_MCLK	**O**	3	I2S0 Master Clock Output pin
17	17	PC.14	**I/O**	0	General purpose input/output pin, port C, bit14
		SPI0_SS0	**I/O**	1	SPI0 Slave Select 0
		I2S0_DI	**I**	2	I2S0 Data input pin
		UART1_RX	**I**	3	UART1 Receiver Serial In
18	18	PC.13	**I/O**	0	General purpose input/output pin, port C, bit13
		SPI0_MISO0	**I/O**	1	SPI0 Master In Slave Out 0
		I2S0_DO	**O**	2	I2S0 Data output pin
		UART1_TX	**O**	3	UART1 Transmitter Serial Out
19	19	PC.12	**I/O**	0	General purpose input/output pin, port C, bit12
		SPI0_CLK	**I/O**	1	SPI0 Serial Clock
		I2S0_BCLK	**I/O**	2	I2S0 Bit Clock pin
		UART1_nRTS	**O**	3	UART1 Request To Send Output
20	20	PC.0	**I/O**	0	General purpose input/output pin, port C, bit0
		XT1_OUT	**O**	1	External 4~24.576 MHz(high speed) crystal output pin
		I2C0_SCL	**I/O**	3	I2C0 clock pin
21	21	PC.1	**I/O**	0	General purpose input/output pin, port C, bit1
		XT1_IN	**I**	1	External 4~24.576 MHz(high speed) crystal input pin
		I2C0_SDA	**I/O**	3	I2C0 data input/output pin
22	22	PC.11	**I/O**	0	General purpose input/output pin, port C, bit11
		SPI0_MOSI0	**I/O**	1	SPI0 Master Out Slave In 0
		I2S0_LRCK	**I/O**	2	I2S0 left right channel clock pin
		UART1_nCTS	**I**	3	UART1 Clear To Send Input
23	23	PC.10	**I/O**	0	General purpose input/output pin, port C, bit10
		SPI0_MOSI1	**I/O**	1	SPI0 Master Out Slave In 1
		I2S0_MCLK	**O**	2	I2S0 Master Clock Output pin
		MCLKI	**I**	3	External Clock Input

I91535ADI Pin No.	I91535H02DI Pin No.	Name	Type	Alt CFG	Description
24	24	PC.9	**I/O**	0	General purpose input/output pin, port C, bit9
		SPI0_MISO1	**I/O**	1	SPI0 Master In Slave Out 1
		PWM1_ch3	**O**	3	PWM1 channel 3 output
		PWM1_ch2	**O**	3	PWM1 channel 2 output
25		PC.8	**I/O**	0	General purpose input/output pin, port C, bit8
		SPI0_SS1	**O**	1	SPI0 Slave Select 1
		I2S0_MCLK	**O**	2	I2S0 Master Clock Output pin
		PWM1_ch2	**O**	3	PWM1 channel 2 output
26	25	PC.7	**I/O**	0	General purpose input/output pin, port C, bit7
		I2C0_SDA	**I/O**	1	I2C0 data input/output pin
		SPI1_SS1	**O**	2	SPI1 Slave Select 1
		PWM1_ch1	**O**	3	PWM1 channel 1 output
27	26	PC.6	**I/O**	0	General purpose input/output pin, port C, bit6
		I2C0_SCL	**I/O**	1	I2C0 clock pin
		SPI1_SS0	**I/O**	2	SPI1 Slave Select 0
		PWM1_ch0	**O**	3	PWM1 channel 0 output
28	27	PC.5	**I/O**	0	General purpose input/output pin, port C, bit5
		UART0_RX	**I**	1	UART0 Receiver Serial In
		I2S0_DI	**I**	2	I2S0 Data input pin
		PWM0_ch3	**O**	3	PWM0 channel 3 output
29	28	PC.4	**I/O**	0	General purpose input/output pin, port C, bit4
		UART0_TX	**O**	1	UART0 Transmitter Serial Out
		I2S0_DO	**O**	2	I2S0 Data output pin
		PWM0_ch2	**O**	3	PWM0 channel 2 output
30	29	PC.3	**I/O**	0	General purpose input/output pin, port C, bit3
		UART0_nRTS	**O**	1	UART0 Request To Send Output
		I2S0_BCLK	**I/O**	2	I2S0 Bit Clock pin
		PWM0_ch1	**O**	3	PWM0 channel 1 output
31	30	PC.2	**I/O**	0	General purpose input/output pin, port C, bit2
		UART0_nCTS	**I**	1	UART0 Clear To Send Input
		I2S0_LRCK	**I/O**	2	I2S0 left right channel clock pin
		PWM0_ch0	**O**	3	PWM0 channel 0 output
32	31	nRESET	**I**		Reset input, low active, internal pull-high

I91535ADI Pin No.	I91535H02DI Pin No.	Name	Type	Alt CFG	Description
33	32	USB_VBUS	**P**		Power supply from USB or HUB
34	33	USB_D-	**A**		USB differential signal D-
35	34	USB_D+	**A**		USB differential signal D+
36	35	USB_CAP	**P**		USB Internal regulator output decoupling pin. A 1uF cap returning to VSSD must be placed on it.
37	36	PA.15	**I/O**	0	General purpose input/output pin, port A, bit15
		SPI0_SS0	**I/O**	1	SPI0 Slave Select 0
		UART1_RX	**I**	2	UART1 Receiver Serial In
38	37	PA.14	**I/O**	0	General purpose input/output pin, port A, bit14
		SPI0_MISO0	**I/O**	1	SPI0 Master In Slave Out 0
		UART1_TX	**O**	2	UART1 Transmitter Serial Out
39	38	PA.13	**I/O**	0	General purpose input/output pin, port A, bit13
		SPI0_CLK	**I/O**	1	SPI0 Serial Clock
		UART0_nRTS	**O**	3	UART0 Request To Send Output
40	39	PA.12	**I/O**	0	General purpose input/output pin, port A, bit12
		SPI0_MOSI0	**I/O**	1	SPI0 Master Out Slave In 0
		I2C1_SDA	**I/O**	2	I2C1 data input/output pin
		UART0_nCTS	**I**	3	UART0 Clear To Send Input
	40	VCCPST	**P**		Digital IO Power Supply(Include GPB,GPC,GPD)
41	41	VCCD	**P**		Main Digital Power Supply(Also include GPA IO power)
42	42	LDOCAP	**P**		Regulator output decoupling pin for core logic. A 1uF cap returning to VSSD must be placed on it.
43	43	VSSD	**P**		Digital ground
44	44	PA.11	**I/O**	0	General purpose input/output pin, port A, bit11
		SPI0_MOSI1	**I/O**	1	SPI0 Master Out Slave In 1
		I2C1_SCL	**I/O**	2	I2C1 clock pin
		UART0_RX	**I**	3	UART0 Receiver Serial In
45	45	PA.10	**I/O**	0	General purpose input/output pin, port A, bit10
		SPI0_MISO1	**I/O**	1	SPI0 Master In Slave Out 1
		MCLKI	**I**	2	External Clock Input
		UART0_TX	**O**	3	UART0 Transmitter Serial Out

I91535ADI Pin No.	I91535H02DI Pin No.	Name	Type	Alt CFG	Description
46	46	PA.9	**I/O**	0	General purpose input/output pin, port A, bit9
		SPI0_SS1	**O**	1	SPI0 Slave Select 1
		UART0_RX	**I**	2	UART0 Receiver Serial In
		PWM1_ch3	**O**	3	PWM1 channel 3 output
47	47	PA.8	**I/O**	0	General purpose input/output pin, port A, bit8
		TMR2	**I**	1	Timer2 external clock input
		UART0_TX	**O**	2	UART0 Transmitter Serial Out
		PWM1_ch2	**O**	3	PWM1 channel 2 output
48	48	PA.7	**I/O**	0	General purpose input/output pin, port A, bit7
		TMR1	**I**	1	Timer1 external clock input
		SPI1_SS1	**O**	2	SPI1 Slave Select 1
		PWM1_ch1	**O**	3	PWM1 channel 1 output
49	49	PA.6	**I/O**	0	General purpose input/output pin, port A, bit6
		TMR0	**I**	1	Timer0 external clock input
		CAP1	**I**	2	Capture input based on PWM1 timer
		PWM1_ch0	**O**	3	PWM1 channel 0 output
50	50	PA.5	**I/O**	0	General purpose input/output pin, port A, bit5
		MCLKI	**I**	1	External Clock Input
		SPI1_SS0	**I/O**	3	SPI1 Slave Select 0
51	51	PA.4	**I/O**	0	General purpose input/output pin, port A, bit4
		I2S0_DI	**I**	1	I2S0 Data input pin
		UART1_RX	**I**	2	UART1 Receiver Serial In
		SPI1_MISO0	**I/O**	3	SPI1 Master In Slave Out 0
52	52	PA.3	**I/O**	0	General purpose input/output pin, port A, bit3
		I2S0_DO	**O**	1	I2S0 Data output pin
		UART1_TX	**O**	2	UART1 Transmitter Serial Out
		SPI1_CLK	**I/O**	3	SPI1 Serial Clock
53	53	PA.2	**I/O**	0	General purpose input/output pin, port A, bit2
		I2S0_BCLK	**I/O**	1	I2S0 Bit Clock pin
		I2C0_SDA	**I/O**	2	I2C0 data input/output pin
		SPI1_MOSI0	**I/O**	3	SPI1 Master Out Slave In 0

I91535ADI Pin No.	I91535H02DI Pin No.	Name	Type	Alt CFG	Description
54	54	PA.1	**I/O**	0	General purpose input/output pin, port A, bit1
		I2S0_LRCK	**I/O**	1	I2S0 left right channel clock pin
		I2C0_SCL	**I/O**	2	I2C0 clock pin
		SPI1_MOSI1	**I/O**	3	SPI1 Master Out Slave In 1
55	55	PA.0	**I/O**	0	General purpose input/output pin, port A, bit0
		I2S0_MCLK	**O**	1	I2S0 Master Clock Output pin
		IR	**O**	2	IR carrier generator based on Timer1 interval
		SPI1_MISO1	**I/O**	3	SPI1 Master In Slave Out 1
56	56	MICBIAS	**A**		Microphone Bias Output
57	57	VMIDH	**P**		Mid Rail Reference High, Connect 4.7uF to VSSA
58	58	MICN	**A**		Negative Microphone Input
59	59	MICP	**A**		Positive Microphone Input
60	60	VMIDL	**P**		Mid Rail Reference Low, Connect 4.7uF to VSSA
61	61	VCCA	**P**		Main Analog Circuitry Power Supply
62	62	HPOR	**A**		Headphone Right Channel Output
63	63	HPOL	**A**		Headphone Left Channel Output
64	64	VSSA	**P**		Ground for Analog Circuitry

Note 1:
I: Digital Input, O: Digital Output, A: Analog pin, P: Power Pin

Note 2:
VCCD & VCCA must be supplied same voltage level, and VCCD must larger or equal to VCCPST.
For I91535ADI, VCCD pin also supply all IO power.

3.3.2 QFN48

I91535AQI Pin No.	I91535H02QI Pin No.	Name	Type	Alt CFG	Description
1	1	PD.13	**I/O**	0	General purpose input/output pin; port D, bit13
		I2C1_SDA	**I/O**	1	I2C1 data input/output pin
		SPI0_MISO1	**I/O**	2	SPI0 Master In Slave Out 1
		ICE_DAT	**I/O**	3	SWD Interface, Serial Data
2	2	PD.12	**I/O**	0	General purpose input/output pin, port D, bit12
		I2C1_SCL	**I/O**	1	I2C1 clock pin
		SPI0_MOSI1	**I/O**	2	SPI0 Master Out Slave In 1
		ICE_CLK	**I/O**	3	SWD Interface, Serial Clock
3	3	PD.11	**I/O**	0	General purpose input/output pin, port D, bit11
		PWM1_ch3	**I/O**	1	PWM1 channel 3 output
		SPI0_MOSI0	**I/O**	2	SPI0 Master Out Slave In 0
		I2C1_SDA	**I/O**	3	I2C1 data input/output pin
4	4	PD.10	**I/O**	0	General purpose input/output pin, port D, bit10
		PWM1_ch2	**I/O**	1	PWM1 channel 2 output
		SPI0_CLK	**I/O**	2	SPI0 Serial Clock
		I2C1_SCL	**I/O**	3	I2C1 clock pin
5	5	PD.9	**I/O**	0	General purpose input/output pin, port D, bit9
		PWM1_ch1	**I/O**	1	PWM1 channel 1 output
		SPI0_MISO0	**I/O**	2	SPI0 Master In Slave Out 0
		UART0_RX	**I**	3	UART0 Receiver Serial In
6	6	PD.8	**I/O**	0	General purpose input/output pin, port D, bit8
		PWM1_ch0	**I/O**	1	PWM1 channel 0 output
		SPI0_SS0	**I/O**	2	SPI0 Slave Select 0
		UART0_TX	**O**	3	UART0 Transmitter Serial Out
7	7	PC.14	**I/O**	0	General purpose input/output pin, port C, bit14
		SPI0_SS0	**I/O**	1	SPI0 Slave Select 0
		I2S0_DI	**I**	2	I2S0 Data input pin
		UART1_RX	**I**	3	UART1 Receiver Serial In
8	8	PC.13	**I/O**	0	General purpose input/output pin, port C, bit13
		SPI0_MISO0	**I/O**	1	SPI0 Master In Slave Out 0
		I2S0_DO	**O**	2	I2S0 Data output pin
		UART1_TX	**O**	3	UART1 Transmitter Serial Out

I91535AQI Pin No.	I91535H02QI Pin No.	Name	Type	Alt CFG	Description
9	9	PC.12	**I/O**	0	General purpose input/output pin, port C, bit12
		SPI0_CLK	**I/O**	1	SPI0 Serial Clock
		I2S0_BCLK	**I/O**	2	I2S0 Bit Clock pin
		UART1_nRTS	**O**	3	UART1 Request To Send Output
10	10	PC.0	**I/O**	0	General purpose input/output pin, port C, bit0
		XT1_OUT	**O**	1	External 4~24.576 MHz(high speed) crystal output pin
		I2C0_SCL	**I/O**	3	I2C0 clock pin
11	11	PC.1	**I/O**	0	General purpose input/output pin, port C, bit1
		XT1_IN	**I**	1	External 4~24.576 MHz(high speed) crystal input pin
		I2C0_SDA	**I/O**	3	I2C0 data input/output pin
12	12	PC.11	**I/O**	0	General purpose input/output pin, port C, bit11
		SPI0_MOSI0	**I/O**	1	SPI0 Master Out Slave In 0
		I2S0_LRCK	**I/O**	2	I2S0 left right channel clock pin
		UART1_nCTS	**I**	3	UART1 Clear To Send Input
13	13	PC.10	**I/O**	0	General purpose input/output pin, port C, bit10
		SPI0_MOSI1	**I/O**	1	SPI0 Master Out Slave In 1
		I2S0_MCLK	**O**	2	I2S0 Master Clock Output pin
		MCLKI	**I**	3	External Clock Input
14	14	PC.7	**I/O**	0	General purpose input/output pin, port C, bit7
		I2C0_SDA	**I/O**	1	I2C0 data input/output pin
		SPI1_SS1	**O**	2	SPI1 Slave Select 1
		PWM1_ch1	**O**	3	PWM1 channel 1 output
15	15	PC.6	**I/O**	0	General purpose input/output pin, port C, bit6
		I2C0_SCL	**I/O**	1	I2C0 clock pin
		SPI1_SS0	**I/O**	2	SPI1 Slave Select 0
		PWM1_ch0	**O**	3	PWM1 channel 0 output
16	16	PC.5	**I/O**	0	General purpose input/output pin, port C, bit5
		UART0_RX	**I**	1	UART0 Receiver Serial In
		I2S0_DI	**I**	2	I2S0 Data input pin
		PWM0_ch3	**O**	3	PWM0 channel 3 output

I91535AQI Pin No.	I91535H02QI Pin No.	Name	Type	Alt CFG	Description
17	17	PC.4	**I/O**	0	General purpose input/output pin, port C, bit4
		UART0_TX	**O**	1	UART0 Transmitter Serial Out
		I2S0_DO	**O**	2	I2S0 Data output pin
		PWM0_ch2	**O**	3	PWM0 channel 2 output
18	18	PC.3	**I/O**	0	General purpose input/output pin, port C, bit3
		UART0_nRTS	**O**	1	UART0 Request To Send Output
		I2S0_BCLK	**I/O**	2	I2S0 Bit Clock pin
		PWM0_ch1	**O**	3	PWM0 channel 1 output
19	19	PC.2	**I/O**	0	General purpose input/output pin, port C, bit2
		UART0_nCTS	**I**	1	UART0 Clear To Send Input
		I2S0_LRCK	**I/O**	2	I2S0 left right channel clock pin
		PWM0_ch0	**O**	3	PWM0 channel 0 output
20	20	nRESET	**I**		Reset input, low active, internal pull-high
21	21	USB_VBUS	**P**		Power supply from USB or HUB
22	22	USB_D-	**A**		USB differential signal D-
23	23	USB_D+	**A**		USB differential signal D+
24	24	USB_CAP	**P**		USB Internal regulator output decoupling pin. A 1uF cap returning to VSSD must be placed on it.
25	25	PA.15	**I/O**	0	General purpose input/output pin, port A, bit15
		SPI0_SS0	**I/O**	1	SPI0 Slave Select 0
		UART1_RX	**I**	2	UART1 Receiver Serial In
26	26	PA.14	**I/O**	0	General purpose input/output pin, port A, bit14
		SPI0_MISO0	**I/O**	1	SPI0 Master In Slave Out 0
		UART1_TX	**O**	2	UART1 Transmitter Serial Out
27	27	PA.13	**I/O**	0	General purpose input/output pin, port A, bit13
		SPI0_CLK	**I/O**	1	SPI0 Serial Clock
		UART0_nRTS	**O**	3	UART0 Request To Send Output
28	28	PA.12	**I/O**	0	General purpose input/output pin, port A, bit12
		SPI0_MOSI0	**I/O**	1	SPI0 Master Out Slave In 0
		I2C1_SDA	**I/O**	2	I2C1 data input/output pin
		UART0_nCTS	**I**	3	UART0 Clear To Send Input
	29	VCCPST	**P**		Digital IO Power Supply(Include GPB,GPC,GPD)
29	30	VCCD	**P**		Main Digital Power Supply(Also include GPA IO power)

I91535AQI Pin No.	I91535H02QI Pin No.	Name	Type	Alt CFG	Description
30	31	LDO_CAP	**P**		Regulator output decoupling pin for core logic. A 1uF cap returning to VSSD must be placed on it.
31	32	VSSD	**P**		Digital ground
32	33	PA.11	**I/O**	0	General purpose input/output pin, port A, bit11
		SPI0_MOSI1	**I/O**	1	SPI0 Master Out Slave In 1
		I2C1_SCL	**I/O**	2	I2C1 clock pin
		UART0_RX	**I**	3	UART0 Receiver Serial In
33	34	PA.10	**I/O**	0	General purpose input/output pin, port A, bit10
		SPI0_MISO1	**I/O**	1	SPI0 Master In Slave Out 1
		MCLKI	**I**	2	External Clock Input
		UART0_TX	**O**	3	UART0 Transmitter Serial Out
34	35	PA.9	**I/O**	0	General purpose input/output pin, port A, bit9
		SPI0_SS1	**O**	1	SPI0 Slave Select 1
		UART0_RX	**I**	2	UART0 Receiver Serial In
		PWM1_ch3	**O**	3	PWM1 channel 3 output
35	36	PA.4	**I/O**	0	General purpose input/output pin, port A, bit4
		I2S0_DI	**I**	1	I2S0 Data input pin
		UART1_RX	**I**	2	UART1 Receiver Serial In
		SPI1_MISO0	**I/O**	3	SPI1 Master In Slave Out 0
36	37	PA.3	**I/O**	0	General purpose input/output pin, port A, bit3
		I2S0_DO	**O**	1	I2S0 Data output pin
		UART1_TX	**O**	2	UART1 Transmitter Serial Out
		SPI1_CLK	**I/O**	3	SPI1 Serial Clock
37	38	PA.2	**I/O**	0	General purpose input/output pin, port A, bit2
		I2S0_BCLK	**I/O**	1	I2S0 Bit Clock pin
		I2C0_SDA	**I/O**	2	I2C0 data input/output pin
		SPI1_MOSI0	**I/O**	3	SPI1 Master Out Slave In 0
38	39	PA.1	**I/O**	0	General purpose input/output pin, port A, bit1
		I2S0_LRCK	**I/O**	1	I2S0 left right channel clock pin
		I2C0_SCL	**I/O**	2	I2C0 clock pin
		SPI1_MOSI1	**I/O**	3	SPI1 Master Out Slave In 1

I91535AQI Pin No.	I91535H02QI Pin No.	Name	Type	Alt CFG	Description
39	40	PA.0	**I/O**	0	General purpose input/output pin, port A, bit0
		I2S0_MCLK	**O**	1	I2S0 Master Clock Output pin
		IR	**O**	2	IR carrier generator based on Timer1 interval
		SPI1_MISO1	**I/O**	3	SPI1 Master In Slave Out 1
40	41	MICBIAS	**A**		Microphone Bias Output
41	42	VMIDH	**P**		Mid Rail Reference High, Connect 4.7uF to VSSA
42	43	MICN	**A**		Negative Microphone Input
43	44	MICP	**A**		Positive Microphone Input
44	45	VMIDL	**P**		Mid Rail Reference Low, Connect 4.7uF to VSSA
45	46	VCCA	**P**		Main Analog Circuitry Power Supply
46	47	HPOR	**A**		Headphone Right Channel Output
47	48	HPOL	**A**		Headphone Left Channel Output
48 49(L/F)	49(L/F)	VSSA	**P**		Ground for Analog Circuitry

Note 1:

I: Digital Input, O: Digital Output, A: Analog pin, P: Power Pin

Note 2:

VCCD & VCCA must be supplied same voltage level, and VCCD must larger or equal to VCCPST.

For I91535AQI, VCCD pin also supply all IO power.

3.4 Pin Alternate Function

GPIO	Power	ALT =1	I/O of ALT = 1	ALT =2	I/O of ALT = 2	ALT =3	I/O of ALT = 3	Special Modes
GPA0*	VCCD	I2S0_MCLK	O	IROUT	O	SPI1_MISO1	I/O	AIN0
GPA1*	VCCD	I2S0_LRCK	I/O	I2C0_SCL	I/O	SPI1_MOSI1	I/O	AIN1
GPA2*	VCCD	I2S0_BCLK	I/O	I2C0_SDA	I/O	SPI1_MOSI0	I/O	AIN2
GPA3*	VCCD	I2S0_DO	O	UART1_TX	O	SPI1_CLK	I/O	AIN3
GPA4*	VCCD	I2S0_DI	I	UART1_RX	I	SPI1_MISO0	I/O	AIN4
GPA5*	VCCD	MCLKI	I	-		SPI1_SS0	I/O	AIN5
GPA6*	VCCD	TMR0	I	CAP1	I	PWM1_ch0	O	AIN6
GPA7*	VCCD	TMR1	I	SPI1_SS1	I/O	PWM1_ch1	O	AIN7
GPA8*	VCCD	TMR2	I	UART0_TX	O	PWM1_ch2	O	AIN8
GPA9*	VCCD	SPI0_SS1	O	UART0_RX	I	PWM1_ch3	O	AIN9
GPA10*	VCCD	SPI0_MISO1	I/O	MCLKI	I	UART0_TX	O	AIN10
GPA11*	VCCD	SPI0_MOSI1	I/O	I2C1_SCL	I/O	UART0_RX	I	AIN11
GPA12*	VCCD	SPI0_MOSI0	I/O	I2C1_SDA	I/O	UART0_nCTS	I	
GPA13*	VCCD	SPI0_CLK	I/O	-		UART0_nRTS	O	
GPA14*	VCCD	SPI0_MISO0	I/O	UART1_TX	O	-		
GPA15* (wake up)	VCCD	SPI0_SS0	I/O	UART1_RX	I	-		
GPB0*	VCCPST	I2C1_SCL	I/O	-		-		
GPB1*	VCCPST	I2C1_SDA	I/O	-		-		
GPC0*	VCCPST	XT1_OUT	O	-		I2C0_SCL	I/O	
GPC1*	VCCPST	XT1_IN	I	-		I2C0_SDA	I/O	
GPC2*	VCCPST	UART0_nCTS	I	I2S0_LRCK	I/O	PWM0_ch0	O	

GPIO	Power	ALT =1	I/O of ALT = 1	ALT =2	I/O of ALT = 2	ALT =3	I/O of ALT = 3	Special Modes
GPC3*	VCCPST	UART0_nRTS	O	I2S0_BCLK	I/O	PWM0_ch1	O	
GPC4*	VCCPST	UART0_TX	O	I2S0_DO	O	PWM0_ch2	O	
GPC5*	VCCPST	UART0_RX	I	I2S0_DI	I	PWM0_ch3	O	
GPC6*	VCCPST	I2C0_SCL	I/O	SPI1_SS0	I/O	PWM1_ch0	O	
GPC7*	VCCPST	I2C0_SDA	I/O	SPI1_SS1	I/O	PWM1_ch1	O	
GPC8*	VCCPST	SPI0_SS1	O	I2S0_MCLK	O	PWM1_ch2	O	
GPC9*	VCCPST	SPI0_MISO1	I/O	-		PWM1_ch3	O	
GPC10*	VCCPST	SPI0_MOSI1	I/O	I2S0_MCLK	O	MCLKI	I	
GPC11*	VCCPST	SPI0_MOSI0	I/O	I2S0_LRCK	I/O	UART1_nCTS	I	
GPC12*	VCCPST	SPI0_CLK	I/O	I2S0_BCLK	I/O	UART1_nRTS	O	
GPC13*	VCCPST	SPI0_MISO0	I/O	I2S0_DO	O	UART1_TX	O	
GPC14*	VCCPST	SPI0_SS0	I/O	I2S0_DI	I	UART1_RX	I	
GPC15*	VCCPST	-		MCLKI	I	-		
GPD0*	VCCPST	UART1_nCTS	I	PWM0_ch0	O	I2S0_MCLK	O	
GPD1*	VCCPST	UART1_nRTS	O	PWM0_ch1	O	I2S0_LRCK	I/O	
GPD2*	VCCPST	UART1_TX	O	PWM0_ch2	O	I2S0_BCLK	I/O	
GPD3*	VCCPST	UART1_RX	I	PWM0_ch3	O	I2S0_DO	O	
GPD4*	VCCPST	PWM0_ch0	O	CAP0	I	I2S0_DI	I	
GPD5*	VCCPST	PWM0_ch1	O	-		SPI1_MOSI0	I/O	
GPD6*	VCCPST	PWM0_ch2	O	-		SPI1_CLK	I/O	
GPD7*	VCCPST	PWM0_ch3	O	-		SPI1_MISO0	I/O	
GPD8*	VCCPST	PWM1_ch0	O	SPI0_SS0	I/O	UART0_TX	O	

GPIO	Power	ALT =1	I/O of ALT = 1	ALT =2	I/O of ALT = 2	ALT =3	I/O of ALT = 3	Special Modes
GPD9*	VCCPST	PWM1_ch1	O	SPI0_MISO0	I/O	UART0_RX	I	
GPD10*	VCCPST	PWM1_ch2	O	SPI0_CLK	I/O	I2C1_SCL	I/O	
GPD11*	VCCPST	PWM1_ch3	O	SPI0_MOSI0	I/O	I2C1_SDA	I/O	
GPD12	VCCPST	I2C1_SCL	I/O	SPI0_MOSI1	I/O	ICE_CLK*	I/O	
GPD13	VCCPST	I2C1_SDA	I/O	SPI0_MISO1	I/O	ICE_DAT*	I/O	
GPD14*	VCCPST	I2C0_SCL	I/O	SPI0_SS1	O	SPI1_MISO1	I/O	
GPD15*	VCCPST	I2C0_SDA	I/O	-		SPI1_MOSI1	I/O	

I: Input, O: Output

* :

Note 1: AIN0~AIN11 are SARADC inputs, when using SARADC input please select GPIO input mode and disable pull-up option.

Note 2: The suffix * is for the reset state of each GPIO

4 BLOCK DIAGRAM

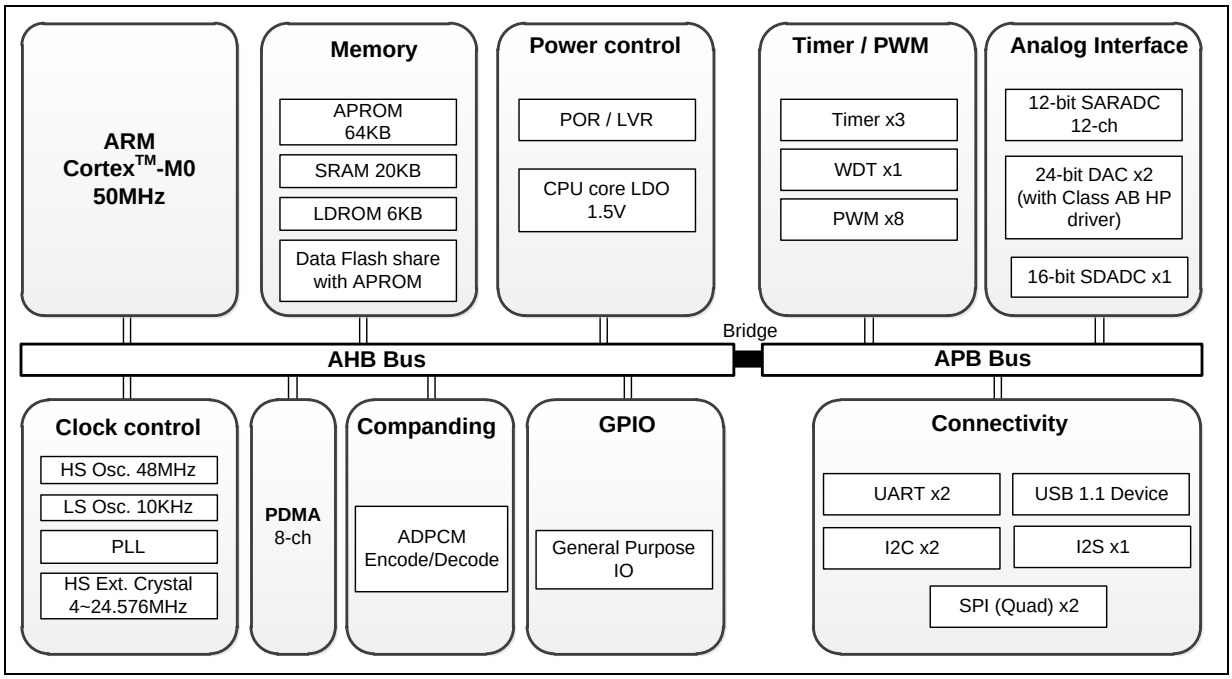


Figure 4-1 Functional Block Diagram 1

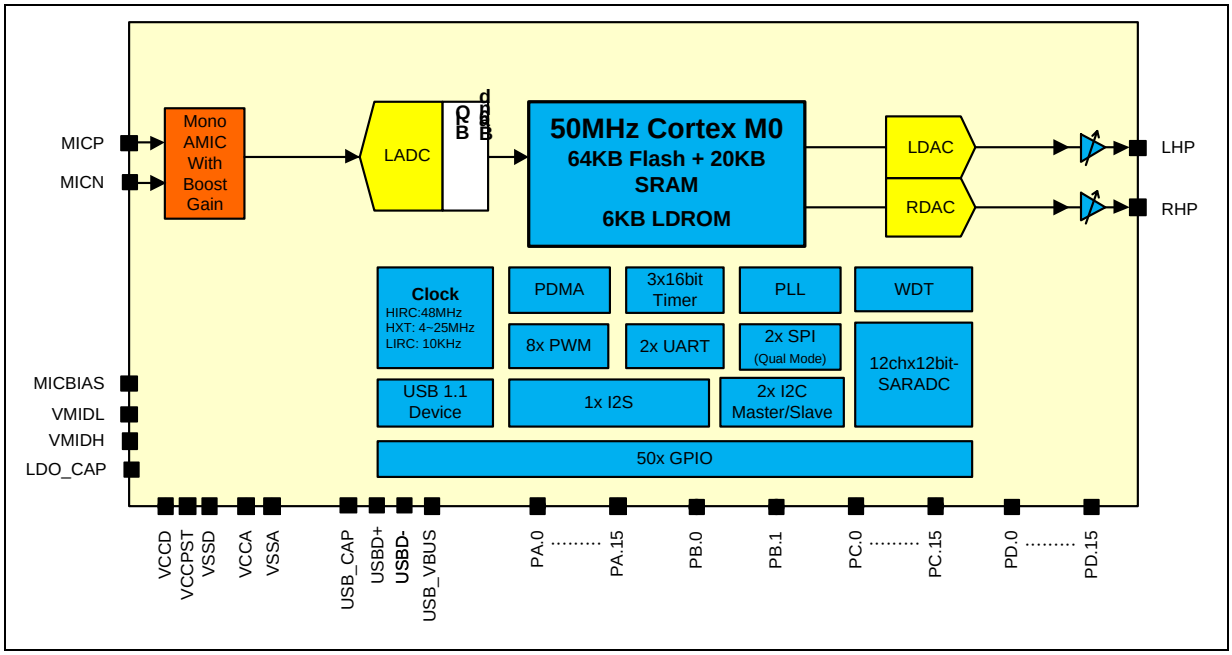
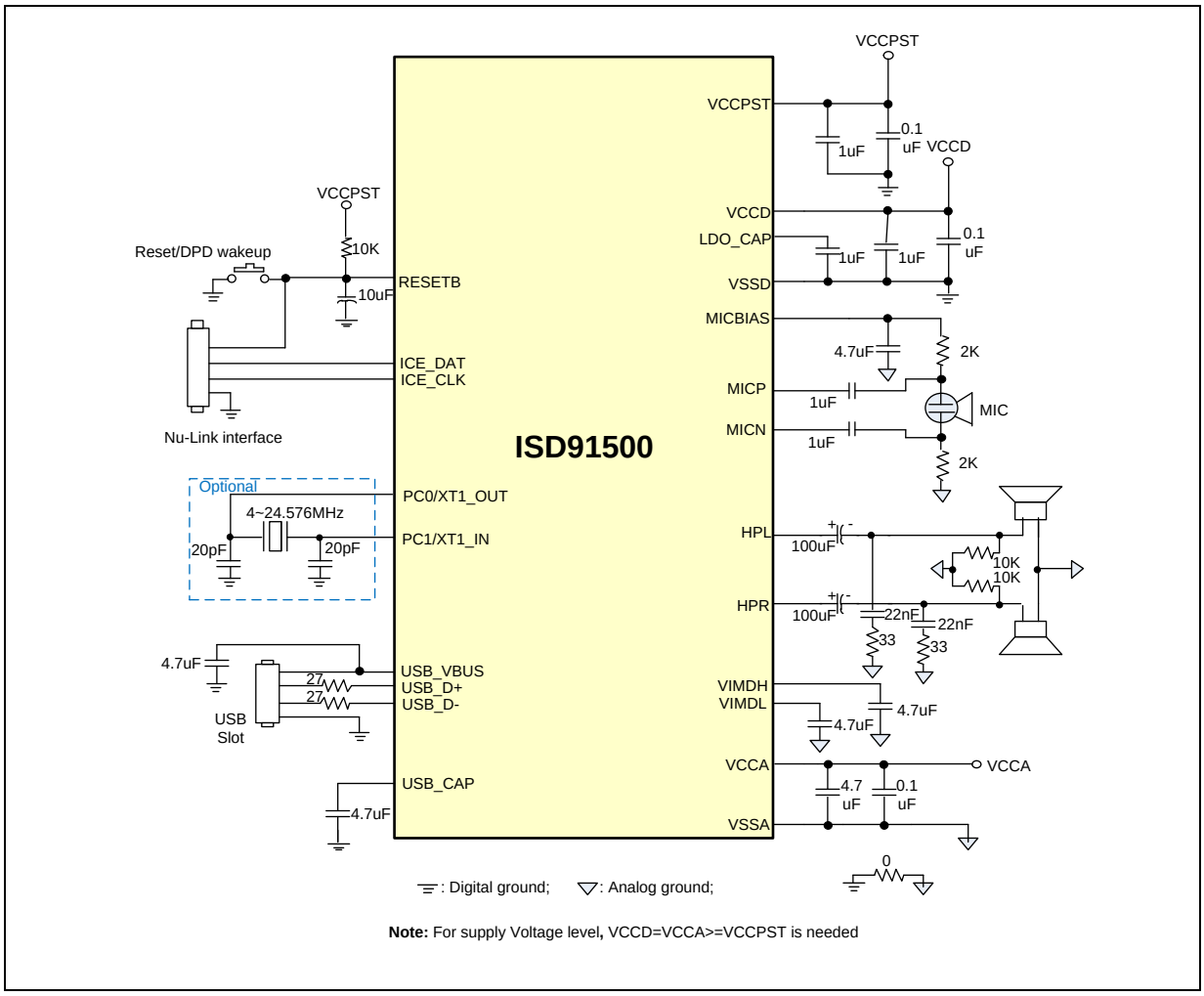


Figure 4-2 Functional Block Diagram 2

5 APPLICATION CIRCUIT



Note: For supply Voltage level**,** VCCD=VCCA>=VCCPST is needed

6 ELECTRICAL CHARACTERISTICS

6.1 Absolute Maximum Ratings

PARAMETER	SYMBOL	MIN	MAX	UNIT
DC Power Supply	VDD–VSS	-0.3	+3.6	V
Input Voltage	VIN	VSS-0.3	VDD+0.3	V
Oscillator Frequency	$1/t_{CLCL}$	0	50	MHz
Operating Temperature	TA	-40	+85	°C
Storage Temperature	TST	-55	+150	°C
Maximum Current into V_{DD}		-	120	mA
Maximum Current out of V_{SS}			120	mA
Maximum Current sunk by a I/O pin			35	mA
Maximum Current sourced by a I/O pin			35	mA
Maximum Current sunk by total I/O pins			100	mA
Maximum Current sourced by total I/O pins			100	mA

Note:

1. VDD is VCCD & VCCPST, VSS is VSSD.
2. Exposure to conditions beyond those listed under absolute maximum ratings may adversely affects the lift and reliability of the device.

Table 6.1-1 Absolute Maximum Ratings

6.2 DC Electrical Characteristics

(VDD-VSS=3.3V, TA=25°C, HCLK=49.152MHz, no load unless otherwise specified.)

PARAMETER	SYM.	SPECIFICATION				TEST CONDITIONS
		MIN.	TYP.	MAX.	UNIT	
Operation voltage	V_{DD}	1.7		3.6	V	
Power Ground	V_{SSD} V_{SSA}	-0.3			V	
Analog Operating Voltage	V_{CCA}	1.7		3.6	V	
Supply Current at Normal Run Mode (M0 run while(1) { } from Flash)	I_{DD1}		15		mA	enable all IP ,HCLK=49.152M Hz
	I_{DD1}		10		mA	disable all IP ,HCLK=49.152M Hz
Supply Current at Idle Mode (M0 run "WFI")	I_{IDLE1}		7		mA	enable all IP ,HCLK=49.152M Hz
	I_{IDLE2}		5		mA	disable all IP ,HCLK=49.152M Hz
Supply Current at DeepSleep Mode	I_{SB}			140	μA	disable all IP except LIRC is operating(Flash power off)
Supply Current at STOP Mode	I_{STP}			15	μA	disable all IP, except LIRC is operating (Flash power off)
Input current GPA/B/C/D with pull up active	I_{IN}	3.6		95	μA	V_{IN}=0V
Equivalent pull up resistance	R_{PU}	58	145	500	kOhm	V_{IN}=0V
Input Leakage Current GPA/B/C/D	I_{LK}	-1		+1	μA	0<V_{IN}<V_{DD}
Input Low Voltage GPA/B/C/D	V_{IL1}	-0.3		$0.2V_{DD}$	V	
Input High Voltage GPA/B/C/D	V_{IH1}	$0.7V_{DD}$		V_{DD}+0.2	V	V_{DD}=3.6V
Negative Going Threshold (Schmitt input)	V_{ILS}		$0.4V_{DD}$		V	Schmitt trigger selected
Positive Going Threshold (Schmitt input)	V_{IHS}		$0.6V_{DD}$		V	Schmitt trigger selected
Hysteresis Voltage	V_{HY}		$0.2V_{DD}$		V	Schmitt trigger selected
High level output voltage	V_{OH}	2.8			V	I_{OH}=4mA, VDD≥3.3V
Low level output voltage	V_{OL}			0.4	V	I_{OL}=3mA
Sink Current	I_{Osink}	4.3			mA	V_{OL}=0.2V, 3.3≤V_{DD}<3.6V
	I_{Osink}	2.1			mA	V_{OL}=0.2V, 1.8≤V_{DD}<3.3V
Source Current	$I_{Osource}$	2.0			mA	V_{OH}=V_{DD}-0.2V, 3.3≤V_{DD}<3.6V
	$I_{Osource}$	1.0			mA	V_{OH}=V_{DD}-0.2V, 1.8≤V_{DD}<3.3V

Notes:

1. VDD is VCCD & VCCPST, VSS is VSSD.
2. nRESET pin is a Schmitt trigger input and it follows VCCPST level.
3. VCCD & VCCA must be supplied same voltage level, and VCCD must larger or equal to VCCPST

Table 6.2-1 DC Electrical Characteristics

6.3 AC Electrical Characteristics

(V_{CCD}-V_{SSD}=3.3V, TA=25°C, no load unless otherwise specified.)

6.3.1 Internal High Speed RC Oscillator (HIRC) Characteristics

PARAMETER	CONDITION	MIN.	TYP.	MAX.	UNIT
Calibrated Output Frequency	49.152MHz selected		49.152		MHz
	48MHz selected		48		MHz
Startup time			90		ns
Stability Calibrated Internal Oscillator Frequency	T=25°C	-1		+1	%
	-40°C~+85°C	-4	-	+4	%

Table 6.3-1 Internal High Speed RC Oscillator (HIRC) Characteristics

6.3.2 Internal Low Speed RC Oscillator (LIRC) Characteristics

PARAMETER	CONDITION	MIN.	TYP.	MAX.	UNIT
Oscillation Frequency	T=25°C		10		kHz
Supply Current				1	μA

Table 6.3-2 Internal Low Speed RC Oscillator (LIRC) Characteristics

6.3.3 External High Speed Crystal (HXT) Characteristics

PARAMETER	CONDITION	MIN.	TYP.	MAX.	UNIT
Input clock frequency	External crystal	4	-	24.576	MHz
Temperature	-	-40	-	85	℃
V_{CCD}	-	1.8	-	3.6	V

Table 6.3-3 External High Speed Crystal (HXT) Characteristics

6.4 Analog Characteristics

(May be final after silicon mass production)

(V_{CCA}-V_{SSA}=3.3V, TA=25°C, no load unless otherwise specified.)

6.4.1 12-bit SAR ADC

PARAMETER	SYM.	MIN.	TYP.	MAX.	UNIT
Resolution	-	-	12		Bit
Offset error	EO	-4	±0.5	+4	LSB
Gain error (Transfer gain)	EG		±1	±3	%
Monotonic	-	Guaranteed			-
Sample rate	FS	-	-	200	ksps
Supply voltage	VCCA	2.4		3.6	V
Supply current (Avg.)	IDD	-	-	1.5	mA
Input voltage range	VIN	0	-	VCCA	V
ENOB		10			bit
No Missing Code			12		bit
Integral Non-Linearity Error	INL		±1		LSB
Differential Non-Linearity	DNL		±0.5		LSB

Note: Performance is not guaranteed when VCCA is out of spec.

Table 6.4-1 12-bit SARADC Characteristics

6.4.2 LDO15

PARAMETER	CONDITION	MIN.	TYP.	MAX.	UNIT
Input voltage		1.7	-	3.6	V
LDO output voltage			1.5		V

Table 6.4-2 LDO15 Characteristics

6.4.3 PGA

PARAMETER	SYM.	CONDITION	MIN.	TYP.	MAX.	UNIT
Operation Voltage	VCCA		2.4		3.6	V
Programmable gain			-12		34.5	dB
Programmable gain step size		Guaranteed Monotonic		1.5		dB

Note: Performance is not guaranteed when VCCA is out of spec.

Table 6.4-3 PGA Characteristics

6.4.4 MICBIAS

PARAMETER	SYM.	CONDITION	MIN.	TYP.	MAX.	UNIT
Bias voltage	$V_{MICBIAS}$		1.2,2.4,1.717,2.0 90%,65%,75%,50% VCCA			V
Output voltage tolerance			±5			%

Table 6.4-4 MICBIAS Characteristics

6.4.5 Low Voltage Reset and Brown-out Detector

BOD	SYMBOL	VALUE			UNIT
		MIN.	TYP.	MAX.	
Brown-out voltage	BOD_SEL[3:0] =1111		3.4		V
	BOD_SEL[3:0] =1110		3.4		V
	BOD_SEL[3:0] =1101		3.4		V
	BOD_SEL[3:0] =1100		3.4		V
	BOD_SEL[3:0] =1011		3.4		V
	BOD_SEL[3:0] =1010		3.4		V
	BOD_SEL[3:0] =1001		3.1		V
	BOD_SEL[3:0] =1000		3.0		V
	BOD_SEL[3:0] =0111		2.8		V
	BOD_SEL[3:0] =0110		2.6		V
	BOD_SEL[3:0] =0101		2.4		V
	BOD_SEL[3:0] =0100		2.2		V
	BOD_SEL[3:0] =0011		2.1		V
	BOD_SEL[3:0] =0010		2.0		V
	BOD_SEL[3:0] =0001		1.9		V
	BOD_SEL[3:0] =0000		1.8		V
LVR output	LVR		1.6		V
BOD Hysteresis	V_{hys}		60		mV

Table 6.4-5 Low Voltage Reset and Brown-out Detector Characteristics

6.4.6 Headphone Output (HPO)

PARAMETER	CONDITION	MIN.	TYP.	MAX.	UNIT
Operation Voltage		2.4		3.6	V
THD+N	VCCA@3.3V, 20mW with 32ohm load		-75		dB
SNR	VCCA@3.3V		90		dB

Table 6.4-6 Headphone Output Characteristics

6.4.7 SDADC

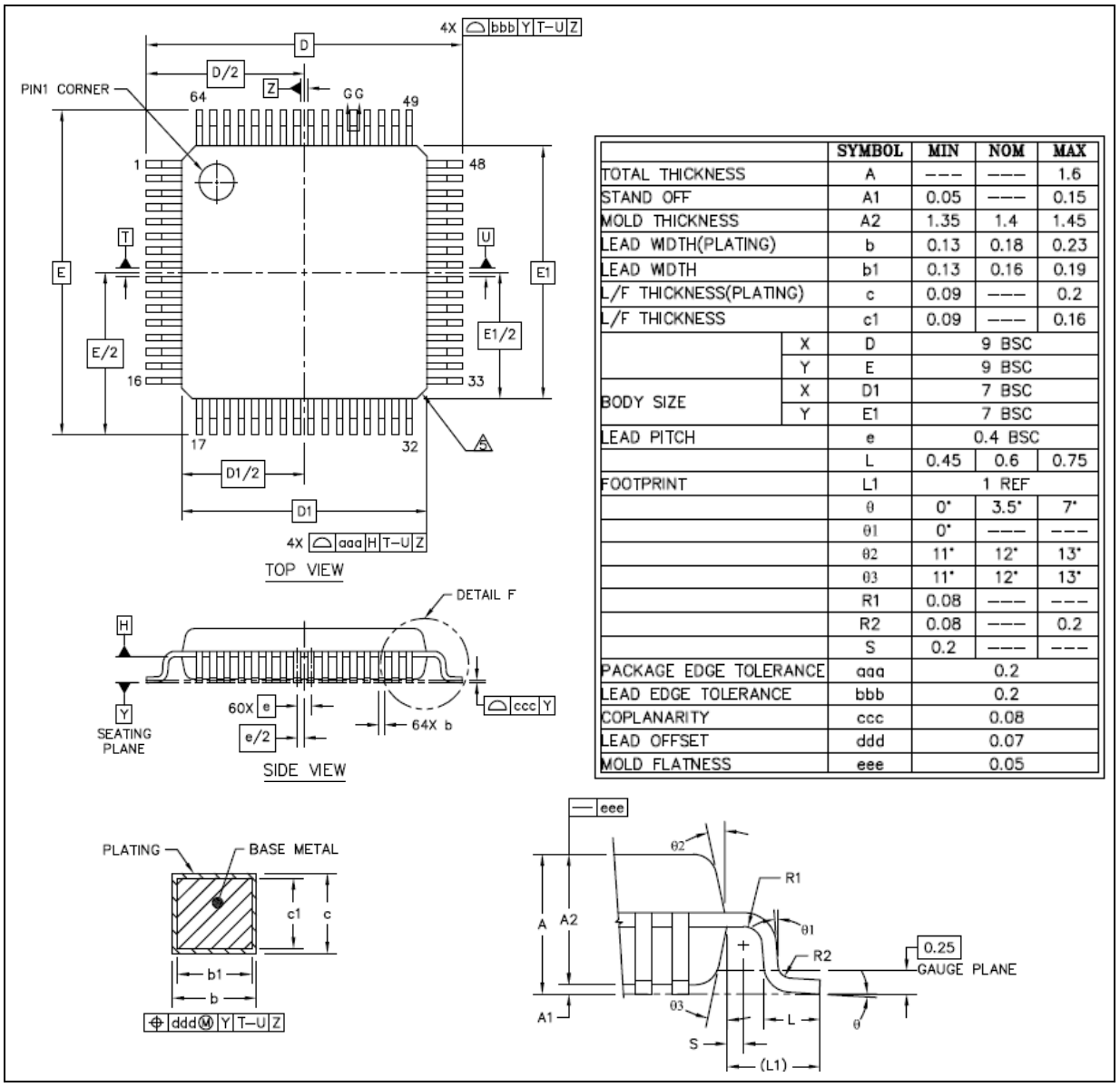
Conditions: VCCD = 3.3V, VCCA = 3.3V, T_A = +25°C, 1kHz signal, fs = 48kHz, 16-bit audio data, unless otherwise stated.

PARAMETER	SYMBOL	CONDITION	MIN.	TYP.	MAX.	UNIT
Analog to Digital Converter (SDADC)						
Operation Voltage	VCCA		2.4		3.6	V
Full scale input signal	V_{INFS}	PGAGAIN = 0dB		0.8		Vrms
Signal-to-noise ratio	SNR	Gain = 0dB, A-weighted		90		dB
Total harmonic distortion	THD+N	Input = -3dB FS input		-80		dB

Table 6.4-7 SDADC Characteristics

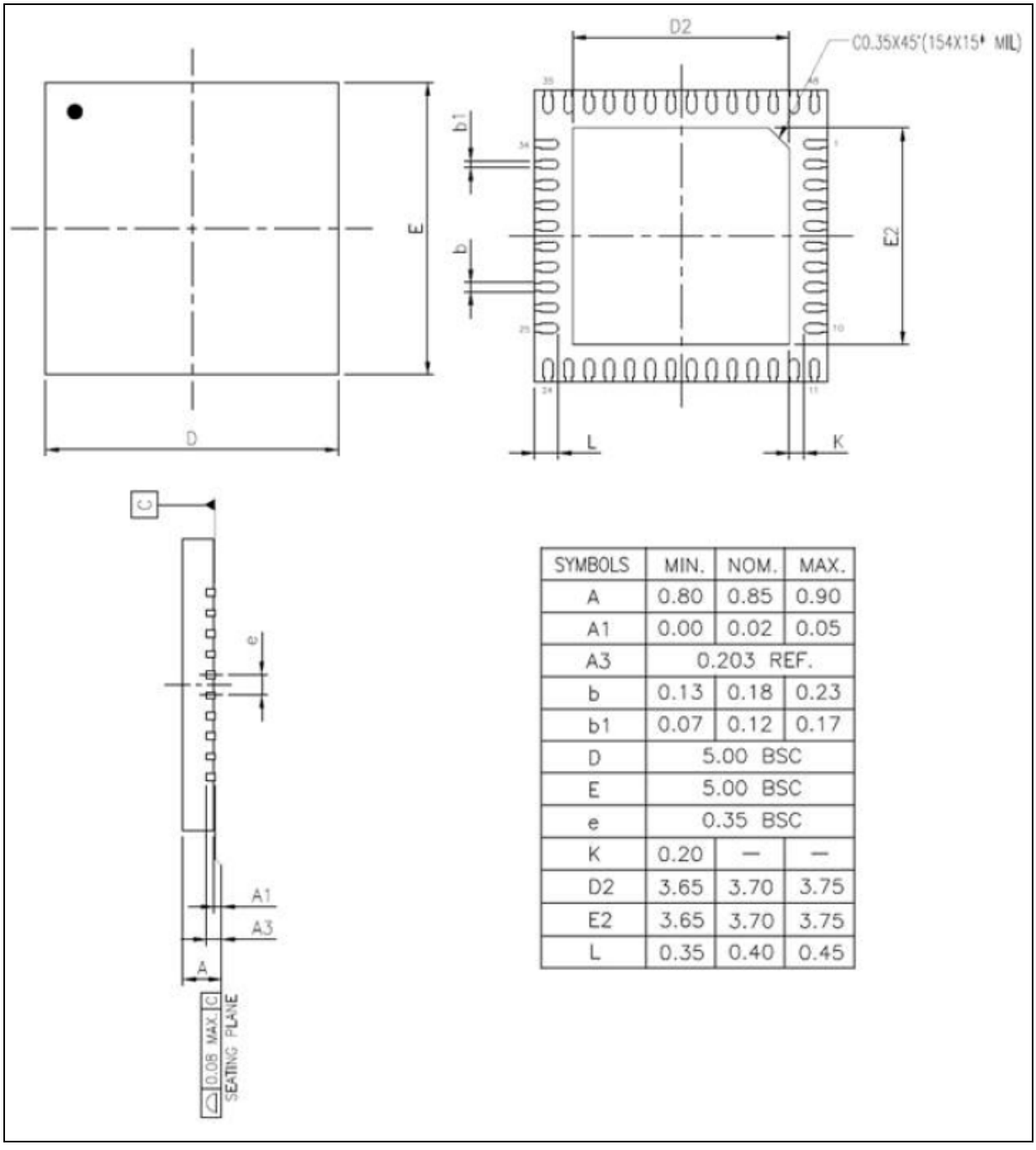
7 PACKAGE DIMENSIONS

7.1 LQFP 64L (7x7x1.4 mm^3 footprint 2.0 mm)



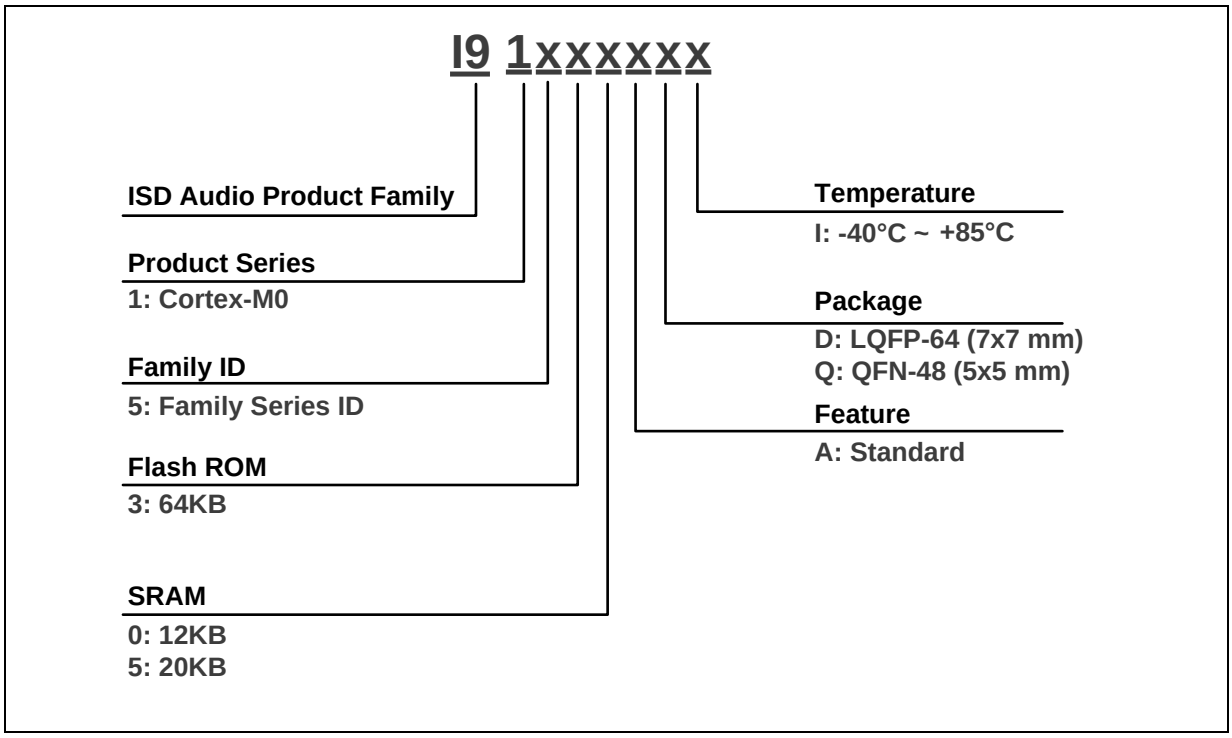
		SYMBOL	MIN	NOM	MAX
TOTAL THICKNESS		A	---	---	1.6
STAND OFF		A1	0.05	---	0.15
MOLD THICKNESS		A2	1.35	1.4	1.45
LEAD WIDTH(PLATING)		b	0.13	0.18	0.23
LEAD WIDTH		b1	0.13	0.16	0.19
L/F THICKNESS(PLATING)		c	0.09	---	0.2
L/F THICKNESS		c1	0.09	---	0.16
BODY SIZE	X	D	9 BSC		
	Y	E	9 BSC		
	X	D1	7 BSC		
	Y	E1	7 BSC		
LEAD PITCH		e	0.4 BSC		
		L	0.45	0.6	0.75
FOOTPRINT		L1	1 REF		
		θ	0°	3.5°	7°
		θ1	0°	---	---
		θ2	11°	12°	13°
		θ3	11°	12°	13°
		R1	0.08	---	---
		R2	0.08	---	0.2
		S	0.2	---	---
PACKAGE EDGE TOLERANCE		aaa	0.2		
LEAD EDGE TOLERANCE		bbb	0.2		
COPLANARITY		ccc	0.08		
LEAD OFFSET		ddd	0.07		
MOLD FLATNESS		eee	0.05		

7.2 QFN 48 (5x5x0.9 mm^3 EP SIZE 3.7x3.7 mm)



SYMBOLS	MIN.	NOM.	MAX.
A	0.80	0.85	0.90
A1	0.00	0.02	0.05
A3		0.203 REF.	
b	0.13	0.18	0.23
b1	0.07	0.12	0.17
D		5.00 BSC	
E		5.00 BSC	
e		0.35 BSC	
K	0.20	—	—
D2	3.65	3.70	3.75
E2	3.65	3.70	3.75
L	0.35	0.40	0.45

8 ORDERING INFORMATION



Package Number	Part Number	Ordering Number	Flash	SRAM	Package	Notes
ISD91530AQI	ISD91530AQI	I91530AQI	64KB	12KB	QFN-48	
ISD91530ADI	ISD91530ADI	I91530ADI	64KB	12KB	LQFP-64	
ISD91535AQI	ISD91535AQI	I91535AQI	64KB	20KB	QFN-48	
ISD91535ADI	ISD91535ADI	I91535ADI	64KB	20KB	LQFP-64	
ISD91535H02QI	ISD91535H02QI	I91535H02QI	64KB	20KB	QFN-48	Special part - Independent IO power Teams library support
ISD91535H02DI	ISD91535H02DI	I91535H02DI	64KB	20KB	LQFP-64	Special part - Independent IO power Teams library support

9 REVISION HISTORY

VERSION	DATE	DESCRIPTION	NOTE
1.0	Jul 1, 2021	Formal version release	
1.1	Jul 30, 2021	Update SDADC & DAC operation voltage spec Add note for VCCD = VCCA in feature and application SCH	
2.0	Sep 30, 2021	Update pin diagram & description. Update alternative function Update application SCH	
2.1	Mar 4, 2022	Update DC characteristic for Note2 Update feature for BOD & LVR description Update DAC digital volume range in feature Update pin diagram & description Update Ordering information	
2.2	Mar 18, 2022	Update DAC AC characteristic table	
2.3	Aug 18, 2022	Update format Update General Description	
2.4	Feb. 8, 2023	Added “Package is Halogen-free, RoHS-compliant and TSCA-compliant” in section 2 Update format	

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