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ISL12059

Low Cost and Low Power I^2C Bus Real Time Clock/Calendar Low Power and Low Cost RTC

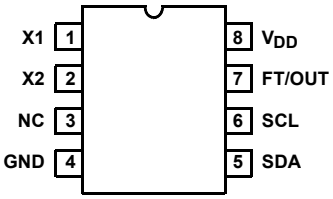
FN6757
Rev 0.00
Jun 15, 2009

The ISL12059 device is a low power real time clock with clock/calendar, and 512Hz/digital output function.

The oscillator uses an external, low-cost 32.768kHz crystal. The real time clock tracks time with separate registers for hours, minutes, and seconds. The device has calendar registers for date, month, year and day of the week. The calendar is accurate through 2099, with automatic leap year correction.

Pinout

ISL12059
(8 LD SOIC)
TOP VIEW



Features

- Real Time Clock/Calendar
  - Tracks Time in Hours, Minutes, and Seconds
  - Day of the Week, Date, Month, and Year
- 512Hz Frequency Output
- I^2C Bus
  - 400kHz Data Transfer Rate
- Small Package Option
  - 8 Ld SOIC Package
  - Pb-Free (RoHS Compliant)
- Low Cost 3V Alternative to M41T00S, DS1340 and ISL12008

Applications

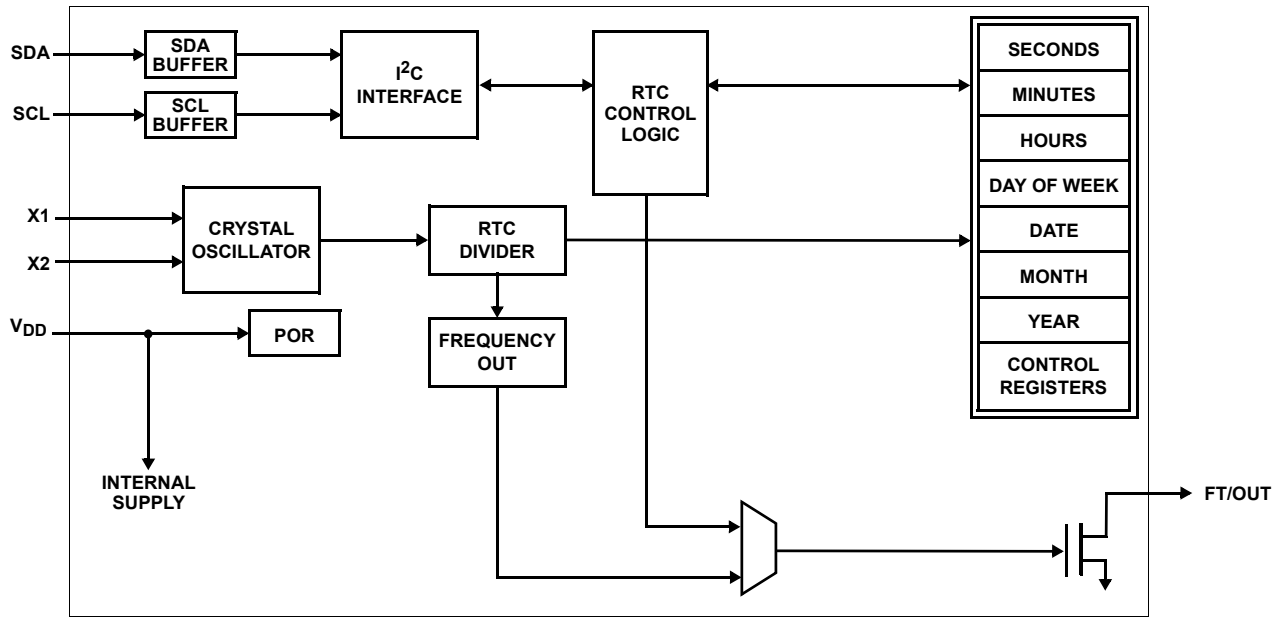
- Utility Meters
- HVAC Equipment
- Audio/Video Components
- Set-Top Box/Television
- Modems
- Network Routers, Hubs, Switches, Bridges
- Cellular Infrastructure Equipment
- Fixed Broadband Wireless Equipment
- Pagers/PDA
- Point Of Sale Equipment
- Test Meters/Fixtures
- Office Automation (Copiers, Fax)
- Home Appliances
- Computer Products
- Other Industrial/Medical/Automotive

Ordering Information

PART NUMBER (Note)	PART MARKING	V_{DD} RANGE (V)	TEMP. RANGE (°C)	PACKAGE (Pb-Free)	PKG. DWG. #
ISL12059IBZ	12059 IBZ	1.4 to 3.6	-40 to +85	8 Ld SOIC	M8.15
ISL12059IBZ-T*	12059 IBZ	1.4 to 3.6	-40 to +85	8 Ld SOIC (Tape and Reel)	M8.15

*Please refer to TB347 for details on reel specifications.
NOTE: These Intersil Pb-free plastic packaged products employ special Pb-free material sets, molding compounds/die attach materials, and 100% matte tin plate plus anneal (e3 termination finish, which is RoHS compliant and compatible with both SnPb and Pb-free soldering operations). Intersil Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020.

Block Diagram



Pin Descriptions

PIN NUMBER	SYMBOL	DESCRIPTION
1	X1	The X1 pin is the input of an inverting amplifier and is intended to be connected to one pin of an external 32.768kHz quartz crystal.
2	X2	The X2 pin is the output of an inverting amplifier and is intended to be connected to one pin of an external 32.768kHz quartz crystal.
3	NC	No Connection. Can be connected to GND or left floating.
4	GND	Ground
5	SDA	Serial Data (SDA) is a bi-directional pin used to transfer serial data into and out of the device. It has an open drain output and may be wire OR'ed with other open drain or open collector outputs.
6	SCL	The Serial Clock (SCL) input is used to clock all serial data into and out of the device.
7	FT/OUT	512Hz Frequency Output or digital output pin. The function is set via the configuration register. This pin is open drain and requires an external pull-up resistor. It has a default output of high impedance at power-up.
8	V_{DD}	Power supply

Absolute Maximum Ratings

Voltage on V_{DD} Pin (respect to GND) . . . . . -0.2V to 4V
Voltage on FT/OUT, SCL and SDA Pins
(respect to GND) . . . . . -0.2V to 6V
Voltage on X1 and X2 Pins (respect to GND) . . . . . -0.2V to 4V
ESD Rating ((Per MIL-STD-883 Method 3014)
Human Body Model . . . . . >4kV
Machine Model . . . . . >350V

Thermal Information

Thermal Resistance (Typical, Note 1) θ_{JA} (°C/W)
8 Lead SOIC 120
Storage Temperature Range . . . . . -65°C to +150°C
Pb-Free Reflow Profile. . . . . .see link below
http://www.intersil.com/pbfree/Pb-FreeReflow.asp

CAUTION: Do not operate at or near the maximum ratings listed for extended periods of time. Exposure to such conditions may adversely impact product reliability and result in failures not covered by warranty.

NOTE:

1. θ_{JA} is measured with the component mounted on a high effective thermal conductivity test board in free air. See Tech Brief TB379 for details.

DC Operating Characteristics – RTC

Temperature = -40°C to +85°C unless otherwise stated.

SYMBOL	PARAMETER	CONDITIONS	MIN (Note 4)	TYP (Note 3)	MAX (Note 4)	UNITS	NOTES
V_{DD}	Main Power Supply		1.8		3.6	V	
V_{DDT}	Timekeeping Power Supply		1.4		1.8	V	
I_{DD1}	Standby Supply Current	V_{DD} = 3.6V		600	950	nA	2, 8
		V_{DD} = 3.0V		500		nA	
I_{DD2}	Timekeeping Current	V_{DD} = 1.8V		400	650	nA	2, 8
		V_{DD} = 1.4V		350		nA	
I_{DD3}	Supply Current With I^2C Active at Clock Speed of 400kHz	V_{DD} = 3.6V		15	40	µA	2
I_{LI}	Input Leakage Current on SCL		-100		100	nA	
I_{LO}	I/O Leakage Current on SDA		-100		100	nA	
FT/OUT							
V_{OL}	Output Low Voltage	V_{DD} = 1.8V, I_{OL} = 3mA			0.4	V	

Serial Interface Specifications

Over the recommended operating conditions unless otherwise specified.

SYMBOL	PARAMETER	TEST CONDITIONS	MIN (Note 4)	TYP (Note 3)	MAX (Note 4)	UNITS	NOTES
SERIAL INTERFACE SPECS							
V_{IL}	SDA and SCL Input Buffer LOW Voltage		-0.3		0.3 x V_{DD}	V	
V_{IH}	SDA and SCL Input Buffer HIGH Voltage		0.7 x V_{DD}		5.5	V	
Hysteresis	SDA and SCL Input Buffer Hysteresis			0.04 x V_{DD}		V	
V_{PULLUP}	Maximum Pull-up Voltage on SDA during I^2C Communication				V_{DD}+2	V	7
V_{OL}	SDA Output Buffer LOW Voltage, Sinking 3mA	V_{DD} > 1.8V, V_{PULLUP} = 5.0V	0		0.4	V	
Cpin	SDA and SCL Pin Capacitance	T_A = +25°C, f = 1MHz, V_{DD} = 5V, V_{IN} = 0V, V_{OUT} = 0V			10	pF	5, 6
f_{SCL}	SCL Frequency				400	kHz	
t_{IN}	Pulse width Suppression Time at SDA and SCL Inputs	Any pulse narrower than the max spec is suppressed			50	ns	

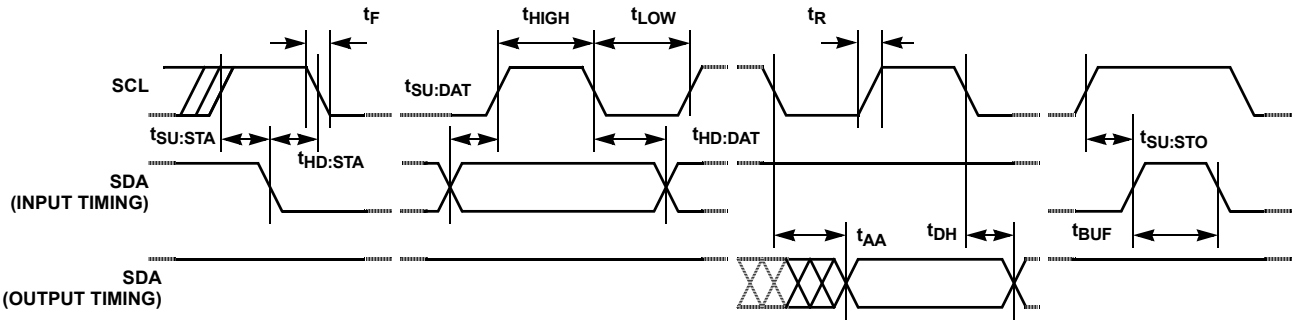
Serial Interface Specifications Over the recommended operating conditions unless otherwise specified. **(Continued)**

SYMBOL	PARAMETER	TEST CONDITIONS	MIN (Note 4)	TYP (Note 3)	MAX (Note 4)	UNITS	NOTES
t_{AA}	SCL Falling Edge to SDA Output Data Valid	SCL falling edge crossing 30% of V_{DD}, until SDA exits the 30% to 70% of V_{DD} window			900	ns	7
t_{BUF}	Time the Bus Must Be Free Before the Start of a New Transmission	SDA crossing 70% of V_{DD} during a STOP condition, to SDA crossing 70% of V_{DD} during the following START condition	1300			ns	
t_{LOW}	Clock LOW Time	Measured at the 30% of V_{DD} crossing	1300			ns	
t_{HIGH}	Clock HIGH Time	Measured at the 70% of V_{DD} crossing	600			ns	
$t_{SU:STA}$	START Condition Setup Time	SCL rising edge to SDA falling edge. Both crossing 70% of V_{DD}	600			ns	
$t_{HD:STA}$	START Condition Hold Time	From SDA falling edge crossing 30% of V_{DD} to SCL falling edge crossing 70% of V_{DD}	600			ns	
$t_{SU:DAT}$	Input Data Setup Time	From SDA exiting the 30% to 70% of V_{DD} window, to SCL rising edge crossing 30% of V_{DD}	100			ns	
$t_{HD:DAT}$	Input Data Hold Time	From SCL falling edge crossing 30% of V_{DD} to SDA entering the 30% to 70% of V_{DD} window	0		900	ns	
$t_{SU:STO}$	STOP Condition Setup Time	From SCL rising edge crossing 70% of V_{DD}, to SDA rising edge crossing 30% of V_{DD}	600			ns	
$t_{HD:STO}$	STOP Condition Hold Time	From SDA rising edge to SCL falling edge. Both crossing 70% of V_{DD}	600			ns	
t_{DH}	Output Data Hold Time	From SCL falling edge crossing 30% of V_{DD}, until SDA enters the 30% to 70% of V_{DD} window	0			ns	
t_R	SDA and SCL Rise Time	From 30% to 70% of V_{DD}	20 + 0.1xCb		300	ns	5, 6
t_F	SDA and SCL Fall Time	From 70% to 30% of V_{DD}	20 + 0.1xCb		300	ns	5, 6, 7
Cb	Capacitive Loading of SDA or SCL	Total on-chip and off-chip	10		400	pF	5, 6
Rpu	SDA and SCL Bus Pull-Up Resistor Off-Chip	Maximum is determined by t_R and t_F For Cb = 400pF, max is about 2kΩ to~2.5kΩ For Cb = 40pF, max is about 15kΩ to ~20kΩ	1			kΩ	5, 6

NOTES:

2. FT/OUT Inactive.
3. Typical values are for T = +25°C and 3.3V supply voltage.
4. Parameters with MIN and/or MAX limits are 100% tested at +25°C, unless otherwise specified. Temperature limits established by characterization and are not production tested.
5. Limits should be considered typical and are not production tested.
6. These are I^2C specific parameters and are not production tested, however, they are used to set conditions for testing devices to validate specification.
7. Parts will work with SDA pull-up voltage above the V_{PULLUP} limit but the t_{AA} and $t_F$in the I^2C parameters are not guaranteed.
8. Specified at +25°C.

SDA vs SCL Timing



Symbol Table

WAVEFORM	INPUTS	OUTPUTS
	Must be steady	Will be steady
	May change from LOW to HIGH	Will change from LOW to HIGH
	May change from HIGH to LOW	Will change from HIGH to LOW
	Don't Care: Changes Allowed	Changing: State Not Known
	N/A	Center Line is High Impedance

EQUIVALENT AC OUTPUT LOAD CIRCUIT FOR V_{DD} = 3.0V

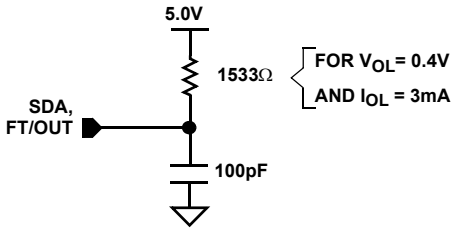


FIGURE 1. STANDARD OUTPUT LOAD FOR TESTING THE DEVICE WITH V_{DD} = 3.0V, V_{PULLUP} = 5.0V

Typical Performance Curves

Temperature is +25°C unless otherwise specified.

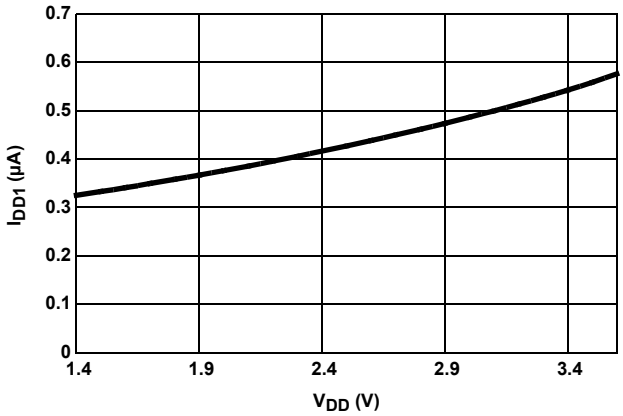


FIGURE 2. I_{DD1} vs V_{DD}

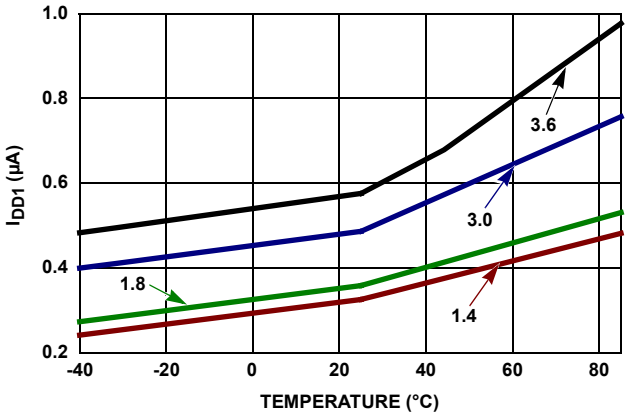


FIGURE 3. I_{DD1} vs TEMPERATURE

General Description

The ISL12059 device is a low power real time clock with clock/calendar, and 512Hz/Digital Output function.

The oscillator uses an external, low-cost 32.768kHz crystal. The real time clock tracks time with separate registers for hours, minutes, and seconds. The device has calendar registers for date, month, year and day of the week. The calendar is accurate through 2099, with automatic leap year correction.

Pin Description

X1, X2

The X1 and X2 pins are the input and output, respectively, of an inverting amplifier. An external 32.768kHz quartz crystal is used with the ISL12059 to supply a timebase for the real time clock. Refer to Figure 4.

The device can also be driven directly from a 32.768kHz square wave source with peak-to-peak voltage from 0V to VDD at X1 pin with X2 pin floating.

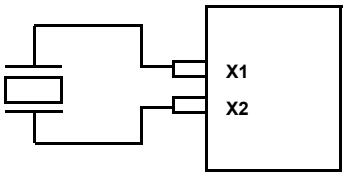


FIGURE 4. RECOMMENDED CRYSTAL CONNECTION

FT/OUT(512Hz Frequency Output/Logic Output)

This dual function pin can be used as a 512Hz frequency output or a simple digital output control via I^2C. The FT/OUT mode is selected via the OUT and FT control bits of the control/status register (address 07h). The FT/OUT pin is an open drain output that requires the use of a pull-up resistor, and it can accept a pull-up voltage up to 5.5V. This pin is at high impedance at power-up.

Serial Clock (SCL)

The SCL input is used to clock all serial data into and out of the device. The input buffer on this pin is always active (not gated). The SCL pin can accept a logic high voltage up to 5.5V.

Serial Data (SDA)

SDA is a bi-directional pin used to transfer data into and out of the device. It has an open drain output and may be ORed with other open drain or open collector outputs. The input buffer is always active (not gated) in normal mode.

An open drain output requires the use of a pull-up resistor, and it can accept a pull-up voltage up to 5.5V. The output circuitry controls the fall time of the output signal with the use of a slope controlled pull-down. The circuit is designed for 400kHz I^2C interface speeds.

NOTE: Parts will work with SDA pull-up voltage above the V_{PULLUP} limit but the t_{AA} and t_F in the I^2C parameters are not guaranteed.

V_{DD}, GND

Chip power supply and ground pins. The device will have full operation with a power supply from 1.8V to 3.6V, and timekeeping function with a power supply from 1.4V to 3.6V.

A 0.1µF decoupling capacitor is recommended on the V_{DD} pin to ground.

NC (No Connection)

The NC pin is not connected to the die. The pin can be connected to GND or left floating.

Functional Description

Real Time Clock Operation

The Real Time Clock (RTC) uses an external 32.768kHz quartz crystal to maintain an accurate internal representation of second, minute, hour, day of week, date, month, and year. The RTC also has leap-year correction. The RTC also corrects for months having fewer than 31 days. The clock will begin incrementing after power-up with valid oscillator condition.

TABLE 1. REGISTER MEMORY MAP

ADDR.	SECTION	REG NAME	BIT								REG	
			7	6	5	4	3	2	1	0	RANGE	DEFAULT
00h	RTC	SC	ST	SC22	SC21	SC20	SC13	SC12	SC11	SC10	0 to 59	00h
01h		MN	OF	MN22	MN21	MN20	MN13	MN12	MN11	MN10	0 to 59	80h
02h		HR	CEB	CB	HR21	HR20	HR13	HR12	HR11	HR10	0 to 23	00h
03h		DW	0	0	0	0	0	DW12	DW11	DW10	1 to 7	01h
04h		DT	0	0	DT21	DT20	DT13	DT12	DT11	DT10	1 to 31	01h
05h		MO	0	0	0	MO20	MO13	MO12	MO11	MO10	1 to 12	01h
06h		YR	YR23	YR22	YR21	YR20	YR13	YR12	YR11	YR10	0 to 99	00h
07h	Control	FT/OUT	OUT	FT	0	0	0	0	0	PF	N/A	81h

Accuracy of the Real Time Clock

The accuracy of the Real Time Clock depends on the frequency of the quartz crystal that is used as the time base for the RTC. Since the resonant frequency of a crystal is temperature dependent, the RTC performance will also be dependent upon temperature. The frequency deviation of the crystal is a function of the turnover temperature of the crystal from the crystal's nominal frequency. For example, a ~20ppm frequency deviation translates into an accuracy of ~1 minute per month. These parameters are available from the crystal manufacturer.

I^2C Serial Interface

The ISL12059 has an I^2C serial bus interface that provides access to the real time clock registers, and control and status registers. The I^2C serial interface is compatible with other industry I^2C serial bus protocols using a bi-directional data signal (SDA) and a clock signal (SCL).

Register Descriptions

The registers are accessible following a slave byte of "1101000x" and reads or writes to addresses [00h:07h]. The defined addresses and default values are described in Table 1.

REGISTER ACCESS

The contents of the registers can be modified by performing a byte or a page write operation directly to any register address. The address will wrap around from 07h to 00h.

The registers are divided into 2 sections. These are:

1. Real Time Clock (7 bytes): Address 00h to 06h.
2. Control and Status (1 byte): Address 07h.

There are no addresses above 07h.

A register can be read by performing a random read at any address at any time. This returns the contents of that register location. Additional registers are read by performing a sequential read. For the RTC registers, the read instruction latches all clock registers into a buffer, so an update of the clock does not change the time being read. A sequential read will not result in the output of data from the memory array. At the end of a read, the master supplies a stop condition to end the operation and free the bus. After a read or write instruction, the address remains at the previous address +1 so the user can execute a current address read and continue reading the next register.

Real Time Clock Registers

Addresses [00h to 06h]

RTC REGISTERS (SC, MN, HR, DW, DT, MO, YR)

These registers depict BCD representations of the time. As such, SC (Seconds, address 00h) and MN (Minutes, address 01h) range from 0 to 59, HR (Hour, address 02h) is in a 24-hour mode with a range from 0 to 23, DW (Day of the Week, address 03h) is 0 to 6, DT (Date, address 04h) is 1 to 31, MO (Month, address 05h) is 1 to 12, and YR (Year, address 06h) is 0 to 99.

The DW register provides a Day of the Week status and uses three bits DW2 to DW0 to represent the seven days of the week. The counter advances in the cycle 1-2-3-4-5-6-7-1-2-…
The assignment of a numerical value to a specific day of the week is arbitrary and may be decided by the system software designer.

Bit D7 of SC register contain the crystal enable/disable bit (ST). Setting ST to "1" will disable the crystal from oscillating and stop the counting in RTC register for the device to enter into power saving mode. The ST bit is set to "0" on power-up for normal operation.

Bit D7 of MN register contain the Oscillator Fail Indicator bit (OF). This bit is set to a "1" when there is no oscillation on X1 pin. The OSF bit can only be reset by having an oscillation on X1 and a write operation to reset it.

Bits D6 and D7 of HR register (century/hours register) contain the century enable bit (CEB) and the century bit (CB). Setting CEB to a '1' will cause CB to toggle, either from '0' to '1' or from '1' to '0' at the turn of the century (depending upon its initial state). If CEB is set to a '0', CB will not toggle.

LEAP YEARS

Leap years add the day February 29 and are defined as those years that are divisible by 4. Years divisible by 100 are not leap years, unless they are also divisible by 400. This means that the year 2000 is a leap year, the year 2100 is not. The ISL12059 does not correct for the leap year in the year 2100.

Control and Status Register

FT/OUT Control Register (FT/OUT) [Address 07h]

TABLE 2. FT/OUT CONTROL REGISTER

ADDR	7	6	5	4	3	2	1	0
07h	OUT	FT	0	0	0	0	0	PF
Default	1	0	0	0	0	0	0	1

POWER FAILURE BIT (PF)

This bit is set to a “1” after a total power failure. This is a read only bit that is set by hardware (ISL12059 internally) when the device powers up after having lost power to the device. On power-up after a total power failure, all registers are set to their default states. The first valid write to the RTC section after a complete power failure resets the PF bit to “0” (writing one byte is sufficient).

512Hz FREQUENCY OUTPUT ENABLE BIT (FT)

This bit enables/disables the 512Hz frequency output on the FT/OUT pin. When the FT is set to “1”, the FT/OUT pin outputs the 512Hz frequency, regardless of the Digital Output selection bit (OUT). When the FT is set to “0”, the 512Hz frequency is disabled and the function of FT/OUT pin is selected by the Digital Output selection bit (OUT). The FT bit is set to “0” on power-up.

DIGITAL OUTPUT SELECTION BIT (OUT)

This bit selects the output status of the FT/OUT. 512Hz Frequency Output Enable bit (FT) must be set to “0” (disable) for OUT to take effect on FT/OUT pin. When the OUT is set to “1”, and FT is set to “0”, the FT/OUT is set to logic level high. The FT/OUT voltage level is controlled by the voltage of the pull-up resistor on FT/OUT pin. When the OUT is set to “0”, and FT is set to “0”, the FT/OUT is set to logic level low. The voltage level of FT/OUT is set to VOL level. The OUT bit is set to “1” on power-up.

I^2C Serial Interface

The ISL12059 supports a bi-directional bus oriented protocol. The protocol defines any device that sends data onto the bus as a transmitter and the receiving device as the receiver. The device controlling the transfer is the master and the device being controlled is the slave. The master always initiates data transfers and provides the clock for both transmit and receive operations. Therefore, the ISL12059 operates as a slave device in all applications.

All communication over the I^2C bus is conducted by sending the MSB of each byte of data first.

Protocol Conventions

Data states on the SDA line can change only during SCL LOW periods. SDA state changes during SCL HIGH are reserved for indicating START and STOP conditions (see Figure 5). On power-up of the ISL12059, the SDA pin is in the input mode.

All I^2C interface operations must begin with a START condition, which is a HIGH to LOW transition of SDA while SCL is HIGH. The ISL12059 continuously monitors the SDA and SCL lines for the START condition and does not respond to any command until this condition is met (see Figure 5). A START condition is ignored during the power-up sequence.

All I^2C interface operations must be terminated by a STOP condition, which is a LOW to HIGH transition of SDA while SCL is HIGH (see Figure 5). A STOP condition at the end of a read operation or at the end of a write operation to memory only places the device in its standby mode.

An acknowledge (ACK) is a software convention used to indicate a successful data transfer. The transmitting device, either master or slave, releases the SDA bus after transmitting 8 bits. During the ninth clock cycle, the receiver pulls the SDA line LOW to acknowledge the reception of the 8 bits of data (see Figure 6).

The ISL12059 responds with an ACK after recognition of a START condition followed by a valid Identification Byte, and once again after successful receipt of an Address Byte. The ISL12059 also responds with an ACK after receiving a Data Byte of a write operation. The master must respond with an ACK after receiving a Data Byte of a read operation.

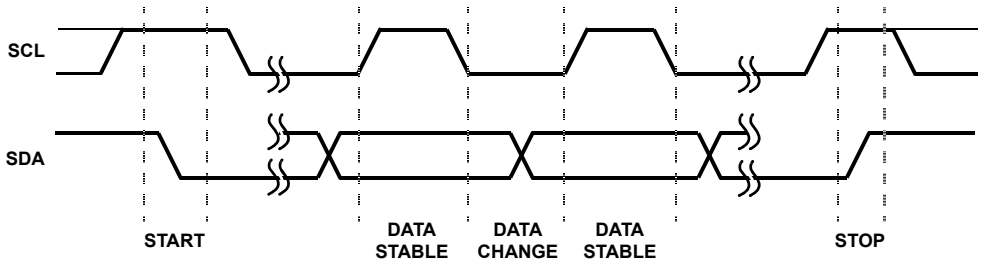


FIGURE 5. VALID DATA CHANGES, START, AND STOP CONDITIONS

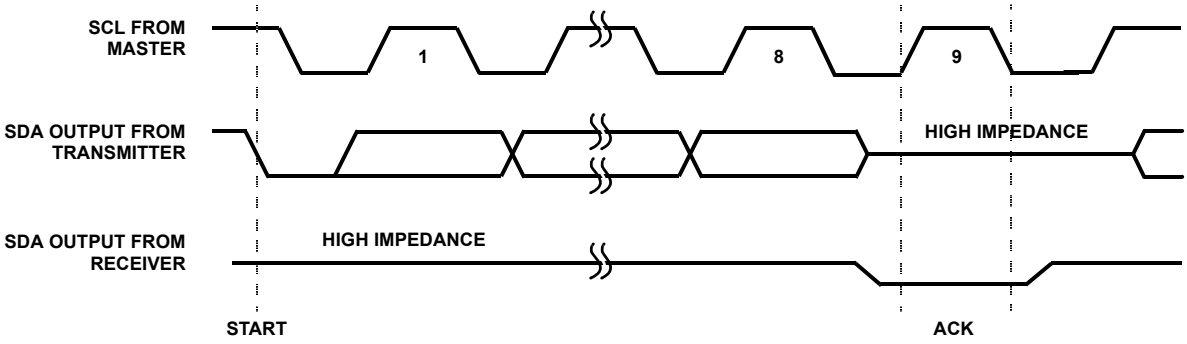


FIGURE 6. ACKNOWLEDGE RESPONSE FROM RECEIVER

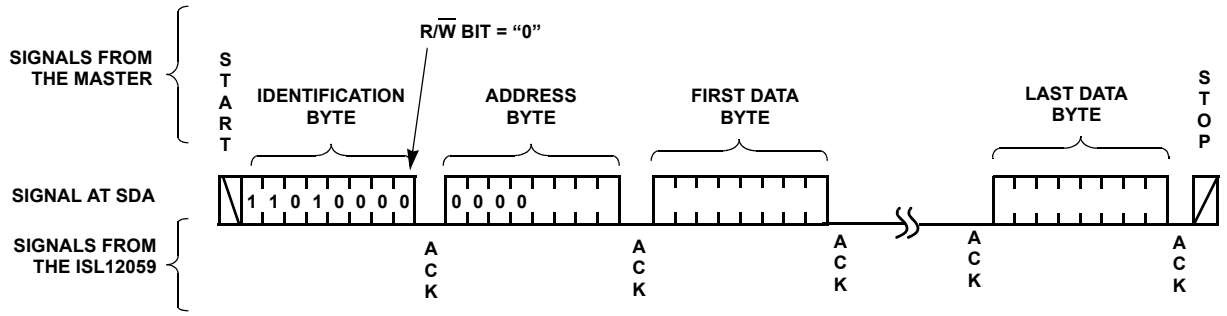


FIGURE 7. SEQUENTIAL BYTE WRITE SEQUENCE

Device Addressing

Following a start condition, the master must output a Slave Address Byte. The 7 MSBs of the Slave Address Byte are the device identifier bits, and the device identifier bits are "1101000".

The last bit of the Slave Address Byte defines a read or write operation to be performed. When this R/$\overline{W}$ bit is a "1", then a read operation is selected. A "0" selects a write operation (refer to Figure 8).

After loading the entire Slave Address Byte from the SDA bus, the ISL12059 compares the device identifier bits with "1101000". Upon a correct compare, the device outputs an acknowledge on the SDA line.

Following the Slave Address Byte is a one byte register address. The register address is supplied by the master device. On power-up the internal address counter is set to address 0h, so a current address read of the RTC array starts at address 0h. When required, as part of a random read, the master must supply the 1 Word Address Bytes as shown in Figure 9.

In a random read operation, the slave byte in the "dummy write" portion must match the slave byte in the "read" section. For a random read of the Clock/Control Registers, the slave byte must be "1101000x" in both places.

Write Operation

A Write operation requires a START condition, followed by a valid Identification Byte, a valid Address Byte, a Data Byte, and a STOP condition. After each of the three bytes, the ISL12059 responds with an ACK. At this time, the I^2C bus enters a standby state.

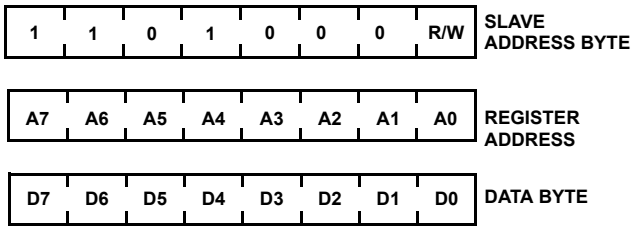


FIGURE 8. SLAVE ADDRESS, WORD ADDRESS, AND DATA BYTES

Read Operation

A Read operation consists of a three byte instruction followed by one or more Data Bytes (see Figure 9). The master initiates the operation issuing the following sequence: a START, the Identification byte with the R/$\overline{W}$ bit set to "0", an Address Byte, a second START, and a second Identification byte with the R/$\overline{W}$ bit set to "1". After each of the three bytes, the ISL12059 responds with an ACK. Then the ISL12059 transmits Data Bytes as long as the master responds with an ACK during the SCL cycle following the eighth bit of each byte. The master terminates the read operation (issuing a STOP condition) following the last bit of the last Data Byte (see Figure 9).

The Data Bytes are from the memory location indicated by an internal pointer. This pointer's initial value is determined by the Address Byte in the Read operation instruction, and increments by one during transmission of each Data Byte. After reaching the memory location 1Fh the pointer "rolls over" to 00h, and the device continues to output data for each ACK received.

Application Section

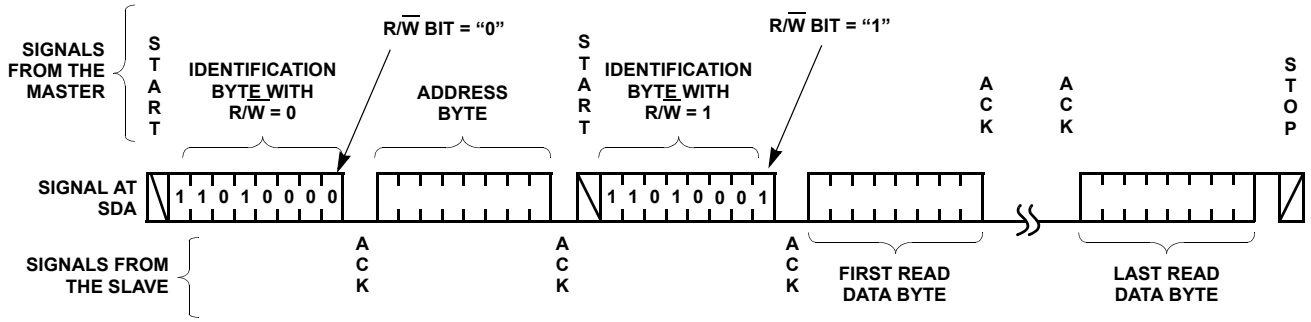


FIGURE 9. MULTIPLE BYTES READ SEQUENCE

Oscillator Crystal Requirements

The ISL12059 uses a standard 32.768kHz crystal. Either through hole or surface mount crystals can be used. Table 6 lists some recommended surface mount crystals and the parameters of each. This list is not exhaustive and other surface mount devices can be used with the ISL12059 if their specifications are very similar to the devices listed. The crystal should have a required parallel load capacitance of 12.5pF and an equivalent series resistance of less than 50k. The crystal's temperature range specification should match the application. Many crystals are rated for -10°C to +60°C (especially through-hole and tuning fork types), so an appropriate crystal should be selected if extended temperature range is required.

TABLE 3. SUGGESTED SURFACE MOUNT CRYSTALS

MANUFACTURER	PART NUMBER
Citizen	CM200S
MicroCrystal	MS3V
Raltron	RSM-200S
SaRonix	32S12
Ecliptek	ECPSM29T-32.768K
ECS	ECX-306
Fox	FSM-327

Layout Considerations

The crystal input at X1 has a very high impedance, and oscillator circuits operating at low frequencies such as 32.768kHz are known to pick up noise very easily if layout precautions are not followed. Most instances of erratic clocking or large accuracy errors can be traced to the susceptibility of the oscillator circuit to interference from adjacent high speed clock or data lines. Careful layout of the RTC circuit will avoid noise pickup and insure accurate clocking.

Figure 10 shows a suggested layout for the ISL12059 device using a surface mount crystal. Two main precautions should be followed:

Do not run the serial bus lines or any high speed logic lines in the vicinity of the crystal. These logic level lines can induce noise in the oscillator circuit to cause misclocking.

Add a ground trace around the crystal with one end terminated at the chip ground. This will provide termination for emitted noise in the vicinity of the RTC device.

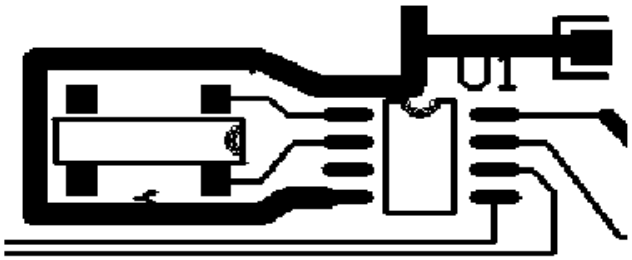
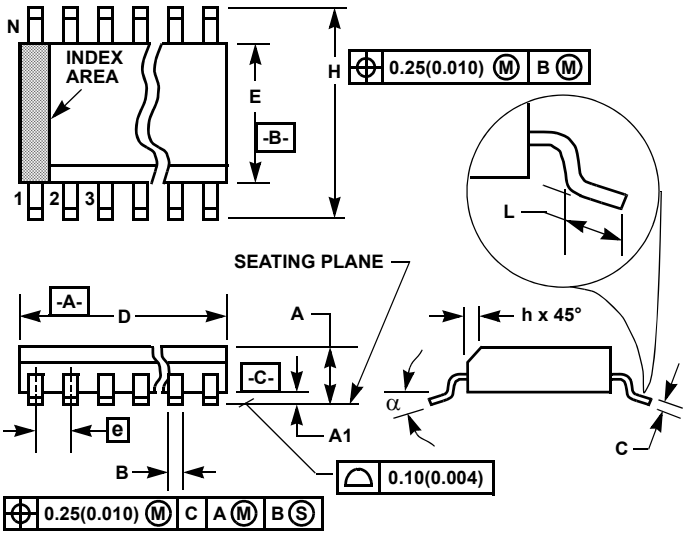


FIGURE 10. SUGGESTED LAYOUT FOR ISL12059 AND

In addition, it is a good idea to avoid a ground plane under the X1 and X2 pins and the crystal, as this will affect the load capacitance and therefore the oscillator accuracy of the circuit. If the FT/OUT pin is used as a clock, it should be routed away from the RTC device as well. The traces for the V_{DD} pins can be treated as a ground, and should be routed around the crystal.

Small Outline Plastic Packages (SOIC)



NOTES:

1. Symbols are defined in the “MO Series Symbol List” in Section 2.2 of Publication Number 95.
2. Dimensioning and tolerancing per ANSI Y14.5M-1982.
3. Dimension “D” does not include mold flash, protrusions or gate burrs. Mold flash, protrusion and gate burrs shall not exceed 0.15mm (0.006 inch) per side.
4. Dimension “E” does not include interlead flash or protrusions. Interlead flash and protrusions shall not exceed 0.25mm (0.010 inch) per side.
5. The chamfer on the body is optional. If it is not present, a visual index feature must be located within the crosshatched area.
6. “L” is the length of terminal for soldering to a substrate.
7. “N” is the number of terminal positions.
8. Terminal numbers are shown for reference only.
9. The lead width “B”, as measured 0.36mm (0.014 inch) or greater above the seating plane, shall not exceed a maximum value of 0.61mm (0.024 inch).
10. Controlling dimension: MILLIMETER. Converted inch dimensions are not necessarily exact.

M8.15 (JEDEC MS-012-AA ISSUE C)
8 LEAD NARROW BODY SMALL OUTLINE PLASTIC PACKAGE

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	0.0532	0.0688	1.35	1.75	-
A1	0.0040	0.0098	0.10	0.25	-
B	0.013	0.020	0.33	0.51	9
C	0.0075	0.0098	0.19	0.25	-
D	0.1890	0.1968	4.80	5.00	3
E	0.1497	0.1574	3.80	4.00	4
e	0.050 BSC		1.27 BSC		-
H	0.2284	0.2440	5.80	6.20	-
h	0.0099	0.0196	0.25	0.50	5
L	0.016	0.050	0.40	1.27	6
N	8		8		7
α	0°	8°	0°	8°	-

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