Data Sheet | December 1, 2006 | FN7465.2

Light-to-Digital I^2C Sensor

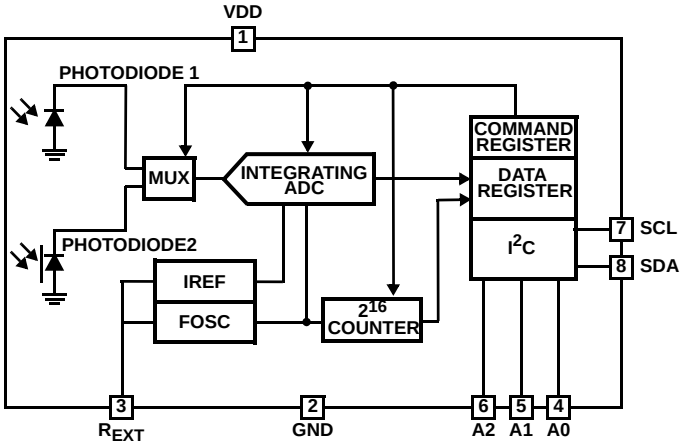
The ISL29002 is an integrated light sensor with a built-in integrating type ADC and a standard I^2C interface. The device transforms illuminance, ambient light level in lux, into a digital output signal accessible through I^2C. The sensor precisely converts illuminance from 1lux to 100,000lux. The ADC features up to 15-bit effective resolution. The sensor includes another photodiode covered with metal to reduce the effects of dark output reading that may be significant in low lux levels.

The ISL29002 can control display panel backlighting depending on ambient light conditions, adding artificial intelligence by approximating the response of a human eye. The ISL29002 can also manage portable peripheral illumination based upon lighting conditions extending battery life.

In normal operation, the ISL29002 consumes less than 300µA of supply current. A software power down mode is controlled via the I^2C interface and disables all but the I^2C interface. The supply current is then reduced to less than 88µA.

Designed to operate on supplies from 2.5V to 3.3V, the ISL29002 is specified for operation over the -40°C to +85°C ambient temperature range. It is packaged in a clear, Pb-free 8 Ld ODFN package.

Block Diagram



Features

- I^2C interface fast mode at 400kHz
- 88µA disabled current
- Adjustable max lux range: 10,000lux to 100,000lux
- Up to 15-bit effective resolution
- Adjustable resolution: 0.15 to 1.65 counts per lux
- Simple output code proportional to lux
- Flicker/noise rejection
- Variable integration time; 50ms to 550ms
- 2.5V to 3.3V supply
- 8 Ld ODFN (3mmx3mm)
- Temperature compensation
- Pb-free available (RoHS compliant)

Applications

- Backlight sensing
- Automatic backlight adjustment
- Backlight linearity adjustments

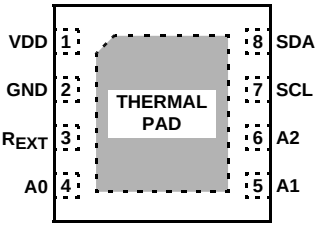
Ordering Information

PART NUMBER (Note)	TEMP. RANGE (°C)	TAPE & REEL	PACKAGE (Pb-Free)	PKG. DWG. #
ISL29002IROZ	-40 to +85	-	8 Ld 3x3 ODFN	MDP0052
ISL29002IROZ-T7	-40 to +85	7”	8 Ld 3x3 ODFN	MDP0052

NOTE: Intersil Pb-free ODFN products employ special Pb-free material sets; molding compounds/die attach materials and 100% matte tin plate termination finish, which are RoHS compliant and compatible with both SnPb and Pb-free soldering operations. Intersil Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020.

Pinout

ISL29002
(8 LD ODFN)
TOP VIEW



Absolute Maximum Ratings (T_A = +25°C)

Maximum Supply Voltage between V_{DD} and GND 3.6V
I^2C Address Pin Voltage (A2, A1, A0) . . . . . -0.2V to 3.6V
I^2C Bus Pin Voltage (SCL, SDA) . . . . . -0.2V to 5.5V
I^2C Bus Pin Current (SCL, SDA) . . . . . <10mA
R_{EXT} Pin Voltage . . . . . -0.2V to 3.6V
Operating Temperature . . . . . -40°C to +85°C
Maximum Die Temperature . . . . . +125°C
Storage Temperature . . . . . -45°C to +100°C
ESD, Human Body Model 2kV

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

IMPORTANT NOTE: All parameters having Min/Max specifications are guaranteed. Typical values are for information purposes only. Unless otherwise noted, all tests are at the specified temperature and are pulsed tests, therefore: $T_J = T_C = T_A$

Electrical Specifications

V_{DD} = 3V, T_A = +25°C, R_{EXT} = 100kΩ 1%, I^2C command = 00(hex) (Note 1), unless otherwise specified.

PARAMETER	DESCRIPTION	CONDITION	MIN	TYP	MAX	UNIT
V_{DD}	Power Supply Range		2.25		3.63	V
I_{DD}	Supply Current			0.3	0.375	mA
I_{DD1}	Supply Current	Software disabled		88	110	µA
t_{UPD}	Internal Update Time/Conversion Time		85	110	135	ms
f_{OSC}	Internal Oscillator Frequency			300		kHz
F_{I2C}	I^2C Clock Rate	(Note 2)	1		400	kHz
DATA0	Dark ADC Code	E = 0lux E = 0lux, integration time = 550ms		 4	1	Counts
DATA1	ADC Code	ADC full scale count value			32,768	Counts
DATA2	ADC Code	E = 25,000lux, Fluorescent light (Note 3)	13,500	16,000	18,500	Counts
V_{REF}	Voltage of R_{EXT} Pin		0.45	0.51	0.53	V
V_{TL}	SCL, SDA, A0, A1, and A2 Threshold LO	(Note 4)		1.05		V
V_{TH}	SCL, SDA, A0, A1, and A2 Threshold HI	(Note 4)		1.95		V
I_{SDA}	SDA Current Sinking Capability		3	5		mA
I_{IL}	A0, A1, and A2 Input Current LO	A0 = A1 = A2 = GND		0.1		µA
I_{IH}	A0, A1, and A2 Input Current HI	A0 = A1 = A2 = V_{DD}		0.1		µA

NOTES:

1. For I^2C command = 00H, the ADC converts the current of (photo) diode 1 into a 16 bit data with an internally timed integration of 110ms for R_{EXT} = 100kΩ, 1% tolerance.
2. Minimum I^2C Clock Rate is guaranteed by design.
3. Fluorescent light is substituted by an LED at production.
4. The voltage threshold levels of the SDA and SCL pins are VDD dependent: $V_{TL} = 0.35*V_{DD}$. $V_{TH} = 0.65*V_{DD}$.

Pin Descriptions

PIN NUMBER	PIN NAME	DESCRIPTION	
1	VDD	Positive supply. Connect to a clean 2.25V to 3.3V supply	
2	GND	Ground. The thermal pad is connected to the GND pin	
3	R_{EXT}	External resistor pin is for the ADC reference current, the integration time adjustment in internal timing mode, and lux range/resolution adjustment. 100kΩ 1% tolerance resistor recommended.	
4	A0	Bit 0 of the I^2C address.	The address pins have an open gate equivalent circuit. These are the least-significant bits of the I^2C address. The eight possible addresses are 40(hex) through 48(hex).
5	A1	Bit 1 of the I^2C address.	
6	A2	Bit 2 of the I^2C address.	
7	SCL	I^2C serial clock line	The I^2C bus lines can pulled above V_{DD}, 5.5V max.
8	SDA	I^2C serial data line	

Typical Performance Curves R_{EXT} = 100kΩ

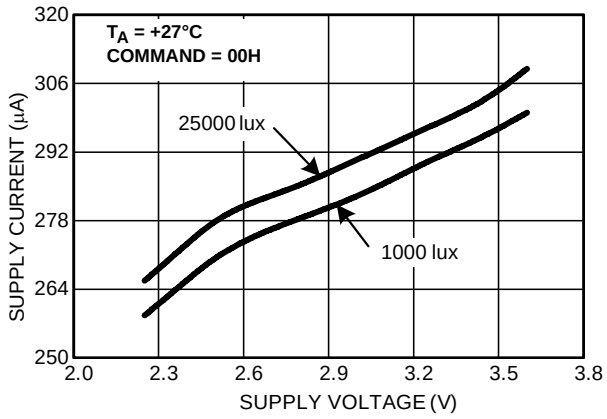


FIGURE 1. SUPPLY CURRENT vs SUPPLY VOLTAGE

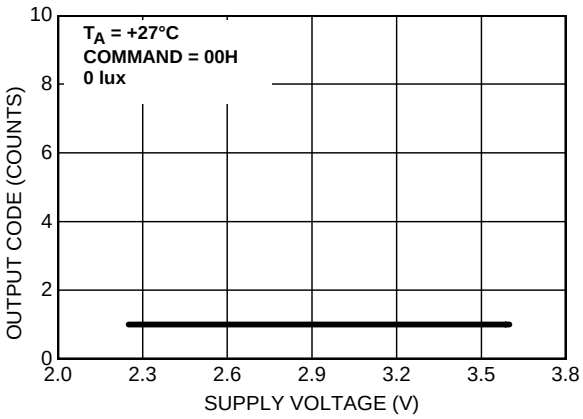


FIGURE 2. OUTPUT CODE FOR 0LUX vs SUPPLY VOLTAGE

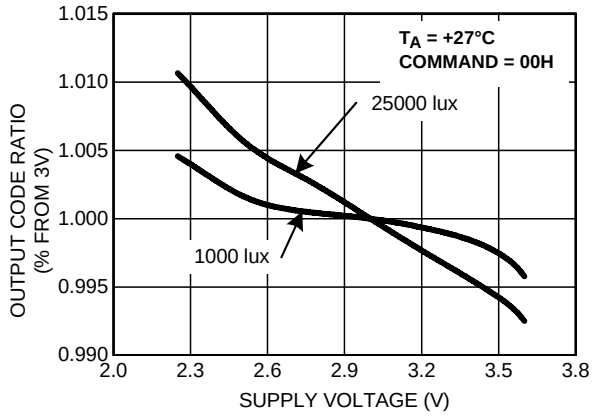


FIGURE 3. OUTPUT CODE vs SUPPLY VOLTAGE

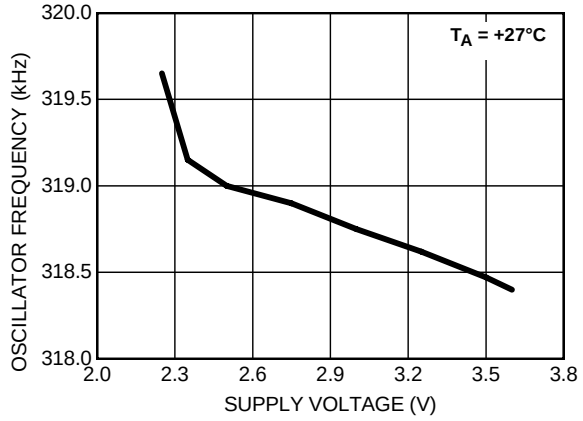


FIGURE 4. OSCILLATOR FREQUENCY vs SUPPLY VOLTAGE

Typical Performance Curves R_{EXT} = 100kΩ (Continued)

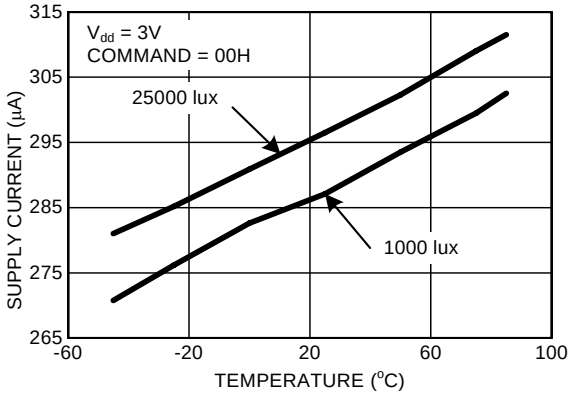


FIGURE 5. SUPPLY CURRENT vs TEMPERATURE

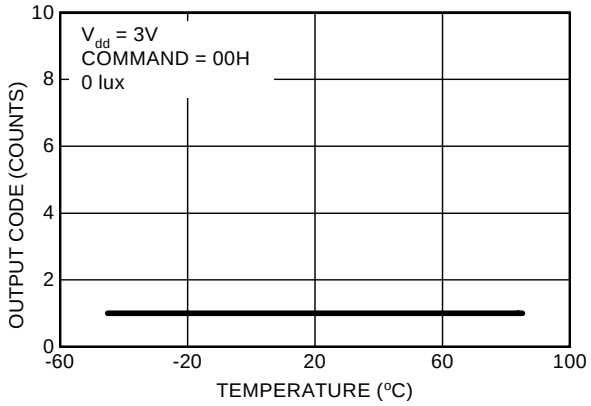


FIGURE 6. OUTPUT CODE FOR 0LUX vs TEMPERATURE

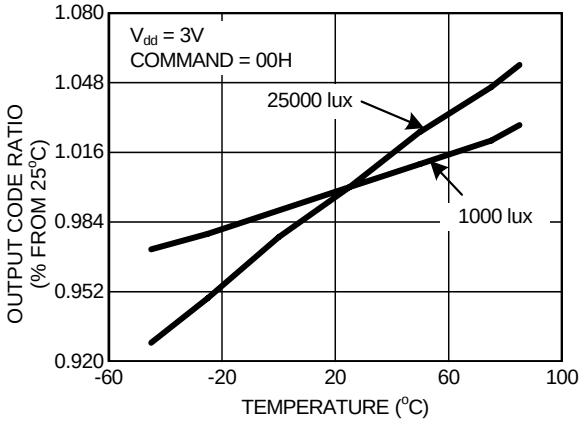


FIGURE 7. OUTPUT CODE vs TEMPERATURE

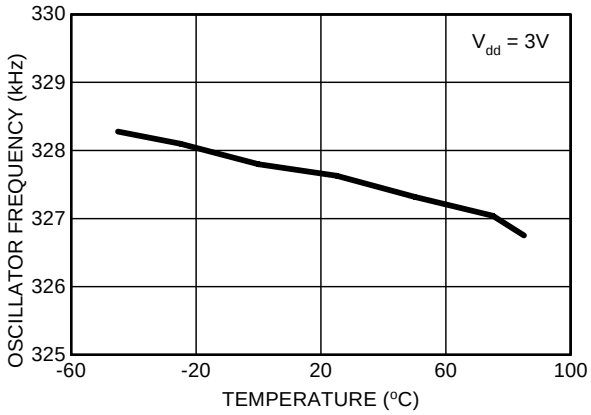


FIGURE 8. OSCILLATOR FREQUENCY vs TEMPERATURE

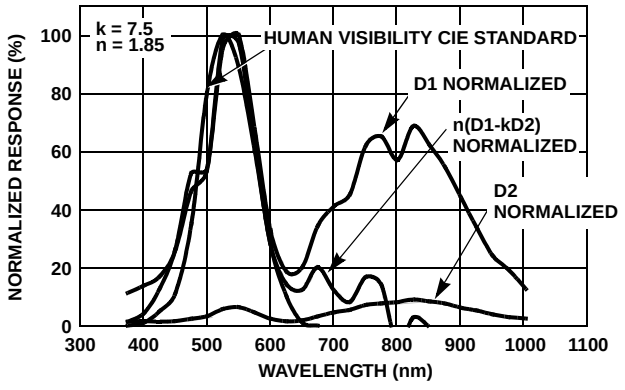


FIGURE 9. RELATIVE INTENSITY

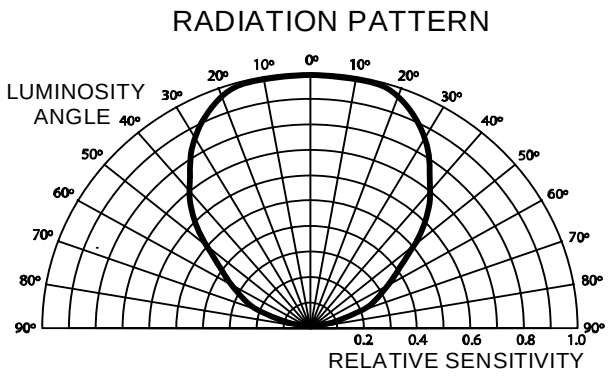


FIGURE 10. RADIATION PATTERN

Principles of Operation

Photodiodes and ADC

The ISL29002 contains two photodiodes. One of the photodiodes is sensitive to visible and infrared light (Diode 1). Another photodiode (Diode 2) is covered with metal and can be used to cancel the effects of dark output code, the unwanted number of counts in the absence of light. Diode 2 can also be used to cancel the presence of IR. See IR rejection in the applications section. The ISL29002 also contains an on-chip integrating analog-to-digital converter (ADC) to convert photodiode currents into digital data. The interface to the ADC is implemented using the standard I^2C interface.

The ISL29002's built-in ADC is a charge-balancing integrating converter type. The integrating ADC converts the photodiode current to frequency. The repetition rate is then counted by a binary counter to output a digital code - number of counts. The ISL29002 can be configured (in external timing mode) to output a maximum 2^{16} (65,536) counts.

The ADC has two timing controls, internal timing and external timing. With internal timing, the number of clock cycles per integration time is fixed at 2^{15} (32,726), hence the number of counts is limited to 2^{15} (32,7268). With external timing, the user have the flexibility to vary the maximum number of counts up to 2^{16} (65,536).

In addition, the ADC has three operating modes (Please consult Table 1 for a complete list of modes.) In the first operating mode, the ADC only integrates Diode 1's current. In the second operating mode, the ADC only integrates the other diode, Diode 2's current. Both operating mode 1 and mode 2 has a 16-bit unsigned-magnitude format. In the third operating mode, the ADC integrates Diode 2's current first, then Diode 1's current. In this mode, the output is a 16-bit 2's complement format. The total integration time is doubled, and the digital output is the difference of the two photodiode currents (Diode 1's current minus Diode 2's current). Any of the three operating modes can be used with either of the two timing controls, either internally or externally controlled integration timing.

I^2C Interface

The ISL29002 contains a single 8-bit command register that can be written via the I^2C interface. The command register defines the operation of the device, which does not change until the command register is overwritten.

The ISL29002 contains four 8-bit data registers that can be read via the I^2C interface. The first two data registers contain the ADC's latest digital output, while the second two registers contain the number of clock cycles in the previous integration period.

The ISL29002's I^2C address is pin-selectable by pins A0, A1, and A2. These pins can be tied or driven either high or low. They comprise the least-significant three bits of the I^2C address, while the four most-significant bits are hardwired as 1000. The eight possible addresses are therefore 40H through 47H.

Figure 11B shows a sample one-byte read. (A typical application will read two to four bytes, however.) The I^2C bus master always drives the SCL (clock) line, while either the master or the slave can drive the SDA (data) line. Every I^2C transaction begins with the master asserting a start condition (SDA falling while SCL remains high). The following byte is driven by the master, and includes the slave address and read/write bit. The receiving device is responsible for pulling SDA low during the acknowledgement period.

Any writes to the ISL29002 overwrite the command register, changing the device's mode. Any reads from the ISL29002 return two or four bytes of sensor data and counter value, depending upon the operating mode. Neither the command register nor the data registers have internal addresses, and none of the registers can be individually addressed.

Every I^2C transaction ends with the master asserting a stop condition (SDA rising while SCL remains high).

I^2C Transaction Flow

To WRITE, the master sends slave address 44(hex) plus the write bit. Then master sends the ADC command to the device which defines its operation. As soon as the ISL29002 receives the ADC command, it will execute and then store the readings in the register after the analog-to-digital conversion is complete. While the ISL29002 is executing the command and also after the execution, the I^2C bus is available for transactions other than the ISL29002. After command execution, sensor data readings are stored in the registers. Note that if a READ is received before the execution is finished, the data retrieved is previous data sensor reading. Typical integration/conversion time is 100ms (for R_{EXT} = 100k and internal timing mode). It is recommended that a READ is sent 120ms later because the fosc variation is 20%.

The operation of the device does not change until the command register is overwritten. Hence, when the master sends a slave address 44(hex) and a write bit, the ISL29002 will repeat the same command from the previous WRITE transaction.

To READ, master sends slave address 44(hex) plus the read bit. Then ISL29002 will hold the SDA line to send data to master. Note that the master need not send an address register to access the data. As soon as the ISL29002 receives the read bit. It will send 4 bytes. The 1st byte is the LSB of the sensor reading. The 2nd byte is the MSB of the sensor reading. The 3rd byte is LSB of the counter reading. The 4th byte is the MSB of the counter reading. If internal timing mode is selected, only the 1st and 2nd data byte are necessary; the master can assert a stop after the 2nd data byte is received.

For more information about the I^2C standard, please consult the Philips® I^2C specification documents.

Command Register

The command register is used to define the ADC's operations. Table 1 shows the primary commands used to control the ADC.

Note that there are two classes of operating commands: three for internal timing, and three for external (arbitrary) timing.

When using any of the three internal timing commands, the device self-times each conversion, which is nominally 110ms (with R_{EXT} = 100kΩ).

When using any of the three external timing commands, each command received by the device ends one conversion and begins another. The integration time of the device is thus the time between one I^2C external timing command and the next. The integration time can be between 1ms and 100ms. The external timing commands can be used to synchronize the ADC's integrating time to a PWM dimming frequency in a backlight system in order to eliminate noise.

TABLE 1. COMMAND REGISTERS AND FUNCTIONS

COMMAND	FUNCTION	
8C(hex)	ADC is powered-down. To enable ADC from a powered-down state, send any command to the ISL29002.	
0C(hex)	ADC is reset. A reset restarts the counter value to zero and returns the clock cycle to zero.	
00(hex)	Internal Timing Mode. Integration time is 110ms per photodiode.	ADC converts Diode 1's current (I_{DIODE1}) into an unsigned-magnitude 16-bit data.
04(hex)		ADC converts Diode 2's current (I_{DIODE2}) into unsigned-magnitude 16-bit data.
08(hex)		ADC converts I_{DIODE1}-I_{DIODE2} into 2's-complement 16-bit data.
30(hex)	External Timing Mode. Each external timing command sent to the device ends one integration period and begins another.	ADC converts Diode 1's current (I_{DIODE1}) into unsigned-magnitude 16-bit data.
34(hex)		ADC converts Diode 2's current (I_{DIODE1}) into unsigned-magnitude 16-bit data.
38(hex)		ADC converts I_{DIODE1}-I_{DIODE2} into 2's-complement 16-bit data.
1xxx_xxxx (binary)		I^2C communication test. The value written to the command register can be read back via the I^2C bus.

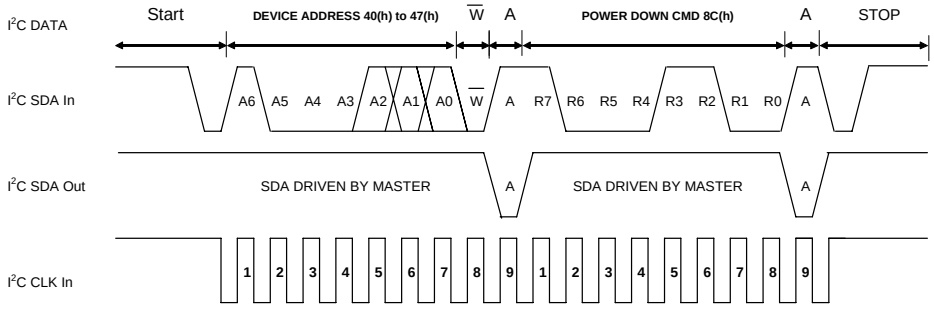


FIGURE 11A. I^2C WRITE TIMING DIAGRAM SAMPLE

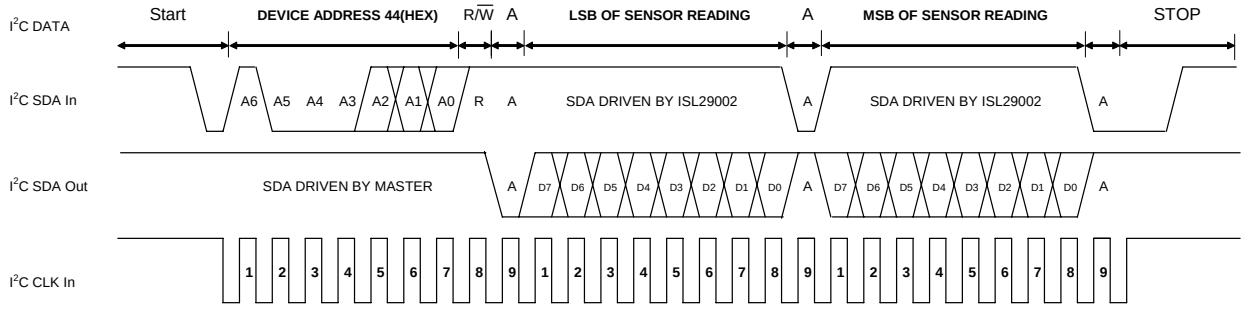


FIGURE 11B. I^2C READ TIMING DIAGRAM SAMPLE

FIGURE 11.

Data Registers

The ISL29002 contains four 8-bit data registers. These registers cannot be specifically addressed, as is conventional with other I^2C peripherals; instead, performing a read operation on the device always returns all available registers in ascending order. See Table 2 for a description of each register.

The first two 8-bit data registers contain the most recent sensor reading. The meaning of the specific value stored in these data registers depends on the command written via the I^2C interface; see Table 1 for information on the various commands. The first byte read over the I^2C interface is the least-significant byte; the second is the most significant. This byte ordering is often called “little-endian” ordering.

The third and fourth 8-bit data registers contain the integration counter value corresponding to the most recent sensor reading. The ISL29002 includes a free-running oscillator, each cycle of which increments a 16-bit counter. At the end of each integration period, the value of this counter is made available in these two 8-bit registers. Like the sensor reading, the integration counter value is read across the I^2C bus in little-endian order.

TABLE 2. DATA REGISTERS

ADDRESS	CONTENTS
00(hex)	Least-significant byte of most recent sensor reading.
01(hex)	Most-significant byte of most recent sensor reading.
02(hex)	Least-significant byte of integration counter value corresponding to most recent sensor reading.
03(hex)	Most-significant byte of integration counter value corresponding to most recent sensor reading.

Note that the integration counter value is only available when using one of the three externally-timed operating modes; when using internally-timed modes, the device will NAK after the two-byte sensor reading has been read.

Internal Timing Mode

When using one of the three internal timing modes, each integration period of the ISL29002 is timed by 2^{15} = 32,768 clock cycles of an internal oscillator. The nominal frequency of the internal oscillator is 300kHz, which provides 110ms internally-timed integration periods. The oscillator frequency is dependent upon an external resistor, R_{EXT}, and can be adjusted by selecting a different resistor value. The resolution and maximum range of the device are also affected by changes in R_{EXT}; see below.

The oscillator frequency, f_{osc} can be calculated with the following equation:

$$f_{osc} = 300kHz \cdot \frac{100k\Omega}{R_{EXT}} \quad \text{(EQ. 1)}$$

R_{EXT} is an external resistor required nominally 100kΩ, and provides 110ms internal timing and a 1-50,000lux range for Diode 1. Doubling this resistor value to 200kΩ halves the internal oscillator frequency, providing 220ms internal timing. In addition, the maximum lux range of Diode 1 is also halved, from 50,000lux to 25,000lux, and the resolution is doubled, from 0.65 counts per lux to 1.3 counts per lux.

The acceptable range of this resistor is 50kΩ (providing 55ms internal timing, 100,000lux maximum reading, ~0.33 counts per lux) to 500kΩ (550ms internal timing, 10,000lux maximum reading, ~3.3 counts per lux). See Table 3 for R_{EXT} selection.

When using one of the three internal timing modes, the ISL29002’s resolution is determined by the ratio of the max lux range to 32,768, the number of clock cycles per integration.

The following equations describe the light intensity, E in lux, as a function of the sensor reading, and the integration time as a function of the external resistor.

$$E(Lux) = \frac{1}{32,768} \cdot \frac{50,000lux}{(R_{ext}/100k\Omega)} \cdot Data1 \quad \text{(EQ. 2)}$$

$$Tint = 110ms \cdot \frac{R_{ext}}{100k\Omega} \quad \text{(EQ. 3)}$$

where,

E is the measured light intensity in lux

Data1 is the sensor reading

T_{int} is the integration time,

R_{EXT} is external resistor value.

TABLE 3. R_{EXT} RESISTOR SELECTION GUIDE

R_{EXT} (kΩ)	INTEGRATION TIME (ms)	LUX RANGE (lux)	RESOLUTION, COUNTS/LUX
50 (Min)	55	100,000	0.33
90.9	100	55,000	0.61
100 Recommended	110	50,000	0.67
200	220	25,000	1.33
500 (Max)	550	10,000	3.33

External Timing Mode

When using one of the three external timing modes, each integration period of the ISL29002 is determined by the time which passes between consecutive external timing commands received over the I^2C bus. The user starts the integration by sending an external command and stops the integration by sending another external command. The integration time, T_{int}, therefore is determined by the following equation:

$$T_{int} = \frac{i_{I2C}}{f_{I2C}} \quad \text{(EQ. 4)}$$

where:

i_{I2C} is the number of I^2C clock cycles to obtain the T_{int}.

f_{I2C} is the I^2C operating frequency.

The internal oscillator, f_{OSC}, operates identically in both the internal and external timing modes, with the same dependence on R_{EXT}. However, when using one of the three external timing modes, the number of clock cycles per

integration is no longer fixed at 32,768, but varies with the chosen integration time, and is limited to 65,536. In order to avoid erroneous lux readings the integration must be short enough not to allow an overflow in the counter register.

$$T_{int} < \frac{65,536}{f_{OSC}} \quad \text{(EQ. 5)}$$

where:

T_{int} = user defined integration time

f_{osc} = 300kHz*100kΩ/R_{EXT}. ISL29002's internal oscillator. Not to be confused with the I^2C's frequency.

R_{EXT} = user defined external resistor to adjust f_{osc}. 100kΩ recommended.

The number of clock cycles in the previous integration period is provided in the third and fourth bytes of data read across the I^2C bus. This two-byte value is called the integration counter value.

When using one of the three external timing modes, the ISL29002's resolution varies with the integration time. The resolution is determined by the ratio of the max lux range to the number of clock cycles per integration.

The following equations describe the light intensity as a function of sensor reading, integration counter value, and integration time:

$$E(lux) = \frac{50,000lux}{(R_{EXT}/100k\Omega)} \cdot \frac{Data1}{Data2} \quad \text{(EQ. 6)}$$

T_{int} = Time Interval between external time commands

where L is the measured light intensity, Data1 is the sensor reading, Data2 is the integration counter value, T is the integration time, and R_{EXT} is external resistor value.

Noise Rejection and Integration Time

In general, integrating type ADC's have an excellent noise-rejection characteristics for periodic noise sources whose frequency is an integer multiple of the integration time. For instance, a 60Hz AC unwanted signal's sum from 0ms to n*16.66ms (n = 1,2...n_i) is zero. Similarly, setting the ISL29002's integration time to an integer multiple of periodic noise signal greatly improves the light sensor output signal in the presence of noise. The integration time, T_{int}, of the ISL29002 is set by an external resistor R_{EXT}.
See Equation 3.

Design Example 1

Using the ISL29002, determine a suitable integration time, T_{int}, that will ignore the presence of both 60Hz and 50Hz noise. Accordingly, specify the R_{EXT} value. Given that the I^2C clock is at f_{I2C} = 10kHz.

Solution 1 - Using Internal Timing

T_{int} = n(1/60Hz) = m(1/50Hz). In order to achieve both 60Hz and 50Hz AC rejection, the integration time needs to be adjusted to coincide with an integer multiple of the AC noise cycle times.

n/m = 60Hz/50Hz = 6/5. The first instance of integer values at which T_{int} rejects both 60Hz and 50Hz is when m = 5, and n = 6.

T_{int} = 6(1/60Hz) = 5(1/50Hz) = 100ms

From Equation 3:
R_{EXT} = T_{int} * (100kΩ/110ms) = 90.9kΩ. By populating R_{EXT} = 90kΩ, the ISL29002 defaults to 100ms integration time and will reject the presence of both 60Hz and 50Hz power line signals.

Solution 2 - Using External Timing

From solution 1, the desired integration time is 100ms. Note that the R_{EXT} resistor does not determine the integration time when using external timing mode. Instead, the integration and the 16-bit counter starts when an external timing mode command is sent and end when another external timing mode is sent. In other words, the time between two external timing mode command is the integration time. The programmer determines how many clock cycles to wait between two external timing commands.

i_{I2C} = f_{I2C} * T_{int}, where i_{I2C} = number of I^2C cycles

i_{I2C} = 10kHz *100ms

i_{I2C} = 1,000 I^2C clock cycles. An external timing command 1,000 cycles after another external timing command rejects both 60Hz and 50Hz AC noise signals.

IR Rejection

Any filament type light source has a high presence of infrared component invisible to the human eye. A white fluorescent lamp, on the other hand has a low IR content. As a result, output sensitivity may vary depending on the light source. Maximum attenuation of IR can be achieved by properly scaling the readings of Diode1 and Diode2. The user obtains data reading from sensor diode 1, D1, which is sensitive to visible and IR, then reading from sensor diode 2, D2 which is mostly sensitive from IR. The graph on Figure 9 shows the effective spectral response after applying Equation 7 of the ISL29002 from 400nm to 1000nm. The equation below describes the method of cancelling IR in internal timing mode.

$$D3 = n(D1 - kD2) \quad \text{(EQ. 7)}$$

Where:

data = lux amount in number of counts less IR presence

D1 = data reading of Diode 1

D2 = data reading of Diode 2

n = 1.85. This is a fudge factor to scale back the sensitivity up to ensure Equation 2 is valid.

k = 7.5. This is a scaling factor for the IR sensitive Diode 2.

Typical Circuit

A typical application circuit is shown in Figure 12.

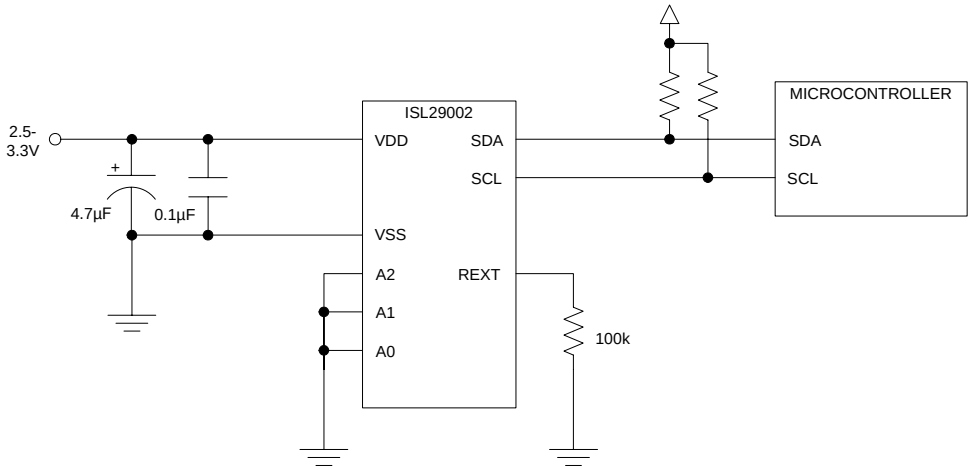


FIGURE 12. TYPICAL CIRCUIT

Suggested PCB Footprint

See Figure 13. Footprint pads should be a nominal 1-to-1 correspondence with package pads. The large, exposed central die-mounting paddle in the center of the package requires neither thermal nor electrical connection to the PCB, and such connection should be avoided.

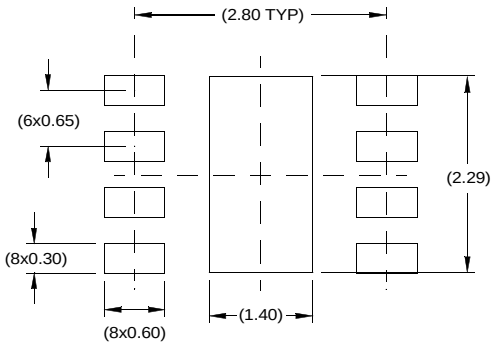


FIGURE 13. SUGGESTED PCB FOOTPRINT

Layout Considerations

The ISL29002 is relatively insensitive to layout. Like other I^2C devices, it is intended to provide excellent performance even in significantly noisy environments. There are only a few considerations that will ensure best performance.

Route the supply and I^2C traces as far as possible from all sources of noise. Use two power-supply decoupling capacitors, 4.7µF and 0.1µF, placed close to the device.

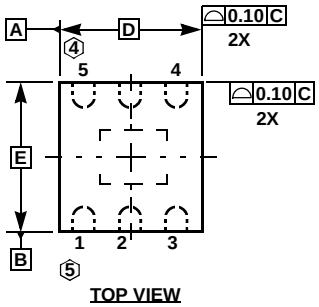
Soldering Considerations

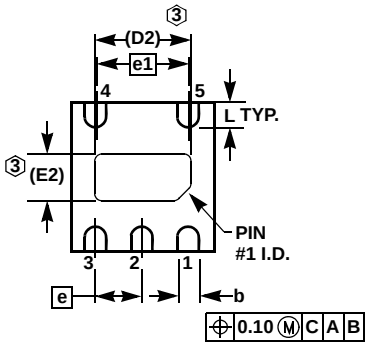
Convection heating is recommended for reflow soldering; direct-infrared heating is not recommended. The ISL29002's plastic ODFN package does not require a custom reflow soldering profile, and is qualified to +260°C. A standard reflow soldering profile with a +260°C maximum is recommended.

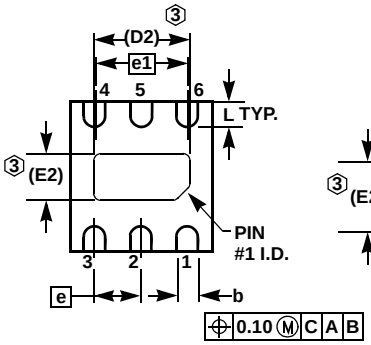
Special Handling

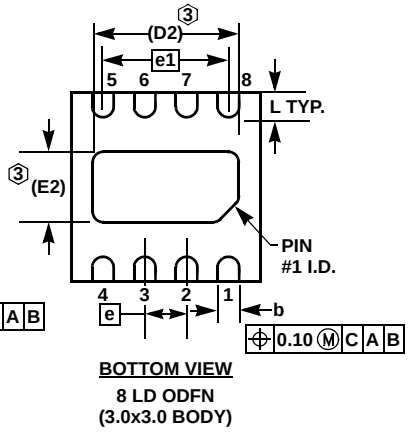
ODFN8 is rated as JEDEC moisture level 4. Standard JEDEC Level 4 procedure should be followed: 72hr floor life at less than +30°C 60% RH. When baking the device, the temperature required is +110°C or less due to special molding compound.

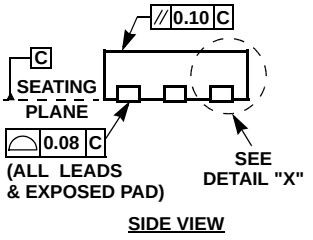
Optical Dual Flat No-Lead Family (ODFN)

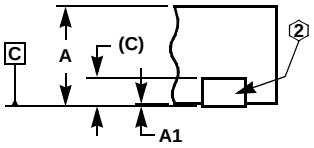












MDP0052

OPTICAL DUAL FLAT NO-LEAD FAMILY

SYMBOL	ODFN5	ODFN6	ODFN8	TOLERANCE	NOTE
A	0.70	0.70	0.70	±0.05	
A1	0.02	0.02	0.02	+0.03/-0.02	
b	0.30	0.30	0.30	±0.05	
c	0.20	0.20	0.20	Reference	2
D	2.00	2.00	3.00	Basic	
D2	1.35	1.35	2.29	Reference	3
E	2.10	2.10	3.00	Basic	
E2	0.65	0.65	1.40	Reference	3
e	0.65	0.65	0.65	Basic	
e1	1.30	1.30	1.95	Basic	
L	0.35	0.35	0.40	±0.05	

Rev. 4 5/06

NOTES:

1. Dimensioning and tolerancing per ASME Y14.5M-1994.
2. Exposed lead at side of package is a non-functional feature.
3. Dimension D2 and E2 define the size of the exposed pad.
4. ODFN 5 Ld version has no center lead (shown as dashed line).