OBSOLETE PRODUCT
POSSIBLE SUBSTITUTE PRODUCT
ISL3158E

ISL3158AE

±16.5kV ESD (IEC61000-4-2) Protected, Large Output Swing, 5V, Full Fail-Safe, 1/8 Unit Load, RS-485/RS-422 Transceiver

FN6886
Rev 1.00
October 15, 2013

The ISL3158AE is a BiCMOS, IEC61000 ESD protected, 5V powered, single transceiver that meets both the RS-485 and RS-422 standards for balanced communication. Each driver output and receiver input is protected against ±16.5kV ESD strikes without latch-up.

The ISL3158AE transmitter delivers exceptional differential output voltages (2.4V min), into the RS-485 required 54Ω load, for better noise immunity or to allow up to eight 120Ω terminations in “star” or other non-standard bus topologies.

This device has very low bus currents (+125µA/-75µA), so it presents a true “1/8 unit load” to the RS-485 bus. This allows up to 256 transceivers on the network without violating the RS-485 specification’s 32 unit load maximum, and without using repeaters.

Receiver (Rx) inputs feature a “Full Fail-Safe” design, which ensures a logic high Rx output if Rx inputs are floating, shorted, or on a terminated but undriven bus. Rx outputs feature high drive levels - typically 28mA @ V_{OL} = 1V (to ease the design of optocoupled isolated interfaces).

Hot Plug circuitry ensures that the Tx and Rx outputs remain in a high impedance state until the power supply has stabilized, and the Tx outputs are fully short circuit protected.

The ISL3158AE is a half duplex version. It multiplexes the Rx inputs and Tx outputs to allow transceivers with output disable functions in an 8 Ld package.

Features

- High Driver V_{OD} . . . . . 2.4V (Min) @ R_D = 54Ω
  - Better Noise Immunity, or Drive Up to 8 Terminations
- IEC61000 ESD Protection on RS-485 I/O Pins . . ±16.5kV
  - Class 3 ESD Level on all Other Pins . . . . . >7kV HBM
- Full Fail-safe (Open, Short, Terminated and Undriven) Receivers
- High Rx I_{OL} to Drive Opto-Couplers for Isolated Applications
- Hot Plug Circuitry - Tx and Rx Outputs Remain Three-State During Power-up/Power-down
- True 1/8 Unit Load Allows up to 256 Devices on the Bus
- Specified for Single 5V, 10% Tolerance, Supplies
- High Data Rates. . . . . up to 10Mbps
- Low Quiescent Supply Current 600µA
  Ultra Low Shutdown Supply Current 70nA
- -7V to +12V Common Mode Input Voltage Range
- Half Duplex Pinouts
- Pb-free (RoHS compliant)
- Three-State Rx and Tx Outputs
- Current Limiting for Driver Overload Protection

Applications

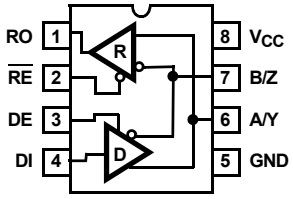
- Utility Meters and Automated Meter Reading Systems
- High Node Count Systems
- PROFIBUS® and Field Bus Networks, and Factory Automation
- Security Camera Networks
- Building Lighting and Environmental Control Systems
- Industrial/Process Control Networks

TABLE 1. SUMMARY OF FEATURES

PART NUMBER	HALF/FULL DUPLEX	DATA RATE (Mbps)	SLEW-RATE LIMITED?	HOT PLUG	# DEVICES ON BUS	Rx/Tx ENABLE?	QUIESCENT I_{CC} (µA)	LOW POWER SHUTDOWN?	PIN COUNT
ISL3158AEM	Half	10	No	Yes	256	Yes	600	Yes	8
ISL3158AEMW	Half	10	No	Yes	256	Yes	600	Yes	N/A

Pinout

ISL3158AE
(8 LD SOIC)
TOP VIEW



Ordering Information

PART NUMBER (Notes 2, 3)	PART MARKING	TEMP. RANGE (°C)	PACKAGE (Pb-Free)	PKG. DWG. #
ISL3158AEMBZ (Note 1)	3158A EMBZ	-55 to +125	8 Ld SOIC	M8.15
ISL3158AEMW		-55 to +125	Wafer	

NOTES:

1. Add “-T*” suffix for tape and reel. Please refer to TB347 for details on reel specifications.
2. These Intersil Pb-free plastic packaged products employ special Pb-free material sets, molding compounds/die attach materials, and 100% matte tin plate plus anneal (e3 termination finish, which is RoHS compliant and compatible with both SnPb and Pb-free soldering operations). Intersil Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020.
3. For Moisture Sensitivity Level (MSL), please see device information page for ISL3158AE. For more information on MSL, please see tech brief TB363.

Truth Tables

TRANSMITTING				
INPUTS			OUTPUTS	
$\overline{RE}$	DE	DI	Z	Y
X	1	1	0	1
X	1	0	1	0
0	0	X	High-Z	High-Z
1	0	X	High-Z*	High-Z*

NOTE: *Shutdown Mode (See Note 10).

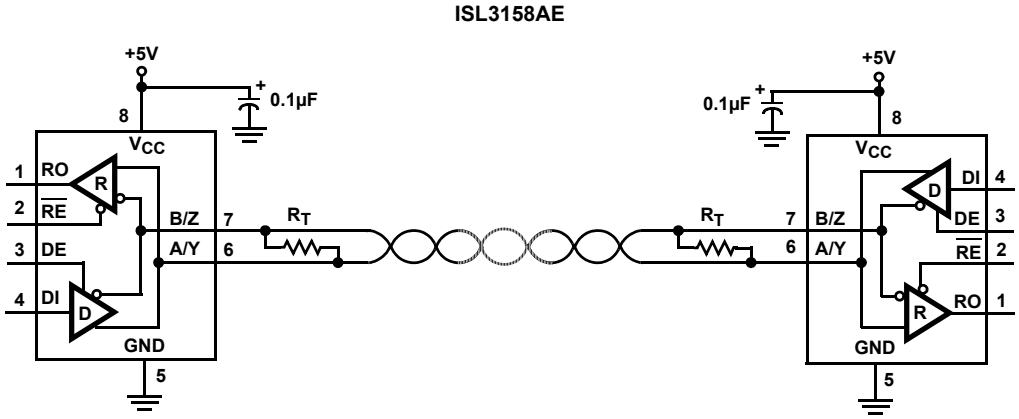
RECEIVING				
INPUTS				OUTPUT
$\overline{RE}$	DE Half Duplex	DE Full Duplex	A-B	RO
0	0	X	≥ -0.05V	1
0	0	X	≤ -0.2V	0
0	0	X	Inputs Open/Shorted	1
1	0	0	X	High-Z*
1	1	1	X	High-Z

NOTE: *Shutdown Mode (See Note 10).

Pin Descriptions

PIN	FUNCTION
RO	Receiver output: If A-B ≥ -50mV, RO is high; If A-B ≤ -200mV, RO is low; RO = High if A and B are unconnected (floating) or shorted.
$\overline{RE}$	Receiver output enable. RO is enabled when $\overline{RE}$ is low; RO is high impedance when $\overline{RE}$ is high.
DE	Driver output enable. The driver outputs, Y and Z, are enabled by bringing DE high. They are high impedance when DE is low.
DI	Driver input. A low on DI forces output Y low and output Z high. Similarly, a high on DI forces output Y high and output Z low.
GND	Ground connection.
A/Y	±16.5kV IEC61000 ESD Protected RS-485/RS-422 level, non-inverting receiver input and noninverting driver output. Pin is an input if DE = 0; pin is an output if DE = 1.
B/Z	±16.5kV IEC61000 ESD Protected RS-485/RS-422 level, inverting receiver input and inverting driver output. Pin is an input if DE = 0; pin is an output if DE = 1.
V_{CC}	System power supply input (4.5V to 5.5V).

Typical Operating Circuit



Absolute Maximum Ratings

V_{CC} to Ground 7V
Input Voltages
DI, DE, $\overline{RE}$ . . . . . -0.3V to (V_{CC} + 0.3V)
Input/Output Voltages
A/Y, B/Z . . . . . -9V to +13V
A/Y, B/Z (Transient Pulse Through 100Ω) . . . . . ±25V
RO . . . . . -0.3V to (V_{CC} +0.3V)
Short Circuit Duration
Y, Z . . . . . Continuous
ESD Rating . . . . . See Specifications Table

Thermal Information

Thermal Resistance (Typical, Note 4) θ_{JA} (°C/W)
8 Ld SOIC 120
Maximum Junction Temperature (Plastic Package) . . . . . +150°C
Maximum Storage Temperature Range . . . . . -65°C to +150°C
Pb-Free Reflow Profile . . . . . .see link below
http://www.intersil.com/pbfree/Pb-FreeReflow.asp

Operating Conditions

Temperature Range . . . . . -55°C to +125°C

CAUTION: Do not operate at or near the maximum ratings listed for extended periods of time. Exposure to such conditions may adversely impact product reliability and result in failures not covered by warranty.

NOTE:

4. θ_{JA} is measured with the component mounted on a high effective thermal conductivity test board in free air. See Tech Brief TB379 for details.

Electrical Specifications

Test Conditions: V_{CC} = 4.5V to 5.5V; Unless Otherwise Specified. Typicals are at V_{CC} = 5V, T_A = +25°C (Note 5). Parameters with MIN and/or MAX limits are 100% tested at +25°C, unless otherwise specified. Temperature limits established by characterization and are not production tested.

PARAMETER	SYMBOL	TEST CONDITIONS		TEMP (°C)	MIN	TYP	MAX	UNITS
DC CHARACTERISTICS								
Driver Differential V_{OUT} (No load)	V_{OD1}			Full	-	-	V_{CC}	V
Driver Differential V_{OUT} (Loaded)	V_{OD2}	R_L = 100Ω (RS-422) (Figure 1A)		Full	2.8	3.6	-	V
		R_L = 54Ω (RS-485) (Figure 1A)		Full	2.4	3.1	V_{CC}	V
		R_L = 15Ω (Eight 120Ω terminations) (Note 13)		25	-	1.65	-	V
		R_L = 60Ω, -7V ≤ V_{CM} ≤ 12V (Figure 1B)		Full	2.4	3	-	V
Change in Magnitude of Driver Differential V_{OUT} for Complementary Output States	ΔV_{OD}	R_L = 54Ω or 100Ω (Figure 1A)		Full	-	0.01	0.2	V
Driver Common-Mode V_{OUT}	V_{OC}	R_L = 54Ω or 100Ω (Figure 1A)		Full	-	-	3.15	V
Change in Magnitude of Driver Common-Mode V_{OUT} for Complementary Output States	ΔV_{OC}	R_L = 54Ω or 100Ω (Figure 1A)		Full	-	0.01	0.2	V
Logic Input High Voltage	V_{IH}	DE, DI, $\overline{RE}$		Full	2	-	-	V
Logic Input Low Voltage	V_{IL}	DE, DI, $\overline{RE}$		Full	-	-	0.8	V
DI Input Hysteresis Voltage	V_{HYS}			25	-	100	-	mV
Logic Input Current	I_{IN1}	DE, DI, $\overline{RE}$		Full	-2	-	2	µA
Input Current (A/Y, B/Z)	I_{IN2}	DE = 0V, V_{CC} = 0V or 5.5V	V_{IN} = 12V	Full	-	70	125	µA
			V_{IN} = -7V	Full	-75	55	-	µA
Driver Short-Circuit Current, V_O = High or Low	I_{OSD1}	DE = V_{CC}, -7V ≤ V_Y or V_Z ≤ 12V (Note 7)		Full	-	-	±250	mA
Receiver Differential Threshold Voltage	V_{TH}	-7V ≤ V_{CM} ≤ 12V (Note 15)		Full	-200	-90	-50	mV
Receiver Input Hysteresis	ΔV_{TH}	V_{CM} = 0V		25	-	20	-	mV
Receiver Output High Voltage	V_{OH}	I_O = -8mA, V_{ID} = -50mV		Full	V_{CC} - 1.2	4.3	-	V
Receiver Output Low Voltage	V_{OL}	I_O = -8mA, V_{ID} = -200mV		Full	-	0.25	0.5	V
Receiver Output Low Current	I_{OL}	V_O = 1V, V_{ID} = -200mV		Full	15	28	-	mA

Electrical Specifications Test Conditions: V_{CC} = 4.5V to 5.5V; Unless Otherwise Specified. Typicals are at V_{CC} = 5V, T_A = +25°C (Note 5). Parameters with MIN and/or MAX limits are 100% tested at +25°C, unless otherwise specified. Temperature limits established by characterization and are not production tested. **(Continued)**

PARAMETER	SYMBOL	TEST CONDITIONS		TEMP (°C)	MIN	TYP	MAX	UNITS
Three-State (High Impedance) Receiver Output Current	I_{OZR}	0.4V ≤ V_O ≤ 2.4V		Full	-1	0.03	1	µA
Receiver Input Resistance	R_{IN}	-7V ≤ V_{CM} ≤ 12V		Full	96	160	-	kΩ
Receiver Short-Circuit Current	I_{OSR}	0V ≤ V_O ≤ V_{CC}		Full	±7	65	±85	mA
SUPPLY CURRENT								
No-Load Supply Current (Note 6)	I_{CC}	Half Duplex Versions, DE = V_{CC}, $\overline{RE}$ = X, DI = 0V or V_{CC}		Full	-	650	800	µA
		All Versions, DE = 0V, $\overline{RE}$ = 0V, or Full Duplex Versions, DE = V_{CC}, $\overline{RE}$ = X. DI = 0V or V_{CC}		Full	-	550	700	µA
Shutdown Supply Current	I_{SHDN}	DE = 0V, $\overline{RE}$ = V_{CC}, DI = 0V or V_{CC}		Full	-	0.07	3	µA
ESD PERFORMANCE								
RS-485 Pins (A/Y, B/Z)		IEC61000-4-2, Air-Gap Discharge Method	1/2 Duplex	25	-	±16.5	-	kV
		IEC61000-4-2, Contact Discharge Method		25	-	±9	-	kV
		Human Body Model, From Bus Pins to GND		25	-	±16.5	-	kV
All Pins		Human Body Model, per MIL-STD-883 Method 3015		25	-	±7	-	kV
		Machine Model		25	-	400	-	V
DRIVER SWITCHING CHARACTERISTICS (ISL3158AE)								
Driver Differential Output Delay	t_{PLH}, t_{PHL}	R_{DIFF} = 54Ω, C_L = 100pF (Figure 2)		Full	-	21	30	ns
Driver Differential Output Skew	t_{SKEW}	R_{DIFF} = 54Ω, C_L = 100pF (Figure 2)		Full	-	0.2	3	ns
Driver Differential Rise or Fall Time	t_R, t_F	R_{DIFF} = 54Ω, C_L = 100pF (Figure 2)		Full	-	12	16	ns
Maximum Data Rate	f_{MAX}	C_D = 470pF (Figure 4), (Note 15)		Full	-	10	-	Mbps
Driver Enable to Output High	t_{ZH}	R_L = 500Ω, C_L = 100pF, SW = GND (Figure 3), (Note 8)		Full	-	30	45	ns
Driver Enable to Output Low	t_{ZL}	R_L = 500Ω, C_L = 100pF, SW = V_{CC} (Figure 3), (Note 8)		Full	-	28	45	ns
Driver Disable from Output Low	t_{LZ}	R_L = 500Ω, C_L = 15pF, SW = V_{CC} (Figure 3)		Full	-	50	65	ns
Driver Disable from Output High	t_{HZ}	R_L = 500Ω, C_L = 15pF, SW = GND (Figure 3)		Full	-	38	65	ns
Time to Shutdown	t_{SHDN}	(Notes 10, 15)		Full	-	160	-	ns
Driver Enable from Shutdown to Output High	$t_{ZH(SHDN)}$	R_L = 500Ω, C_L = 100pF, SW = GND (Figure 3), (Notes 10, 11)		Full	-	-	200	ns
Driver Enable from Shutdown to Output Low	$t_{ZL(SHDN)}$	R_L = 500Ω, C_L = 100pF, SW = V_{CC} (Figure 3), (Notes 10, 11)		Full	-	-	200	ns
RECEIVER SWITCHING CHARACTERISTICS (ISL3158AE)								
Maximum Data Rate	f_{MAX}	(Figure 5) (Note 15)		Full	-	10	-	Mbps
Receiver Input to Output Delay	t_{PLH}, t_{PHL}	(Figure 5)		Full	-	33	50	ns
Receiver Skew | t_{PLH} - t_{PHL} |	t_{SKD}	(Figure 5)		Full	-	2.5	5	ns
Receiver Enable to Output Low	t_{ZL}	R_L = 1kΩ, C_L = 15pF, SW = V_{CC} (Figure 6), (Note 9)		Full	-	8	15	ns

Electrical Specifications Test Conditions: V_{CC} = 4.5V to 5.5V; Unless Otherwise Specified. Typicals are at V_{CC} = 5V, T_A = +25°C (Note 5). Parameters with MIN and/or MAX limits are 100% tested at +25°C, unless otherwise specified. Temperature limits established by characterization and are not production tested. **(Continued)**

PARAMETER	SYMBOL	TEST CONDITIONS	TEMP (°C)	MIN	TYP	MAX	UNITS
Receiver Enable to Output High	t_{ZH}	R_L = 1kΩ, C_L = 15pF, SW = GND (Figure 6), (Note 9)	Full	-	7	15	ns
Receiver Disable from Output Low	t_{LZ}	R_L = 1kΩ, C_L = 15pF, SW = V_{CC} (Figure 6)	Full	-	8	15	ns
Receiver Disable from Output High	t_{HZ}	R_L = 1kΩ, C_L = 15pF, SW = GND (Figure 6)	Full	-	8	15	ns
Time to Shutdown	t_{SHDN}	(Notes 10, 15)	Full	60	160	600	ns
Receiver Enable from Shutdown to Output High	$t_{ZH(SHDN)}$	R_L = 1kΩ, C_L = 15pF, SW = GND (Figure 6), (Notes 10, 12)	Full	-	-	200	ns
Receiver Enable from Shutdown to Output Low	$t_{ZL(SHDN)}$	R_L = 1kΩ, C_L = 15pF, SW = V_{CC} (Figure 6), (Notes 10, 12)	Full	-	-	200	ns

NOTES:

5. All currents into device pins are positive; all currents out of device pins are negative. All voltages are referenced to device ground unless otherwise specified.
6. Supply current specification is valid for loaded drivers when DE = 0V.
7. Applies to peak current. See “Typical Performance Curves” beginning on page 12 for more information.
8. Keep $\overline{RE}$ = 0 to prevent the device from entering SHDN.
9. The $\overline{RE}$ signal high time must be short enough (typically <100ns) to prevent the device from entering SHDN.
10. Transceivers are put into shutdown by bringing $\overline{RE}$ high and DE low. If the inputs are in this state for less than 60ns, the parts are guaranteed not to enter shutdown. If the inputs are in this state for at least 600ns, the parts are guaranteed to have entered shutdown. See “Low Power Shutdown Mode” on page 11.
11. Keep $\overline{RE}$ = VCC, and set the DE signal low time >600ns to ensure that the device enters SHDN.
12. Set the $\overline{RE}$ signal high time >600ns to ensure that the device enters SHDN.
13. See Figure 8 for more information, and for performance over-temperature.
14. For wafer sale, the switching test limits are established by characterization.
15. Limits established by characterization and are not production tested.

Test Circuits and Waveforms

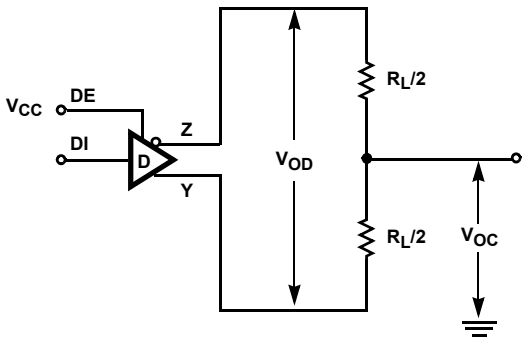


FIGURE 1A. V_{OD} AND V_{OC}

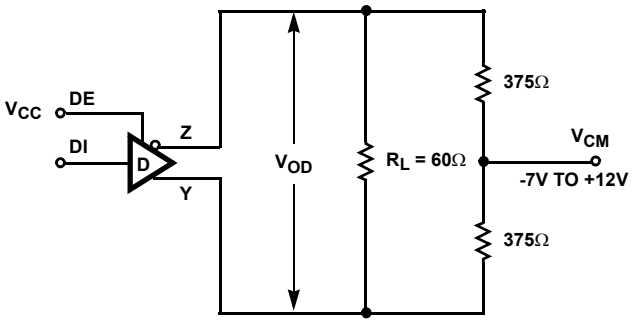


FIGURE 1B. V_{OD} WITH COMMON MODE LOAD

FIGURE 1. DC DRIVER TEST CIRCUITS

Test Circuits and Waveforms (Continued)

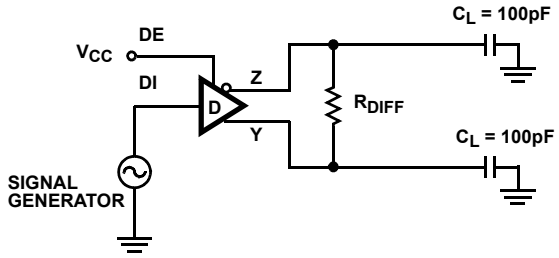


FIGURE 2A. TEST CIRCUIT

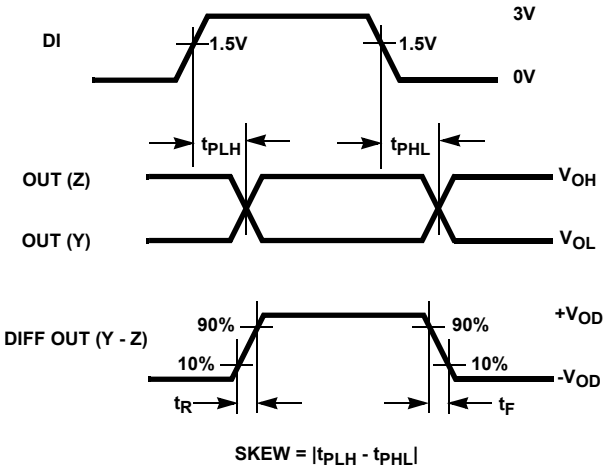
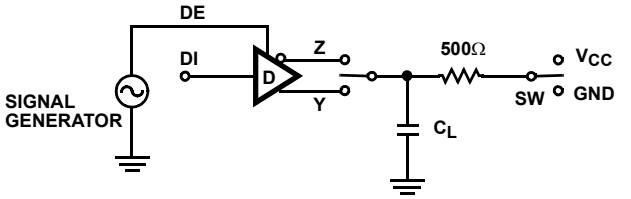


FIGURE 2B. MEASUREMENT POINTS

FIGURE 2. DRIVER PROPAGATION DELAY AND DIFFERENTIAL TRANSITION TIMES



PARAMETER	OUTPUT	$\overline{RE}$	DI	SW	C_L (pF)
t_{HZ}	Y/Z	X	1/0	GND	15
t_{LZ}	Y/Z	X	0/1	V_{CC}	15
t_{ZH}	Y/Z	0 (Note 8)	1/0	GND	100
t_{ZL}	Y/Z	0 (Note 8)	0/1	V_{CC}	100
$t_{ZH(SHDN)}$	Y/Z	1 (Note 11)	1/0	GND	100
$t_{ZL(SHDN)}$	Y/Z	1 (Note 11)	0/1	V_{CC}	100

FIGURE 3A. TEST CIRCUIT

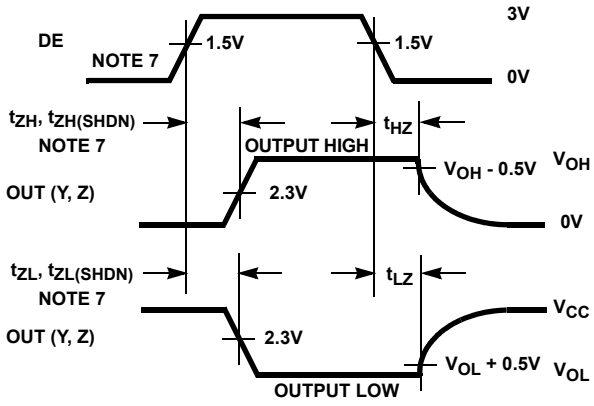


FIGURE 3B. MEASUREMENT POINTS

FIGURE 3. DRIVER ENABLE AND DISABLE TIMES

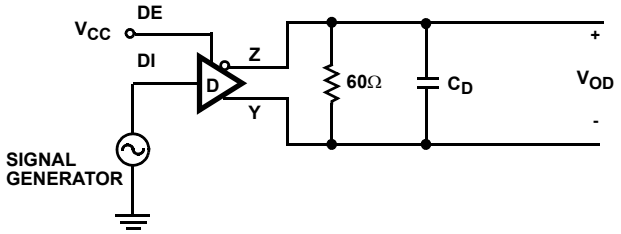


FIGURE 4A. TEST CIRCUIT

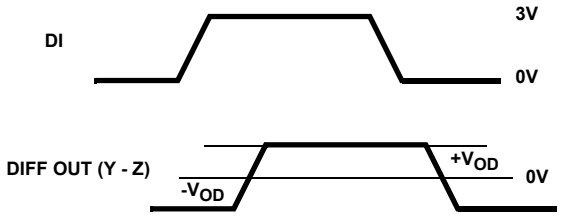


FIGURE 4B. MEASUREMENT POINTS

FIGURE 4. DRIVER DATA RATE

Test Circuits and Waveforms (Continued)

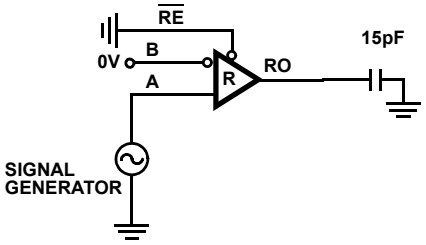


FIGURE 5A. TEST CIRCUIT

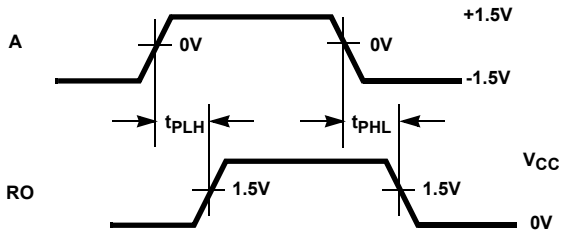
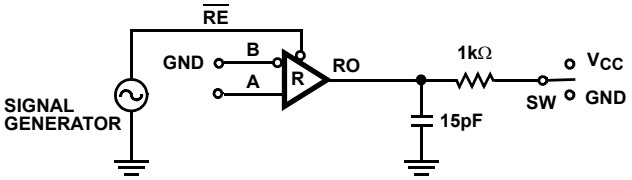


FIGURE 5B. MEASUREMENT POINTS

FIGURE 5. RECEIVER PROPAGATION DELAY AND DATA RATE



PARAMETER	DE	A	SW
t_{HZ}	0	+1.5V	GND
t_{LZ}	0	-1.5V	V_{CC}
t_{ZH} (Note 9)	0	+1.5V	GND
t_{ZL} (Note 9)	0	-1.5V	V_{CC}
$t_{ZH(SHDN)}$ (Note 12)	0	+1.5V	GND
$t_{ZL(SHDN)}$ (Note 12)	0	-1.5V	V_{CC}

FIGURE 6A. TEST CIRCUIT

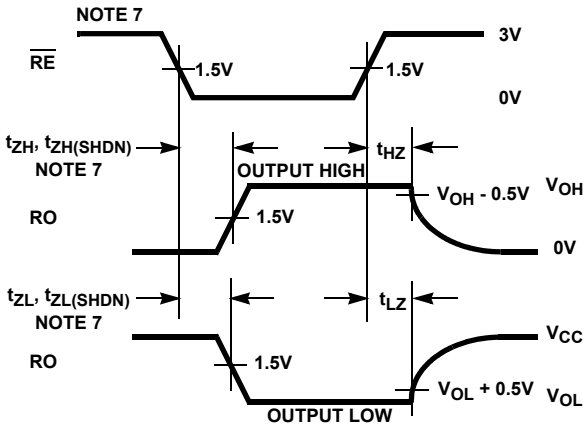


FIGURE 6B. MEASUREMENT POINTS

FIGURE 6. RECEIVER ENABLE AND DISABLE TIMES

Application Information

RS-485 and RS-422 are differential (balanced) data transmission standards used for long haul or noisy environments. RS-422 is a subset of RS-485, so RS-485 transceivers are also RS-422 compliant. RS-422 is a point-to-multipoint (multidrop) standard, which allows only one driver and up to 10 (assuming one unit load devices) receivers on each bus. RS-485 is a true multipoint standard, which allows up to 32 one unit load devices (any combination of drivers and receivers) on each bus. To allow for multipoint operation, the RS-485 specification requires that drivers must handle bus contention without sustaining any damage.

Another important advantage of RS-485 is the extended common mode range (CMR), which specifies that the driver outputs and receiver inputs withstand signals that range from +12V to -7V. RS-422 and RS-485 are intended for long runs, so the wide CMR is necessary to handle ground potential differences, as well as voltages induced in the cable by external fields.

Receiver (Rx) Features

This device utilizes a differential input receiver for maximum noise immunity and common mode rejection. Input sensitivity is better than ±200mV, as required by the RS-422 and RS-485 specifications.

Rx outputs feature high drive levels (typically 28mA @ V_{OL} = 1V to ease the design of optically coupled isolated interfaces).

Receiver input resistance of 96kΩ surpasses the RS-422 specification of 4kΩ, and is eight times the RS-485 “Unit Load (UL)” requirement of 12kΩ minimum. Thus, this product is known as a “one-eighth UL” transceiver, and there can be up to 256 of these devices on a network while still complying with the RS-485 loading specification.

Rx inputs function with common mode voltages as great as ±7V outside the power supplies (i.e., +12V and -7V), making them ideal for long networks where induced voltages are a realistic concern.

All the receivers include a “full fail-safe” function that guarantees a high level receiver output if the receiver inputs are unconnected (floating), shorted together, or connected to a terminated bus with all the transmitters disabled.

Receivers easily meet the data rates supported by the corresponding driver, and all receiver outputs are three-statable via the active low $\overline{RE}$ input.

Driver (Tx) Features

The RS-485/RS-422 driver is a differential output device that delivers at least 2.4V across a 54Ω load (RS-485), and at least 2.8V across a 100Ω load (RS-422). The driver features low propagation delay skew to maximize bit width, and to minimize EMI, and all drivers are three-stateable via the active high DE input.

Outputs of the ISL3158AE driver is not limited, so faster output transition times allow data rates of at least 10Mbps

High V_{OD} Improves Noise Immunity and Flexibility

The ISL3158AE driver design delivers larger differential output voltages (V_{OD}) than the RS-485 standard requires, or than most RS-485 transmitters can deliver. The minimum ±2.4V V_{OD} guarantees at least ±900mV more noise immunity than networks built using standard 1.5V V_{OD} transmitters.

Another advantage of the large V_{OD} is the ability to drive more than two bus terminations, which allows for utilizing the ISL3158AE in “star” and other multi-terminated, “non-standard” network topologies. Figure 8, details the transmitter’s V_{OD} vs I_{OUT} characteristic, and includes load lines for six (20Ω) and eight (15Ω) 120Ω terminations. The figure shows that the driver typically delivers 1.65/1.5V into 6/8 terminations, even at the worst case temperature of +85°C.The RS-485 standard requires a minimum 1.5V V_{OD} into two terminations, but the ISL3158AE delivers RS-485 voltage levels with 3x to 4x the number of terminations.

Hot Plug Function

When a piece of equipment powers up, there is a period of time where the processor or ASIC driving the RS-485 control lines (DE, $\overline{RE}$) is unable to ensure that the RS-485 Tx and Rx outputs are kept disabled. If the equipment is connected to the bus, a driver activating prematurely during power-up may crash the bus. To avoid this scenario, the ISL3158AE devices incorporate a “Hot Plug” function. Circuitry monitoring V_{CC} ensures that, during power-up and power-down, the Tx and Rx outputs remain disabled, regardless of the state of DE and $\overline{RE}$, if V_{CC} is less than ~3.4V. This gives the processor/ASIC a chance to stabilize and drive the RS-485 control lines to the proper states.

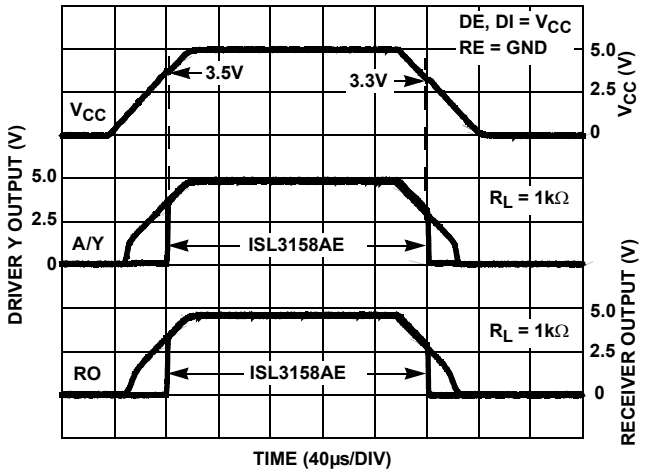


FIGURE 7. HOT PLUG PERFORMANCE (ISL3158AE) vs ISL83088E WITHOUT HOT PLUG CIRCUITRY

ESD Protection

All pins on this device includes class 3 (>7kV) Human Body Model (HBM) ESD protection structures, but the RS-485 pins (driver outputs and receiver inputs) incorporate advanced

structures allowing them to survive ESD events in excess of ±16.5kV HBM and ±16.5kV (1/2 duplex) IEC61000-4-2. The RS-485 pins are particularly vulnerable to ESD strikes because they typically connect to an exposed port on the exterior of the finished product. Simply touching the port pins, or connecting a cable, can cause an ESD event that might destroy unprotected ICs. These new ESD structures protect the device whether or not it is powered up, and without degrading the RS-485 common mode range of -7V to +12V. This built-in ESD protection eliminates the need for board level protection structures (e.g., transient suppression diodes), and the associated, undesirable capacitive load they present.

IEC61000-4-2 Testing

The IEC61000 test method applies to finished equipment, rather than to an individual IC. Therefore, the pins most likely to suffer an ESD event are those that are exposed to the outside world (the RS-485 pins in this case), and the IC is tested in its typical application configuration (power applied) rather than testing each pin-to-pin combination. The IEC61000 standard's lower current limiting resistor coupled with the larger charge storage capacitor yields a test that is much more severe than the HBM test. The extra ESD protection built into this device's RS-485 pins allows the design of equipment meeting level 4 criteria without the need for additional board level protection on the RS-485 port.

AIR-GAP DISCHARGE TEST METHOD

For this test method, a charged probe tip moves toward the IC pin until the voltage arcs to it. The current waveform delivered to the IC pin depends on approach speed, humidity, temperature, etc., so it is difficult to obtain repeatable results. The ISL3158AE 1/2 duplex RS-485 pins withstand ±16.5kV air-gap discharges.

CONTACT DISCHARGE TEST METHOD

During the contact discharge test, the probe contacts the tested pin before the probe tip is energized, thereby eliminating the variables associated with the air-gap discharge. The result is a more repeatable and predictable test, but equipment limits prevent testing devices at voltages higher than ±9kV. The RS-485 pins of all the ISL3158AE versions survive ±9kV contact discharges.

Data Rate, Cables, and Terminations

RS-485/RS-422 are intended for network lengths up to 4000', but the maximum system data rate decreases as the transmission length increases. Devices operating at 10Mbps are limited to lengths of less than 100'.

Twisted pair is the cable of choice for RS-485/RS-422 networks. Twisted pair cables tend to pick up noise and other electromagnetically induced voltages as common mode signals, which are effectively rejected by the differential receivers in these ICs.

Proper termination is imperative, when using the 10Mbps devices, to minimize reflections. Terminations are recommended unless power dissipation is an overriding concern.

In point-to-point, or point-to-multipoint (single driver on bus) networks, the main cable should be terminated in its characteristic impedance (typically 120Ω) at the end farthest from the driver. In multi-receiver applications, stubs connecting receivers to the main cable should be kept as short as possible. Multipoint (multi-driver) systems require that the main cable be terminated in its characteristic impedance at both ends. Stubs connecting a transceiver to the main cable should be kept as short as possible.

Built-In Driver Overload Protection

As stated previously, the RS-485 specification requires that drivers survive worst case bus contentions undamaged. These devices meet this requirement via driver output short circuit current limit circuitry.

The driver output stages incorporate short circuit current limiting circuitry which ensures that the output current never exceeds the RS-485 specification, even at the common mode voltage range extremes.

Low Power Shutdown Mode

This CMOS transceiver uses a fraction of the power required by it's bipolar counterparts, but it also includes a shutdown feature that reduces the already low quiescent I_{CC} to a 70nA trickle. This device enters shutdown whenever the receiver and driver are ***simultaneously*** disabled ($\overline{RE}$ = V_{CC} and DE = GND) for a period of at least 600ns. Disabling both the driver and the receiver for less than 60ns guarantees that the transceiver will not enter shutdown.

Note that receiver and driver enable times increase when the transceiver enables from shutdown. Refer to Notes 8, 9, 10, 11 and 12, at the end of the "Electrical Specification" table on page 6, for more information.

Typical Performance Curves V_{CC} = 5V, T_A = +25°C; Unless Otherwise Specified.

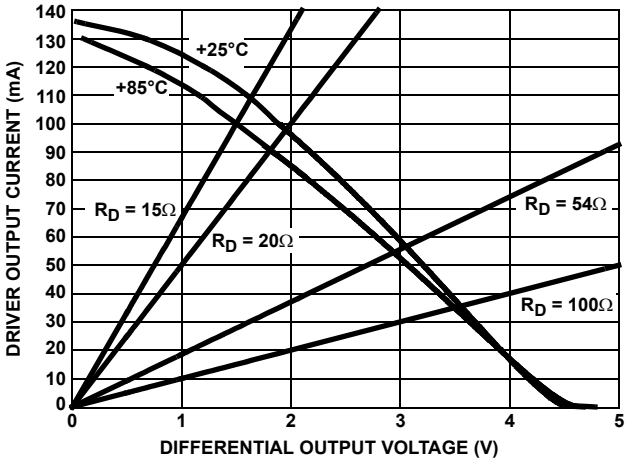


FIGURE 8. DRIVER OUTPUT CURRENT vs DIFFERENTIAL OUTPUT VOLTAGE

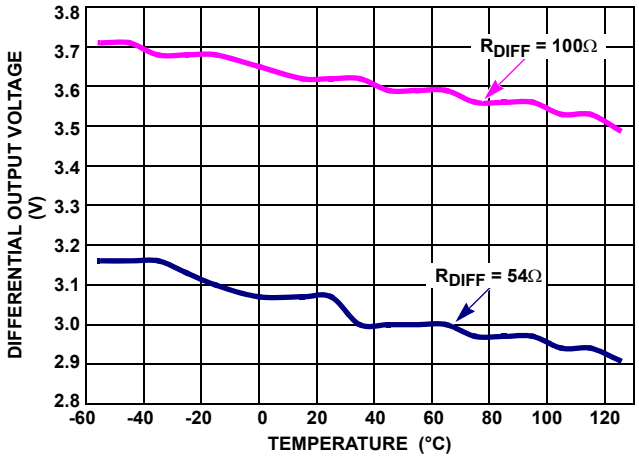


FIGURE 9. DRIVER DIFFERENTIAL OUTPUT VOLTAGE vs TEMPERATURE

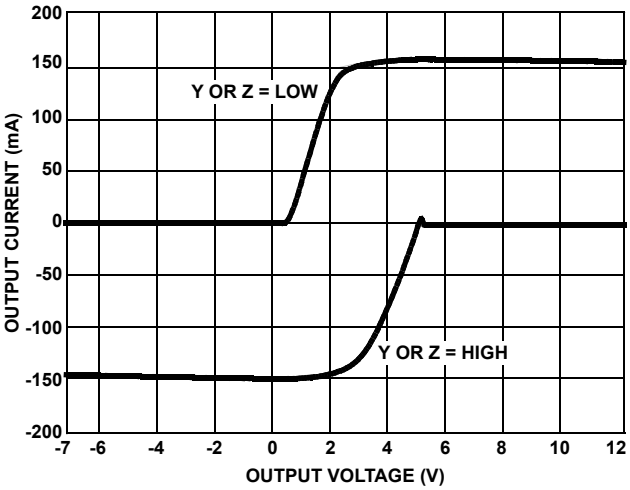


FIGURE 10. DRIVER OUTPUT CURRENT vs SHORT CIRCUIT VOLTAGE

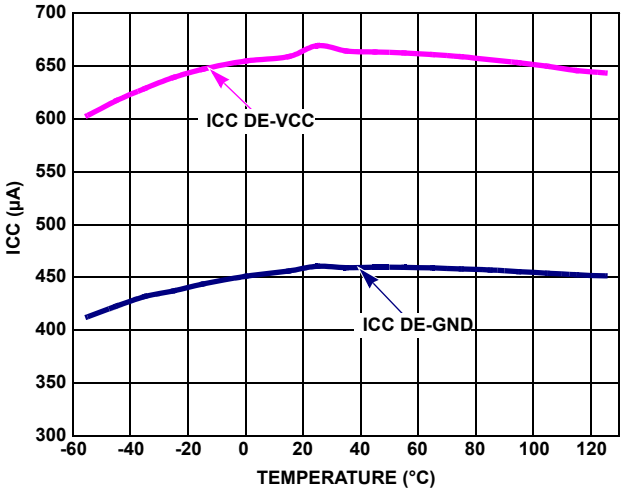


FIGURE 11. SUPPLY CURRENT vs TEMPERATURE

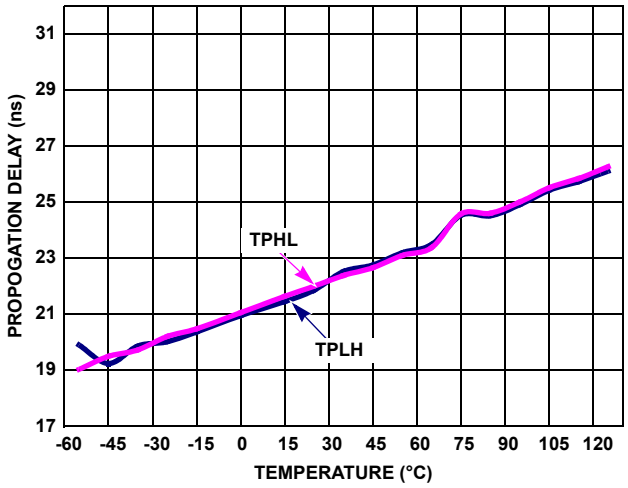


FIGURE 12. DRIVER DIFFERENTIAL PROPAGATION DELAY vs TEMPERATURE (ISL3158AE)

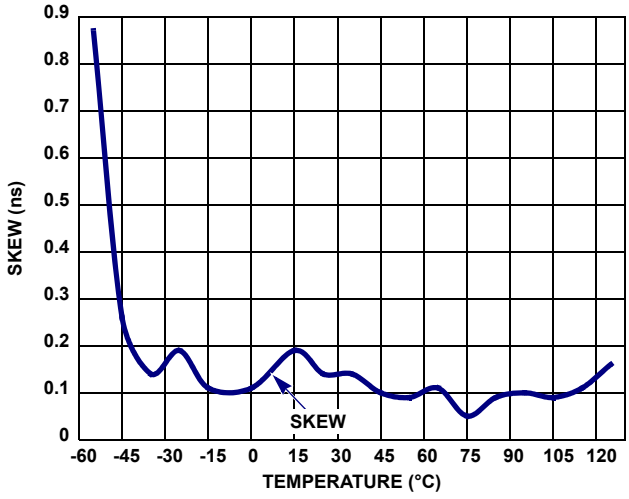


FIGURE 13. DRIVER DIFFERENTIAL SKEW vs TEMPERATURE (ISL3158AE)

Typical Performance Curves V_{CC} = 5V, T_A = +25°C; Unless Otherwise Specified. **(Continued)**

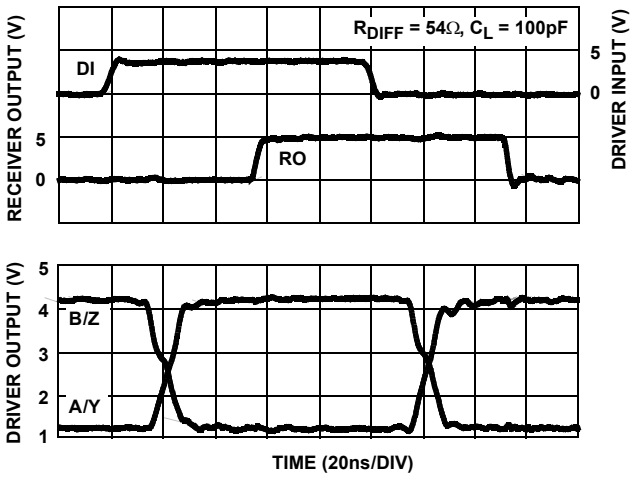


FIGURE 14. DRIVER AND RECEIVER WAVEFORMS, (ISL3158AE)

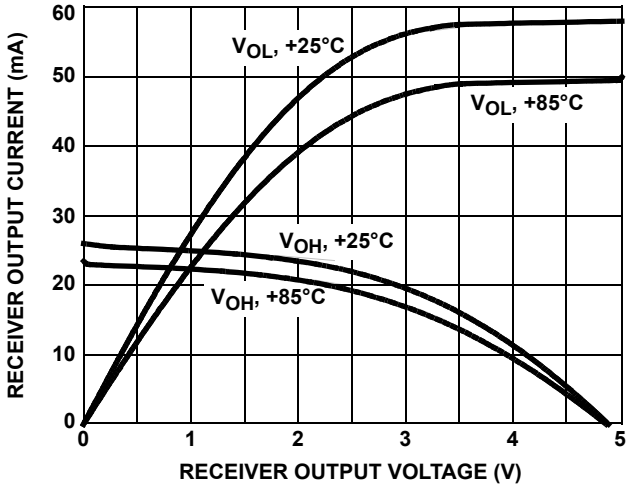


FIGURE 15. RECEIVER OUTPUT CURRENT vs RECEIVER OUTPUT VOLTAGE

Die Characteristics

DIE DIMENSIONS INCLUDING 50MM SCRIBE

Thickness: 14 mils
1400µm x 1530µm

Interface Materials

GLASSIVATION

Sandwich TEOS and Nitride

TOP METALLIZATION

Type: Al with 0.5% Cu
Thickness: 28kÅ

SUBSTRATE

N/A

BACKSIDE FINISH

Silicon/Polysilicon/Oxide

Assembly Related Information

SUBSTRATE POTENTIAL

GND (powered up)

Additional Information

WORST CASE CURRENT DENSITY

N/A

PROCESS

Si GateBiCMOS, IBM P6

TRANSISTOR COUNT

530

PAD OPENING SIZE:

90µm x 90µm

WAFER SIZE:

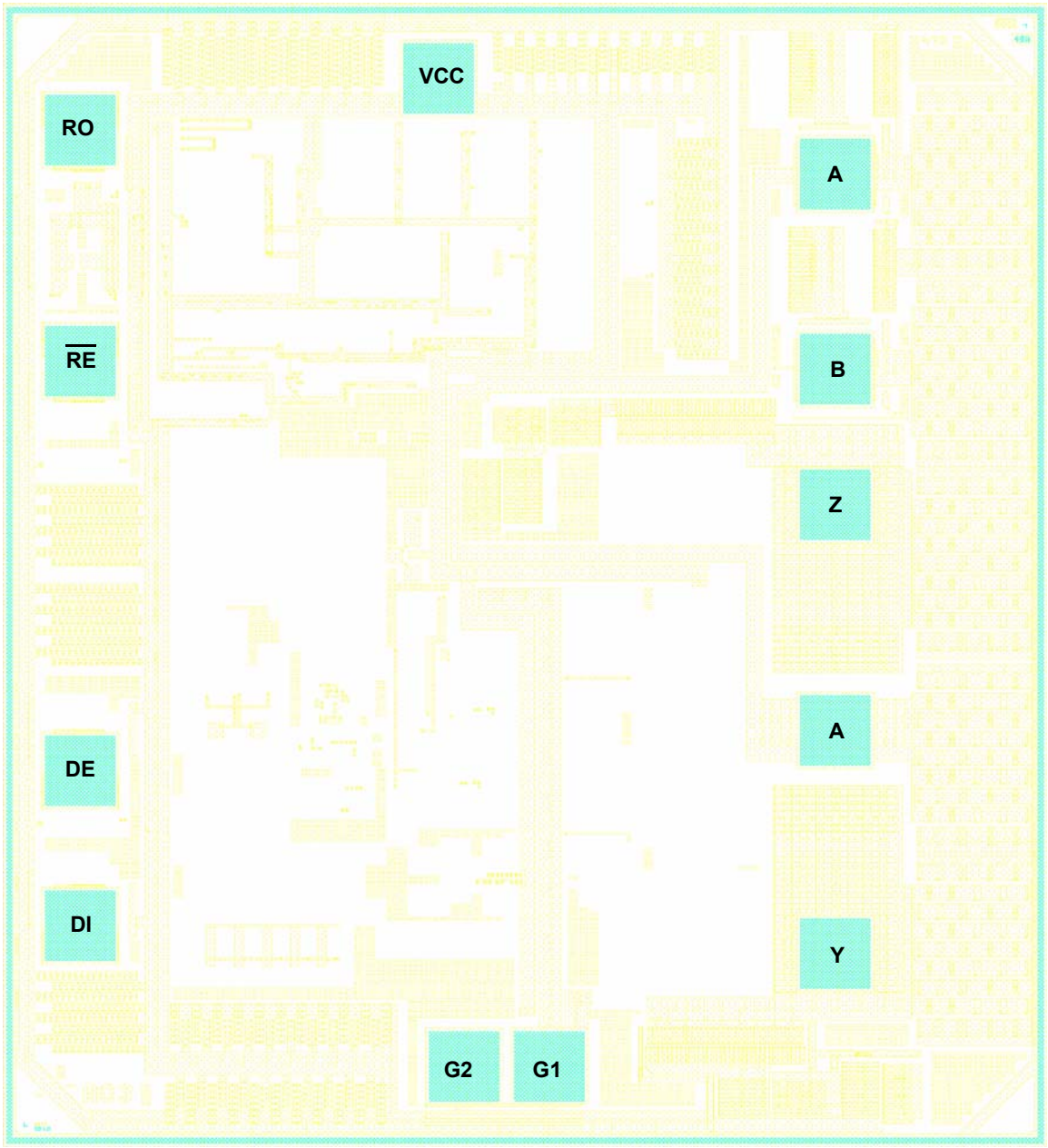
200mm (~8 inch)

TABLE 2. BOND PAD FUNCTION AND COORDINATES

PAD #	FUNCTION	X (µm)	Y (µm)
1	RO	99.5	1308
2	$\overline{RE}$	99.5	1014.35
3	DE	99.5	498.3
4	DI	99.5	286.75
5	GND2	574.3	104.7
6	GND1	684.3	104.7
7	Y	1054	250.6
8	A (half duplex)	1054	540.45
9	Z	1054	831.1
10	B	1054	1004.65
11	A (full duplex)	1054	1256.45
12	V_{CC}	562.55	1385.35

Metallization Mask Layout

ISL3158AE

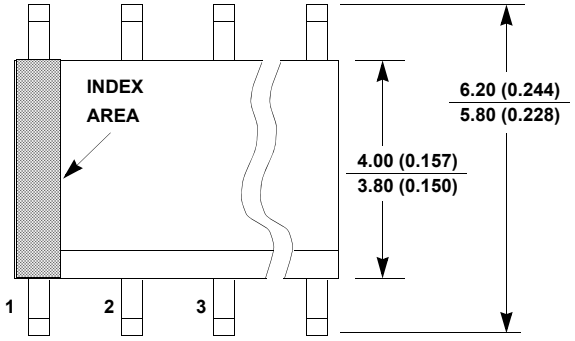


Package Outline Drawing

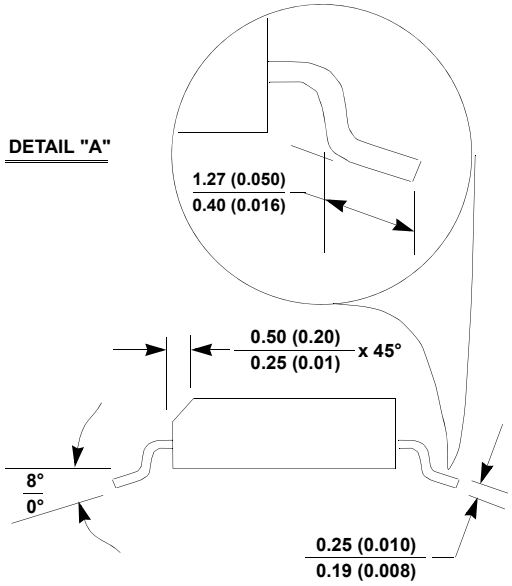
M8.15

8 LEAD NARROW BODY SMALL OUTLINE PLASTIC PACKAGE

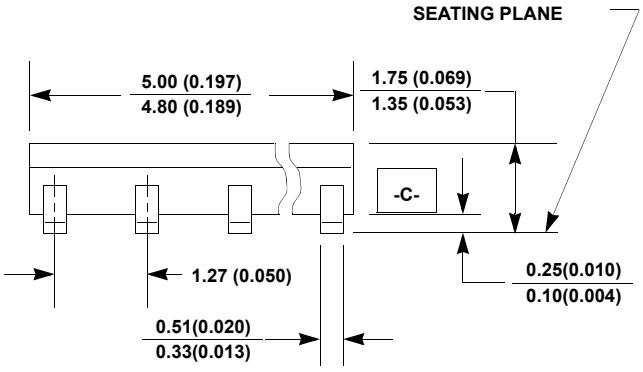
Rev 4, 1/12



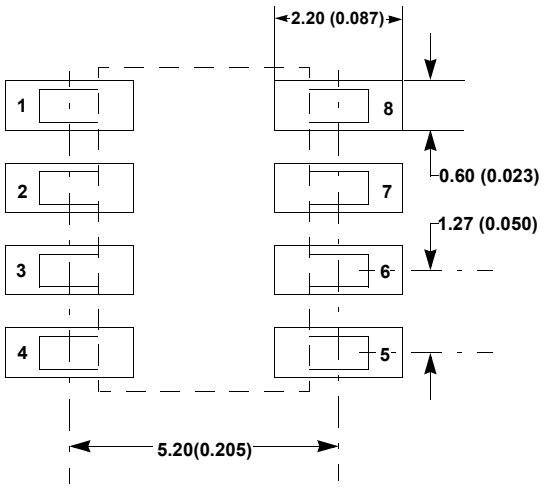
TOP VIEW



SIDE VIEW "B"



SIDE VIEW "A"



TYPICAL RECOMMENDED LAND PATTERN

NOTES:

1. Dimensioning and tolerancing per ANSI Y14.5M-1994.
2. Package length does not include mold flash, protrusions or gate burrs. Mold flash, protrusion and gate burrs shall not exceed 0.15mm (0.006 inch) per side.
3. Package width does not include interlead flash or protrusions. Interlead flash and protrusions shall not exceed 0.25mm (0.010 inch) per side.
4. The chamfer on the body is optional. If it is not present, a visual index feature must be located within the crosshatched area.
5. Terminal numbers are shown for reference only.
6. The lead width as measured 0.36mm (0.014 inch) or greater above the seating plane, shall not exceed a maximum value of 0.61mm (0.024 inch).
7. Controlling dimension: MILLIMETER. Converted inch dimensions are not necessarily exact.
8. This outline conforms to JEDEC publication MS-012-AA ISSUE C.