DATASHEET

# ISL32743E

## Isolated 3.3V Half-Duplex 40Mbps RS-485 Transceiver

FN8987
Rev. 1.00
Jul 9, 2018

The ISL32743E is a galvanically isolated high-speed differential bus transceiver, designed for bidirectional data communication on balanced transmission lines. The device uses Giant Magnetoresistance (GMR) as its isolation technology.

The part is available in a 16 Ld SOICW package providing a true 8mm creepage distance.

A unique ceramic/polymer composite barrier provides excellent isolation and 44000 years of barrier life.

The device is compatible with 3V and 5V input supplies, allowing an interface to standard microcontrollers without additional level shifting.

Current limiting and thermal shutdown features protect against output short-circuits and bus contention that may cause excessive power dissipation. Receiver inputs are a full fail-safe design, ensuring a logic high R-output if A/B are floating or shorted.

## Applications

- Factory automation
- Building environmental control systems
- Process control networks
- Equipment covered under IEC 61010-1 Edition 3

## Features

- 40Mbps data rate
- 2.5k$V_{RMS}$ isolation/600$V_{RMS}$ working voltage
- 3.3V bus
- 20ns propagation delay
- 5ns pulse skew
- 1/5 unit load allows up to 160 devices on the bus
- 50kV/µs (typical), 30kV/µs (minimum) common-mode transient immunity
- 16.5kV ESD protection
- Low EMC footprint
- Thermal shutdown protection
- Temperature range: -40°C to +85°C
- Meets or exceeds ANSI RS-485 and ISO 8482:1987(E)
- True 8mm 16 Ld SOICW packages
- UL 1577 recognized
- VDE V 0884-11 pending

## Related Literature

For a full list of related documents, visit our website

- ISL32743E product page

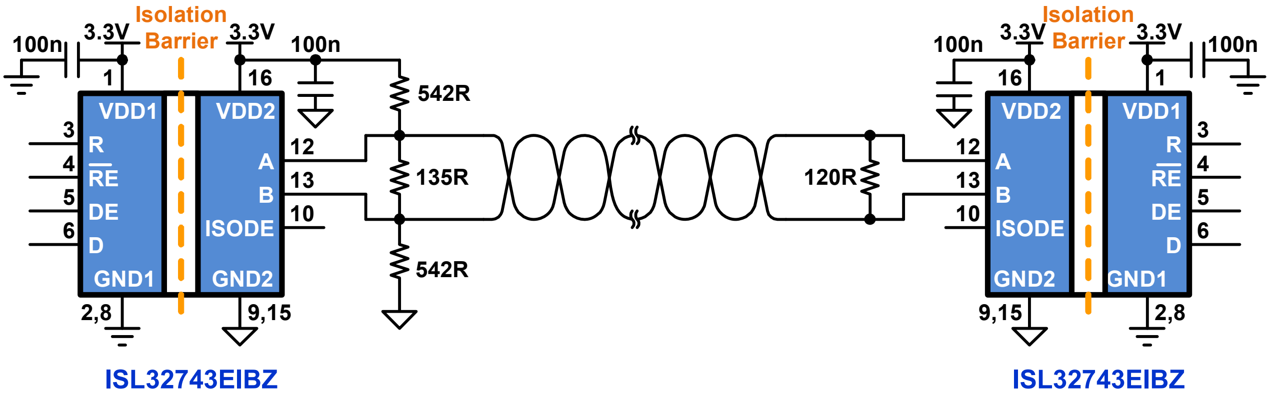


Figure 1. Typical Application

# 1. Overview

## 1.1 Typical Operating Circuits

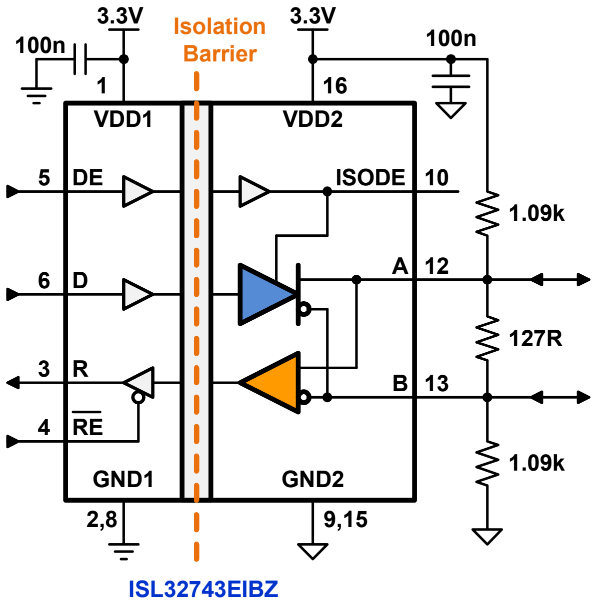


Figure 2. Typical Operating Circuit

## 1.2 Ordering Information

| Part Number (Notes 2, 3) | Part Marking | Temp. Range (°C) | Tape and Reel (Units) (Note 1) | Package (RoHS Compliant) | Pkg. Dwg. # |
|---|---|---|---|---|---|
| ISL32743EIBZ | 32743EIBZ | -40 to +85 | - | 16 Ld SOICW | M16.3A |
| ISL32743EIBZ-T | 32743EIBZ | -40 to +85 | 1k | 16 Ld SOICW | M16.3A |
| ISL32743EIBZ-T7A | 32743EIBZ | -40 to +85 | 250 | 16 Ld SOICW | M16.3A |

Notes:

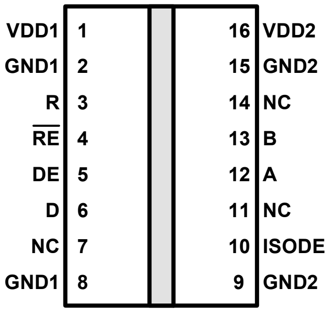
1. Refer to TB347 for details about reel specifications.
2. Pb-free plus anneal products employ special Pb-free material sets; molding compounds/die attach materials and 100% matte tin plate termination finish, which are RoHS compliant and compatible with both SnPb and Pb-free soldering operations. Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020.
3. For Moisture Sensitivity Level (MSL), refer to the ISL32743E product information page. For more information about MSL, refer to TB363.

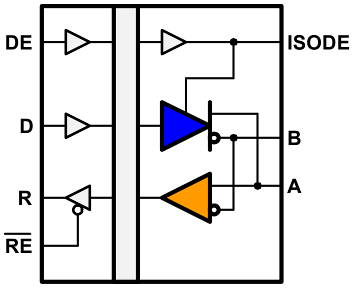
Table 1. Key Differences Between Family of Parts

| Part Number | Full/Half Duplex | $V_{DD1}$ (V) | $V_{DD2}$ (V) | Data Rate (Mbps) | Isolation Voltage ($kV_{RMS}$) |
|---|---|---|---|---|---|
| ISL32704E | Half | 3.0 – 5.5 | 4.5 – 5.5 | 4 | 2.5 |
| ISL32705E | Full | 3.0 – 5.5 | 4.5 – 5.5 | 4 | 2.5 |
| ISL32740E | Half | 3.0 – 5.5 | 4.5 – 5.5 | 40 | 2.5 |
| ISL32741E | Half | 3.0 – 5.5 | 4.5 – 5.5 | 40 | 6 |
| ISL32743E | Half | 3.0 – 5.5 | 3.0 – 3.6 | 40 | 2.5 |
| ISL32745E | Full | 3.0 – 5.5 | 4.5 – 5.5 | 40 | 6 |

## 1.3 Pin Configurations

ISL32743E
(16 Ld SOICW)
Top View





## 1.4 Truth Tables

| Transmitting | | | | |
|---|---|---|---|---|
| Inputs | | Outputs | | |
| DE | D | ISODE | B | A |
| 1 | 1 | 1 | 0 | 1 |
| 1 | 0 | 1 | 1 | 0 |
| 0 | X | 0 | High-Z | High-Z |

| Receiving | | |
|---|---|---|
| Inputs | | Output |
| $\overline{\text{RE}}$ | A-B | RO |
| 0 | $V_{AB} \geq -0.05V$ | 1 |
| 0 | $-0.05 > V_{AB} > -0.2V$ | Undetermined |
| 0 | $V_{AB} \leq -0.2V$ | 0 |
| 0 | Inputs Open/Shorted | 1 |
| 1 | X | High-Z |

## 1.5 Pin Descriptions

| Pin Number<br>16 Ld SOICW | Pin Name | Function |
|---|---|---|
| 1 | VDD1 | Input power supply. |
| 2, 8 | GND1 | Input power supply ground return. Pin 2 is internally connected to Pin 8 (for SOIC package). |
| 3 | R | Receiver output: If A-B ≥-50mV, R is high; If A-B ≤-200mV, R is low; R = High if A and B are unconnected (floating) or shorted, or connected to a terminated bus that is not driven. |
| 4 | $\overline{\text{RE}}$ | Receiver output enable. R is enabled when $\overline{\text{RE}}$ is low; R is high impedance when $\overline{\text{RE}}$ is high. If the Rx enable function is not required, connect $\overline{\text{RE}}$ directly to GND1. |
| 5 | DE | Driver output enable. The driver outputs, A and B, are enabled by bringing DE high. They are high impedance when DE is low. If the Tx enable function is not required, connect DE to VDD1 through a 1kΩ or greater resistor. |
| 6 | D | Driver input. A low on D forces output A low and output B high. Similarly, a high on D forces output A high and output B low. |
| 7, 11, 14 | NC | No internal connection. |
| 9, 15 | GND2 | Output power supply ground return. Dual ground pins are connected internally. |
| 10 | ISODE | Isolated DE output for use in applications in which the state of the isolated drive enable node needs to be monitored. |
| 12 | A | ±16.5kV IEC61000 ESD protected RS-485/RS422 level, noninverting receiver input if DE = 0 and noninverting driver output if DE = 1. |
| 13 | B | ±16.5kV IEC61000 ESD protected RS-485/RS422 level, inverting receiver input if DE = 0 and inverting driver output if DE = 1. |
| 16 | VDD2 | Output power supply. |

# 2. Specifications

## 2.1 Absolute Maximum Ratings

| Parameter (Note 4) | Minimum | Maximum | Unit |
|---|---|---|---|
| **Supply Voltages (Note 7)** | | | |
| VDD1 to GND1 | -0.5 | +7 | V |
| VDD2 to GND2 | | 7 | V |
| Input Voltages D, DE, $\overline{RE}$ | -0.5 | VDD1 + 0.5 | V |
| **Input/Output Voltages** | | | |
| A, B | -9 | +13 | V |
| R | -0.5 | VDD1 + 1 | V |
| Short-Circuit Duration A, B | Continuous | | V |
| ESD Rating | See “Electrical Specifications” on page 7 | | |

Note:

4. Absolute Maximum specifications mean the device will not be damaged if operated under these conditions. It does not guarantee performance.

CAUTION: Do not operate at or near the maximum ratings listed for extended periods of time. Exposure to such conditions may adversely impact product reliability and result in failures not covered by warranty.

## 2.2 Thermal Information

| Thermal Resistance (Typical) | $\theta_{JA}$ (°C/W) | $\theta_{JC}$ (°C/W) |
|---|---|---|
| 16 Ld SOICW Package (Notes 5, 6) | 43 | 20 |

Notes:

5. $\theta_{JA}$ is measured in free air with the component soldered to a double-sided board.
6. For $\theta_{JC}$, the “case temp” location is the center of the package top side.

| Parameter | Minimum | Maximum | Unit |
|---|---|---|---|
| Maximum Junction Temperature (Plastic Package) | -55 | +150 | °C |
| Maximum Storage Temperature Range | -55 | +150 | °C |
| Maximum Power Dissipation | | 800 | mW |
| Pb-Free Reflow Profile | see TB493 | | |

## 2.3 Recommended Operation Conditions

| Parameter | Minimum | Maximum | Unit |
|---|---|---|---|
| **Supply Voltages** | | | |
| $V_{DD1}$ | 3.0 | 5.5 | V |
| $V_{DD2}$ | 3.0 | 3.6 | V |
| **High-Level Digital Input Voltage, $V_{IH}$** | | | |
| $V_{DD1}$ = 3.3V | 2.4 | $V_{DD1}$ | V |
| $V_{DD1}$ = 5.0V | 3.0 | $V_{DD1}$ | V |
| Low-Level Digital Input Voltage, $V_{IL}$ | 0 | 0.8 | V |
| Differential Input Voltage, $V_{ID}$ (Note 8) | -7 | 12 | V |

| Parameter | Minimum | Maximum | Unit |
|---|---|---|---|
| High-Level Output Current (Driver), $I_{OH}$ | | 60 | mA |
| High-Level Digital Output Current (Receiver), $I_{OH}$ | | 8 | mA |
| Low-Level Output Current (Driver), $I_{OL}$ | | -60 | mA |
| Low-Level Digital Output Current (Receiver), $I_{OL}$ | | -8 | mA |
| Junction Temperature, $T_J$ | -40 | +110 | °C |
| Ambient Operating Temperature, $T_A$ | -40 | +85 | °C |
| Digital Input Signal Rise and Fall Times, $t_{IR}$, $t_{IF}$ | | DC Stable | |

## 2.4 Electrical Specifications

Test conditions: $T_{min}$ to $T_{max}$, $V_{DD2}$ = 3.0V to 3.6V; unless otherwise stated (Note 7).

| Parameter | Symbol | Test Conditions | Min | Typ (Note 11) | Max | Unit |
|---|---|---|---|---|---|---|
| **DC Characteristics** | | | | | | |
| Driver Line Output Voltage ($V_A$, $V_B$) (Note 7) | $V_O$ | No load | - | - | $V_{DD2}$ | V |
| Driver Differential Output Voltage (Note 8) | $V_{OD1}$ | No load | - | - | $V_{DD2}$ | V |
| Driver Differential Output Voltage (Note 8) | $V_{OD2}$ | $R_L$ = 54Ω | 1.5 | 2.1 | $V_{DD2}$ | V |
| Driver Differential Output Voltage (Notes 8, 12) | $V_{OD3}$ | $R_L$ = 60Ω | 1.5 | 2.0 | - | V |
| Change in Magnitude of Differential Output Voltage (Note 13) | $\Delta V_{OD}$ | $R_L$ = 54Ω or 100Ω | - | 0.01 | 0.20 | V |
| Driver Common-Mode Output Voltage | $V_{OC}$ | $R_L$ = 54Ω or 100Ω | - | 2 | 2.5 | V |
| Change in Magnitude of Driver Common-Mode Output Voltage (Note 13) | $\Delta V_{OC}$ | $R_L$ = 54Ω or 100Ω | - | 0.02 | 0.20 | V |
| Bus Input Current (A, B) (Notes 10, 14) | $I_{IN2}$ | DE = 0V $V_{IN}$ = 12V | | - | 220 | µA |
| | | $V_{IN}$ = -7V | -160 | | | µA |
| High-Level Input Current (DI, DE, $\overline{RE}$) | $I_{IH}$ | $V_I$ = 3.5V | - | - | 10 | µA |
| Low-Level Input Current (DI, DE, $\overline{RE}$) | $I_{IL}$ | $V_I$ = 0.4V | -10 | - | - | µA |
| Absolute Short-Circuit Output Current | $I_{OS}$ | DE = $V_{DD1}$, -7V ≤ $V_A$ or $V_B$ ≤ 12V | - | - | ±250 | mA |
| Supply Current | $I_{DD1}$ | $V_{DD1}$ = 5V | - | 4 | 6 | mA |
| | | $V_{DD1}$ = 3.3V | - | 3 | 4 | mA |
| Positive-Going Input Threshold Voltage | $V_{TH+}$ | -7V ≤ $V_{CM}$ ≤ 12V | - | - | -50 | mV |
| Negative-Going Input Threshold Voltage | $V_{TH-}$ | -7V ≤ $V_{CM}$ ≤ 12V | -200 | - | - | mV |
| Receiver Input Hysteresis | $V_{HYS}$ | $V_{CM}$ = 0V | - | 28 | - | mV |
| Differential Bus Input Capacitance | $C_D$ | | - | 9 | 12 | pF |
| Receiver Output High Voltage | $V_{OH}$ | $I_O$ = -20µA, $V_{ID}$ = -50mV | $V_{DD2}$ - 0.2 | - | - | V |
| Receiver Output Low Voltage | $V_{OL}$ | $I_O$ = +20µA, $V_{ID}$ = -200mV | - | - | 0.2 | V |
| High impedance Output Current | $I_{OZ}$ | 0.4V ≤ $V_O$ ≤ ($V_{DD2}$ - 0.5) | -1 | - | 1 | µA |
| Receiver Input Resistance | $R_{IN}$ | -7V ≤ $V_{CM}$ ≤ 12V | 54 | 80 | - | kΩ |
| Supply Current | $I_{DD2}$ | DE = $V_{DD1}$, no load | - | 5 | 16 | mA |

Test conditions: $T_{min}$ to $T_{max}$, $V_{DD2}$ = 3.0V to 3.6V; unless otherwise stated (Note 7). **(Continued)**

| Parameter | Symbol | Test Conditions | Min | Typ (Note 11) | Max | Unit |
|---|---|---|---|---|---|---|
| **ESD Performance** | | | | | | |
| RS-485 Bus Pins (A, B) | | IEC61000-4-2, air-gap discharge to GND2 | - | ±16.5 | - | kV |
| | | IEC61000-4-2, contact discharge to GND2 | - | ±9 | - | kV |
| | | Human Body Model discharge (HBM) to GND2 | - | ±16.5 | - | kV |
| All Pins (R, $\overline{RE}$, D, DE) | | Human Body Model discharge (HBM) to GND1 | - | ±2 | - | kV |
| **Switching Characteristics** | | | | | | |
| **$V_{DD1}$ = 5V, $V_{DD2}$ = 3.3V** | | | | | | |
| Data Rate | DR | $R_L$ = 54Ω, $C_L$ = 50pF | 40 | - | - | Mbps |
| Propagation Delay (Notes 8, 15) | $t_{PD}$ | $V_O$ = -1.5V to 1.5V, $C_L$ = 15pF | - | 20 | 30 | ns |
| Pulse Skew (Notes 8, 16) | $t_{SK}$ (P) | $V_O$ = -1.5V to 1.5V, $C_L$ = 15pF | - | 1 | 5 | ns |
| Skew Limit (Note 9) | $t_{SK}$ (LIM) | $R_L$ = 54Ω, $C_L$ = 50pF | - | 2 | 10 | ns |
| Output Enable Time to High Level | $t_{PZH}$ | $C_L$ = 15pF | - | 15 | 30 | ns |
| Output Enable Time to Low Level | $t_{PZL}$ | $C_L$ = 15pF | - | 15 | 30 | ns |
| Output Disable Time from High Level | $t_{PHZ}$ | $C_L$ = 15pF | - | 15 | 30 | ns |
| Output Disable Time from Low Level | $t_{PLZ}$ | $C_L$ = 15pF | - | 15 | 30 | ns |
| Common-Mode Transient Immunity | CMTI | $V_{CM}$ = 1500 $V_{DC}$, $t_{TRANSIENT}$ = 25ns | 30 | 50 | - | kV/µs |
| **$V_{DD1}$ = 3.3V, $V_{DD2}$ = 3.3V** | | | | | | |
| Data Rate | DR | $R_L$ = 54Ω, $C_L$ = 50pF | 40 | - | - | Mbps |
| Propagation Delay (Notes 8, 9) | $t_{PD}$ | $V_O$ = -1.5V to 1.5V, $C_L$ = 15pF | - | 25 | 35 | ns |
| Pulse Skew (Notes 8, 9) | $t_{SK}$ (P) | $V_O$ = -1.5V to 1.5V, $C_L$ = 15pF | - | 2 | 5 | ns |
| Skew Limit (Note 9) | $t_{SK}$ (LIM) | $R_L$ = 54Ω, $C_L$ = 50pF | - | 4 | 10 | ns |
| Output Enable Time to High Level | $t_{PZH}$ | $C_L$ = 15pF | - | 17 | 30 | ns |
| Output Enable Time to Low Level | $t_{PZL}$ | $C_L$ = 15pF | - | 17 | 30 | ns |
| Output Disable Time from High Level | $t_{PHZ}$ | $C_L$ = 15pF | - | 17 | 30 | ns |
| Output Disable Time from Low Level | $t_{PLZ}$ | $C_L$ = 15pF | - | 17 | 30 | ns |
| Common-Mode Transient Immunity | CMTI | $V_{CM}$ = 1500 $V_{DC}$, $t_{TRANSIENT}$ = 25ns | 30 | 50 | - | kV/µs |

Notes: (Apply to both driver and receiver sections)

7. All voltages on the isolator primary side are with respect to GND1. All line voltages and common-mode voltages on the isolator secondary or bus side are with respect to GND2.
8. Differential I/O voltage is measured at the noninverting bus Terminal A with respect to the inverting Terminal B.
9. Skew limit is the maximum propagation delay difference between any two devices at +25°C.
10. The power-off measurement in ANSI Standard EIA/TIA-422-B applies to disabled outputs only and is not applied to combined inputs and outputs.
11. All typical values are at $V_{DD1}$, $V_{DD2}$ = 5V or $V_{DD1}$ = 3.3V and $T_A$ = +25°C.
12. $-7V < V_{CM} < 12V$; $4.5 < V_{DD} < 5.5V$.
13. $\Delta V_{OD}$ and $\Delta V_{OC}$ are the changes in magnitude of $\Delta V_{OD}$ and $\Delta V_{OD}$ respectively, that occur when the input is changed from one logic state to the other.
14. This applies for both power-on and power-off; refer to ANSI standard RS-485 for the exact condition. The EIA/TIA-422 -B limit does not apply for a combined driver and receiver terminal.
15. Includes 10ns read enable time. Maximum propagation delay is 25ns after read assertion.
16. Pulse skew is defined as $|t_{PLH} - t_{PHL}|$ of each channel.

## 2.5 Insulation Specifications

| Parameter | Symbol | Test Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| Creepage Distance (External) | | Per IEC 60601 | 8.03 | 8.3 | - | mm |
| Total Barrier Thickness (Internal) | | | - | 13 | - | µm |
| Barrier Resistance | $R_{IO}$ | 500V | - | $>10^{14}$ | - | Ω |
| Barrier Capacitance | $C_{IO}$ | f = 1MHz | - | 7 | - | pF |
| Leakage Current | | $240V_{RMS}$, 60Hz | - | 0.2 | - | $\mu A_{RMS}$ |
| Comparative Tracking Index | CTI | Per IEC 60112 | ≥600 | - | - | $V_{RMS}$ |
| High Voltage Endurance (Maximum Barrier Voltage for Indefinite Life) | $V_{IO}$ | At maximum operating temperature | 1000 | - | - | $V_{RMS}$ |
| | | | 1500 | - | - | $V_{DC}$ |
| Barrier Life | | 100°C, $1000V_{RMS}$, 60% CL activation energy | - | 44000 | - | Years |

## 2.6 Magnetic Field Immunity

| Parameter (Note 17) | Symbol | Test Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| **$V_{DD1}$ = 5V, $V_{DD2}$ = 3.3V** | | | | | | |
| Power Frequency Magnetic Immunity | $H_{PF}$ | 50Hz/60Hz | - | 3500 | - | A/m |
| Pulse Magnetic Field Immunity | $H_{PM}$ | $t_P$ = 8µs | - | 4500 | - | A/m |
| Damped Oscillatory Magnetic Field | $H_{OSC}$ | 0.1Hz to 1MHz | - | 4500 | - | A/m |
| Cross-Axis Immunity Multiplier (Note 18) | $K_X$ | | - | 2.5 | - | |
| **$V_{DD1}$ = 3.3V, $V_{DD2}$ = 3.3V** | | | | | | |
| Power Frequency Magnetic Immunity | $H_{PF}$ | 50Hz/60Hz | - | 1500 | - | A/m |
| Pulse Magnetic Field Immunity | $H_{PM}$ | $t_P$ = 8µs | - | 2000 | - | A/m |
| Damped Oscillatory Magnetic Field | $H_{OSC}$ | 0.1Hz to1MHz | - | 2000 | - | A/m |
| Cross-Axis Immunity Multiplier (Note 18) | $K_X$ | | - | 2.5 | - | |

Notes:

17. The relevant test and measurement methods are given in "Electromagnetic Compatibility" on page 10.
18. External magnetic field immunity is improved by this factor if the field direction is "end-to-end" rather than "pin-to-pin". See "Electromagnetic Compatibility" on page 10.

# 3. Safety and Approvals

## 3.1 VDE V 0884-11 (Certification Pending)

Basic Isolation; File Number: Certifications pending

- Working voltage ($V_{IORM}$) 600$V_{RMS}$ (848$V_{PK}$); Basic insulation, Pollution degree 2
- Transient overvoltage ($V_{IOTM}$) 4000$V_{PK}$
- Each part tested at 1590$V_{PK}$ for 1s, 5pC partial discharge limit
- Samples tested at 4000$V_{PK}$ for 60s, then 1358$V_{PK}$ for 10s with 5pC partial discharge limit

| Symbol | Safety-Limiting Values | Value | Unit |
|---|---|---|---|
| $T_S$ | Safety Rating Ambient Temperature | 180 | °C |
| $P_S$ | Safety Rating Power (+180°C) | 270 | mW |
| $I_S$ | Supply Current Safety Rating (Total of supplies) | 54 | mA |

## 3.2 UL 1577

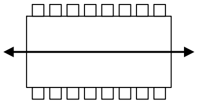
Component Recognition Program File Number: E483309

- Working voltage ($V_{IORM}$) 600$V_{RMS}$ (848$V_{PK}$); basic insulation, Pollution degree 2
- Transient overvoltage ($V_{IOTM}$) 4000$V_{PK}$
- Each part tested at 3000$V_{RMS}$ (4243$V_{PK}$) for 1s
- Each lot of samples tested at 2500$V_{RMS}$ (3536$V_{PK}$) for 60s

# 4. Electromagnetic Compatibility

The ISL32743E is fully compliant with generic EMC standards EN50081, EN50082-1, and the umbrella line-voltage standard for Information Technology Equipment (ITE) EN61000. The isolator’s Wheatstone bridge configuration and differential magnetic field signaling ensure excellent EMC performance against all relevant standards. Compliance tests have been conducted in the following categories:

**Table 2. Compliance Test Categories**

<table>
<tr><th>EN50081-1</th><th>EN50082-2</th><th>EN50204</th></tr>
<tr><td>Residential, Commercial, and Light Industrial:<br>Methods EN55022, EN55014</td><td>Industrial Environment<br>EN61000-4-2 (ESD)<br>EN61000-4-3 (Electromagnetic Field Immunity)<br>EN61000-4-4 (EFT)<br>EN61000-4-6 (RFI Immunity)<br>EN61000-4-8 (Power Frequency Magnetic Field immunity)<br>EN61000-4-9 (Pulsed Magnetic Field)<br>EN61000-4-10 (Damped Oscillatory Magnetic Field)</td><td>Radiated field from digital telephones</td></tr>
<tr><td colspan="2">Immunity to external magnetic fields is even higher if the field direction is “end-to-end” rather than “pin-to-pin” as shown on the right.</td><td></td></tr>
</table>

# 5. Application Information

The ISL32743E is an isolated half-duplex RS-485 transceiver designed for low bus voltage, high-speed data networks.

## 5.1 RS-485 and Isolation

RS-485 is a differential (balanced) data transmission standard for use in long haul networks or noisy environments. It is a true multipoint standard, which allows up to 32 one-unit load devices (any combination of drivers and receivers) on a bus. To allow for multipoint operation, the RS-485 specification requires that drivers must handle bus contention without sustaining any damage.

An important advantage of RS-485 is its wide common-mode range, which specifies that the driver outputs and the receiver inputs withstand signals ranging from +12V to -7V. This common-mode range is the sum of the ground potential difference between driver and receiver, $V_{GPD}$, the driver output common-mode offset, $V_{OC}$, and the longitudinally coupled noise along the bus lines, $V_n$: $V_{CM} = V_{GPD} + V_{OC} + V_n$.

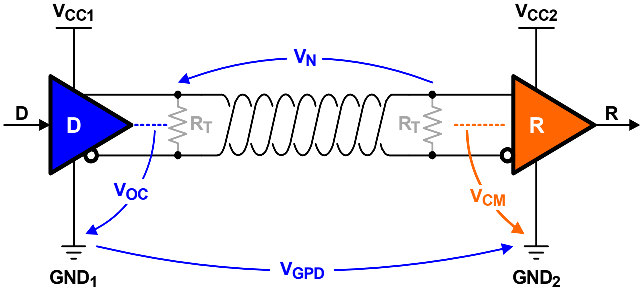


**Figure 3. Common-Mode Voltages in a Non-Isolated Data Link**

However, in networks using isolated transceivers, such as the ISL32743E, the supply and signal paths of the driver and receiver bus circuits are galvanically isolated from their local mains supplies and signal sources.

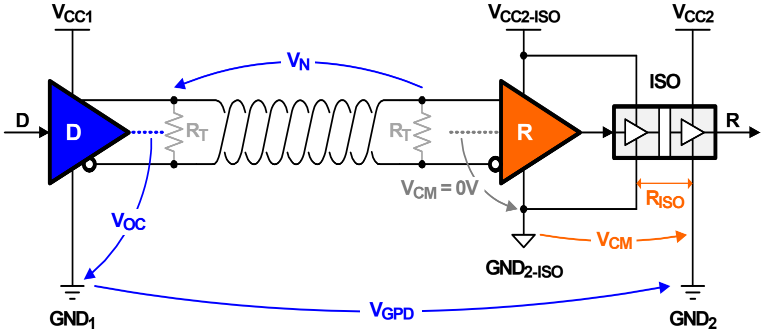


**Figure 4. Common-Mode Voltages in an Isolated Data Link**

Because the ground potentials of isolated bus nodes are isolated from each other, the common-mode voltage of one node's output has no effect on the bus inputs of another node. This is because the common-mode voltage is dropping across the high-resistance isolation barrier of $10^{14}\Omega$. Thus, galvanic isolation extends the maximum allowable common-mode range of a data link to the maximum working voltage of the isolation barrier, which is $600V_{RMS}$ for the ISL32743E.

## 5.2 Digital Isolator Principle

The ISL32743E uses a Giant Magnetoresistance (GMR) isolation. Figure 5 shows the principle operation of a single channel GMR isolator.

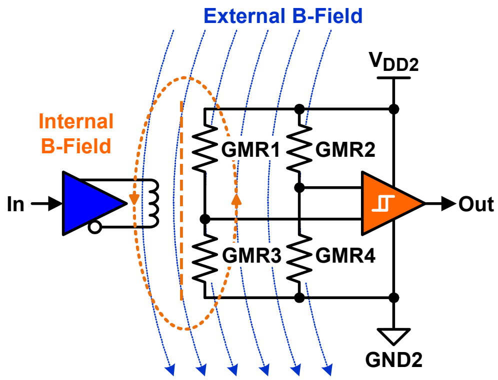


**Figure 5. Single Channel GMR Isolator**

The input signal is buffered and drives a primary coil, which creates a magnetic field that changes the resistance of the GMR resistors 1 to 4. GMR1 to GMR4 form a Wheatstone bridge to create a bridge output voltage that reacts only to magnetic field changes from the primary coil. However, large external magnetic fields are treated as common-mode fields, and are therefore suppressed by the bridge configuration. The bridge output is fed into a comparator with an output signal that is identical in phase and shape to the input signal.

## 5.3 GMR Resistor in Detail

Figure 6 shows a GMR resistor consisting of ferromagnetic alloy layers, B1 and B2, sandwiched around an ultra thin, nonmagnetic conducting middle layer A, typically copper. The GMR structure is designed so that the magnetic moments in B1 and B2 face opposite directions in the absence of a magnetic field, thus causing heavy electron scattering across layer A, which increases its resistance for current C drastically. When a magnetic field D is applied, the magnetic moments in B1 and B2 are aligned and electron scattering is reduced. This lowers the resistance of layer A and increases current C.

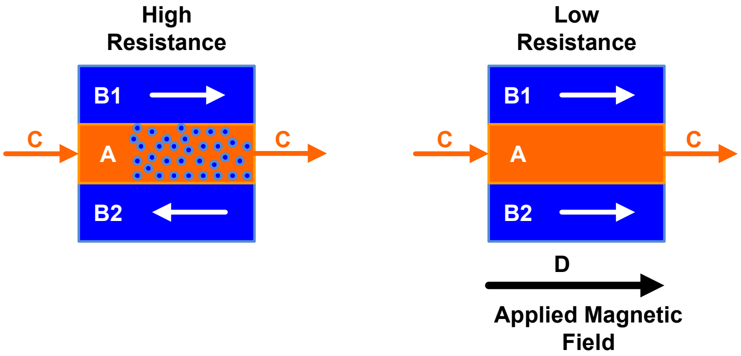


**Figure 6. Multilayer GMR Resistor**

## 5.4 Low Emissions

Because GMR isolators do not use complex encoding schemes, such as RF carriers or high-frequency clocks, and do not include power transfer coils or transformers, their radiated emission spectrum is practically undetectable.

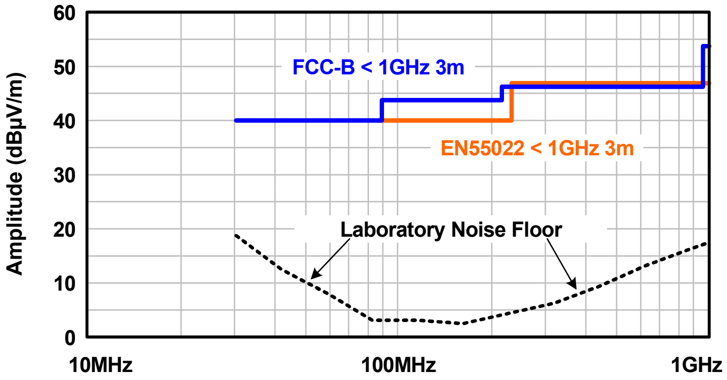


**Figure 7. Undetectable Emissions of GMR Isolators**

## 5.5 Low EMI Susceptibility

Because GMR isolators have no pulse trains or carriers to interfere with, they also have very low EMI susceptibility.

For the list of compliance tests conducted on GMR isolators, refer to "Electromagnetic Compatibility" on page 10.

## 5.6 Receiver (Rx) Features

This transceiver uses a differential input receiver for maximum noise immunity and common-mode rejection. The input sensitivity range is from -50mV to -200mV.

The receiver input resistance is about five times higher than the RS-485 Unit Load (UL) requirement of 12kΩ. The receiver includes a "fail-safe if open or shorted" function that guarantees a high level receiver output if the receiver inputs are unconnected (floating), shorted, or connected to an undriven, terminated bus. The receiver output is tri-statable through the active low $\overline{\text{RE}}$ input.

## 5.7 Driver (Tx) Features

The 3.3V RS-485 driver is a differential output device that delivers at least 1.5V across a 54Ω purely differential load. The driver features low propagation delay skew to maximize bit width and to minimize EMI.

The ISL32743E driver is tri-statable through the active high DE input. The ISL32743E driver outputs are not slew rate limited, so faster output transition times allow data rates of at least 40Mbps.

## 5.8 Built-In Driver Overload Protection

As stated previously, the RS-485 specification requires that drivers survive worst-case bus contentions undamaged. The ISL32743E transmitter meets this requirement through driver output short-circuit current limits and on-chip thermal shutdown circuitry.

The driver output stage incorporates short-circuit current limiting circuitry, which ensures that the output current never exceeds the RS-485 specification. In the event of a major short-circuit condition, the device's thermal shutdown feature disables the driver whenever the die temperature becomes excessive. This eliminates the power dissipation, allowing the die to cool. The driver automatically re-enables after the die temperature drops about 15°C. If the condition persists, the thermal shutdown/re-enable cycle repeats until the fault is cleared. The receiver stays operational during thermal shutdown.

## 5.9 Dynamic Power Consumption

The ISL32743E isolator achieves its low power consumption from the way it transmits data across the barrier. By detecting the edge transitions of the input logic signal and converting these to narrow current pulses, a magnetic field is created around the GMR Wheatstone bridge. Depending on the direction of the magnetic field, the bridge causes the output comparator to switch following the input signal. Because the current pulses are narrow (about 2.5ns), the power consumption is independent of the mark-to-space ratio and depends solely on frequency.

**Table 3. Supply Current Increase with Data Rate**

| Data Rate (Mbps) | $I_{DD1}$ (mA) | $I_{DD2}$ (mA) |
|---|---|---|
| 1 | 0.15 | 0.15 |
| 10 | 1.5 | 1.5 |
| 20 | 3 | 3 |
| 40 | 6 | 6 |

## 5.10 Power Supply Decoupling

Bypass both supplies, $V_{DD1}$ and $V_{DD2}$, with 100nF ceramic capacitors. Place the capacitors as close as possible to the supply pins for proper operation.

## 5.11 DC Correctness

The ISL32743E incorporates a patented refresh circuit to maintain the correct output state with respect to data input. At power-up, the bus outputs follow the truth tables on page 3. Hold the DE input low during power-up to prevent false drive data pulses on the bus.

## 5.12 Data Rate, Cables, and Terminations

RS-485 is intended for network lengths up to 4000 feet, but the maximum system data rate decreases as the transmission length increases. Devices operating at 40Mbps are typically limited to lengths less than 50 feet, but are capable of driving up to 100 feet of cable when allowing for some jitter of 5%.

Twisted pair is the cable of choice for RS-485 networks. Twisted pair cables tend to pick up noise and other electromagnetically induced voltages as common-mode signals, which are effectively rejected by the differential receivers in these ICs.

To minimize reflections, proper termination is imperative when using this high data rate transceiver. In multipoint (multiple driver) networks, terminate the main cable in its characteristic impedance (typically 120Ω for RS-485) at both cable ends. Keep stubs connecting the transceivers to the main cable as short as possible.

A useful guideline for determining the maximum stub lengths is given with Equation 1.

$$L_S \leq \frac{t_r}{10} \times v \times c \qquad \text{(EQ. 1)}$$

where:

- $L_S$ is the stub length (ft)
- $t_r$ is the driver rise time (s)
- c is the speed of light ($9.8 \times 10^8$ ft/s)
- v is the signal velocity as a percentage of c.

To ensure the receiver outputs of all bus transceivers are high when the bus is not actively driven, Renesas recommends fail-safe biasing of the bus lines. Figure 8 on page 15 shows the proper termination of a high-speed data link with fail-safe biasing.

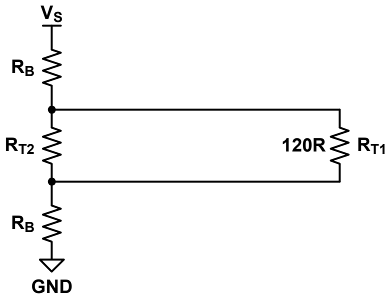


**Figure 8. Failsafe Biasing for a High-speed Data Link**

In this example, the termination resistor value at the cable end without fail-safe biasing matches the characteristic cable impedance: $R_{T1} = Z_0$. The values for $R_B$ and $R_{T2}$ are calculated using Equations 2 and 3.

$$R_B = \frac{V_S/V_{AB} + 1}{0.036} \qquad \text{(EQ. 2)}$$

$$R_{T2} = \frac{R_B \cdot 120\Omega}{R_B - 60\Omega} \qquad \text{(EQ. 3)}$$

where:

- $R_B$ is the value of the biasing resistors
- $R_T$ is the value of the termination resistors
- $V_S$ is the minimum transceiver supply voltage
- $V_{AB}$ is the minimum bus voltage during bus idling
- $Z_0$ is the characteristic cable impedance of 120Ω

## 5.13 Transient Protection

Protecting the ISL32743E against transients exceeding the device's transient immunity requires the addition of an external TVS. For this purpose, Semtech's RClamp0512TQ was chosen due to its high transient protection levels, low junction capacitance, and small form factor.

**Table 4. RClamp0512TQ TVS Features**

| Parameter | | Symbol | Value | Unit |
|---|---|---|---|---|
| ESD (IEC61000-4-2) | Air | $V_{ESD}$ | ±30 | kV |
| | Contact | $V_{ESD}$ | ±30 | kV |
| EFT (IEC61000-4-4) | | $V_{EFT}$ | ±4 | kV |
| Surge (IEC61000-4-5) | | $V_{SURGE}$ | ±1.3 | kV |
| Junction Capacitance | | $C_J$ | 3 | pF |
| Form Factor | | - | 1 x 0.6 | mm |

The TVS is implemented between the bus lines and isolated ground (GND2).

Because transient voltages on the bus lines are referenced to Earth potential, also known as Protective Earth (PE), a high-voltage capacitor ($C_{HV}$) is inserted between GND2 and PE, providing a low-impedance path for high-frequency transients.

Note that the connection from the PE point on the isolated side to the PE point on the non-isolated side (Earth) is usually made using the metal chassis of the equipment, or through a short, thick low inductance wire.

A high-voltage resistor ($R_{HV}$) is added in parallel to $C_{HV}$ to prevent the build-up of static charges on floating grounds (GND2) and cable shields. The bill of materials for the circuit in Figure 9 is listed in Table 5.

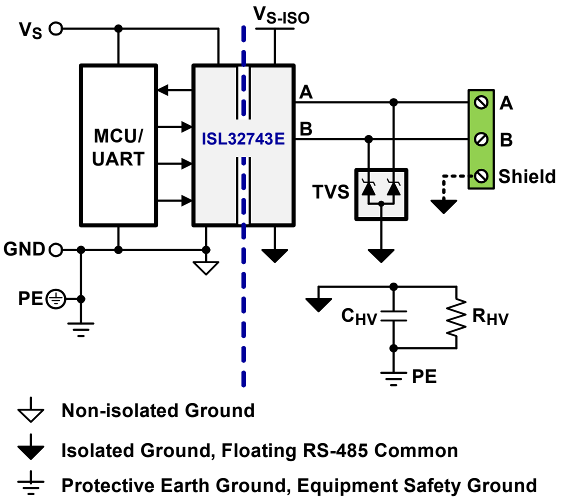


**Figure 9. Transient Protection for the ISL32743E**

**Table 5. BOM for Circuit in Figure 9**

| Name | Function | Order No. | Vendor |
|---|---|---|---|
| TVS | 170W (8, 20µs) 2-LINE PROTECTOR | RCLAMP0512TQ | Semtech |
| $C_{HV}$ | 4.7nF, 2kV, 10% CAPACITOR | 1812B472K202NT | Novacap |
| $R_{HV}$ | 1MΩ, 2kV, 5% RESISTOR | HVC12061M0JT3 | TT-Electronics |

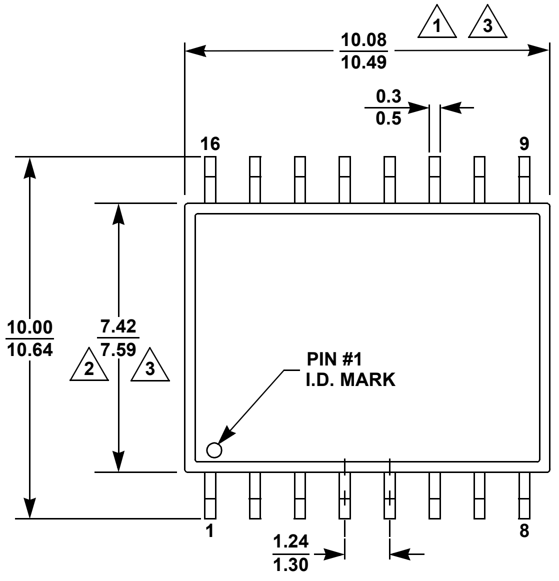
# 6. Revision History

| Rev. | Date | Description |
|---|---|---|
| 1.00 | Jul 9, 2018 | Updated Ordering Information table by adding column for tape and reel and updating Note 1.<br>Corrected the ESD Rating specification cross reference on page 5. |
| 0.00 | Nov 30, 2017 | Initial release. |

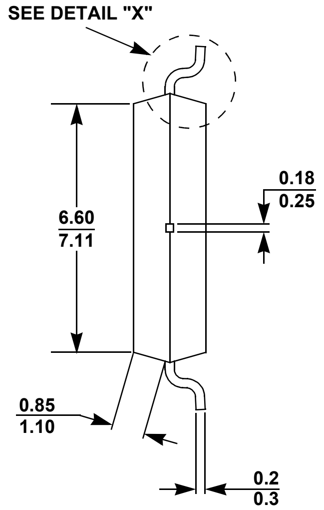
# 7. Package Outline Drawing

For the most recent package outline drawing, see M16.3A.

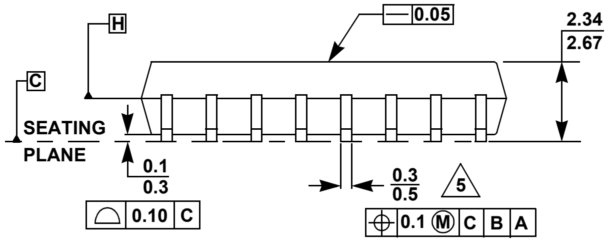
M16.3A
16 LEAD WIDE BODY SMALL OUTLINE PLASTIC PACKAGE (SOICW)
Rev 1, 6/17



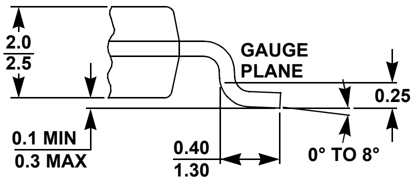
TOP VIEW



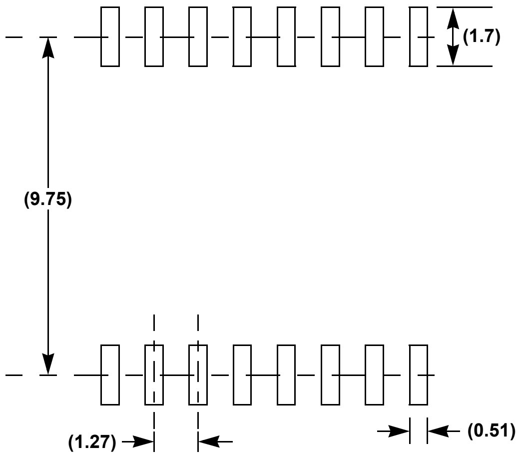
END VIEW



SIDE VIEW



DETAIL X



TYPICAL RECOMMENDED LAND PATTERN

NOTES:

1. Dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 per side.
2. Dimension does not include interlead flash or protrusion. Interlead flash or protrusion shall not exceed 0.25 per side.
3. Dimensions are measured at datum plane H.
4. Dimensioning and tolerancing per ASME Y14.5M-1994.
5. Dimension does not include dambar protrusion.
6. Dimension in ( ) are for reference only.
7. Pin spacing is a BASIC dimension; tolerances do not accumulate.
8. Dimensions are in mm.

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(Rev.4.0-1 November 2017)

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