SOC Dual Channel 400MHz Pin Electronics/DAC/PMU

ISL55161

The ISL55161 is a highly integrated System-on-a-Chip (SOC) pin electronics solution aimed at incorporating every analog function, along with some digital support functionality, required on a per channel basis for Automated Test Equipment. The interface, control and I/O of the chip are all digital; all analog circuitry is inside the chip. Two complete tester channels are integrated into each ISL55161.

The ISL55161 is pin and functionally compatible with Venus4.

Features

- Pin Electronics Driver/Comparator
  - 3-level Driver (DVH/DVL/VTT)
  - 8V Driver Output Swings
  - Extremely Low HiZ Leakage over 16V Range
  - Differential Driver and Comparator Modes
  - 16V Comparator Input Compliance Range
- Load
  - 24mA Imax
  - 16V Input Compliance Range
  - Extremely Low HiZ Leakage over 16V Range
  - Independent Power-down Option
- Deskew
  - Propagation Delay Adjustment
  - Falling Edge Adjustment
- PMU
  - FV, FI, MV, MI
  - FI Voltage Clamps
  - Eight current Ranges (32mA, 8mA, 2mA, 512µA, 128µA, 32µA, 8µA, 2µA)
  - Resistive Load (eight selectable resistor values)
  - Remote Sense Option
- On-chip DC Levels
  - 13 Levels/Channel
  - Gain and Offset Correction/Level
  - DUT Ground Sensing and Correction
- Flexible High Speed Digital Inputs and Outputs
  - Selectable On-chip Terminations for Inputs
  - Read-back Internal States
- Package/Power Dissipation
  - 64-Lead, 10mm x 10mm TQFP with Top Exposed Heat Slug
  - 64-Lead, 9mmx9mm QFN with Top Exposed Heat Slug
  - Pdq ≤ 500mW/Channel @ 11V Operation

Applications

- Automated Test Equipment
- Instrumentation
- ASIC Verifiers

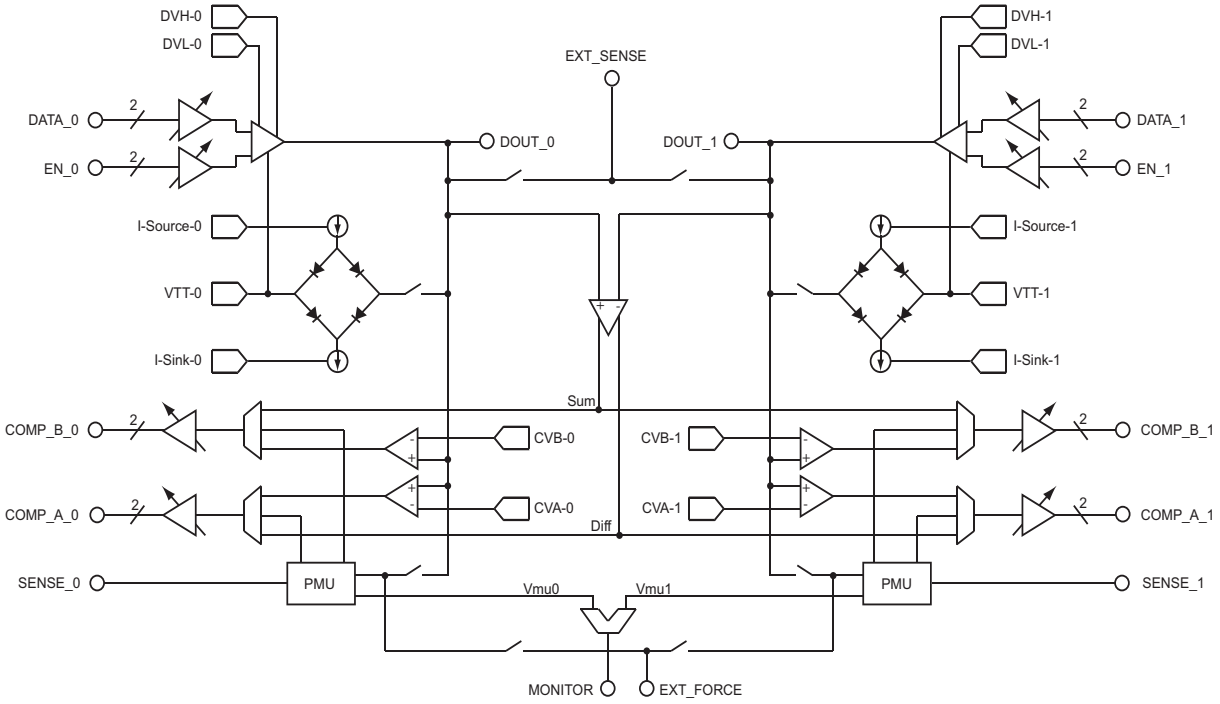

FIGURE 1. BLOCK DIAGRAM

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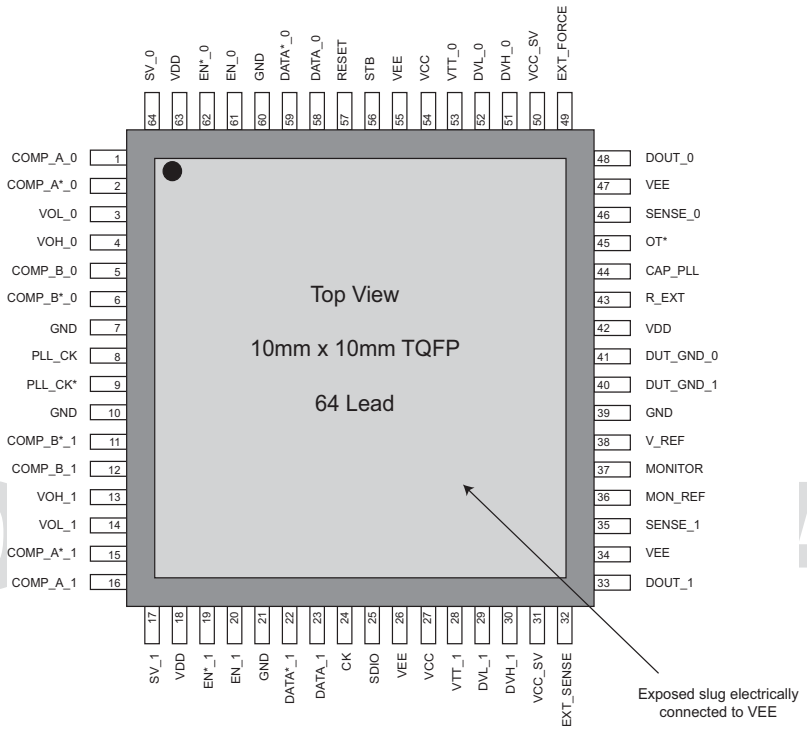
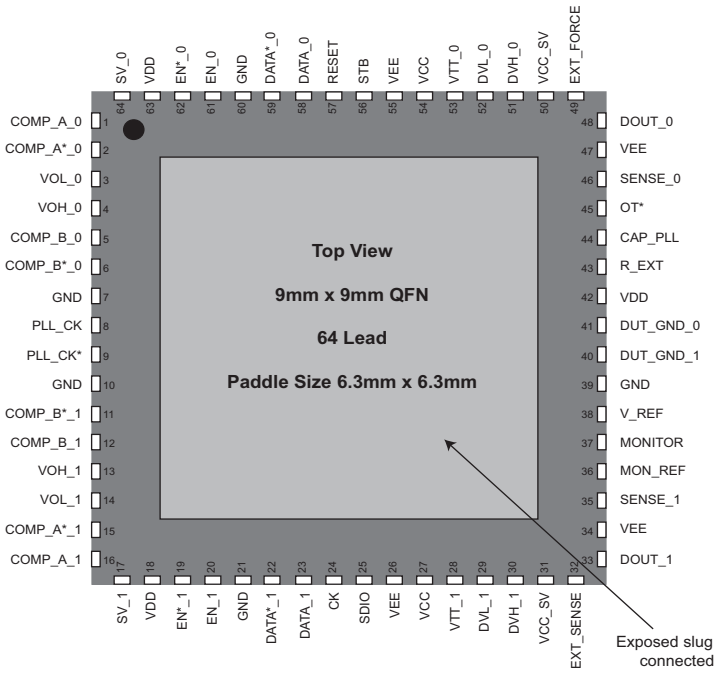
Pin Descriptions

PIN #	PIN NAME	DESCRIPTION
DIGITAL INPUTS		
58, 59	DATA_0, DATA*_0	Channel 0 driver data
61, 62	EN_0, EN*_0	Channel 0 driver enable
64	SV_0	Channel 0 super voltage enable
23, 22	DATA_1, DATA*_1	Channel 1 driver data
20, 19	EN_1, EN*_1	Channel 1 driver enable
17	SV_1	Channel 1 super voltage enable
8, 9	PLL_CK, PLL_CK*	Differential PLL reference signal
DIGITAL OUTPUTS		
1, 2	COMP_A_0, COMP_A*_0	Channel 0, comparator A outputs
5, 6	COMP_B_0, COMP_B*_0	Channel 0, comparator B outputs
16, 15	COMP_A_1, COMP_A*_1	Channel 1, comparator A outputs
12, 11	COMP_B_1, COMP_B*_1	Channel 1, comparator B outputs
DUT PINS		
48, 33	DOUT_0, DOUT_1	Analog I/O pin that connects to Device Under Test
ANALOG PINS		
51, 52, 53	DVH_0, DVL_0, VTT_0	Driver levels for Channel 0
30, 29, 28	DVH_1, DVL_1, VTT_1	Driver levels for Channel 1
38	V_REF	External precision voltage reference
43	R_EXT	External precision resistor
46, 35	SENSE_0, SENSE_1	PMU remote sense input
36	MON_REF	Monitor reference signal
44	CAP_PLL	PLL filter capacitor
45	OT*	Over-temperature open drain digital output
41, 40	DUT_GND_0, DUT_GND_1	Analog voltage input used to track GND at DUT
49, 32	EXT_FORCE, EXT_SENSE	External PMU connection pins
37	MONITOR	Analog voltage output of PPMU
CPU INTERFACE		
24, 25, 56	CK, SDIO, STB	3-bit serial port (Clock, Data, Strobe)
57	RESET	Chip reset
POWER SUPPLIES		
18, 42, 63	VDD	Digital power supply
7, 10, 21, 39, 60	GND	Device ground
27, 54	VCC	Positive analog voltage supply
26, 34, 47, 55	VEE	Negative analog voltage supply
31, 50	VCC_SV	Highest positive analog voltage supply
4, 3	VOH_0, VOL_0	Channel 0 comparator output level supplies
13, 14	VOH_1, VOL_1	Channel 1 comparator output level supplies

Pin Configuration





Absolute Maximum Ratings

Parameter	Min	Typ	Max	Units
Power Supplies				
VCC_SV	VCC		+15	V
VCC	0		+10	V
VEE	–6		0	V
VDD	0		+5	V
VCC_SV – VEE	0		+19	V
VCC – VEE	0		+12	V
VDD – VEE		+8		V
VOH		VCC + 0.5		V
VOL		GND – 0.5		V
Output Voltages				
DOUT	VEE – 0.5		VCC_SV + 0.5	V
SENSE	VEE – 0.5		VCC_SV + 0.5	V
MONITOR	VEE – 0.5		VCC_SV + 0.5	V
$\overline{OT}$*	GND – 0.5		VDD + 0.5	V
Output Currents				
COMP_A, COMP_B	–80		80	mA
SDIO	–20		20	mA
$\overline{OT}$*		20		mA
External References				
R_EXT	8		12	KΩ
V_REF	GND – 0.25V		VCC + 0.25	V
EXT_SENSE	VEE – 0.5		VCC_SV + 0.5	V
EXT_FORCE	VEE – 0.5		VCC_SV + 0.5	V
Thermal Information				
Typical Thermal Resistance θJA (Note 1) - QFN Package		38		°C/W
Typical Thermal Resistance θJA (Note 1) - TQFP Package		39		°C/W
Typical Thermal Resistance θJC (Note 2) - QFN Package		7		°C/W
Typical Thermal Resistance θJC (Note 2) - TQFP Package		1.62		°C/W
Junction Temperature	–55		150	°C

CAUTION: Do not operate at or near the maximum ratings listed for extended periods of time. Exposure to such conditions may adversely impact product reliability and result in failures not covered by warranty.

NOTES:

1. θJA is measured with the component mounted on a high effective thermal conductivity test board in free air.
2. For θJC, the “case temp” location is taken at the package top center.

Recommended Operating Conditions

Parameter	Min	Typ	Max	Units
Power Supplies				
VCC_SV	VCC		+14	V
VCC	+7.75		8.5	V
VEE	–3.5		–2	V
VDD	+3.25		+3.5	V
GND		0		V
VCC_SV – VEE	+10		16.2	V
VCC – VEE	+8		11.5	V
VDD – VEE		<+7.5		V
Comparator Output Supplies				
VOH		<VDD		V
VOL		>GND		V
VOH – VOL	0.4		VDD – GND	V
Digital Inputs (PLL_CK/*; DATA/*; EN/*)				
Differential Input (VIH – VIL)		±250		mV
Common Mode Input ((VIH + VIL)/2)	0.5		+2.5	V
Single-Ended Common Mode Input	0		VDD	V
Driver Levels				
DVH, DVL, VTT	VEE + 1		VCC – 1	V
|DVH – DVL|, |DVH – VTT|, |DVT – VTT|		<8		V
Driver Level Restrictions in HiZ and PMU Mode				
|DOUT – DVH|		<8		V
|DOUT – DVL|		<8		V
|DOUT – VTT|		<8		V
Threshold Levels				
CVA, CVB	VEE + 1		VCC – 1	V
CVA_PPMU, CVB_PPMU	VEE + 1		VCC_SV – 1	V
PPMU FV/MI Range, FI/MV Compliance Range				
No I-Load	VEE + 1.75		VCC – 1.75	V
Maximum I-Load	VEE + 4.75		VCC_SV –4.75	V
FI V-Clamp Levels				
V-Cl-Lo	VEE + 1		VCC_SV – 3	V
V-Cl-Hi	VEE + 3	>1	VCC_SV – 1	V
V-Cl-Hi – V-Cl-Lo		>1		V
Active Load				
I-Source	0		24	mA
I-Sink	–24		0	mA

Recommended Operating Conditions

External Load Capacitance		<1		nF
MONITOR Operating Range	VEE + 1		VCC_SV – 1	V
MONITOR Output Compliance	VEE		VCC_SV	V
External References				
V_REF	+2.99		+3.01	V
R_EXT	9.99		10.01	KΩ
EXT_SENSE	VEE		VCC_SV	V
EXT_FORCE	VEE		VCC-SV	V
Miscellaneous				
Junction Temperature Range	+25		100	°C
CPU Port CK Frequency	10		25	MHz
PLL_CK	100		156.25	MHz
OT*	GND		VDD	V

DC Characteristics

For all of the following DC and Electrical Specifications, compliance to datasheet limits is assured by one or more methods: production test, characterization and/or design.

DC Electrical Specifications – Power Supplies/Junction Temperature

SPEC #	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS	Pd (TYP) 1.5W/Chip
STATIC; MAXIMUM VCC_SV; NO PLL, NO DESKEW							
11420	VCC_SV	VCC_SV = +13.5, VCC = +8.5V,VEE = -3.5V, VDD = +3.5V, Vmid<1:0> = 00, V_REF = 3V, DUT_GND = 0, Q, All deskews not invoked, PMU Comparator Off, PLL Disabled, Bypass Mode	20	34	50	mA	442mW
11120	VCC		15	25	35	mA	200mW
11220	VEE		55	73	95	mA	219mW
11320	VDD		125	200	275	mA	660mW
STATIC; MINIMUM VCC_SV; NO PLL, NO DESKEW							
11430	VCC_SV	VCC_SV = +8.5V, VCC = +8.5V, VEE = -3.5V, VDD = +3.5V, Vmid<1:0> = 00, V_REF = 3V, DUT_GND = 0, Q, All deskews not invoked, PMU Comparator Off, PLL Disabled, Bypass Mode	20	32	50	mA	256mW
11130	VCC		15	25	35	mA	200mW
11230	VEE		55	73	95	mA	219mW
11330	VDD		125	200	275	mA	660mW
STATIC; PLL_CK = 100MHZ							
11450	VCC_SV	VCC_SV = +13.5, VCC = +8.5V,VEE = -3.5V, VDD = +3.5V, Vmid<1:0> = 00, V_REF = 3V, DUT_GND = 0, Q, All deskews not invoked	20	35	50	mA	455mW
11150	VCC		15	25	35	mA	200mW
11250	VEE		55	75	95	mA	225mW
11350	VDD		275	375	475	mA	1,237mW
STATIC; PLL_CK = 156.25MHZ							
11460	VCC_SV	VCC_SV = +13.5, VCC = +8.5V,VEE = -3.5V, VDD = +3.5V, Vmid<1:0> = 00, V_REF = 3V, DUT_GND = 0, Q, All deskews not invoked	20	35	50	mA	455mW
11160	VCC		15	25	35	mA	200mW
11260	VEE		55	75	95	mA	225mW
11360	VDD		320	420	520	mA	1,386mW
DYNAMIC - RING OSCILLATOR CONFIGURATION; PLL_CK = 100MHZ							
12450	VCC_SV	VCC_SV = +13.5, VCC = +8.5V,VEE = -3.5V, VDD = +3.5V, Vmid<1:0> = 00, V_REF = 3V, DUT_GND = 0, Channels 0 and 1 configured as ring oscillators, All deskews invoked	20	35	50	mA	455mW
12150	VCC		35	50	65	mA	400mW
12250	VEE		65	86	110	mA	284mW
12350	VDD		275	385	500	mA	1,270mW
DYNAMIC - RING OSCILLATOR CONFIGURATION; PLL_CK = 156.25MHZ							
12460	VCC_SV	VCC_SV = +13.5, VCC = +8.5V,VEE = -3.5V, VDD = +3.5V, Vmid<1:0> = 00, V_REF = 3V, DUT_GND = 0, Channels 0 and 1 configured as ring oscillators, All deskews invoked	20	35	50	mA	455mW
12160	VCC		40	53	70	mA	424mW
12260	VEE		65	88	110	mA	264mW
12360	VDD		325	435	550	mA	1,435mW

DC Electrical Specifications – CPU Port

VCC_SV = +13V, VCC = +8V, VEE = -3V, VDD = +3.3V, Vmid<1:0> = 00, V_REF = 3.00V, DUT_GND = 0

SPEC #	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
SDIO, CK, STB, RESET						
17100	VIH		2.0			V
17110	VIL				0.8	V
17120	Input Leakage Current		-100	0	+100	nA
17200	VOH (SDIO only)	Output Current = 8mA	2.4			V
17210	VOL (SDIO Only)	Input Current = 8mA			0.4	V

DC Electrical Specifications – Analog Pins

SPEC #	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
10999	V_REF Input Current	Note 1	-100	0	+100	nA
10998	DUT_GND Input Current	Note 1; Tested at 0V	-20	0	+20	nA
10997	EXT_FORCE, EXT_SENSE HiZ Leakage	Note 1; Tested at 0V, Tested at VCC_SV and VEE	-20	0	+20	nA
10992	SENSE Input Leakage	Note 1; Tested at 0V	-5	0	+5	nA
10991	SENSE Input Leakage	Note 1; Tested at VCC_SV and VEE	-15	0	+15	nA
	Capacitance on EXT_FORCE	Limits established by characterization and are not production tested. All other switches open		25		pF
	Capacitance on EXT_SENSE	Limits established by characterization and are not production tested. All other switches open		8		pF

NOTE:

1. VCC_SV = +13V, VCC = +8V, VEE = -3V, VDD = +3.3V, Vmid<1:0> = 00, V_REF = 3V, DUT_GND = 0.

DC Electrical Specifications – Thermal Monitor and Alarm

VCC_SV = +13V, VCC = +8V, VEE = -3V, VDD = +3.3V, Vmid<1:0> = 00, V_REF = 3.00V, DUT_GND = 0

	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
$\overline{OT}$*						
10995	Over-Temperature Threshold		120	135	150	°C
10994	$\overline{OT}$* VOH (HiZ Leakage)	Tested at 0V and VDD	-100	0	+100	nA
10993	VOL	Input current = 5mA			0.4	V

DC Electrical Specifications – PLL

VCC_SV = +13V, VCC = +8V, VEE = -3V, VDD = +3.3V, Vmid<1:0> = 00, V_REF = 3.00V, DUT_GND = 0; PLL_CK = 100MHz

	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
18100	Input Leakage Current	PLL-Z1 = 0; PLL-ZB = 0	–100	0	+100	nA
18110	$\overline{\text{Differential Input Resistance}}$	PLL-ZA = 1; PLL-ZB = 0 or PLL-ZA = 0; PLL-ZB = 1		105		Ω

DC Electrical Specifications – DAC Calibration

All DC tests are performed after the DAC is first calibrated. The upper 5 bits of the DAC are calibrated in the sequence D11 to D15. The DAC Cal bits are adjusted to make the major carries as small as possible.

VCC_SV = +12.75V, VCC = +7.75V, VEE = -2.75V, VDD = +3.25V, Vmid<1:0> = 00, V_REF = 3.00V, DUT_GND = 0

SPEC #	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
16510	D15 Step Error	(DAC @ 8000 - DAC @ 7FFF)/(8000 – 7FFF) – DAC LSB; VR1, Code 8000 – Code 7FFF – LSB; VR1	-5		+5	mV
16520	D14 Step Error	(DAC @ 7000 - DAC @ 3000)/(7000 – 3000) – DAC LSB; VR1, Code 4000 – Code 3FFF – LSB; VR1	-5		+5	mV
16530	D13 Step Error	(DAC @ 7000 - DAC @ 5000)/(7000 – 5000) – DAC LSB; VR1, Code 6000 – Code 5FFF – LSB; VR1	-5		+5	mV
16540	D12 Step Error	(DAC @ 7000 - DAC @ 6000)/(7000 – 6000) – DAC LSB; VR1, Code 7000 – Code 6FFF – LSB; VR1	-5		+5	mV
16550	D11 Step Error	(DAC @ 7800 - DAC @ 7000)/(7800 – 7000) – DAC LSB; VR1, Code 7800 – Code 77FF – LSB; VR1	-5		+5	mV

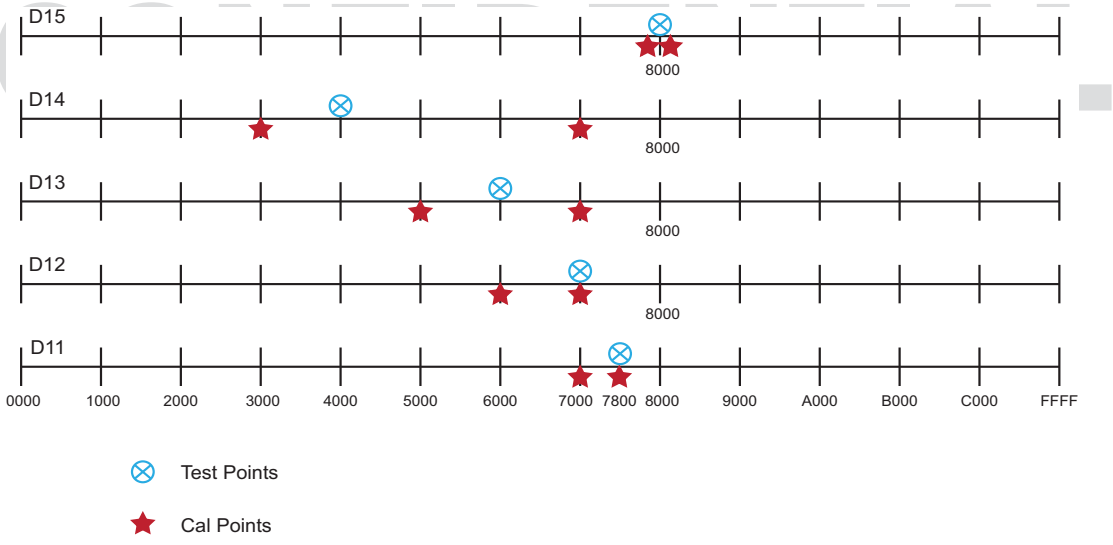


FIGURE 1.

DC Electrical Specifications – DAC

There are three on-chip internal DACs used for: (1) DC Level, (2) DC Level Offset Correction, and (3) DC Level Gain Correction.

These on-chip DACs are not used off chip explicitly as standalone outputs. Rather, they are internal resources that are used by every functional block. The DACs are tested many times over by the DC tests for driver, comparator, and PMU. However, the DACs are specifically tested independently from all other functional blocks to verify basic functionality.

Unless otherwise specified, VCC_SV = +12.75, VCC = +7.75V, VEE = -2.75V, VDD = +3.25V, Vmid<1:0> = 00, V_REF = 3V, DUT_GND = 0

SPEC #	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
LEVEL DAC TEST						
16100	Span	Offset and Gain DACs both programmed to mid scale (Code 7FFF), Span = DAC(FFFF) – DAC(0000) (Note 2)	7.5	8.0	8.5	V
16110	Linearity Error	Offset and Gain DACs both programmed to mid scale (Code 7FFF) (Notes 2, 3	-4	0	+4	mV
16120	Bit Test Error	Offset and Gain DACs both programmed to mid scale (Code 7FFF) (Note 2)	-4	0	+4	mV
	DAC VDD DC PSRR Error	VCC_SV = +13V, VCC = +8V, VEE = -3V, VDD = +3.3V, Vmid<1:0> = 00, V_REF = 3V, DUT_GND = 0, Limits established by characterization and are not production tested. (Note 2)		1		mV/V
16190	Droop Test	Note 3			600	µV/ms
16400	DAC Noise Test	FV = 0V, VR2, Measured at DOUT_0, RMS Value			1	mV
OFFSET DAC TEST						
16200	+ Adjustment Range	Level and Gain DACs both programmed to mid scale (Code 7FFF), Code 0000, FFFF relative to mid scale (8000) (Note 2)	+4.5	+5.2	+6.0	% of Span
16210	- Adjustment Range	Level and Gain DACs both programmed to mid scale (Code 7FFF), Code 0000, FFFF relative to mid scale (8000) (Note 2)	-4.5	-5.2	-6.0	% of Span
16220	Linearity Error	Level and Gain DACs both programmed to mid scale (Code 7FFF), (Notes 2, 3)	-4	0	+4	mV
16230	Bit Test Error	Level and Gain DACs both programmed to mid scale (Code 7FFF) (Note 2)	-4	0	+4	mV
GAIN DAC TEST						
16300	+ Adjustment Range	(Notes 2, 5)	1.07	1.10	1.15	V/V
16310	- Adjustment Range	(Notes 2, 5)	0.850	0.886	0.922	V/V
16320	Linearity Error	(Notes 2, 3, 5)	–3	0	+3	mV/V
16330	Bit Test Error	(Notes 2, 5)	–3	0	+3	mV/V

NOTES:

2. DAC tests performed using the PMU in FV mode and the MONITOR output, Channel 0, VR1.
3. Linearity Test - 17 equal spaced codes relative to a straight line determined by 3/17 and 15/17 measurement points: 0000, 0FFF, **1FFF**, 2FFF, 3FFF....CFFF, **DFFF**, EFFF, FFFF.
4. CPU CK turned off. 66 ms delay between measurements. All DC levels tested one at a time.
5. Level DAC programmed to FFFF and Offset DAC programmed to mid scale (Code 7FFF).

DC Electrical Specifications – Vmid DAC

VCC_SV = +12.75, VCC = +7.75V, VEE = -2.75V, VDD = +3.25V, Vmid<1:0> = 00, V_REF = 3V, DUT_GND = 0; DAC tests performed in FV mode tested and at the MONITOR.

SPEC #	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
V_{MID} SHIFT IN VR0 (NOTE 6)						
16400	Code 01 vs. Code 00	CODE1, Note 6	+0.2	+0.25	+0.3	V
16401	Code 10 vs. Code 00	CODE2, Note 6	-0.3	-0.25	-0.2	V
16402	Code 11 vs. Code 00	CODE3, Note 6	-0.55	-0.5	-0.45	V
V_{MID} SHIFT IN VR1 (NOTE 7)						
16410	Code 01 vs. Code 00	CODE1, Note 7	+0.4	+0.5	+0.6	V
16411	Code 10 vs. Code 00	CODE2, Note 7	-0.6	-0.5	-0.4	V
16412	Code 11 vs. Code 00	CODE3, Note 7	-1.1	-1.0	-0.9	V
V_{MID} SHIFT IN VR2 (NOTE 8)						
16420	Code 01 vs. Code 00	CODE1, Note 8	+0.8	+1.0	+1.2	V
16421	Code 10 vs. Code 00	CODE2, Note 8	-1.2	-1.0	-0.8	V
16422	Code 11 vs. Code 00	CODE3, Note 8	-2.2	-2.0	-1.8	V

NOTES:

6. VR0, Tested with DAC programmed to -0.5V and +3.5V with Vmid<1:0> = 00 as reference voltage.
7. VR1, Tested with DAC programmed to -1V and +7V with Vmid<1:0> = 00 as reference voltage.
8. VR2, Tested with DAC programmed to 0V and +10V with Vmid<1:0> = 00 as reference voltage.

DC Electrical Specifications – Driver

Unless otherwise specified, VCC_SV = +13V, VCC = +8V, VEE = -3V, VDD = +3.3V, Vmid<1:0> = 00, V_REF = 3V, DUT_GND = 0

SPEC #	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
13300	HiZ Leakage	Tested @ DOUT = 0V	-5		+5	nA
13310		Tested @ DOUT = VCC_SV – 1V, VEE + 1V	-15		+15	nA
RANGE 0						
13100	DVH, DVL, VTT Post Cal Error	VCC_SV = +12.75, VCC = +7.75V, VEE = -2.75V, VDD = +3.25V, Vmid<1:0> = 00, V_REF = 3V, DUT_GND = 0, VR0, TP 0 (see Table 1)	-10		+10	mV
RANGE 1						
13120	DVH, DVL, VTT Post Cal Error	VCC_SV = +12.75, VCC = +7.75V, VEE = -2.75V, VDD = +3.25V, Vmid<1:0> = 00, V_REF = 3V, DUT_GND = 0, VR1, TP 1 (see Table 1)	-15		+15	mV
RANGE 2						
13140	DVH, DVL, VTT Post Cal Error	VCC_SV = +12.75, VCC = +7.75V, VEE = -2.75V, VDD = +3.25V, Vmid<1:0> = 00, V_REF = 3V, DUT_GND = 0, VR2, TP 2 (see Table 1)	-25		+25	mV
	Driver Temperature Coefficient	Limits established by characterization and are not production tested. VR1 (see Table 1)		< ±200		µV/C
	Driver VCC DC PSRR Error			1		mV/V
	Driver VEE DC PSRR Error			1		mV/V
DRIVER OUTPUT IMPEDANCE						
13320	DVH, DVL, VTT Nominal Output Impedance	Rout adjust programmed to the nominal value; Note 12		50		Ω
13322	DVH, DVL Minimum Rout Adjust Output Impedance	Rout adjust programmed to the minimum value; Note 12			45	Ω

DC Electrical Specifications – Driver

Unless otherwise specified, VCC_SV = +13V, VCC = +8V, VEE = -3V, VDD = +3.3V, Vmid<1:0> = 00, V_REF = 3V, DUT_GND = 0 **(Continued)**

SPEC #	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
13323	DVH, DVL Maximum Rout Adjust Output Impedance	Rout adjust programmed to the maximum value; Note 12	50			Ω
13324	VTT Minimum Rout Adjust Output Impedance	Rout adjust programmed to the minimum value; Note 12			45	Ω
13325	VTT Maximum Rout Adjust Output Impedance	Rout adjust programmed to the maximum value; Note 12	50			Ω
DRIVER OUTPUT CURRENT						
13321	DC Output Current	VCC_SV = +12.75, VCC = +7.75V, VEE = -2.75V, VDD = +3.25V, Vmid<1:0> = 00, V_REF = 3V, DUT_GND = 0	± 35			mA
	AC Output Current	Limits established by characterization and are not production tested.	± 70			mA
DIFFERENTIAL INPUTS DATA & EN						
13200	Input Leakage Current	(Note 9)	-100	0	+100	nA
12280	Differential Input Resistance	(Note 10 or 11)		105		

NOTES:

9. Data0(1)-ZA = 0; Data0(1)-ZB = 0; En0(1)-ZA = 0; En0(1)-ZB = 0.
10. Data0(1)-ZA = 1; Data0(1)-ZB = 0; En0(1)-ZA = 1; En0(1)-ZB = 0.
11. Data0(1)-ZA = 0; Data0(1)-ZB = 1; En0(1)-ZA = 0; En0(1)-ZB = 1.
12. DVH = 3.0V; 19.2mA sourced @ DOUT; VTT = 1.5V, 19.2mA sink @ DOUT, DVL = 0V, 19.2mA sink @ DOUT.

TABLE 1. DRIVER TEST AND CAL POINTS

VOLTAGE RANGE	CAL POINTS	TEST POINTS (TP #)
VR0	0V, +3V	-0.5V, +1.5V, +3.5V
VR1	0V, +5V	-1V, +3V, +7V
VR2	0V, +5V	-2V, +3V, +7V

DC Electrical Specifications – Comparator Thresholds

The window comparator thresholds are tested using a binary search algorithm at the digital outputs COMP_A and COMP_B.

Unless otherwise specified, VCC_SV = +12.75, VCC = +7.75V, VEE = -2.75V, VDD = +3.25V, Vmid<1:0> = 00, V_REF = 3V, DUT_GND = 0

SPEC #	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
14500	Post Calibration Threshold Error, VR0	Voltage Range 0, (see Table 2) (Note 13)	-10		+10	mV
14510	Post Calibration Threshold Error, VR1	Voltage Range 1, (see Table 2) (Note 14)	-15		+15	mV
14520	Post Calibration Threshold Error, VR2	Voltage Range 2, (see Table 2) (Note 15)	-25		+25	mV
	Threshold Temperature Coefficient	VCC_SV = +13V, VCC = +8V, VEE = -3V, VDD = +3.3V, Vmid<1:0> = 00, V_REF = 3V, DUT_GND = 0; Limits established by characterization and are not production tested, Voltage Range 1 (see Table 2)		< ±200		µV/C
	VCC_SV DC PSRR Error			1		mV/V
	VEE DC PSRR Error			1.5		mV/V
13360	Comparator Output Impedance	VCC_SV = +13V, VCC = +8V, VEE = -3V, VDD = +3.3V, Vmid<1:0> = 00, V_REF = 3V, DUT_GND = 0, Sourcing 20mA, Sinking 20mA		50		Ω
	DOUT Input Capacitance	Limits established by characterization only and are not production tested.		4		pF
DIFFERENTIAL COMPARATOR DIFFERENCE MODE						
14570	Post Calibration DC Error	Diff Mode (see Table 3), Voltage Range 2 (see Table 2)	-25	0	+25	mV
COMMON MODE						
14580	Post Calibration DC Error	CM Mode (see Table 3), Voltage Range 2 (see Table 2)	-25	0	+25	mV

NOTES:

13. Comparator threshold test points, VR0, Test the comparator outputs using a binary search.
14. Comparator threshold test points, VR1, Test the internal references via Test & Cal Mux.
15. Comparator threshold test points, VR2, Test the comparator outputs using a binary search.

TABLE 2. SINGLE-ENDED COMPARATOR THRESHOLD CAL AND TEST POINTS

V RANGE	CAL POINTS	TEST POINTS
VR0	0V +3V	-0.5V +1.5V +3.5V
VR1	0V +5V	-1V +3V +6.5V
VR2	0V +6V	-1V +5V +6.5V

TABLE 3. DIFFERENTIAL COMPARATOR CAL AND TEST POINTS

MODE	CAL POINTS	TEST POINTS
Diff Mode	VCM = 0.5V Vdiff = ±1.0V	VCM = 0V, 1V Vdiff = ±0V, 1V, 2V
Common Mode	VCM = +1V/+4V Vdiff = 0V	VCM = 0V, 3V, 5V Vdiff = 0V

DC Electrical Specifications – Load

Unless otherwise specified, VCC_SV = +12.75, VCC = +7.75V, VEE = -2.75V, VDD = +3.25V, Vmid<1:0> = 00, V_REF = 3V, DUT_GND = 0

SPEC #	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
14900	Source/Sink Post Cal Error	Post calibration, VTT = +3V, DOUT = +0V, +6V/VTT = +3V, DOUT = +6V. FS = 32mA. Test points less than 3.2mA first set to 3.2mA then set to test point value to ensure active load circuit is initialized.	-1		+1	% FS
V_{COM}						
15100	Post Cal Error, VR0	Post calibration. ISINK & ISRC set to 3.2mA.	-10		+10	mV
15200	Post Cal Error, VR1		-15		+15	mV
15300	Post Cal Error, VR2		-25		+25	mV
	Source Temperature Coefficient	VCC_SV = +13V, VCC = +8V, VEE = -3V, VDD = +3.3V, Vmid<1:0> = 00, V_REF = 3V, DUT_GND = 0, Characterized only. Not production		2		µA/°C
	Sink Temperature Coefficient			8		µA/°C
	Vcom Temperature Coefficient	Post calibration, Characterized only. Not production tested.		< ±200		µV/°C
SOURCE CURRENT ADJUST						
14960	Code 1	Post calibration; VTT = +3V, DOUT = 0V; I-Source<15:0> = C000 (+24mA).	0.85 • Nominal	0.9 • Nominal	0.95 • Nominal	mA
14960	Code 2		1.05 • Nominal	1.1 • Nominal	1.15 • Nominal	mA
14960	Code 5		0.75 • Nominal	0.8 • Nominal	0.85 • Nominal	mA
14960	Code 6		1.15 • Nominal	1.2 • Nominal	1.25 • Nominal	mA
SINK CURRENT ADJUST						
14965	Code 1	Post calibration, VTT = +3V, DOUT = +6V; I-Sink<15:0> = C000 (-24mA)	0.85 • Nominal	0.9 • Nominal	0.95 • Nominal	mA
14965	Code 2		1.05 • Nominal	1.1 • Nominal	1.15 • Nominal	mA
14965	Code 5		0.75 • Nominal	0.8 • Nominal	0.85 • Nominal	mA
14965	Code 6		1.15 • Nominal	1.2 • Nominal	1.25 • Nominal	mA

TABLE 4. V_{COM} FOR LOAD

V RANGE	CAL POINTS	TEST POINTS
VR0	0V +3V	-0.5V +1.5V +3.5V
VR1	0V +5V	-1V +3V +6V
VR2	0V +5V	-1V +3V +6V

TABLE 5. LOAD SOURCE AND SINK

CAL POINTS	TEST POINTS
4.8mA 19.2mA	0mA to 1.6mA in 80µA steps 6mA 12mA 18mA 24mA

DC Electrical Specifications – PPMU-FV

The sequence of events performed for Force Voltage (FV) testing is:

1. Program FV
2. Force current at DOUT_# using tester PMU
3. Measure the voltage at DOUT_#.

FV tests:

1. VR0 tested in IR5 (no load)
2. VR1 tested in IR5 (no load)
3. VR2 tested in IR6 and IR7 (no load)
4. VR2 tested in IR0 – IR7 (at maximum load).

Unless otherwise specified, VCC_SV = +12.75, VCC = +7.75V, VEE = -2.75V, VDD = +3.25V, Vmid<1:0> = 00, V_REF = 3V, DUT_GND = 0

SPEC #	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
14250	Output Force Error, VR0, IR0-IR7	FV VR0 Test Points (see Table 6)	-10		+10	mV
14252	Output Force Error, VR1, IR0-IR7	FV VR1 Test Points (see Table 6)	-15		+15	mV
14265	Output Force Error, VR2, IR0-IR7	FV VR2 Test Points (see Table 6)	-25		+25	mV
	FV Temperature Coefficient	VCC_SV = +13V, VCC = +8V, VEE = -3V, VDD = +3.3V, Vmid<1:0> = 00, V_REF = 3V, DUT_GND = 0, Limits established by characterization and are not production tested. VR2 (see Table 6)		< ±200		µV/°C
	VCC_SV SC PSRR Error			1		mV/V
	VEE SC PSRR Error			1		mV/V

TABLE 6. FV

RANGE	CAL POINTS	FV TEST POINTS
VR0 IR5	0V/0µA +3V/0µA	-0.5V/0µA +1.5V/0µA +3.5V/0µA
VR1 IR5	0V/0µA +5V/0µA	-1V/0µA +3V/0µA +7V/0µA
VR2 IR6 & IR7 only	0V/0µA +10V/0µA	-1V/0µA +6V/0µA +11V/0µA
VR2 IR0 – IR7	0V/0µA +10V/0µA	+2V/-Imax +8V/+Imax

DC Electrical Specifications – Measure Current

MI tested in VR2, IR0 – IR7. MI tested post 2-point software calibration.

Unless otherwise specified, VCC_SV = +12.75, VCC = +7.75V, VEE = -2.75V, VDD = +3.25V, Vmid<1:0> = 00, V_REF = 3V, DUT_GND = 0

SPEC #	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
MI (POST CALIBRATION)						
14100	Measure Current Error, IR0	MI Test Points (see Table 7), 4-point software CMRR calibration	-10		+10	nA
14110	Measure Current Error, IR1		-40		+40	nA
14120	Measure Current Error, IR2		-160		+160	nA
14130	Measure Current Error, IR3		-640		+640	nA
14140	Measure Current Error, IR4		-2.56		+2.56	µA
14150	Measure Current Error, IR5		-10		+10	µA
14160	Measure Current Error, IR6		-40		+40	µA
14170	Measure Current Error, IR7		-160		+160	µA
	MI Temperature Coefficient	VCC_SV = +13V, VCC = +8V, VEE = -3V, VDD = +3.3V, Vmid<1:0> = 00, V_REF = 3V, DUT_GND = 0, Limits established by characterization and are not production tested. IR0 – IR7 (see Table 7)		0.01		% Imax/°C
	MI VCC_SV DC PSRR Error			0.015		% Imax/V
	MI VEE DC PSRR			0.05		% Imax/V

TABLE 7. MI

RANGE	CAL POINTS	MI TEST POINTS
IR0 – IR7	+5V/+0.8 • Imax +5V/-0.8 • Imax	-1V/0µA +11V/0µA +2V/-Imax +8V/+Imax

FV/MI Transfer Characteristic, IR0-IR7

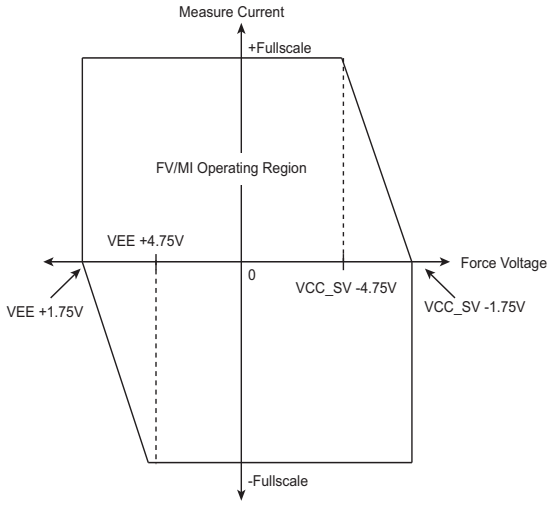


FIGURE 2. MEASURE CURRENT

DC Electrical Specifications – Force Current

The sequence of events performed for FI Testing is:

1. Program FI to the desired current
2. Force voltage with external PMU at DOUT_#
3. Measure the current at DOUT_#.

FI is tested in all eight current ranges.

SPEC #	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
POST CALIBRATION FI ERROR						
14101	Force Current Error, IR0	VCC_SV = +12.75, VCC = +7.75V, VEE = -2.75V, VDD = +3.25V, Vmid<1:0> = 00, V_REF = 3V, DUT_GND = 0 FI Test Point, Post CMRR calibration for FI	-10		+10	nA
14111	Force Current Error, IR1		-40		+40	nA
14121	Force Current Error, IR2		-160		+160	nA
14131	Force Current Error, IR3		-640		+640	nA
14141	Force Current Error, IR4		-2.56		+2.56	µA
14151	Force Current Error, IR5		-10		+10	µA
14161	Force Current Error, IR6		-40		+40	µA
14171	Force Current Error, IR7		-160		+160	µA
	FI Temperature Coefficient	VCC_SV = +13V, VCC = +8V, VEE = -3V, VDD = +3.3V, Vmid<1:0> = 00, V_REF = 3V, DUT_GND = 0, Limits established by characterization and are not production tested. IR0 – IR7 (see Table 8)		0.01		% Imax/°C
	VCC_SV DC PSRR Error			0.05		% Imax/V
	VEE DC PSRR Error			0.1		% Imax/V
COARSE GAIN ADJUST						
14158	Code 10, ±Imax	VCC_SV = +13V, VCC = +8V, VEE = -3V, VDD = +3.3V, Vmid<1:0> = 00, V_REF = 3V, DUT_GND = 0, IR5 (see Table 7)	-9.6	-8	-6.7	% • Imax
14159	Code 11, ±Imax		6.7	+8	9.6	% • Imax
14203	Uncalibrated CMRR Error	VCC_SV = +13V, VCC = +8V, VEE = -3V, VDD = +3.3V, Vmid<1:0> = 00, V_REF = 3V, DUT_GND = 0 (Note 16)	-0.2		+0.2	% Imax/V

NOTE:

16. FV Mode, VR2, Iout = 0 (PMU Switch Open), IR7, FORCE = +2V, +8V, Tight Loop.

TABLE 8.

FI TESTING	CAL POINTS	FI TEST POINTS
IR0 – IR7	+5V/+0.8 • Imax +5V/-0.8 • Imax	-1V/0 +11V/0 +2V/-Imax +8V/+Imax

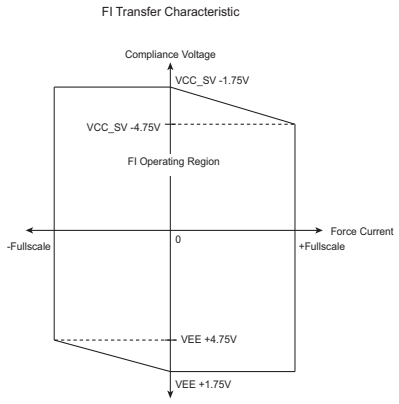


FIGURE 3. FORCE CURRENT

DC Electrical Specifications – Measure Voltage (Monitor)

The sequence of events for testing the MONITOR is:

1. Program FV to the desired voltage (In VR2, IR5, Iload = 0)
2. Measure the voltage at DOUT_0.
3. Measure the voltage at MONITOR, relative to MON_REF.
4. Calculate the difference to determine the error.
5. MONITOR is tested post 2 point software calibration.

Unless otherwise specified, VCC_SV = +12.75, VCC = +7.75V, VEE = -2.75V, VDD = +3.25V, Vmid<1:0> = 00, V_REF = 3V, DUT_GND = 0

SPEC #	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
MONITOR, MON_REF						
14710	HiZ Leakage Current	VCC_SV = +13V, VCC = +8V, VEE = -3V, VDD = +3.3V, Vmid<1:0> = 00, V_REF = 3V, DUT_GND = 0, Tested at MONITOR = 0V, VCC_SV, VEE	-20	0	+20	nA
14700	MONITOR Output Impedance	Tested at +5V, Iout = 0µA, 2mA		0.6	1.0	kΩ
14701	MON_REF Output Impedance			14	17	kΩ
	MV Temperature Coefficient	VCC_SV = +13V, VCC = +8V, VEE = -3V, VDD = +3.3V, Vmid<1:0> = 00, V_REF = 3V, DUT_GND = 0, Characterized only. Not production tested		< 25		µV/°C
	MV VCC_SV/VEE DC PSRR			< 25		µV/V
14720	MV Error	Monitor Test Points (see Table 9)	-5		+5	mV
14741	DUT_GND, GND_REF Error	(Note 17)	-5		+5	mV

NOTE:

17. DUT_Gnd = ±300 mV, FV Mode, V-FV = +3V, measured at Test & Cal relative to GND.

TABLE 9.

MV TESTING	MV CAL POINTS	MV TEST POINTS
IR5	0V/0µA +10V/0µA	-1V/0µA +5V/0µA +11V/0µA

DC Electrical Specifications – PPMU Comparator Thresholds

Unless otherwise specified, VCC_SV = +12.75, VCC = +7.75V, VEE = -2.75V, VDD = +3.25V, Vmid<1:0> = 00, V_REF = 3V, DUT_GND = 0

SPEC #	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
14600	Threshold Error, VR0	VR0 (see Table 10) (Note 18)	-10		+10	mV
14620	Threshold Error, VR1	VR1 (see Table 10) (Note 19)	-15		+15	mV
14640	Threshold Error, VR2	VR2 (see Table 10) (Note 20)	-25		+25	mV
14660	Threshold Error, VIR	VIR (see Table 10) (Note 21)	-8		+8	mV
	VCC_SV DC PSRR Error	VCC_SV = +13V, VCC = +8V, VEE = -3V, VDD = +3.3V, Vmid<1:0> = 00, V_REF = 3V, DUT_GND = 0, Characterized only. Not production tested		1		mV/V
	VEE DC PSRR Error			1.5		mV/V
	Threshold Temperature Coefficient	VCC_SV = +13V, VCC = +8V, VEE = -3V, VDD = +3.3V, Vmid<1:0> = 00, V_REF = 3V, DUT_GND = 0, Characterized only. Not production tested, VR1 (see Table 10)		< ±200		µV/°C

NOTES:

18. PMU comparator threshold test points, VR0, Test the comparator outputs using a binary search.
19. PMU comparator threshold test points, VR1, Test the internal references via Test & Cal Mux.
20. PMU comparator threshold test points, VR2, Test the comparator outputs using a binary search.
21. PMU comparator threshold test points, VIR, Test the internal references via Test & Cal Mux.

TABLE 10. PPMU COMPARATOR THRESHOLD

V RANGE	CAL POINTS	TEST POINTS
VR0	0V +3V	-0.5V +1.5V +3.5V
VR1	0V +5V	-1V +3V +7V
VR2	0V +10V	-1V +6V +11V
VIR	-0.8V +0.8V	-1V 0V +1V

DC Electrical Specifications – Low Voltage Clamps

SPEC #	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
14400	Low Voltage Clamp Error, VR0	Low voltage clamp test points, VR0 (see Table 11); Note 22	-100		+100	mV
14410	Low Voltage Clamp Error, VR1	Low voltage clamp test points, VR1 (see Table 11); Note 22	-100		+100	mV
14420	Low Voltage Clamp Error, VR2	Low voltage clamp test points, VR2 (see Table 11); Note 22	-100		+100	mV
	VCC_SV DC PSRR Error	Limits established by characterization and are not production tested. VR2 (see Table 11); Note 23		5		mV/V
	VEE DC PSRR Error	Limits established by characterization and are not production tested. VR2 (see Table 11); Note 23		20		mV/V
	Temperature Coefficient	Limits established by characterization and are not production tested. VR1 (see Table 11); Note 23		< ±200		µV/V

NOTES:
22. VCC_SV = +12.75, VCC = +7.75V, VEE = -2.75V, VDD = +3.25V, Vmid<1:0> = 00, V_REF = 3V, DUT_GND = 0
23. VCC_SV = +13V, VCC = +8V, VEE = -3V, VDD = +3.3V, Vmid<1:0> = 00, V_REF = 3V, DUT_GND = 0

TABLE 11. LOW VOLTAGE CLAMPS

V RANGE	CAL POINTS	TEST POINTS
VR0	0V +2V	-0.5V +1.5V +2.5V
VR1	0V +5V	-1V +3V +6V
VR2	0V +8V	-1V +5V +10V

Electrical Specifications DC Electrical Specifications – High Voltage Clamps

Spec #	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
14440	High Voltage Clamp Error	High voltage clamp test points, VR0 (see Table 12); Note 24	-100		+100	mV
14450	High Voltage Clamp Error	High voltage clamp test points, VR1 (see Table 12); Note 24	-100		+100	mV
14460	High Voltage Clamp Error	High voltage clamp test points, VR2 (see Table 12); Note 24	-100		+100	mV
	VCC_SV DC PSRR Error	Limits established by characterization and are not production tested. VR2 (see Table 12); Note 25		2		mV/V
	VEE DC PSRR Error	Limits established by characterization and are not production tested. VR2 (see Table 12); Note 25		4		mV/V
	Temperature Coefficient	Limits established by characterization and are not production tested. VR1 (see Table 12); Note 25		< ±200		µV/V

NOTES:
24. VCC_SV = +12.75, VCC = +7.75V, VEE = -2.75V, VDD = +3.25V, Vmid<1:0> = 00, V_REF = 3V, DUT_GND = 0
25. VCC_SV = +13V, VCC = +8V, VEE = -3V, VDD = +3.3V, Vmid<1:0> = 00, V_REF = 3V, DUT_GND = 0

TABLE 12. HIGH VOLTAGE CLAMPS

V RANGE	CAL POINTS	TEST POINTS
VR0	+1V +3V	+1V +1.5V +3.5V
VR1	+1V +5V	+1V +3V +7V
VR2	+1V +10V	+1V +5V +11V

DC Electrical Specifications – Resistor Values/Switch Impedances

VCC_SV = +13V, VCC = +8V, VEE = -3V, VDD = +3.3V, Vmid<1:0> = 00, V_REF = 3V, DUT_GND = 0

SPEC #	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
SENSE RESISTORS						
19000	IR0			500		kΩ
19010	IR1			125		kΩ
19020	IR2			31.25		kΩ
19030	IR3			7.81		kΩ
19040	IR4			1.95		kΩ
19050	IR5			500		Ω
19060	IR6			125		Ω
19070	IR7			31.25		Ω
ON-CHIP FET SWITCHES						
19100	RT PMU (SV) Switch		20	45	70	Ω
19110	External Force Switch		20	45	70	Ω
19120	External Sense Switch		5	8	11	kΩ
19130	Load Enable Switch		20	45	70	Ω

AC Characteristics

For all of the following DC and Electrical Specifications, compliance to datasheet limits is assured by one or more methods: production test, characterization and/or design.

F

AC Electrical Specifications – CPU Port

VCC_SV = +12.75, VCC = +7.75V, VEE = -2.75V, VDD = +3.25V, Vmid<1:0> = 00, V_REF = 3V, DUT_GND = 0

SPEC #	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
SET UP TIME						
27100	SDIO to rising CK		7			ns
27110	STB to rising CK		7			ns
HOLD TIME						
27120	Rising CK to SDIO		7			ns
27130	Rising CK to STB		7			ns
27140	CK Minimum Pulse Width High		18			ns
27150	CK Minimum Pulse Width Low		18			ns
27160	CK Period		40		100	ns
PROPAGATION DELAY						
	Rising CK to SDIO Out	Characterized only. Not production tested.			7	ns
27170	Reset Minimum Pulse Width		100			ns

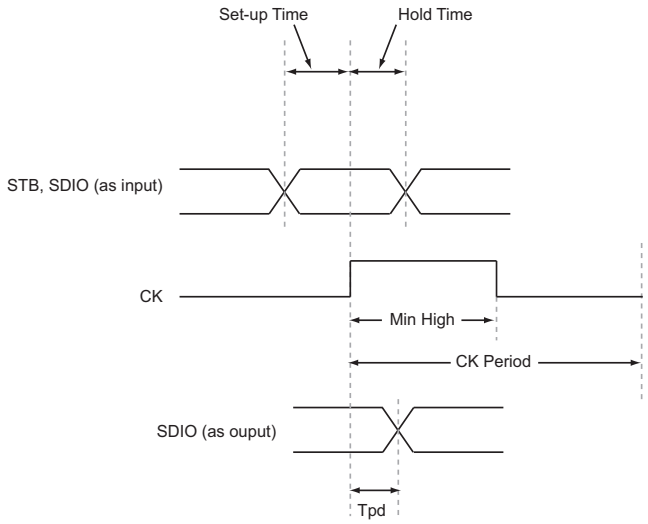


FIGURE 4.

SPEC #	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
RISE/FALL TIMES						
22200	2V	(Note 26)		0.5	1.0	ns
	Minimum Pulse Width	Bypass Mode (Note 26)		1.25		ns
	Minimum Pulse Width	PLL3, All deskews invoked (Note 26)		1.25		ns
PROPAGATION DELAY						
	DATA to DOUT	Bypass Mode		4.5		ns
	EN to DOUT	Bypass Mode (Note 29)		4		ns
	DATA to DOUT	PLL_CK = 156.25MHz, All deskews invoked		17.5		ns
	EN to DOUT	PLL_CK = 156.25MHz, All deskews invoked (Note 29)		17.5		ns
	Output Capacitance @ DOUT	VCC_SV = +13V, VCC = +8V, VEE = -3V, VDD = +3.3V, Vmid<1:0> = 00, V_REF = 3V, DUT_GND = 0		3.5		pF
ΔTPD vs. TEMPERATURE						
	Bypass Mode	DL3, Bypass Mode		+4.2		ps/°C
	With Deskew Elements	DL3, PLL_CK = 156.25MHz, All deskews invoked		+5		ps/°C
ΔTPD vs. PULLSE WIDTH						
	1.5ns Pulse Width	Bypass Mode		<300		ps
	1.25ns Pulse Width	Bypass Mode		<300		ps
	1.8ns Pulse width	All deskews invoked, PLL_CK = 156.25MHz		<100		ps
	1.5ns Pulse Width	All deskews invoked, PLL_CK = 156.25MHz		<400		ps
DRIVER PATH JITTER						
	Bypass Mode	Bypass Mode, 1 sigma		6.2		ps
	With Deskew Elements	All deskews invoked, PLL_CK = 156.25MHz, 1 Sigma		6.9		ps

NOTES:
26. DVH = 2V, DVL = 0V, ≤ 12" 50Ω Coax, 5pF at the end of the line. 10% to 90%.
27. EN to DOUT. Tested at 2.25V and 0.75V. Dr-Mode = 1.

AC Electrical Specifications – Comparator

SPEC #	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
	Minimum Pulse Width	Bypass Mode		1.0		ns
	Minimum Pulse Width	PLL_CK = 156.25MHz, All deskews invoked		1.0		ns
	Comparator Equivalent Bandwidth	VTT Active; VTT = 0V (Note 28)		1		GHz
	Comparator Equivalent Bandwidth	VTT HiZ (Note 28)		1		GHz
	Propagation Delay (DOUT to COMP_A, _B)	Bypass Mode		4		ns
	Propagation Delay (DOUT to COMP_A, _B)	PLL_CK = 156.25MHz, All deskews invoked		11		ns
	Output Rise Time (COMP_A, _B)			400		ps
ΔTPD vs. PULSE WIDTH						
	1.4ns pulse width, Bypass Mode	3V input. 100ns period. 1% to 99%; VR2		<100		ps
	1.25ns pulse width, Bypass Mode	3V input. 100ns period. 1% to 99%; VR2		<300		ps
	1.8ns pulse width, Bypass Mode	3V input. 100ns period. 1% to 99%; VR2, All deskews invoked, PLL_CK = 156.25MHz		<200		ps
	1.5ns pulse width, Bypass Mode	3V input. 100ns period. 1% to 99%; VR2, All deskews invoked, PLL_CK = 156.25MHz		<400		ps
ΔTPD vs. TEMPERATURE						
	Bypass Mode	Bypass Mode		+2		ps/°C
	With Deskew Elements	PLL_CK = 156.25MHz, All deskews invoked		+2		ps/°C
COMPARATOR PATH JITTER (DOUT TO COMP_A, _B)						
	Bypass Mode	Bypass Mode, 1 sigma		5.7		ps
	With Deskew Elements	PLL_CK = 156.25MHz, All deskews invoked, 1 sigma		6.2		ps

NOTE:

28. 10% to 90% BW = 0.35/((Tr-input)**2 - (Tr-measured)**2) ** 0.5; 3V input; Tr/Tf (input) = 1.2ns.

AC Electrical Specifications – PMU

	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
	Voltage Force Settling Time (Note 29)	IR0		4		ms
		IR1		1		ms
		IR2		400		µs
		IR3		100		µs
		IR4		25		µs
		IR5		20		µs
		IR6		20		µs
		IR7		20		µs
	Current Force Settling Time (Note 30)	IR0		350		µs
		IR1		170		µs
		IR2		130		µs
		IR3		130		µs
		IR4		130		µs
		IR5		130		µs
		IR6		130		µs
		IR7		130		µs
	MI Settling Time (through MONITOR) (Note 30)	IR0		250		µs
		IR1		130		µs
		IR2		130		µs
		IR3		130		µs
		IR4		130		µs
		IR5		130		µs
		IR6		130		µs
		IR7		130		µs
	MV Settling Time (through MONITOR) (Note 31)			5		µs

NOTES:

29. 1nF load. 0V to 5V input signal. PMU Sense = DOUT.
30. -Imax to +Imax into an external resistive load equal to Rsense for each current range.
31. 0V to 5V input at DOUT, Tr = 2ns.

AC Electrical Specifications – Ring Oscillator (Driver and Comparator)

All round-trip delay measurements are taken with the driver and comparator configured as a ring oscillator.

NOTE: The loop time measured when the channel is configured as a ring oscillator does NOT indicate the total round trip time of the pin electronics, as some circuitry in the driver signal paths are bypassed and the circuitry of the ring oscillator control logic is inserted into the overall loop. The total delay measured in this configuration is used as a figure of merit to verify part to part AC performance

SPEC #	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
20000	Ring Oscillator Loop Delay @ 100MHz	Channels 0 and 1 configured as ring oscillators; Ring triggered on a rising and falling edge; Ring configured DATA through Comp A and Comp B; Ring configured EN through Comp A and Comp B; All deskews invoked	40	48	56	ns
20001	Ring Oscillator Loop Delay @ 156.25MHz		30	38	46	ns
20115	PLL Lock Test @ 100MHz	VCC_SV = +13V, VCC = +8V, VEE = -3V, VDD = +3.3V, Vmid<1:0> = 00, V_REF = 3V, DUT_GND = 0	1.2	1.5	1.8	V
20125	PLL Lock Test @ 156.25MHz		1.7	2.1	2.5	V

AC Electrical Specifications – Fine Delay

VCC_SV = +13V, VCC = +8V, VEE = -3V, VDD = +3.3V, Vmid<1:0> = 00, V_REF = 3V, DUT_GND = 0; Channels 0 and 1 configured as ring oscillators

SPEC #	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
DATA, EN DELAY BLOCKS; PLL_CK = 100MHz						
25300	Tmin (Tpd+, Tpd- with FD = 0)		1.5	2.2	2.9	ns
25310	Full Scale Delay (Tpd+, Tpd-) (Code 1111 – Code 0000)		300	500	700	ps
	Resolution	Limits established by characterization and are not production tested.		33		ps
DATA, EN DELAY BLOCKS; PLL_CK = 156.25MHZ						
25305	Tmin (Tpd+, Tpd- with FD = 0)		1.0	1.5	2.0	ns
25315	Full Scale Delay (Tpd+, Tpd-) (Code 1111 – Code 0000)		100	200	350	ps
	Resolution	Limits established by characterization and are not production tested.		13		ps
COMP A, B DELAY BLOCKS; PLL_CK = 100MHZ						
25320	Tmin (Tpd+, Tpd- with FD = 0)		1.5	2.2	2.9	ns
25330	Full Scale Delay (Tpd+, Tpd-) (Code 1111 – Code 0000)		300	500	700	ps
	Resolution	Limits established by characterization and are not production tested.		33		ps
COMP A, B DELAY BLOCKS; PLL_CK = 156.25MHZ						
25325	Tmin (Tpd+, Tpd- with FD = 0)		1.0	1.5	2.0	ns
25335	Full Scale Delay (Tpd+, Tpd-) (Code 1111 – Code 0000)		100	200	350	ps
	Resolution	Limits established by characterization and are not production tested.		13		ps

AC Electrical Specifications – Coarse Delay

VCC_SV = +13V, VCC = +8V, VEE = -3V, VDD = +3.3V, Vmid<1:0> = 00, V_REF = 3V, DUT_GND = 0; Channels 0 and 1 configured as ring oscillators

SPEC #	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
DATA, EN DELAY BLOCKS; PLL_CK = 100MHZ						
25100	Tmin (Tpd+, Tpd- with CD = 0)		0.6	1.1	1.6	ns
25110	Full Scale Delay (Tpd+, Tpd-) (Code 1111 – Code 0000)		3.7	4.7	5.7	ns
	Resolution	Limits established by characterization and are not production tested.		312.5		ps
DATA, EN DELAY BLOCKS; PLL_CK = 156.25MHZ						
25105	Tmin (Tpd+, Tpd- with CD = 0)		0.5	1.0	1.5	ns
25115	Full Scale Delay (Tpd+, Tpd-) (Code 1111 – Code 0000)		2.3	3.0	3.7	ns
	Resolution	Limits established by characterization and are not production tested.		200		ps
COMP A, B DELAY BLOCKS; PLL_CK = 100MHZ						
25120	Tmin (Tpd+, Tpd- with CD = 0)		0.6	1.1	1.6	ns
25130	Full Scale Delay (Tpd+, Tpd-) (Code 1111 – Code 0000)		3.7	4.7	5.7	ns
	Resolution	Limits established by characterization and are not production tested.		312.5		ps
COMP A, B DELAY BLOCKS; PLL_CK = 156.25MHZ						
25125	Tmin (Tpd+, Tpd- with CD = 0)		0.5	1.0	1.5	ns
25135	Full Scale Delay (Tpd+, Tpd-) (Code 1111 – Code 0000)		2.3	3.0	3.7	ns
	Resolution	Limits established by characterization and are not production tested.		200		ps

AC Electrical Specifications – Fine Falling Edge Adjust (DATA, EN)

VCC_SV = +13V, VCC = +8V, VEE = -3V, VDD = +3.3V, Vmid<1:0> = 00, V_REF = 3V, DUT_GND = 0; Channels 0 and 1 configured as ring oscillators

SPEC #	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
PLL_CK = 100MHz						
25400	Tmin (Tpd+, Tpd- ; Sel-XX-FFEA = 0; Code = 1000)		2.3	3.0	3.7	ns
25410	ΔTpd- Full Scale Acceleration (Code 0000 relative to 1000)		-450	-300	-150	ps
25420	ΔTpd- Full Scale Delay (Code 1111 relative to 1000)		+150	+270	+400	ps
	Resolution	Limits established by characterization and are not production tested.		35		ps
25421	Tpd+ Error (ΔTpd+ vs. all FFEA codes)		-25	0	+50	ps
PLL_CK = 156.25MHz						
25405	Tmin (Tpd+, Tpd- ; Sel-XX-FFEA = 0; Code = 1000)		1.7	2.2	2.7	ns
25415	ΔTpd- Full Scale Acceleration (Code 0000 relative to 1000)		-250	-150	-50	ps
25425	ΔTpd- Full Scale Delay (Code 1111 relative to 1000)		+50	+150	+250	ps
	Resolution	Limits established by characterization and are not production tested.		20		ps
25421	ΔTpd+ Error (Tpd+ vs. all FFEA codes)		-25	0	+50	ps

AC Electrical Specifications – Fine Falling Edge Adjust (Comparator - COMP_A, _B)

VCC_SV = +13V, VCC = +8V, VEE = -3V, VDD = +3.3V, Vmid<1:0> = 00, V_REF = 3V, DUT_GND = 0; Channels 0 and 1 configured as ring oscillators

SPEC #	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
PLL_CK = 100MHz						
25430	Tmin (Tpd+, Tpd- ; Sel-XX-FFEA = 0; Code = 01000)		3.0	4.2	5.5	ns
25440	ΔTpd- Full Scale Acceleration (Code 00000 relative to 01000)		-720	-500	-300	ps
25450	ΔTpd- Full Scale Delay (Code 11111 relative to 01000)		300	550	750	ps
	Resolution	Limits established by characterization and are not production tested.		35		ps
25421	ΔTpd+ vs. all FFEA		-25	0	+50	ps
PLL_CK = 156.25MHz						
26535	Tmin (Tpd+, Tpd- ; Sel-XX-FFEA = 0; Code = 01000)		2.3	3.0	3.7	ns
25445	ΔTpd- Full Scale Acceleration (Code 00000 relative to 01000)		-370	-220	-100	ps
25455	ΔTpd- Full Scale Delay (Code 11111 relative to 01000)		+120	+250	+400	ps
	Resolution	Limits established by characterization and are not production tested.		20		ps
25421	ΔTpd+ vs. all FFEA		-25	0	+50	ps

AC Electrical Specifications – Coarse Falling Edge Adjust (DATA, EN)

VCC_SV = +13V, VCC = +8V, VEE = -3V, VDD = +3.3V, Vmid<1:0> = 00, V_REF = 3V, DUT_GND = 0; Channels 0 and 1 configured as ring oscillators

SPEC #	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
PLL_CK = 100MHz						
25200	Tmin (Tpd+, Tpd- ; Sel-XX-CFEA = 0; Code = 1000)		3.0	4.0	5.0	ns
25210	ΔTpd- Full Scale Acceleration (Code 0000 relative to 1000)		-3.2	-2.5	-1.9	ns
25220	ΔTpd- Full Scale Delay (Code 1111 relative to 1000)		+1.6	+2.2	+2.8	ns
	Resolution	Limits established by characterization and are not production tested.		312.5		ps
25221	ΔTpd+ vs. all CFEA codes		-150	0	+100	ps
PLL_CK = 156.25MHz						
25205	Tmin (Tpd+, Tpd- ; Sel-XX-CFEA = 0; Code = 1000)		2.2	3.0	3.8	ns
25215	ΔTpd- Full Scale Acceleration (Code 0000 relative to 1000)		-2.0	-1.6	-1.2	ns
25225	ΔTpd- Full Scale Delay (Code 1111 relative to 1000)		+1.0	+1.4	+1.8	ns
	Resolution	Limits established by characterization and are not production tested.		200		ps
25221	ΔTpd+ vs. all CFEA codes (all codes except 8 and 9)		-150	0	+100	ps

Chip Overview

The ISL55161 is a highly integrated System-on-a-Chip pin electronics solution aimed at incorporating every analog function, along with some digital support circuitry, required on a per channel basis for Automatic Test Equipment (see Figure 6). The interface, control and I/O of the chip are all digital; all analog circuitry is inside the chip. Two complete tester channels are integrated into each chip.

ISL55161 is pin and functionally compatible with Venus, Venus Plus and Venus 4.

CPU Control

All chip setup, configuration control, and writing to and reading back of the internal registers and memory is controlled through the 3-bit serial data CPU port. The CPU port is typically used to set up the operating mode of the chip prior to executing a test, or to change modes during a test.

An internal register chart (see tables in “Memory Space” section starting on page 74) documents all programmable control signals and their addresses, and shows how to program each internal signal.

High Speed Control

All real-time control and observation is accomplished via the real-time input and output signals:

- DATA_0, DATA_1 (Differential Inputs)
- EN_0, EN_1 (Differential Inputs)
- SV_0, SV_1 (Single-ended Inputs)
- COMP_A_0, COMP_B_0 (Differential Outputs)
- COMP_A_1, COMP_B_1 (Differential Outputs)

Analog Reference

All on-chip analog functions are related to one of several off-chip precision reference inputs:

- PLL_CK
- R_EXT
- V_REF

These external references are used to provide accurate and stable analog circuit performance that does not vary over time, temperature, supply voltage, or process changes.

External Signal Nomenclature

All input and output pins, when referred to in the datasheet or in any circuit diagram, use the following naming conventions:

- All capital letters (i.e., DATA, CK, SDIO)
- Underscores for clarity (i.e., EXT_SENSE, EN_0)
- Shown next to an I/O circle in any schematic

CPU Programmed Control Line Nomenclature

Any internal signal, DAC level, or control signal that is programmed via the CPU port uses a different nomenclature:

- The first letter in a word is always a capital letter.
- Subsequent letters within the same word are lower case.
- Dashes (but never an underscore) for clarity.
- NOT shown with an I/O circle in any schematic.

Control lines, internal registers, and other internal signals, which are programmable by the CPU port, are listed in the tables in the “Memory Space” section starting on page 74.

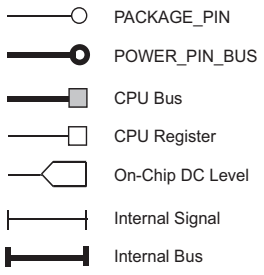


FIGURE 5.

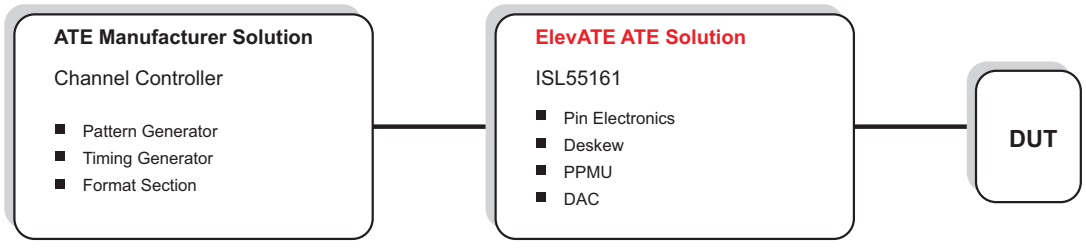
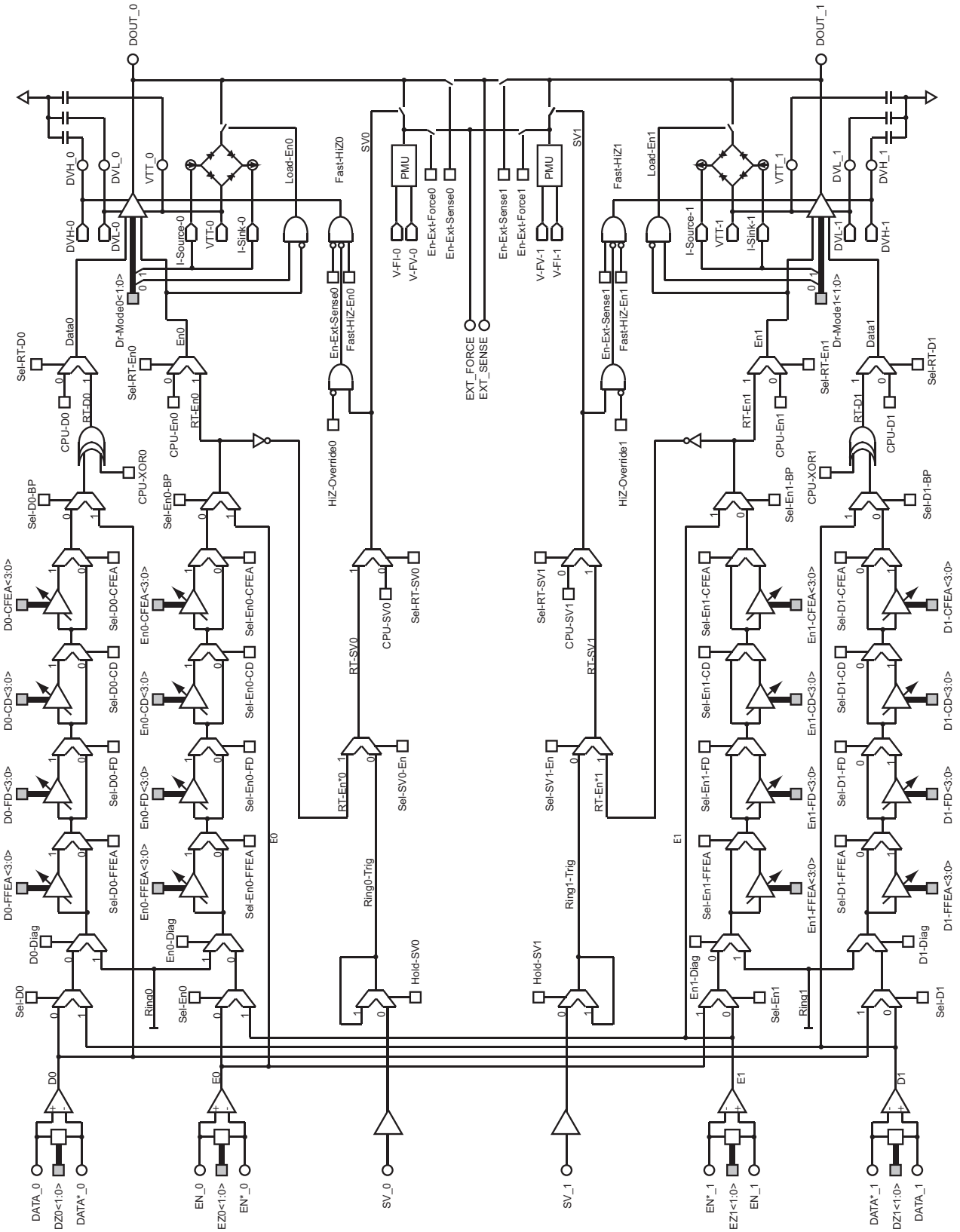
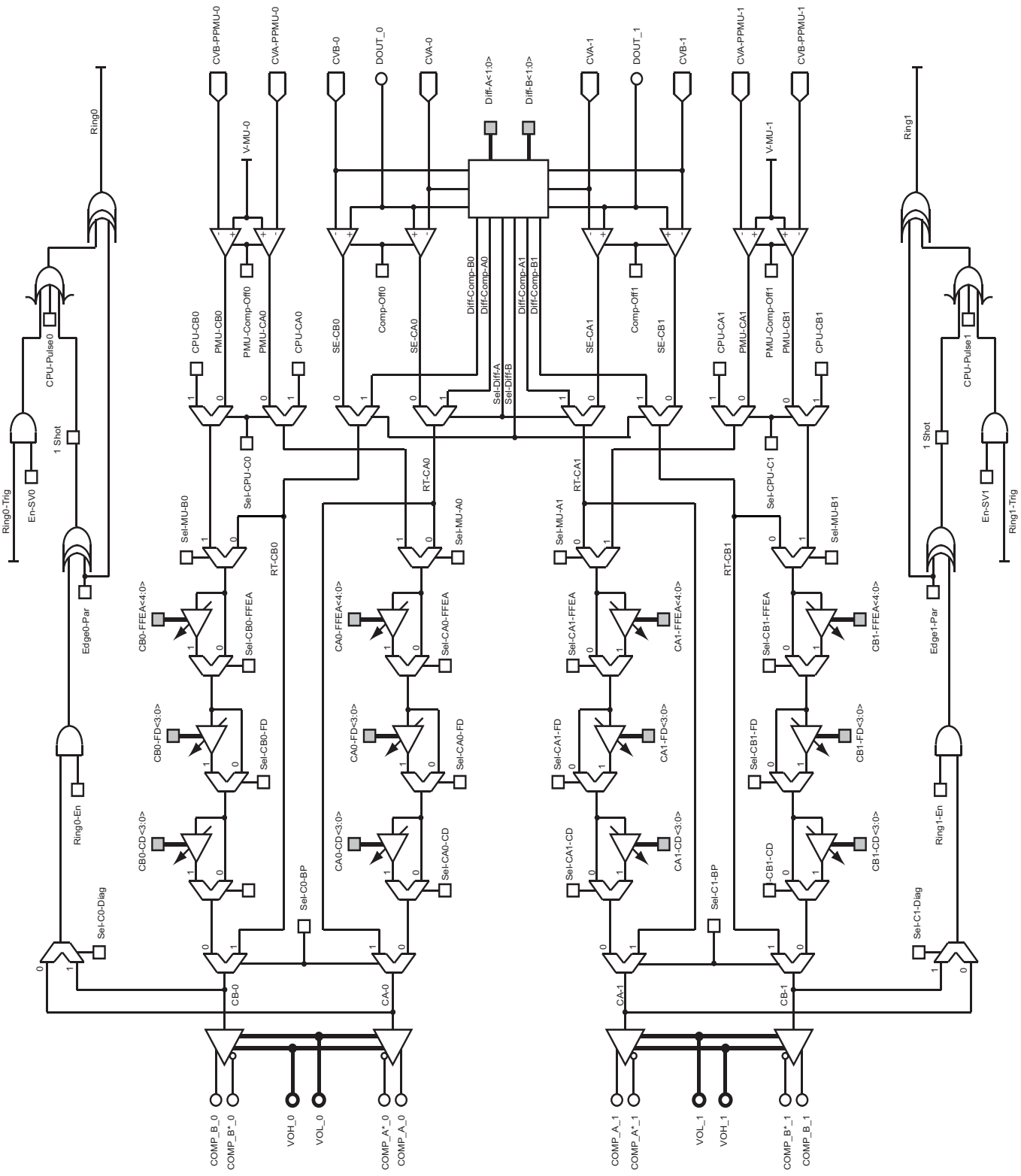


FIGURE 6.

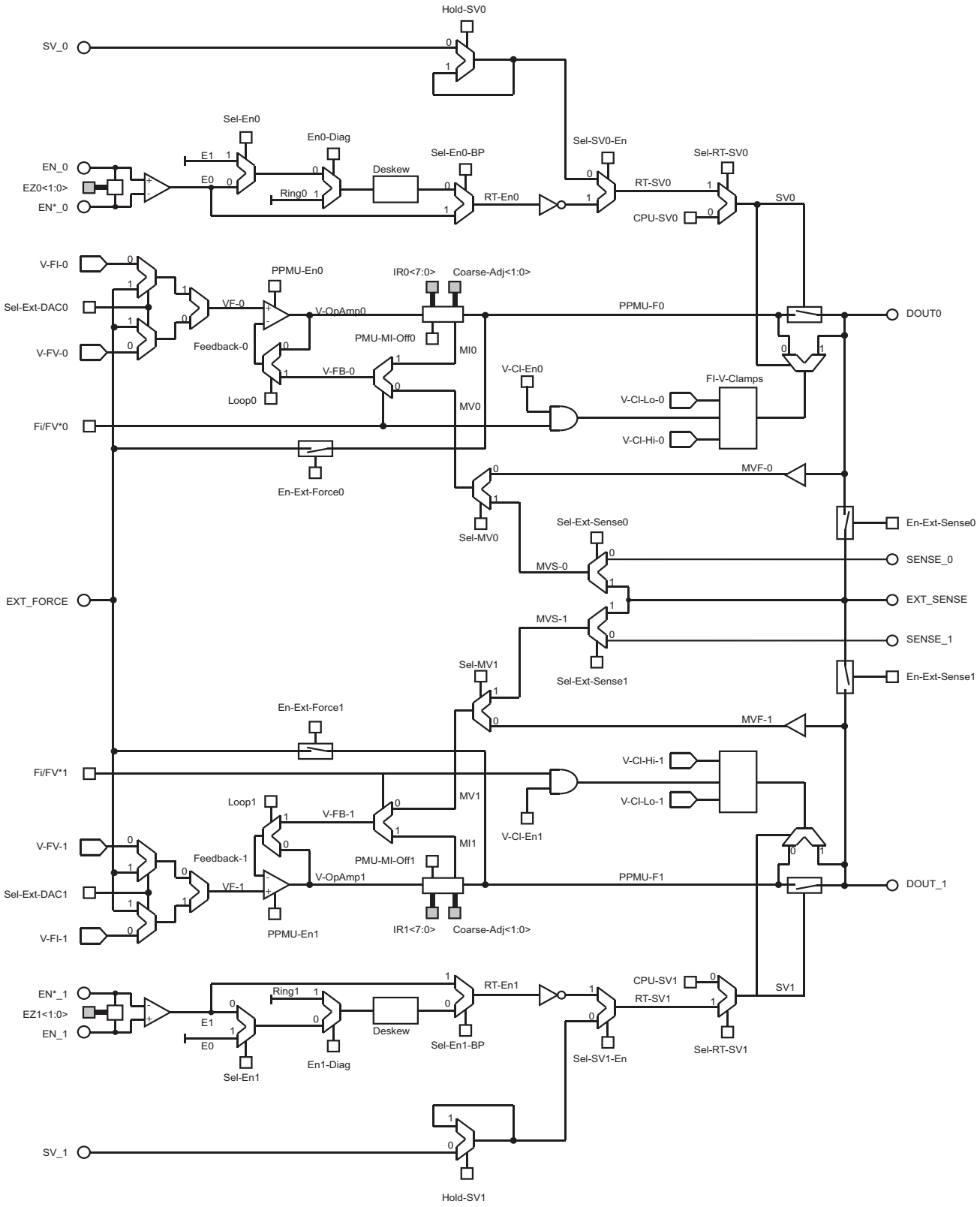
Driver/VTT/Load Block Diagram



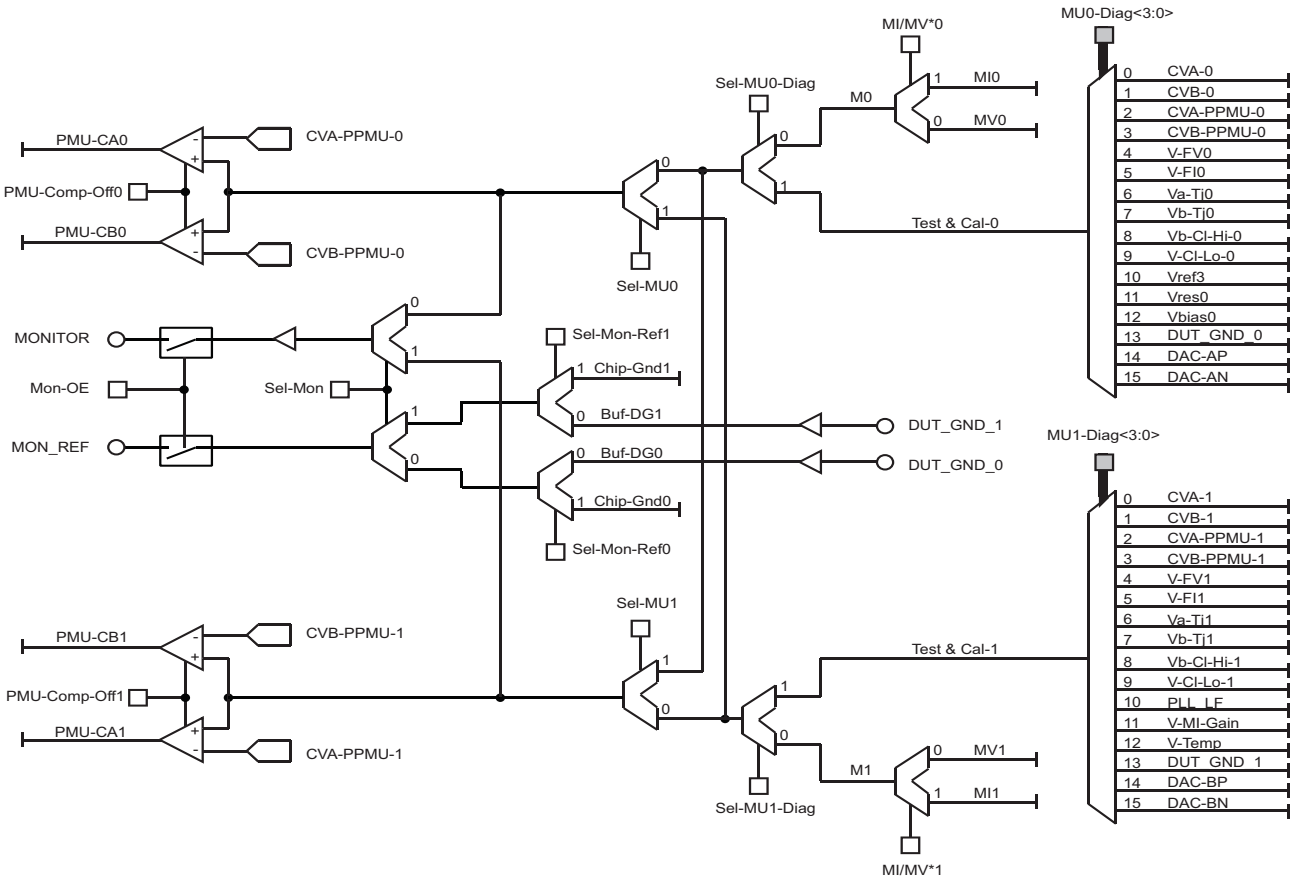
Comparator Block Diagram



PMU Block Diagram



Measurement Unit Block Diagram



PLL Overview

There is an on-chip PLL that sets the full-scale delay range and resolution of all internal deskew elements.

PLL_CK is required only if any deskew element is used. If no delay elements are used, PLL_CK may be left in a static low state.

Lock Range

The PLL lock range is total span of PLL_CK frequencies for which the PLL can capture and lock to the input signal.

100MHz ≤ PLL_CK Frequency ≤ 156.25MHz

10.0ns ≥ PLL_CK Period ≥ 6.4ns

Track Range

The track range of the PLL is the span of PLL_CK frequencies that the PLL can track, once lock has already been achieved. The track range is wider than the lock range.

Frequency Clamps

A frequency clamp exists that limits the lower end of the frequency range for which the PLL will lock. If no signal is on PLL_CK, or if the frequency of PLL_CK is too low, the clamps will limit the effective locking frequency to the clamping frequency.

The frequency clamps are programmed via the CPU port and should be established prior to executing any real-time patterns. As long as PLL_CK is faster than the Fclamp limit, the frequency clamps have no function or effect on PLL operation.

The recommended clamp setting for all PLL_CK inputs is the default condition:

- Fclamp1 = 0
- Fclamp0 = 0

Internal Swing Settings

There are two CPU register bits that slightly alter the internal behavior of the delay cells and the logic gates in the high-speed timing path by changing the amplitude of the internal swings.

TABLE 13. INTERNAL SWING SETTINGS

V_{SWING}<1:0>	MODE
00	Lowest Bandwidth, Lowest Power
01	•
10	•
11	Highest Bandwidth, Highest Power

PLL Disable

The CPU port may connect the PLL output voltage to ground through an on-chip switch. The PLL and the PLL_CK input buffer are powered down when the PLL is disabled.

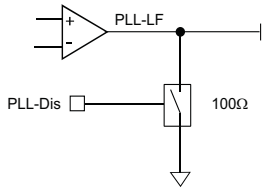


FIGURE 7.

TABLE 14. PLL DISABLE

PLL-DIS	PLL-LF	PLL HARDWARE
0	Active	Active
1	Disabled (100Ω to GND)	Powered Down

On-Chip Terminations

PLL_CK/PLL_CK* inputs have on-chip termination options that support three different termination schemes:

1. No termination (open circuit)
2. 100Ω across the differential inputs
3. 50Ω single-ended termination

All of these termination schemes may be realized without requiring any external resistors.

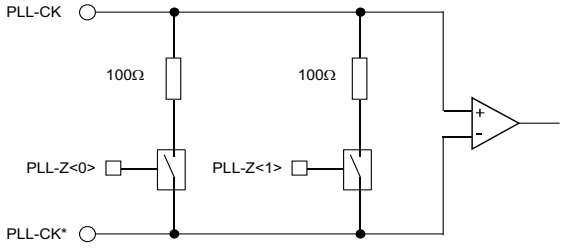


FIGURE 8.

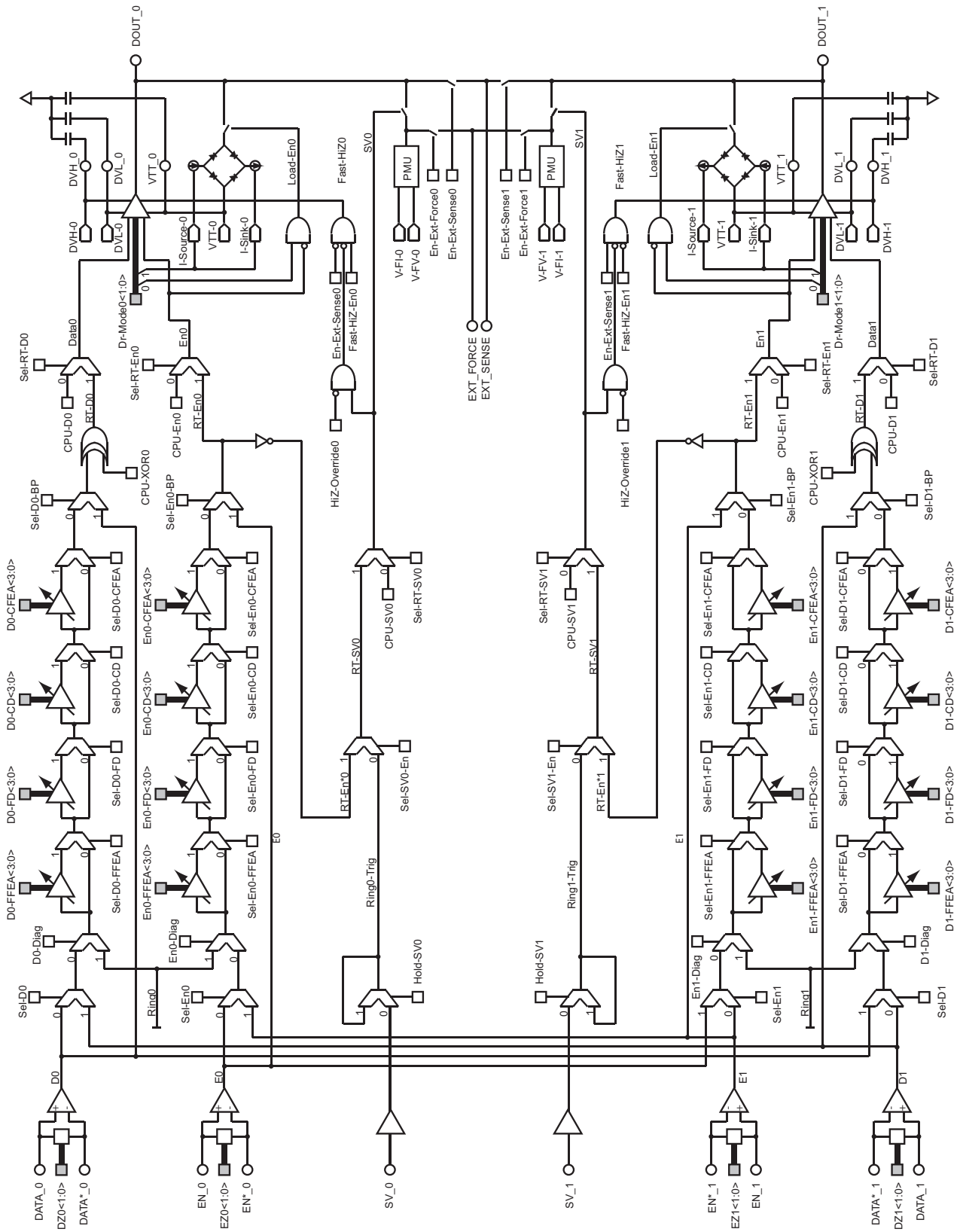
The selection of any on-chip termination is made through the CPU port. PLL-Z<1:0> are internal control bits that select the termination option. Their addresses are listed in the tables in the “Memory Space” section starting on page 74.

TABLE 15. PLL ON-CHIP TERMINATIONS

PLL-Z<1:0>	TERMINATION OPTION
00	No Termination
01	100Ω Differential
10	100Ω Differential
11	50Ω Single-Ended

Driver

Detailed Block Diagram



Real-time Digital Inputs

Each channel has real-time digital inputs, DATA and EN, which control the real-time operation of the driver, and SV, which controls the real-time PMU connection.

UNIVERSAL INPUTS

DATA_0/DATA*_0, DATA_1/DATA*_1, EN_0/EN*_0, and EN_1/EN*_1 are differential inputs that directly accept most standard technologies which operate between VDD (+3.3V) and ground without requiring any external translation.

ON-CHIP TERMINATIONS

Each channel's DATA and EN inputs have independent on-chip termination options which support three different termination schemes:

1. No termination (open circuit)
2. 100Ω across the differential input
3. 50Ω single-ended termination

All of these termination schemes may be realized without requiring any external resistors. Access and control of these termination resistors is accomplished via the CPU port, through which the individual enable bits can be set or cleared.

TABLE 16. ON-CHIP TERMINATIONS

EZ#<1:0> DZ#<1:0>	INPUT TERMINATION
0 0	No Termination
0 1	100Ω
1 0	100Ω
1 1	50Ω

50Ω SINGLE-ENDED TERMINATION

Selecting both 100Ω terminators creates a single-ended 50Ω termination. The inverting input then becomes the termination voltage for the input signal, and the appropriate termination voltage level must be applied to this pin. Vterm must be able to handle any current flow required for proper termination.

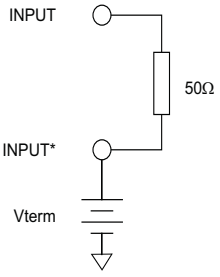


FIGURE 9.

100Ω DIFFERENTIAL TERMINATION

By selecting either, but not both, 100Ω terminators, a 100Ω resistance is connected between the differential inputs, thus cleanly terminating differential inputs connected by 50Ω transmission lines on the PCB.

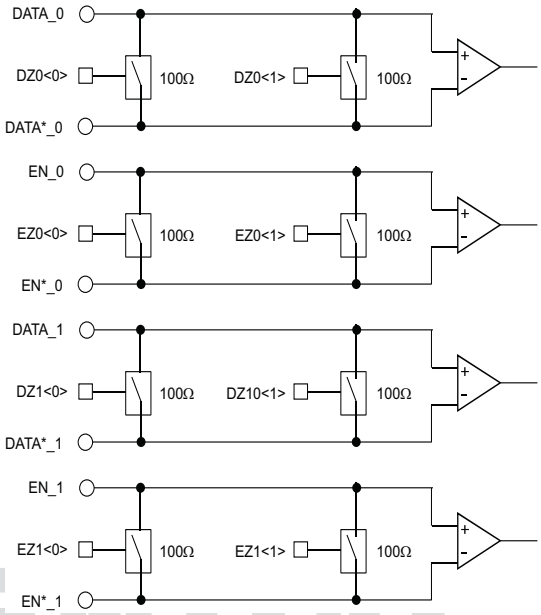


FIGURE 10.

SUPER VOLTAGE

SV# is a single-ended, real-time digital input that can be used to connect and disconnect the PMU.

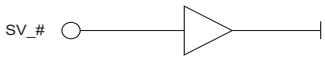


FIGURE 11.

Digital Signal Processing Options

DATA AND ENABLE CROSS POINT SWITCH

The DATA and EN inputs for each channel may be routed independently to either channel. This up-front, 2X2 cross point switch is extremely useful in creating a 1:2 fanout tree for these two high-speed digital inputs without requiring any external circuitry. This switch is also used when combining both channels into a differential driver.

There are no restrictions between the selected DATA or EN signals on Channel 0 and Channel 1 in that either channel's signals may drive either, or both, channel's signal paths. The various mux select control lines are internal registers controlled via the CPU port and are documented in the tables in the "Memory Space" section starting on page 74.

TABLE 17. DATA CROSS POINT SWITCH

SEL-D#	DATA# SOURCE
0	DATA_#
1	DATA(1-#)

TABLE 18. ENABLE CROSS POINT SWITCH

SEL-EN#	ENABLE# SOURCE
0	EN_#
1	EN_(1-#)

RING OSCILLATOR MODE

The data and enable paths may be used to configure the channel as a ring oscillator. This configuration is useful for calibration of the delay elements.

TABLE 19. RING OSCILLATOR MODE

D#-DIAG EN#-DIAG	DATA PATH SOURCE ENABLE PATH SOURCE
0	DATA_#, EN_#
1	Ring#

BYPASS MODE

The DATA and EN deskew elements may be bypassed completely. This mode results in the shortest Tpd and highest bandwidth across the chip and is useful in applications where the digital features and channel deskew are performed in an external IC. When set high, these bits will slightly lower the power by ~45mW per channel.

TABLE 20. BYPASS MODE

SEL-D#-BP SEL-EN#-BP	RT-D# RT-EN#
0	Deskews Enabled
1	Deskews Bypassed

DATA INVERSION

The CPU port can invert the polarity of the data signal. This inversion is useful when creating the inverting signal of a differential driver.

TABLE 21. DATA INVERSION

CPU-XOR#	RT-D#
0	True Data Signal
1	Inverted Data Signal

CPU CONTROL

The CPU port can take control over the driver data and enable signals and override any real-time inputs.

TABLE 22. CPU DATA CONTROL

SEL-RT-D#	DATA#
0	CPU-D#
1	RT-D#(*)

TABLE 23. CPU ENABLE CONTROL

SEL-RT-EN#	EN#
0	CPU-En#
1	RT-En#

Ring Oscillator

Each channel may be placed into a ring oscillator configuration where the comparator outputs are fed back into the driver. This mode is used primarily for test and characterization and it may also be used for calibrating the deskew elements.

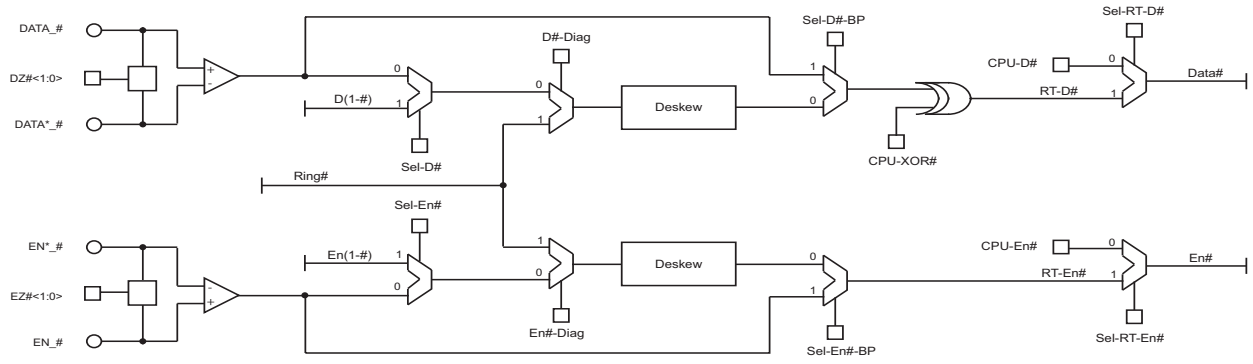


FIGURE 12.

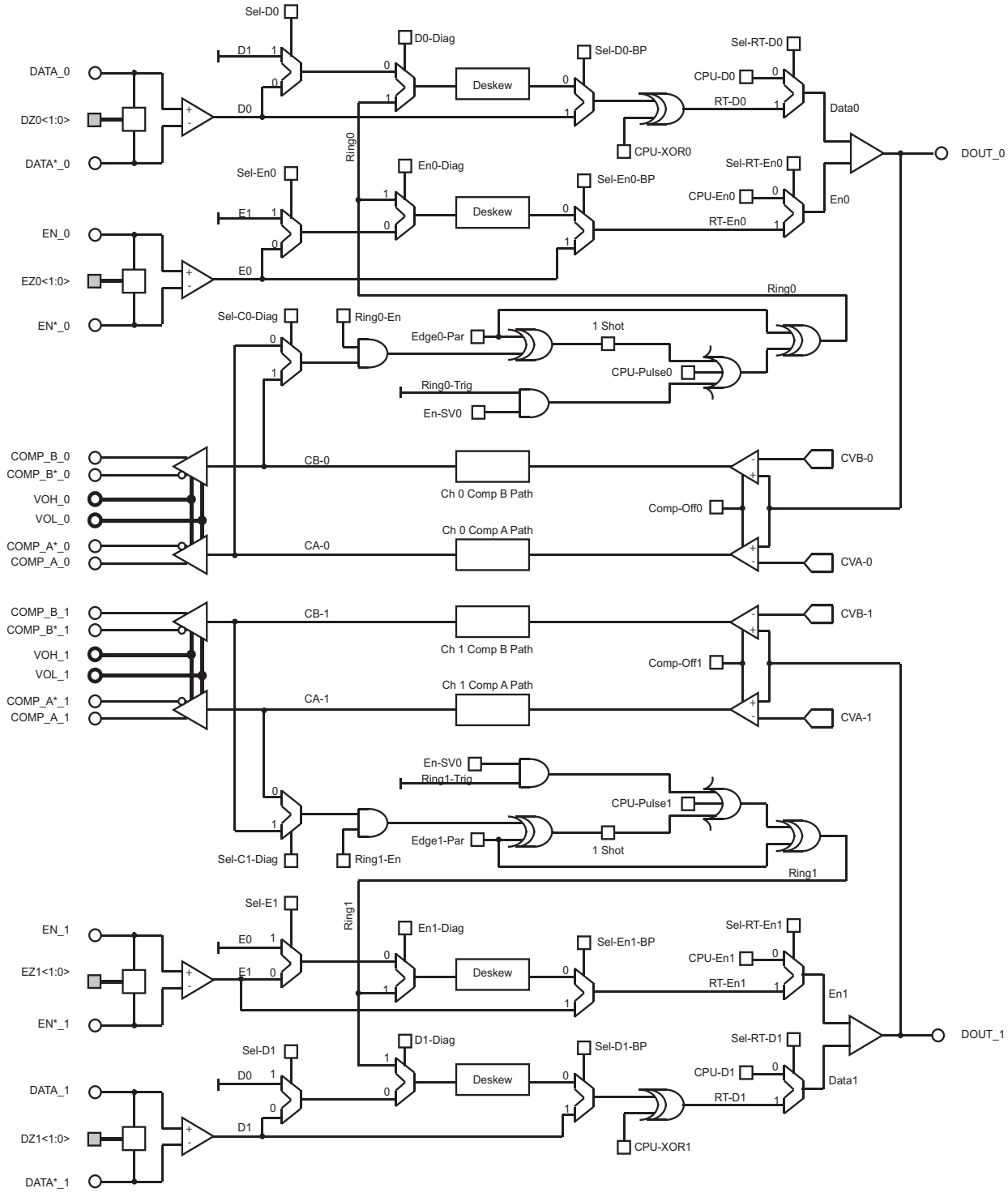


FIGURE 13. RING OSCILLATOR

RING OSCILLATOR – DRIVER PATH SELECTION

Either the data or enable path may be chosen as the source of the driver input and is determined by the CPU port.

It is important to choose either the data or the enable path, but not both.

Ring Oscillator – Comparator Path Selection

Either comparator path A or B may be selected as the return path for the ring oscillator.

TABLE 24. COMPARATOR PATH SELECTION

SEL-C#-DIAG	COMPARATOR PATH
0	Comp A
1	Comp B

RING OSCILLATOR – EDGE PARITY

The ring oscillator may be triggered by either a positive or a negative driver transition. This flexibility is useful when measuring the falling edge timing errors due to duty cycle or pulse width.

TABLE 25. RING OSCILLATOR EDGE PARITY

EDGE#-PAR	RING # TRIGGER POLARITY
0	Positive Edge
1	Negative Edge

RING OSCILLATOR - ENABLE

Once the ring is configured, it will not oscillate until the enable signal is set high by the CPU port.

TABLE 26. RING OSCILLATOR ENABLE

RING#-EN	RING # OSCILLATOR STATUS
0	Ring Disabled
1	Ring Enabled

RING OSCILLATOR – START-UP

There are two methods to start-up the ring oscillator:

1. CPU port
2. SV input pin

CPU PORT START-UP

The ring starts up by the CPU port executing a CPU-Pulse# transaction. This write-only function fires off a one-shot pulse that initiates the ring oscillation.

Only one CPU transaction is needed to start-up the ring.

SV START-UP

SV_# may be used to initiate the ring oscillator by injecting one narrow positive pulse (~ 10ns) into this pin. En-SV# enables and disables this start-up path.

TABLE 27.

EN-SV#	SV# START-UP PATH
0	Disabled
1	Enabled

ENABLE PATH CONFIGURATION

To use the enable path for the ring oscillator, the enable signal must be routed into the driver's data input through either the XOR or the OR option multiplexer. The following steps should be taken to set up the configuration correctly:

- CPU control over the enable signal, driver on.
  - Sel-RT-En0(1) = 0
  - CPU-En0(1) = 1

XOR Gate Option

- Enable path connected as the driver data.
  - Sel-RT-D0(1) = 1
  - Sel-D0(1)-OR = 0
  - D0-XOR = 1

OR Gate Option

- Enable path connected as the driver data.
  - Sel-RT-D0(1) = 1
  - D0(1)-XOR = 0
  - CPU-XOR0(1) = 0
  - Sel-D0(1)-OR = 1

Either the XOR path or the OR path may be used to configure the ring to use the enable signal path to force the driver, but not both at the same time. In either case, D0(1) must be placed in a static low state; otherwise, this signal will affect proper ring oscillator operation.

Deskew

Each channel's high-speed DATA and EN inputs have timing adjustment capability with the following characteristics:

- Separate and independent delay circuitry for the DATA and EN paths.
- Separate and independent delay circuitry for Channel 0 and Channel 1.
- Propagation delay adjust (both rising (Tpd+) and falling (Tpd-) edge are delayed equally).
- Falling edge adjust (FEA) (falling edge may be adjusted, rising edge Tpd remains constant).
- Timing delay range and resolution established by an external frequency.
- If bypassed, the delay element shuts down and consumes no power.

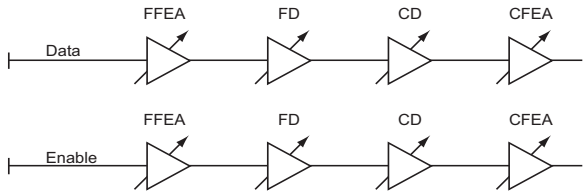


FIGURE 14.

PROPAGATION DELAY ADJUST

The propagation delay circuitry adds timing delay to the rising edge (Tpd+) and the falling edge (Tpd-) in equal amounts. Propagation delay adjustment is typically used for aligning the timing of multiple channels inside a tester.

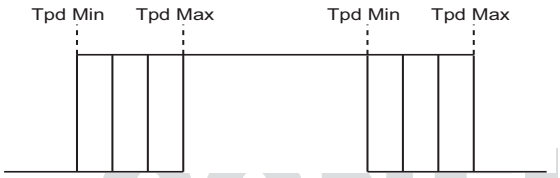


FIGURE 15.

The delay circuitry is divided into two separate blocks:

1. Coarse Delay
2. Fine Delay

PROPAGATION DELAY FALLING EDGE ADJUST

The falling edge delay circuitry adds or subtracts timing delay to or from the falling edge (Tpd-) while having no effect on the rising edge (Tpd+). Propagation delay adjustment is typically used for removing any pulse width distortion inside a tester.

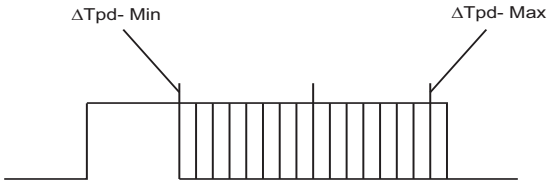


FIGURE 16.

BYPASS MODE

All DATA and EN digital processing and deskew options may be bypassed completely by having DATA and EN have direct control over the driver. This mode results in the shortest Tpd across the chip and is useful in applications where the digital features and channel deskew are performed in an external IC.

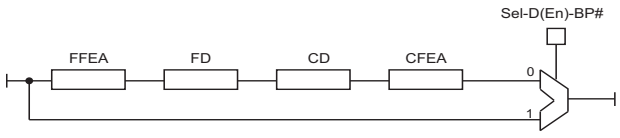


FIGURE 17.

TABLE 28. BYPASS MODE

SEL-D#-BP SEL-EN#-BP	RT-D# RT-EN#
0	Deskew Elements in Signal Path
1	Deskew Elements Bypassed

COARSE DELAY

Coarse delay divides the overall delay range (established by the period of PLL_CK) into equal segments and then selects one of those delays.

- Tspan (CD) = (15/32) • T
- Resolution = T/32

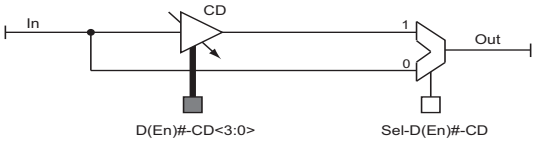


FIGURE 18.

Coarse delay is programmed by the CPU port and may be bypassed. If bypassed, the circuitry powers down.

TABLE 29.

SEL-D(EN)#-CD	SIGNAL PATH
0	CD Bypassed and Powered Down
1	CD Invoked

TABLE 30.

PLL_CK	T = 6.4ns	T = 10ns
Tspan	3.0ns	4.6875ns
Resolution	200 ps	312.5 ps

TABLE 31.

D(En)#-CD<3:0>	ΔTpd±	ΔTpd±
0000	0 ps	0 ps
0001	+200ps	+312.5ps
0010	+400ps	+625ps
0011	+600ps	+937.5ps
0100	+800ps	+1.25ns
0101	+1.0ns	+1.5625ns
0110	+1.2ns	+1.875ns
0111	+1.4ns	+2.1875ns
1000	+1.6ns	+2.5ns
1001	+1.8ns	+2.8125ns
1010	+2.0ns	+3.125ns
1011	+2.2ns	+3.4375ns
1100	+2.4ns	+3.75ns
1101	+2.6ns	+4.0625ns
1110	+2.8ns	+4.375ns
1111	+3.0ns	+4.6875ns

FINE DELAY

Fine delay adjust makes very small corrections to Tpd+ and Tpd- and affects both rising and falling edges equally. FD allows edge placement between coarse delay LSB steps.

- Tspan (FD) = 15 • T/512
- Resolution = T/512

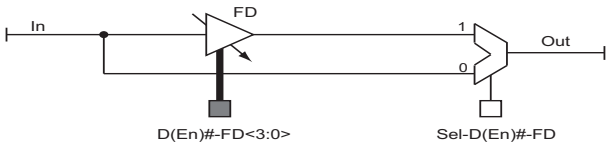


FIGURE 19.

Fine delay is programmed by the CPU port and may be bypassed. If bypassed, the circuitry powers down.

TABLE 32.

SEL-D(EN)#-FD	SIGNAL PATH
0	FD Bypassed and Powered Down
1	FD Invoked

TABLE 33.

PLL_CK	T = 6.4ns	T = 10ns
Tspan	187.5ps	292.96875ps
Resolution	12.5ps	19.53125ps

TABLE 34.

FD<3:0>	ΔTpd±	ΔTpd±
0000	0ps	0 ps
0001	+12.5ps	+19.53125ps
0010	+25ps	+39.0625ps
•	•	•
•	•	•
1101	+162.5ps	+253.90625ps
1110	+175ps	+273.4375ps
1111	+187.5ps	+292.96875ps

FINE FALLING EDGE ADJUST

FFEA offers a selection of 16 different falling edge adjustments as selected by the CPU port. The total range for FFEA is related to the PLL_CK period by the relationship:

Tpd- Min = - T/64

Tpd- Max = + 7 • T/512

Resolution = T/512

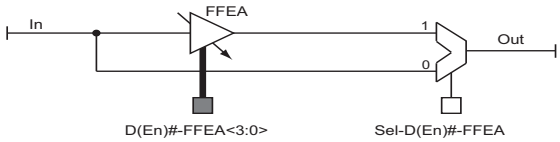


FIGURE 20.

FFEA may be bypassed via the CPU port. If bypassed, the circuitry powers down.

TABLE 35.

SEL-D(EN)#-FFEA	SIGNAL PATH
0	FFEA Bypassed and Powered Down
1	FFEA Invoked

TABLE 36.

PLL_CK	T = 6.4ns	T = 10ns
Tpd- (min)	-100ps	-156.25ps
Tpd- (max)	+87.5ps	+136.71875ps
Resolution	12.5ps	19.53125ps

TABLE 37.

FFEA<3:0>	ΔTpd-	ΔTpd-
0000	-100ps	-156.25ps
0001	-87.5ps	-136.71875ps
0010	-75ps	-117.1875ps
0011	-62.5ps	-97.65625ps
0100	-50ps	-78.125ps
0101	-37.5ps	-58.59375ps
0110	-25ps	-39.0625ps
0111	-12.5ps	-19.53125ps
1000	0ps	0ps
1001	+12.5ps	+19.53125ps
1010	+25ps	+39.0625ps
1011	+37.5ps	+58.59375ps
1100	+50ps	+78.125ps
1101	+62.5ps	+97.65625ps
1110	+75ps	+117.1875ps
1111	+87.5ps	+136.71875ps

COARSE FALLING EDGE ADJUST

CFEA offers a selection of 16 different falling edge adjustments as selected by the CPU port. The total range for CFEA is related to the PLL_CK period by the relationship:

Tpd- Min = - (1/4) • T

Tpd- Max = + (7/32) • T

Resolution = T/32

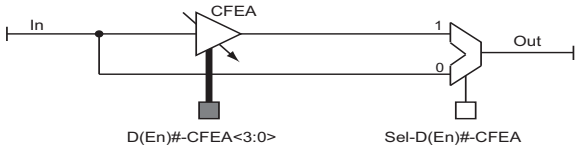


FIGURE 21.

CFEA may be bypassed via the CPU port. If bypassed, the circuitry powers down.

TABLE 38.

Sel-D(En)#-CFEA	SIGNAL PATH
0	CFEA Bypassed and Powered Down
1	CFEA Invoked

TABLE 39.

PLL_CK	T = 6.4ns	T = 10ns
Tpd- (min)	-1.6ns	-2.5ns
Tpd- (max)	+1.4ns	+2.1875ns
Resolution	200ps	312.5ps

TABLE 40.

CFEA<3:0>	ΔTpd-	ΔTpd-
0000	-1.6ns	-2.5ns
0001	-1.4ns	-2.1875ns
0010	-1.2ns	-1.875ns
0011	-1.0ns	-1.5625ns
0100	-800ps	-1.25ns
0101	-600ps	-937.5ps
0110	-400ps	-625ps
0111	-200ps	+312.5ps
1000	0ps	0ps
1001	+200ps	+312.5ps
1010	+400ps	+625ps
1011	+600ps	+937.5ps
1100	+800ps	+1.25ns
1101	+1.0ns	+1.5625ns
1110	+1.2ns	+1.875ns
1111	+1.4ns	+2.1875ns

Driver Output Control

The driver has 50Ω output impedance and supports four output states:

1. High level (DVH)
2. Low level (DVL)
3. Termination voltage VTT
4. High impedance

TABLE 41. DRIVER OUTPUT CONTROL

Dr-Mode#<1:0>	En#	Data#	Driver#	DOUT_#
X X	1	0	Active	DVL-#
X X	1	1	Active	DVH-#
0 0	0	X	HiZ	HiZ
0 1	0	X	Active	VTT
1 0	0	X	HiZ	Not Allowed
1 1	0	X	HiZ	Active Load

DATA AND ENABLE SOURCES

There are multiple sources for the driver data and enable inputs:

- Real time data and enable input pins
- Differential data and enable signals
- CPU port.

TABLE 42. DATA AND ENABLE SOURCES

Sel-D# Sel-En#	D#-Diag En#-Diag	Sel-D#-BP Sel-En#-BP	Sel-RT-D# Sel-RT-En#	Data Source Enable Source
X	X	X	0	CPU-D# CPU-En#
0	0	0	1	D# En#
0	X	1	1	D# En#
1	X	1	1	D(1-#) En(1-#)
X	1	0	1	Ring# Ring#

DIFFERENTIAL DRIVER

Both channels may be combined into one differential channel with the following steps:

1. Select the same D# and En # for both channels
2. Invert one channel's data signal by setting CPU-XOR# high.

Either channel's data and enable input may be selected to control the differential driver, and either channel may be defined as the true or inverting output.

High Impedance

There are two different high impedance modes:

1. Fast HiZ
2. Slow HiZ

FAST HIZ

Fast HiZ is used during high-speed functional test patterns when the driver is forcing DVH and DVL. In Fast HiZ, the driver maintains low leakage between VEE and VCC. For DOUT voltages more positive than VCC, the high-speed driver starts to turn on. Driver transition times going into and out of high impedance are

quicker and more accurate when the driver is in Fast HiZ mode than when in Slow HiZ mode.

It is acceptable and legal for the DUT to exceed VCC in Fast HiZ mode, but the DUT will see a 50Ω load to VCC + 1.25V, once that voltage is exceeded. No damage will be done to the driver.

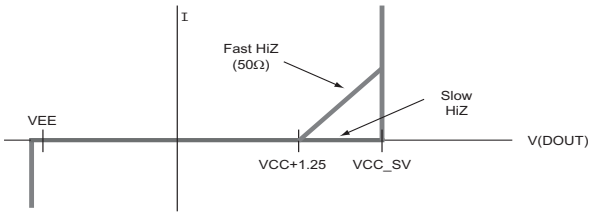


FIGURE 22.

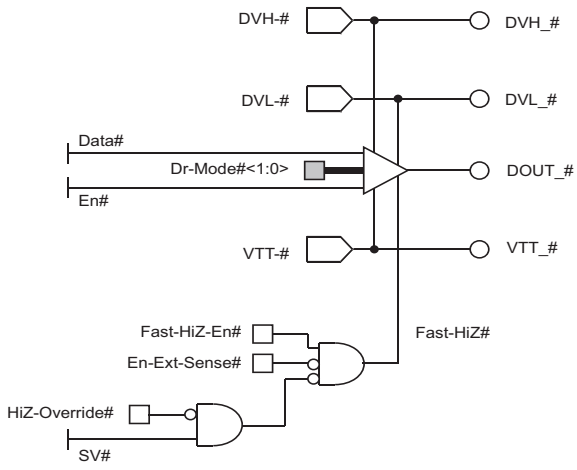


FIGURE 23.

SLOW HIZ

Slow HiZ is used primarily during wide voltage PPMU operation, and is the default mode upon power-up or reset. In Slow HiZ, the driver maintains a very low leakage when tracking any voltage between VEE and VCC_SV, and therefore the DOUT pin has a wider input compliance voltage range.

Slow HiZ is automatically selected any time the PPMU or external FET switches are enabled, unless overridden by the HiZ-Override function. In addition, this wider voltage mode may be forced by the CPU port setting, Fast-HiZ-En = 0. It may be desirable to force Slow HiZ when the Comparator is testing a large positive voltage in excess of VCC. In Slow HiZ, the driver functions the same as in Fast HiZ, but the driver transition times into and out of HiZ, as well as driver minimum pulse widths, will be slightly slower.

TABLE 43.

Fast-HiZ-En#	En-Ext-Sense#	SV#	HiZ-Override#	Channel # HiZ Mode
0	X	X	X	Slow HiZ
X	1	X	X	Slow HiZ
X	X	1	0	Slow HiZ
1	0	0	X	Fast HiZ
1	0	X	1	Fast HiZ

DRIVER LEVEL RESTRICTIONS IN HIZ AND PMU MODE

The ISL55161 driver levels (DVH, DVL, VTT) should be programmed to the midpoint between VCC_SV and VEE when in HiZ or PMU Mode.

Output Impedance

The driver is designed to maintain constant output impedance regardless of any changes due to:

- Ambient temperature
- Part-to-part variation

by tracking a precision and temperature compensated off-chip resistor (R_EXT) with a ratio of 204:1. Nominal conditions are:

- ..... R_EXT = 10.00kΩ
- .....Rout = 49Ω

Rout may be adjusted over a limited range by varying R_EXT.

OUTPUT IMPEDANCE ADJUSTMENTS

The driver tracks R_EXT equally for DVH, DVL, and VTT levels. However, it is possible to make fine adjustments to Rout for each drive level separately. This independent adjustment is useful for calibrating waveforms in precision applications. It can may be used to accommodate any transmission line impedance errors on a load board, as well as to adjust a characteristic in a waveform's DVH, DVL, or VTT performance, without affecting its characteristics when driving the other two levels.

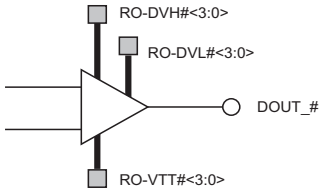


FIGURE 24.

Fine control is programmed through the CPU port and is normally set up before the execution of any real-time patterns. The default condition (Reset, Power up) is Radj = 0Ω.

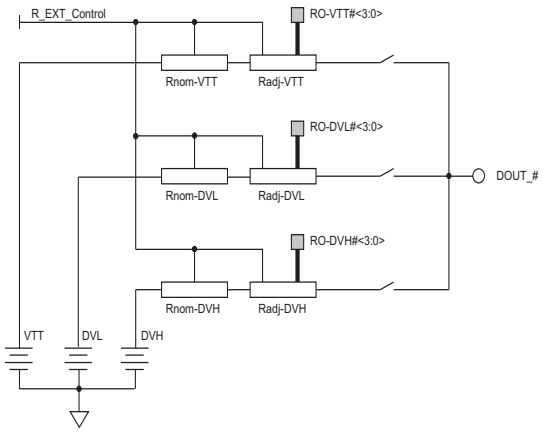


FIGURE 25.

FINE ADJUSTMENT RANGE

Each level has a fine adjustment range of ±10%, or ±5 for R_EXT = 10kΩ. The total output impedance of the driver is the nominal output impedance plus the fine adjustment.

- Rnom = R_EXT/204
- Radj Resolution = R_EXT/16,000
- Rout Max = Rnom + 7 * Radj Resolution
- Rout Min = Rnom – 8 * Radj Resolution

TABLE 44.

RO-DVH#<3:0> RO-DVL#<3:0> RO-VTT#<3:0>	DVH# ADJUST DVL# ADJUST VTT# ADJUST	DVH# ADJUST (%) DVL# ADJUST (%) VTT# ADJUST (%)
0111	+4.375Ω	+ 8.92
0110	+3.75Ω	+ 7.65
0101	+3.125Ω	+ 6.38
0100	+2.5Ω	+ 5.1
0011	+1.875Ω	+ 3.83
0010	+1.25Ω	+ 2.55
0001	+0.625Ω	+ 1.28
0000	0Ω	0
1111	-0.625Ω	- 1.28
1110	-1.25Ω	- 2.55
1101	-1.875Ω	- 3.83
1100	-2.5Ω	- 5.1
1011	-3.125Ω	- 6.38
1010	-3.75Ω	- 7.65
1001	-4.375Ω	- 8.92
1000	-5.0Ω	- 10.2

NOTE: The numbers in the table are based upon R_EXT = 10.0kΩ.

Active Load

Each channel has an active diode bridge load that may:

- Source up to 24mA
- Sink up to 24mA
- Be placed in a high impedance state

TABLE 45.

EN#	DR-MODE<0>	LOAD-EN#	CHANNEL # ACTIVE LOAD
1	X	0	HiZ
0	0	0	HiZ
0	1	1	Connected

Source and Sink Currents

The source and sink current levels are supplied by on-chip programmable current sources and may be programmed to different values.

TABLE 46.

I-Source-#<15:0>	Source Current	I-Sink#<15:0>	Sink Current
0000 Hex	0mA	0000 Hex	0mA
C000 Hex	24mA	C000 Hex	24mA
FFFF Hex	32mA	FFFF Hex	32mA

Resolution = 0.4883µA

The CPU port can independently adjust the source and sink currents slightly upward or downward.

TABLE 47.

SOURCE-ADJ#<2:0>	SINK-ADJ#<2:0>	I_{MAX}
000	000	Nominal
001	001	0.9 • Nominal
010	010	1.1 • Nominal
011	011	Not Allowed
100	100	Nominal
101	101	0.8 • Nominal
110	110	1.2 • Nominal
111	111	Not Allowed

Commutating Voltage

The on-chip DC level VTT-# is used to set the commutating voltage of the active load.

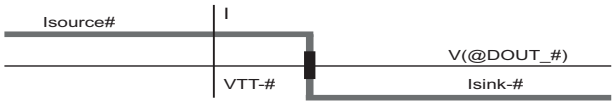


FIGURE 26.

Load Enable Sources

An active load is present and may be activated by:

- CPU port
- EN_# input

The active load and the VTT termination function are mutually exclusive in that the CPU sets up which resource is active when the driver goes into HiZ.

The active load is controlled by the signal:

Load-En# = En#* • Dr-Mode#<0>

If VTT mode is selected, I-Source-# and I-Sink-# are automatically programmed to 0mA.

Current Source Enable

The CPU port can override the programmed values of the source and sink currents (without changing the RAM value) and set them to 0. The default state upon power up and reset is 0.

TABLE 48.

DR-MODE#<1>	SOURCE CURRENT	SINK CURRENT
0	0	0
1	I-Source-#<15:0>	I-Sink-#<15:0>

For proper operation of the active load circuit when programming loads less than 3.2ma, the following is required:

1. Set the Isink/Isource current to the value of 3.2mA.
2. Set the Isink/Isource current to the intended lower value.

This procedure will ensure that the active load circuit is initialized and active for currents less than 3.2mA. During this process, the Ld-Ed# switch can either be in the opened or closed position. This is not necessary if the split load circuit has already been initialized with the above procedure and is programmed below 3.2mA.

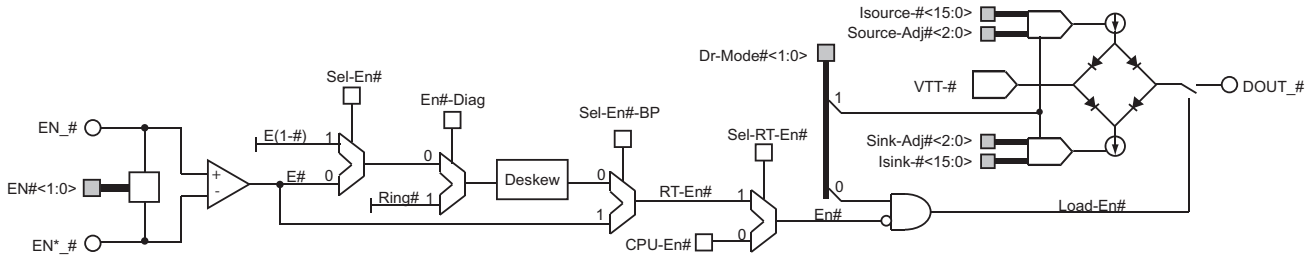


FIGURE 27.

Resistive Load/Super Voltage

The PMU may be connected and disconnected in real time under pattern control. This capability is useful in order to provide a resistive load or a fourth driver level.

TABLE 49.

SV#	PPMU# TO DOUT_#
0	Disconnected
1	Connected

Resistive Load Enable Sources

The resistive load may be activated by:

- CPU port
- EN_# input
- SV_# input.

TABLE 50.

SEL-SV#-EN	SEL-RT-SV#	SV#
X	0	CPU-SV#
0	1	SV_#
1	1	EN*_#

When the real-time enable signal is chosen for the SV# control line, the inverted enable signal is selected so the PMU becomes connected when the driver enters HiZ and becomes disconnected when the driver becomes active.

SV HOLD FUNCTION

The SV signal may be held at a constant level regardless of any real-time changes present at the SV_# pin.

TABLE 51.

HOLD-SV#	SV# SOURCE
0	Real Time SV_#
1	Latched State

HIGH IMPEDANCE

When disabled, the PMU maintains an extremely low leakage current when DOUT_# remains between the two analog supply levels VCC_SV and VEE.

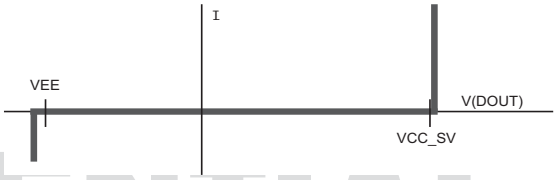


FIGURE 28.

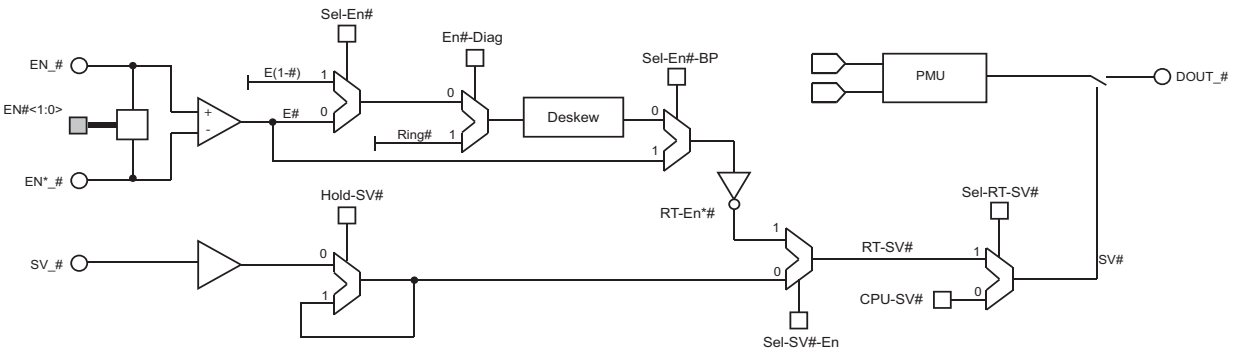
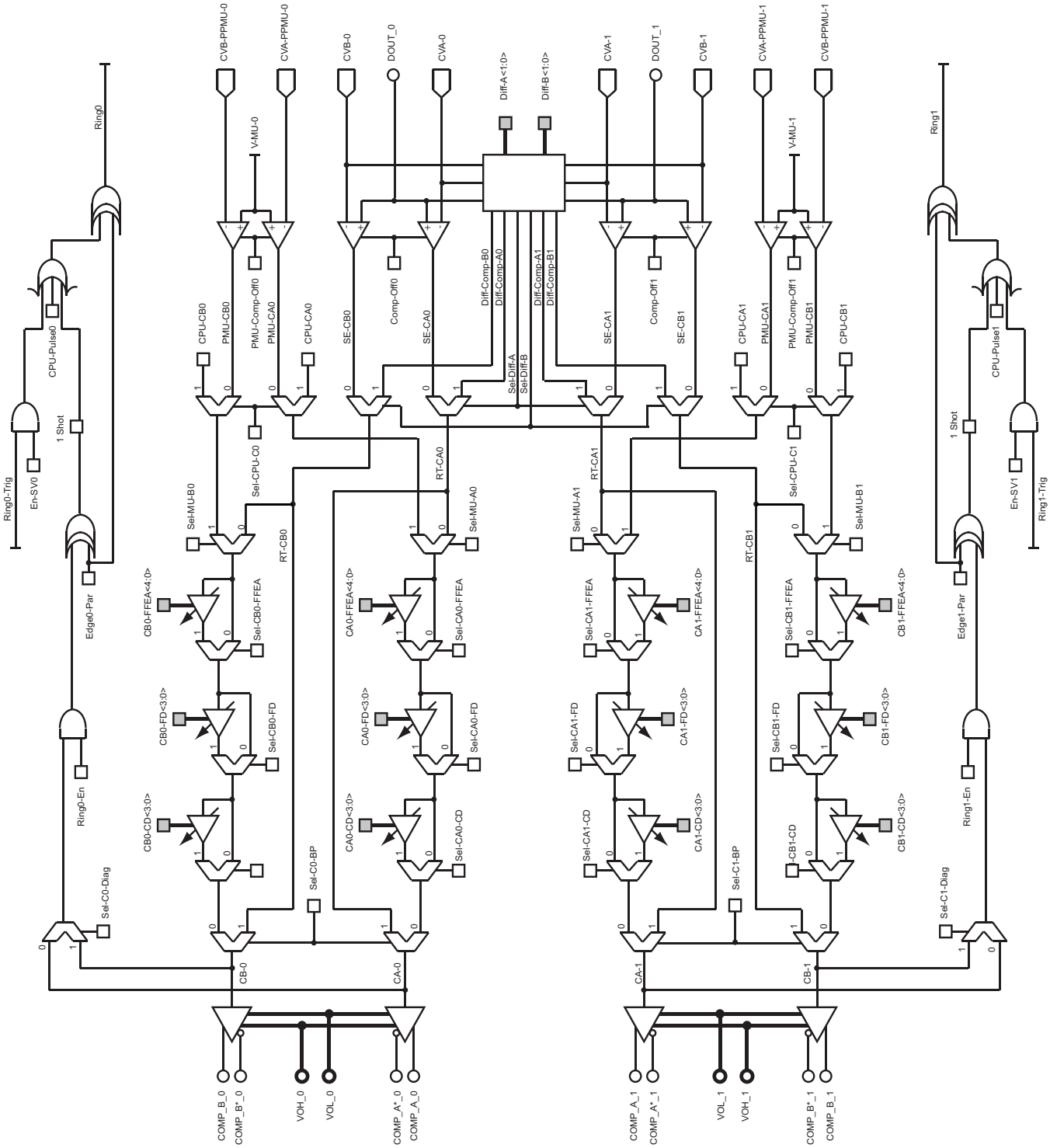


FIGURE 29.

Comparator

Detailed Block Diagram



Comparator Overview

Each channel supports two comparator output signals, COMP_A_# and COMP_B_#, that may be driven by a variety of signal sources:

- Functional comparators
- PMU comparators
- CPU port
- Differential common-mode comparators
- Differential differential-mode comparators

THRESHOLD GENERATION

The DC threshold reference levels per channel:

- ..... CVA-#, CVB-#
- ..... CVA-PPMU-#, CVB-PPMU-#

are independent on-chip DC levels programmed through the CPU port.

INTERNAL STATE READBACK

The internal nodes RT-CA#, RT-CB#, PMU-CA#, and PMU-CB# may be read back via the CPU port.

REAL-TIME COMPARATOR

The functional comparator is a high-speed window comparator with extremely low input leakage current when DOUT is between the power supply rails VEE and VCC_SV. It is normally selected for real-time functional testing of the Device Under Test.

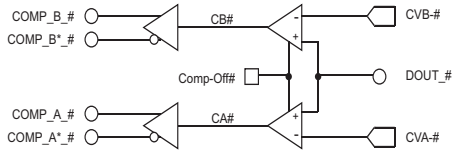


FIGURE 30.

Comparator Source Selection

The CPU port defines the differential comparator operating mode.

TABLE 52. COMPARATOR SOURCE SELECTION

Sel-C#-BP	Sel-Diff-A(B)	Sel-CPU-C#	Sel-MU-A(B)#	CA(B)# Source	Mode
0	X	0	1	PMU-CA(B)#	PMU
0	X	1	1	CPU-CA(B)#	CPU
0	0	X	0	SE-CA(B)#	Functional
0	1	X	0	Diff-CompA(B)#	Differential
1	0	X	X	SE-CA(B)#	Functional
1	1	X	X	Diff-CompA(B)#	Differential

REAL-TIME COMPARATOR POWER-DOWN

The CPU port can power-down the comparators to save power in applications where the window comparators are not used. When powered down, the quiescent power is reduced by ~270mW/channel.

TABLE 53. REAL-TIME COMPARATOR POWER-DOWN

COMP-OFF#	REAL-TIME WINDOW COMPARATOR
0	Active
1	Powered Down

When the real-time comparators are powered down, either the PMU comparator or the CPU port must be selected as the comparator signal path source in order for the comparator outputs to be in a defined state.

PMU COMPARATOR

The parametric measurement comparator is a window comparator with its input (V-MU) generated by the PPMU and is normally selected for parametric testing of the Device Under Test.

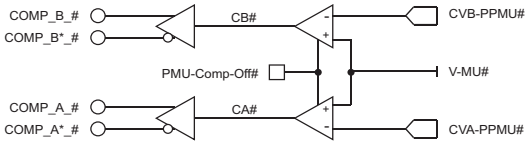


FIGURE 31.

This source selection is performed separately for comparators A and B of the same channel to allow both functional and parametric information to be simultaneously present at the real-time comparator outputs.

The CPU port can power-down the PMU comparators, reducing the quiescent power consumption by ~20mW/channel.

TABLE 54. PMU COMPARATOR

PMU-COMP-OFF	PMU COMPARATORS
0	Active
1	Powered Off

CPU COMPARATOR CONTROL

The CPU port can set the Comparator A and B status and override any real-time status from the measurement unit. This CPU control allows the comparator outputs to be placed in a known state, typically for diagnostic and debugging purposes within a tester.

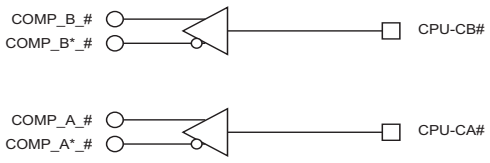


FIGURE 32.

Differential Comparator

The two channels may be combined into one differential comparator that tracks:

- Common mode voltage between DOUT_0 and DOUT_1.
- Differential voltage between DOUT_0 and DOUT_1.

TABLE 55. DIFFERENTIAL COMPARATOR

DIFF-A(B)<1:0>	COMPARATOR MODE
00	Single-Ended
01	Differential – Difference Mode 01
10	Differential – Difference Mode 10
11	Differential – Common Mode

COMMON MODE OPERATION

In common mode operation, the differential comparator tracks the sum of the two inputs.

- Diff-A<1:0> = 1,1
- Diff-B<1:0> = 1,1

TABLE 56.

INPUT CONDITION	DIFF-COMP-A
D0 + D1 < CVA-0 + CVA-1	0
D0 + D1 > CVA-0 + CVA-1	1

TABLE 57.

INPUT CONDITION	DIFF-COMP-B
D0 + D1 < CVB-0 + CVB-1	0
D0 + D1 > CVB-0 + CVB-1	1

Threshold Programming Rules

The effective thresholds for the differential comparators are established by the individual per channel references and follow Equations 1 and 2:

$$CVA-0 = CVA-1$$
$$\text{Effective Threshold} = 2 \bullet CVA-\# \quad \text{(EQ. 1)}$$

$$CVB-0 = CVB-1$$
$$\text{Effective Threshold} = 2 \bullet CVB-\# \quad \text{(EQ. 2)}$$

Channel Restrictions

Only one channel of Diff-Comp-A and Diff-Comp-B may be calibrated. The other channel is not recommended for use.

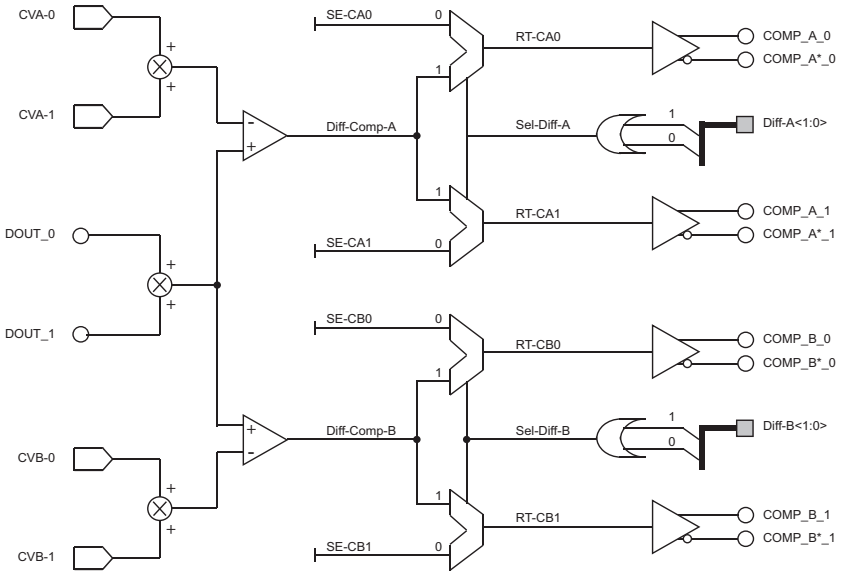


FIGURE 33. DIFFERENTIAL COMPARATOR - COMMON MODE

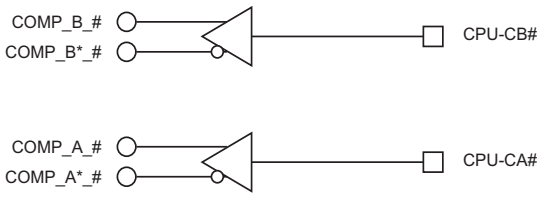


FIGURE 34.

Difference Mode 01 Operation

In difference mode operation, the differential comparator tracks the difference between the two inputs.

- Diff-A<1:0> = 0,1
- Diff-B<1:0> = 0,1

TABLE 58.

INPUT CONDITION	DIFF-COMP-A0
D0 - D1 < CVA-0 - CVA-1	0
D0 - D1 > CVA-0 - CVA-1	1

TABLE 59.

INPUT CONDITION	DIFF-COMP-A1
D1 – D0 < CVA-1 - CVA-0	0
D1 – D0 > CVA-1 - CVA-0	1

TABLE 60.

INPUT CONDITION	DIFF-COMP-B0
D0 - D1 < CVB-0 - CVB-1	0
D0 - D1 > CVB-0 - CVB-1	1

TABLE 61.

INPUT CONDITION	DIFF-COMP-B1
D1 – D0 < CVB-1 - CVB-0	0
D1 – D0 > CVB-1 - CVB-0	1

Threshold Programming Rules

The effective thresholds for the differential comparators are established by the individual per channel references and follow Equations 3 and 4:

$$CVA(B) - 0 = VCM - (V_{DIFF}/2) \quad \text{(EQ. 3)}$$

$$CVA(B) - 1 = VCM + (V_{DIFF}/2) \quad \text{(EQ. 4)}$$

- VCM = Expected common mode crossing point of the input.
- Vdiff = Desired effective differential threshold level.

Channel Restrictions

Only one channel of Diff-Comp-A and Diff-Comp-B may be calibrated. The other channel is not recommended for use.

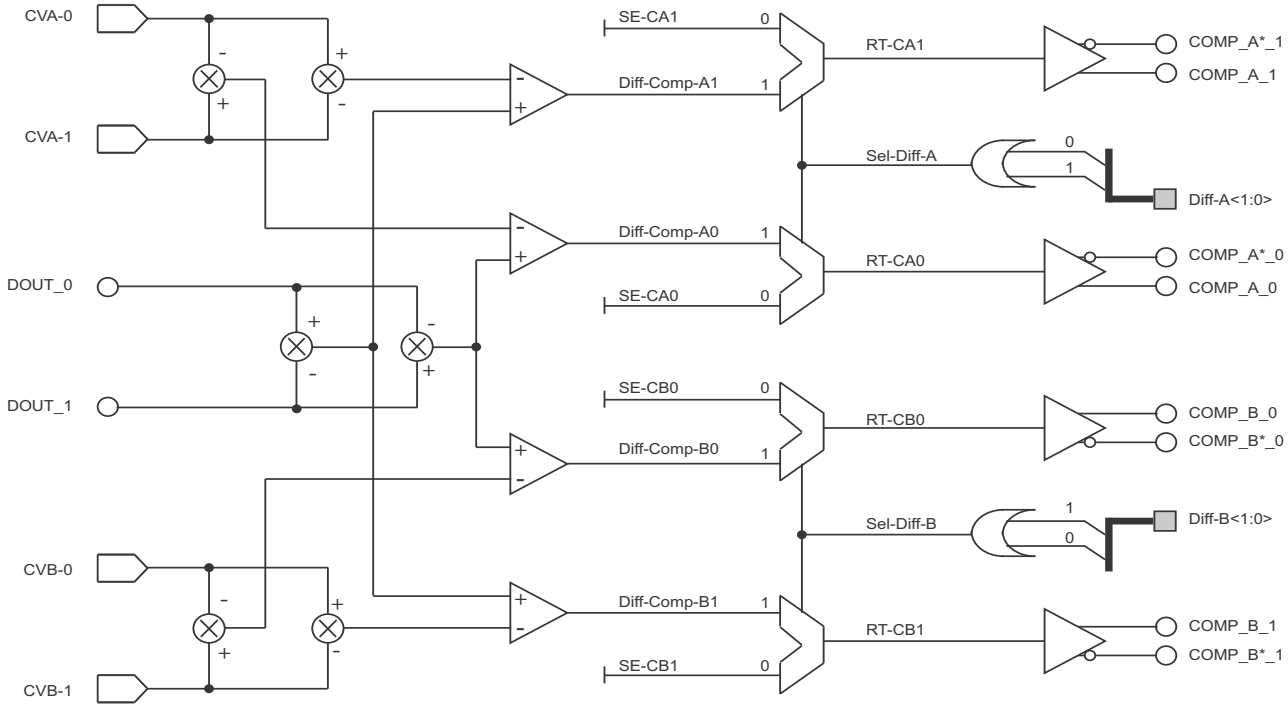


FIGURE 35. DIFFERENTIAL COMPARATOR - DIFFERENCE MODE

DIFFERENCE MODE 10 OPERATION

In difference mode operation, the differential comparator tracks the difference between the two inputs.

- Diff-A<1:0> = 1,0
- Diff-B<1:0> = 1,0

TABLE 62.

INPUT CONDITION	DIFF-COMP-A0
D1 – D0 < CVA-1 - CVA-0	0
D1 – D0 > CVA-1 - CVA-0	1

TABLE 63.

INPUT CONDITION	DIFF-COMP-A1
D0 – D1 < CVA-0 - CVA-1	0
D0 – D1 > CVA-0 - CVA-1	1

TABLE 64.

INPUT CONDITION	DIFF-COMP-B0
D1 – D0 < CVB-1 - CVB-0	0
D1 – D0 > CVB-1 - CVB-0	1

TABLE 65.

INPUT CONDITION	DIFF-COMP-B1
D0 – D1 < CVB-0 - CVB-1	0
D0 – D1 > CVB-0 - CVB-1	1

Threshold Programming Rules

The effective thresholds for the differential comparators are established by the individual per channel references and follow Equations 5 and 6:

$$CVA(B) - 0 = VCM + (V_{DIFF}/2) \quad \text{(EQ. 5)}$$

$$CVA(B) - 1 = VCM - (V_{DIFF}/2) \quad \text{(EQ. 6)}$$

- VCM = Expected common mode crossing point of the input.
- Vdiff = Desired effective differential threshold level.

Channel Restrictions

Only one channel of Diff-Comp-A and Diff-Comp-B may be calibrated. The other channel is not recommended for use.

Deskew

Each channel's COMP_A and COMP_B outputs have timing adjustment capability with the following characteristics:

- Separate and independent delay circuitry for the COMP_A and COMP_B paths.
- Separate and independent delay circuitry for Channel 1 and Channel 2.
- Propagation delay adjust (both rising (Tpd+) and falling (Tpd-) edge are delayed equally).
- Falling edge adjust (FEA) (falling edge may be adjusted, rising edge Tpd remains constant).
- Timing delay range and resolution established by an external frequency.
- If bypassed, the delay element shuts down and consumes no power.

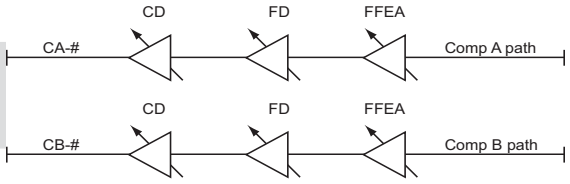


FIGURE 36.

Propagation Delay Adjust

The propagation delay circuitry adds timing delay to the rising edge (Tpd+) and the falling edge (Tpd-) in equal amounts. Propagation delay adjustment is typically used for aligning the timing of multiple channels inside a tester.

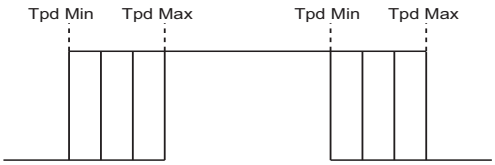


FIGURE 37.

The delay circuitry is divided into two separate blocks:

- Coarse Delay
- Fine Delay

Propagation Delay Falling Edge Adjust

The falling edge delay circuitry adds or subtracts timing delay to or from the falling edge (Tpd-) while having no effect on the rising edge (Tpd+). Propagation delay adjustment is typically used for removing any pulse width distortion inside a tester.

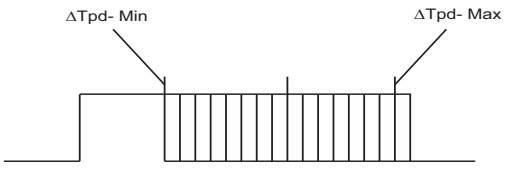


FIGURE 38.

BYPASS MODE

The deskew elements may be bypassed, resulting in the shortest Tpd and the highest bandwidth configuration. When set high, this bit will slightly lower the power by ~30mW per channel.

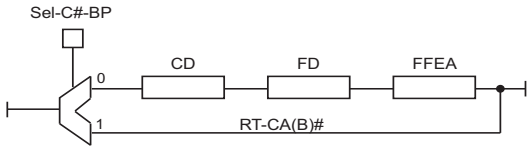


FIGURE 39.

TABLE 66.

SEL-C#-BP	COMPARATOR PATH
0	Deskew Elements in Signal Path
1	Deskew Elements Bypassed

COARSE DELAY

Coarse delay divides the overall delay range (established by the period of PLL_CK) into equal segments, and then selects one of those delays.

- Tspan (CD) = (15/32) • T
- Resolution = T/32

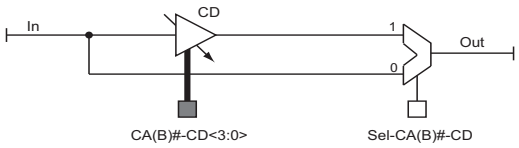


FIGURE 40.

Coarse delay is programmed by the CPU port and may be bypassed. If bypassed, the circuitry powers down.

TABLE 67.

SEL-CA(B)#-CD	SIGNAL PATH
0	CD Bypassed and Powered Down
1	CD Invoked

TABLE 68.

PLL_CK	T = 6.4ns	T = 10ns
Tspan	3.0ns	4.6875ns
Resolution	200ps	312.5ps

TABLE 69.

CA(B)#-CD<3:0>	ΔTpd±	ΔTpd±
0000	0ps	0ps
0001	+200ps	+312.5ps
0010	+400ps	+625ps
0011	+600ps	+937.5ps
0100	+800ps	+1.25ns
0101	+1.0ns	+1.5625ns
0110	+1.2ns	+1.875ns

TABLE 69. (Continued)

CA(B)#-CD<3:0>	ΔTpd±	ΔTpd±
0111	+1.4ns	+2.1875ns
1000	+1.6ns	+2.5ns
1001	+1.8ns	+2.8125ns
1010	+2.0ns	+3.125ns
1011	+2.2ns	+3.4375ns
1100	+2.4ns	+3.75ns
1101	+2.6ns	+4.0625ns
1110	+2.8ns	+4.375ns
1111	+3.0ns	+4.6875ns

FINE DELAY

Fine delay adjust makes very small corrections to Tpd+ and Tpd- and affects both rising and falling edges equally. FD allows edge placement between coarse delay LSB steps.

- Tspan (FD) = 15 • T/512
- Resolution = T/512

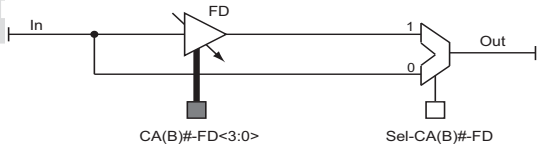


FIGURE 41.

Fine delay is programmed by the CPU port and may be bypassed. If bypassed, the circuitry powers down.

TABLE 70.

SEL-CA(B)#-FD	SIGNAL PATH
0	FD Bypassed and Powered Down
1	FD Invoked

TABLE 71.

PLL_CK	T = 6.4ns	T = 10ns
Tspan	187.5ps	292.96875ps
Resolution	12.5ps	19.53125ps

TABLE 72.

FD<3:0>	ΔTpd±	ΔTpd±
0000	0ps	0ps
0001	+12.5ps	+19.53125ps
0010	+25ps	+39.0625ps
•	•	•
•	•	•
1101	+162.5ps	+253.90625ps
1110	+175ps	+273.4375ps
1111	+187.5ps	+292.96875ps

FINE FALLING EDGE ADJUST

FFEA offers a selection of 32 different falling edge adjustments as selected by the CPU port. The total range for FFEA is related to the PLL_CK period by the relationship:

- Tpd- Min = - T/64
- Tpd- Max = + 15 • T/1024
- Resolution = T/1024.

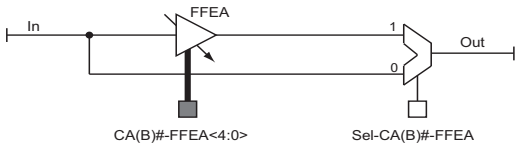


FIGURE 42.

FFEA may be bypassed via the CPU port. If bypassed, the circuitry powers down.

TABLE 73.

SEL-CA(B)#-FFEA	SIGNAL PATH
0	FFEA Bypassed and Powered Down
1	FFEA Invoked

FIGURE 43.

TABLE 74.

PLL_CK	T = 6.4ns	T = 10ns
Tpd- (min)	-100ps	-156.25ps
Tpd- (max)	+93.7ps	+146.5ps
Resolution	6.25ps	9.76ps

TABLE 75.

CA(B)#-FFEA<4:0>	ΔTpd-	ΔTpd-
00000	-100ps	-156.25ps
00001	-93.74ps	-146.5ps
00010	-87.5ps	-136.7ps
00011	-81.25ps	-127ps
00100	-75ps	-117.2ps
00101	-68.75ps	-107.4ps
00110	-62.5ps	-97.7ps
00111	-56.25ps	-87.9ps
01000	-50ps	-78.125ps
01001	-43.75ps	-68.36ps
01010	-37.5ps	-58.6ps
01011	-31.25ps	-48.8ps
01100	-25ps	-39ps

TABLE 75. (Continued)

CA(B)#-FFEA<4:0>	ΔTpd-	ΔTpd-
01101	-18.75ps	-29.3ps
01110	-12.5ps	-19.53ps
01111	-6.25ps	-9.76ps
10000	0	0
10001	+6.25ps	+9.76ps
10010	+12.5ps	+19.53ps
10011	+18.75ps	+29.3ps
10100	+25ps	+39ps
10101	+31.25ps	+48.8ps
10110	+37.5ps	+58.6ps
10111	+43.75ps	+68.36ps
11000	+50ps	+78.125ps
11001	+56.25ps	+87.9ps
11010	+62.5ps	+97.7ps
11011	+68.75ps	+107.4ps
11100	+75ps	+117.2ps
11101	+81.25ps	+127ps
11110	+87.5ps	+136.7ps
11111	+93.74ps	+146.5ps

Output Stage

Each channel supports two comparator outputs with the following characteristics:

- Differential outputs
- 50Ω series terminated outputs
- Programmable high and low levels
- Separate high and low levels per channel.

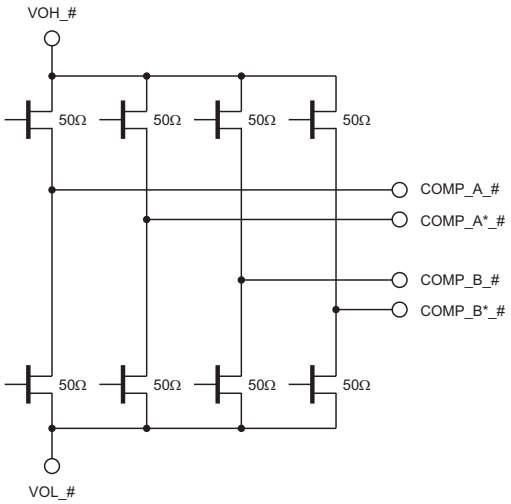


FIGURE 44.

COMPARATOR OUTPUT SUPPLY LEVELS

VOH_# and VOL_# are power supply inputs that set the high and low level of each channel. There are no restrictions between the two channels. VOH_# and VOL_# provide the current required to drive the off-chip transmission line and any DC current associated with any termination used. Therefore, these voltage inputs should be driven by a low impedance and low inductance source with ample current drive.

SOURCE TERMINATION

No external components are required, and full amplitude at the destination is achieved with source termination.

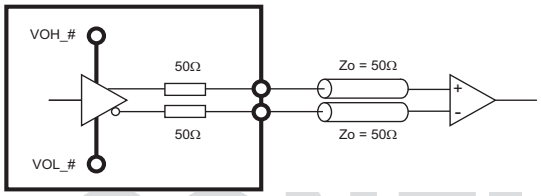


FIGURE 45.

SOURCE AND DESTINATION (DOUBLE) TERMINATION

One external component is required and one half the signal amplitude is realized at the destination with double termination.

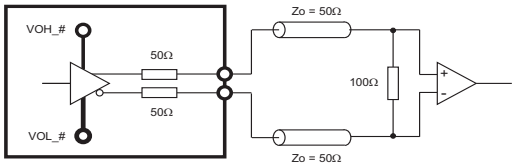
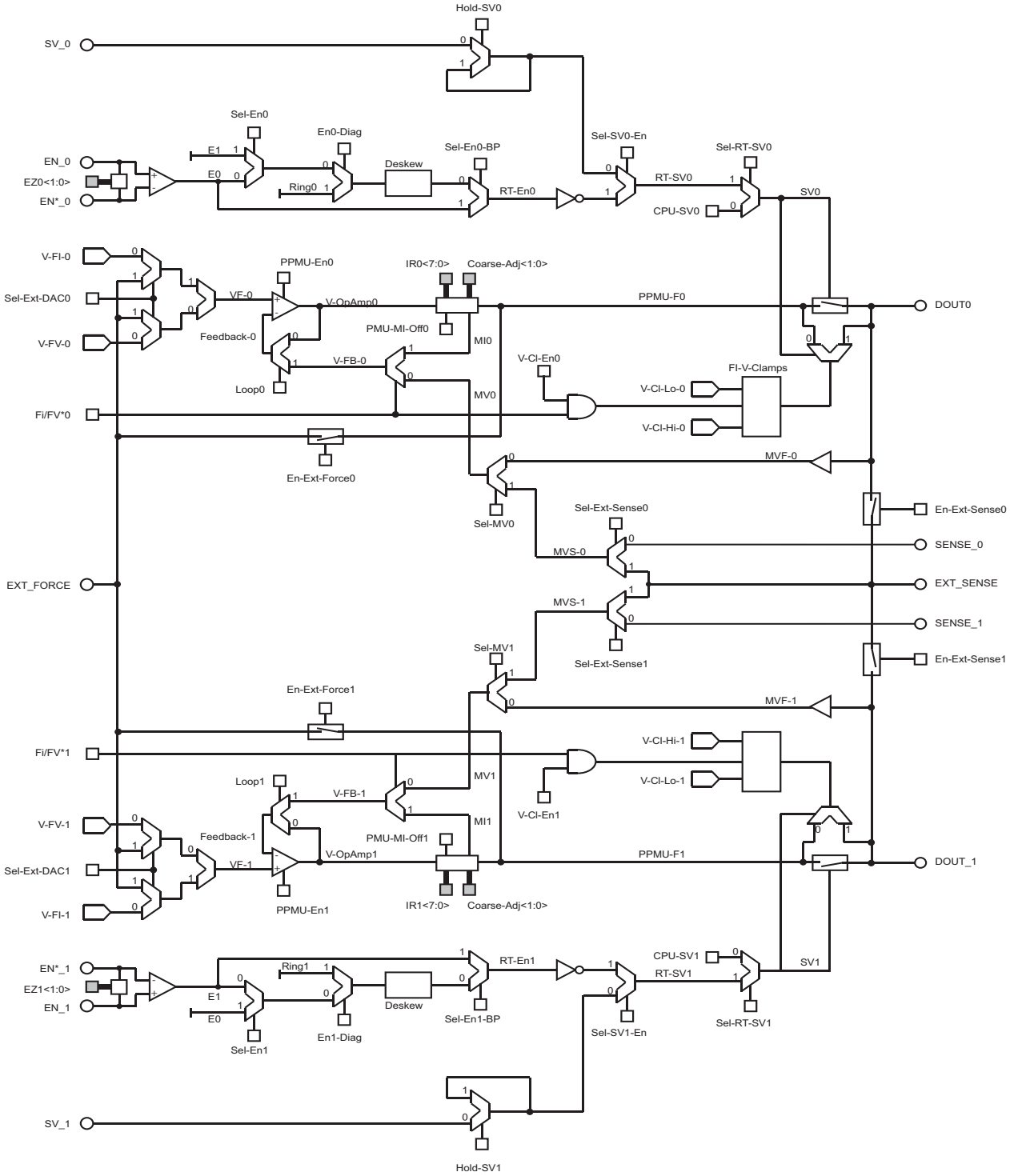


FIGURE 46.

PMU

Detailed Block Diagram



PMU Overview

Each channel has a per-pin parametric measurement unit with the ability to:

- Force Current (FI)
- Force Voltage (FV)
- Measure Current (MI)
- Measure Voltage (MI)

The current or voltage measured may be tested via two different mechanisms:

- On-board PMU window comparator
- MONITOR analog output voltage

High Impedance

The forcing op amp may be placed into a HiZ state, although care should be exercised when doing this due to the large transient response possible when turning the op amp back on.

TABLE 76.

PPMU-EN#	CH # FORCING OP AMP STATUS
0	HiZ
1	Active

Setting PPMU-En# to 0 powers off the forcing op amp and reduces quiescent power consumption by ~16mW/channel. However, the recommended PMU HiZ function is through the SV switch.

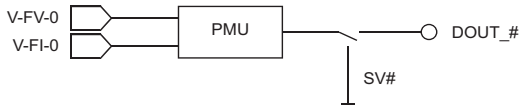


FIGURE 47.

TABLE 77.

SV#	Ch # PMU
0	HiZ
1	Active

When disabled through the SV Switch, the PMU maintains an extremely low leakage current when DOUT_# remains between the two analog supply levels, VCC_SV and VEE.

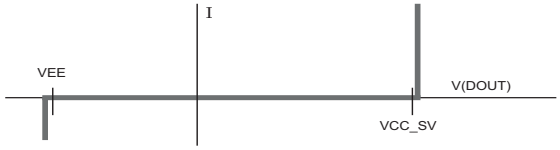


FIGURE 48.

PMU OPERATING MODE

The decision whether to force current or voltage, or to measure current or voltage, is controlled by the CPU port. There are no restrictions between FI/FV* and MI/MV* in that all combinations are legal modes.

TABLE 78.

FI/FV*#	CH # FORCE FUNCTION
0	FV#
1	FI#

TABLE 79.

MI/MV*#	CH # MEASURE FUNCTION
0	MVF-#
1	MI#

MI Power-down

The CPU port can power-down the measure current amplifier, reducing the quiescent power consumption by ~24mW/channel.

TABLE 80.

PMU-MI-OFF#	MI AMPLIFIER
0	Active
1	Powered Down

Current Force

FI mode has the following transfer function translating the voltage input to a current output.

TABLE 81.

V-FI	CURRENT AT DOUT
-1V	-Imax
0V	0
+1V	+Imax

Current Ranges

The PMU can force current up to a maximum of 32mA. In order to achieve the maximum accuracy while measuring smaller currents, eight current ranges are supported.

TABLE 82.

IR#<7:0>	CURRENT RANGE	IMAX	RSENSE
00000001	IR0	2µA	500kΩ
00000010	IR1	8µA	125kΩ
00000100	IR2	32µA	31.25kΩ
00001000	IR3	128µA	7.81kΩ
00010000	IR4	512µA	1.95kΩ
00100000	IR5	2mA	500Ω
01000000	IR6	8mA	125Ω
10000000	IR7	32mA	31.25Ω

The CPU selects the current range by setting the range select bit high. Each range select bit is independent in that it is possible to select more than one range simultaneously. However, this option should be used only when changing ranges as a means of

controlling the transient response associated with a range change.

It is not recommended that more than one range be active at the same time when taking a measurement.

Coarse Gain Adjust

Prior to any DC calibration, the FI and MI gain may be adjusted upward or downward. This coarse adjustment is useful to center the transfer function to guarantee that full-scale current can be met. Coarse Gain Adjust affects both the FI and the MI gain and corresponding transfer functions.

TABLE 83.

COARSE-ADJ#<1:0>	I_{MAX}
00	Nominal
01	Nominal
10	0.92 • Nominal
11	1.08 • Nominal

FI Voltage Clamps

Each PMU has a set of programmable voltage clamps that limit the voltage swing at forcing op amp feedback voltage (V-FB) when the PMU is forcing current. These clamps protect the DUT when current is being forced into a high impedance node at the DUT.

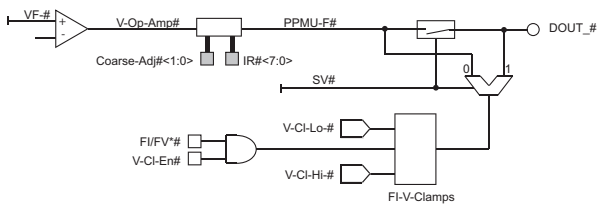


FIGURE 49.

The clamps may be turned off by setting Cl-En = 0, in which case the clamps have no effect while DOUT varies between the supply voltages, VCC-SV and VEE.

TABLE 84.

V-CL-EN#	V-FB	CH # CLAMPS
0	X	Not Active
1	V-FB > V-Cl-Hi	DOUT = V-Cl-Hi
1	V-FB < V-Cl-Lo	DOUT = V-Cl-Lo
1	V-Cl-Lo < V-FB < V-Cl-Hi	Not Active

If the sensed voltage exceeds the high or low voltage clamp, the PMU reduces the output current in order for the output voltage to not exceed the clamp. If the voltage subsequently returns back to within the clamp thresholds, the PMU resumes forcing the programmed current.

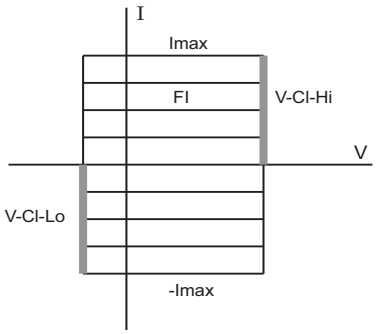


FIGURE 50.

LOCAL SENSE

Local sense changes the voltage clamp sense point automatically whenever the real-time PMU switch is open, to guarantee that the voltage clamps do not false-activate whenever the switch is opened.

Voltage Force

In FV mode, the source of the forced voltage may be selected from either on-chip DC level V-FV or the voltage on the EXT_FORCE pin.

TABLE 85.

SEL-EXT-DAC#	CH # FV SOURCE	DOUT_#
0	V-FV-#	V-FV-#
1	EXT_FORCE	EXT_FORCE

FEEDBACK OPTIONS

When forcing a voltage, the PMU has a variety of configurations with different voltage feedback points:

- Forcing op amp output
- PMU force node
- DOUT_#
- SENSE
- EXT_SENSE

TABLE 86.

Loop#	FI/FV*#	Sel-MV#	Sel-Ext-Sense#	Mode	Feedback#
0	X	X	X	FV	V Op Amp#
1	1	X	X	FI	MI#
1	0	0	X	FV	MVF-#
1	0	1	0	FV	SENSE_#
1	0	1	1	FV	EXT_SENSE

REMOTE SENSE

Selecting the SENSE pin allows for more accurate FV operation.

TIGHT LOOP OPTION

With Loop = 0, the forcing op amp will be configured as a unity gain amplifier tracking either V-FV or V-FI. This tight loop is the default condition upon reset or power-up.

The tight loop configuration is NOT used for any traditional PMU FI or FV function. It is used mainly for:

- A stable default condition
- Resistive load applications
- Super voltage applications

Real-time PMU Control

The PMU may be connected and disconnected in real time under pattern control in order to provide a resistive load or a fourth driver level.

TABLE 87.

SV#	PMU# TO DOUT_#
0	Disconnected
1	Connected

Resistive Load Enable Sources

The resistive load may be activated by:

- CPU port
- EN_# input
- SV_# input

TABLE 88.

SEL-SV#-EN	SEL-RT-SV#	SV#
X	0	CPU-SV#
0	1	RT-En*#
1	1	SV_#

When the real-time enable signal is chosen for the SV# control line, the inverted enable signal is selected so the PMU becomes connected when the driver enters HiZ and becomes disconnected when the driver becomes active.

Measurement Unit

The measurement unit is the circuitry which translates the voltage or the current being sensed into an output voltage (V-MU-#) that can be measured or compared against an upper and lower limit. In addition to measuring the voltage or current at a channel's DOUT pin, the measurement unit may also monitor the V-MU from the other channel or a variety of internal test nodes.

TABLE 89.

SEL-MU#	SEL-MU#-DIAG	MI/MV*#	V-MU-#
1	X	X	V-Sense-(1-#)
0	1	X	Test & Cal-#
0	0	0	MV#
0	0	1	MI#

An on-chip window comparator supports a 2-bit "go/no-go" test. V-MU is the input voltage to the comparators, and the thresholds are set via on-chip DC level generators through the CPU port. The window comparator outputs PPMU-CA, and PPMU-CB may be read back directly through the CPU port, providing direct access to the actual comparator status at any time, or they may be routed off chip through the COMP_A and COMP_B pins.

Current Measure

When MI/MV* = 1, V-Sense will be an analog voltage that is proportional to the current flowing through DOUT. Imax is determined by the current range selection.

TABLE 90.

V-SENSE	I_{OUT}
-1V	-Imax
0V	0
+1V	+Imax

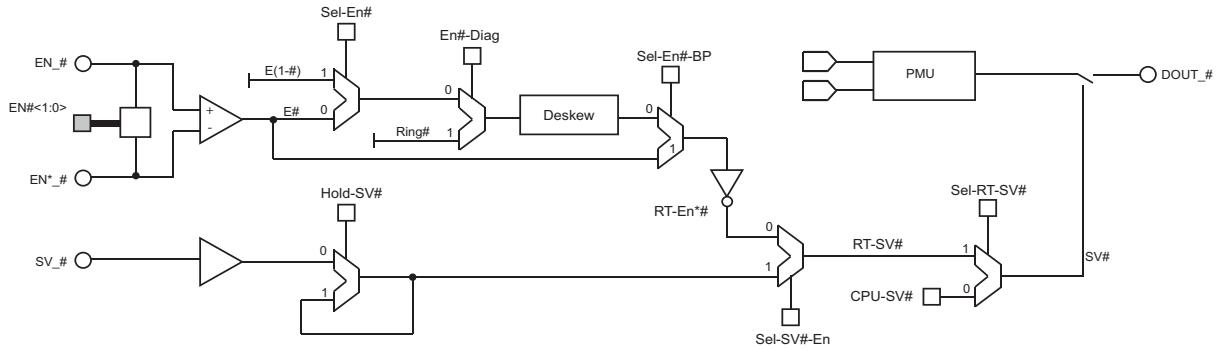


FIGURE 51.

Prior to any DC calibration, the gain of the MI transfer function may be adjusted upward or downward. This function is described in the FI section.

Voltage Measure

When MI/MV* = 0, V-Sense will be an analog voltage equal to the voltage present at MV#.

V-Sense-# = MV#

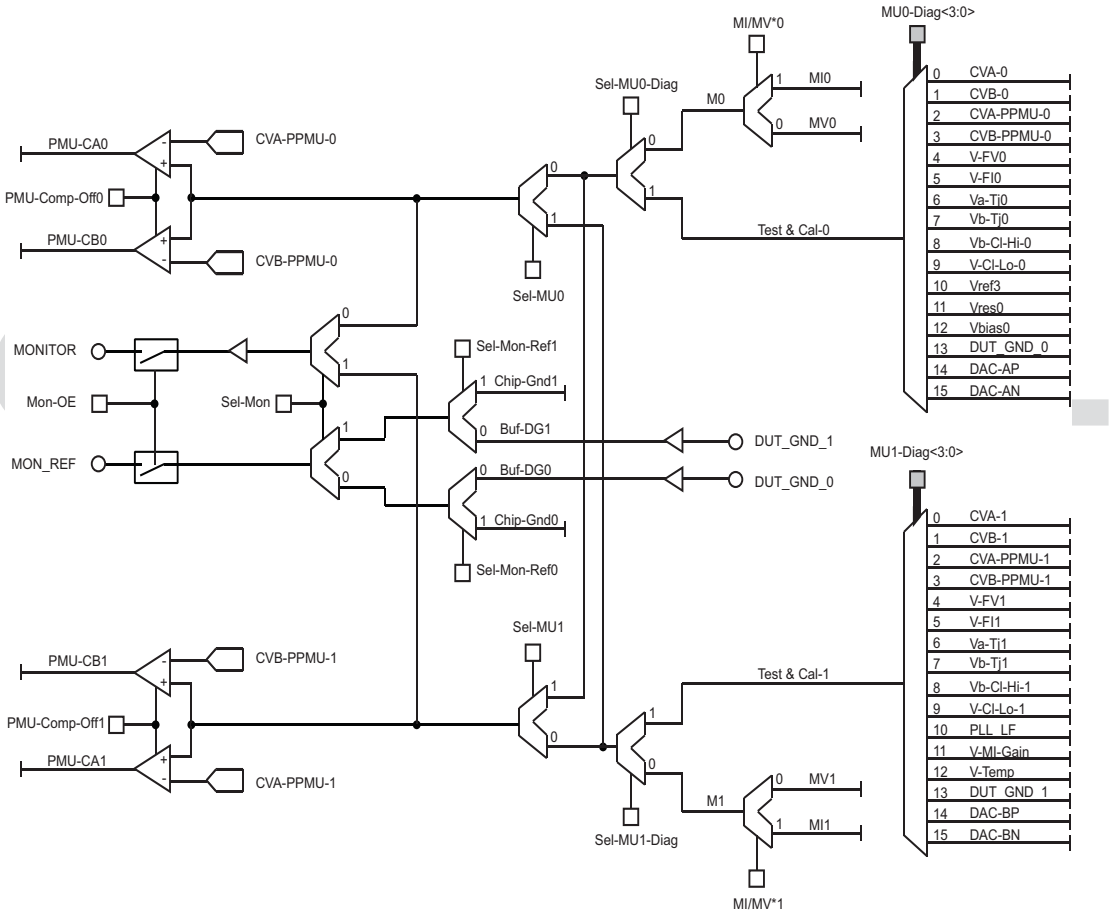


FIGURE 52. MEASUREMENT UNIT

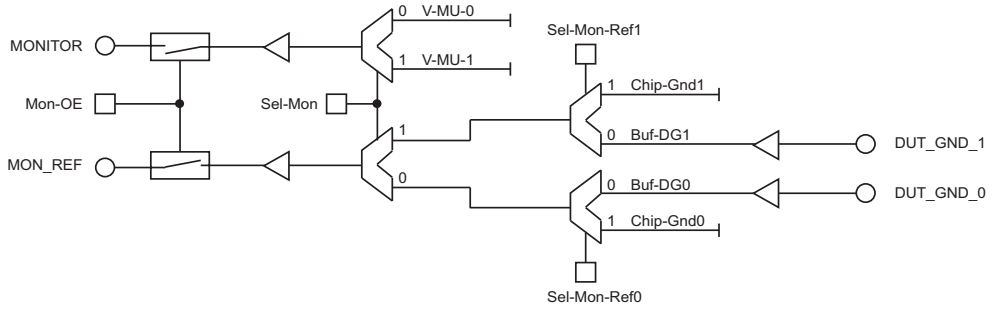


FIGURE 53.

MONITOR

MONITOR_# is an analog voltage output whose voltage source is the measurement unit output from either channel (V-MU-0 or V-MU-1).

MONITOR TRANSFER FUNCTION

When measuring voltage, MONITOR_# has a 1:1 transfer function with DOUT. When measuring current, MONITOR_# varies between –1V and +1V for –Imax and +Imax.

TABLE 91.

MODE	MONITOR	DOUT
MV	Voltage at DOUT	DOUT
MI	-1V	-Imax
MI	0V	0
MI	+1V	+Imax

MONITOR REFERENCE

MON_REF is a reference signal used as the inverting input to a differential off-chip ADC. The CPU port selects the reference signal as well as controls the high impedance function.

TABLE 92.

SEL-MON-REF#	MON-REF#
0	Buf-DG#
1	Chip-Gnd#

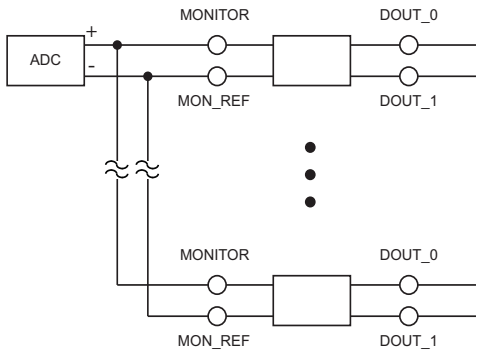


FIGURE 54.

MONITOR HIGH IMPEDANCE

The monitor outputs may be placed into a high impedance state. This HiZ feature is useful when connecting multiple MONITOR pins from multiple ICs to one A to D converter.

TABLE 93.

MON-OE	SEL-MON	MONITOR	MON-REF
0	X	HiZ	HiZ
1	0	V-MU-0	Mon-Ref0
1	1	V-MU-1	Mon-Ref1

Resistive Load

The PMU may be configured as a resistive load that acts like a selectable resistor to a programmable voltage level.

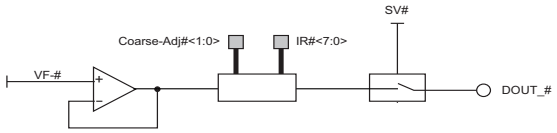


FIGURE 55.

LOAD VOLTAGE

To establish the load voltage source, select V-FV, program it to the desired voltage level and set Loop = 0. In this configuration the forcing op amp will be a low impedance voltage source.

- FI/$\overline{FV}$ = 0 (FV mode)
- V-FV = Desired Load Voltage
- Loop = 0 (Tight Loop)

LOAD RESISTOR

The resistance between the load voltage and DOUT will be the series combination of the sense resistor inside the PMU and the on resistance of the real time super voltage controlled isolation switch.

$$Rload = Rsense + R(SV\ Switch) \quad \text{(EQ. 7)}$$

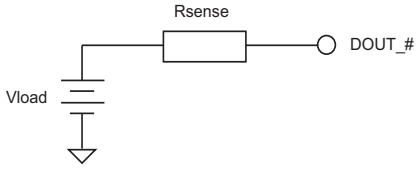


FIGURE 56.

RSENSE

The value of the sense resistor is determined by the current range selection.

TABLE 94.

IR#<7:0>	CURRENT RANGE	I_{MAX}	R_{SENSE}
00000001	IR0	2µA	500kΩ
00000010	IR1	8µA	125kΩ
00000100	IR2	32µA	31.25kΩ
00001000	IR3	128µA	7.81kΩ
00010000	IR4	512µA	1.95kΩ
00100000	IR5	2mA	500Ω
01000000	IR6	8mA	125Ω
10000000	IR7	32mA	31.25Ω

HIZ FORCE

HiZ force uses a similar configuration as does the resistive load. However, in this case, the PMU is placed into a low current mode (high Rsense value) and is connected whenever the driver goes into HiZ. The PMU will pull the transmission line between the pin electronics and the DUT to a known and programmed state, rather than letting it float.

Temperature Sensing

Each channel has its own independent temperature sense capability. There are two internal voltages:

- Va-Tj
- Vb-Tj

When measured, these may be used to calculate the junction temperature associated with each channel, as shown in Equation 8.

$$T_J[°C] = \{(V_A - T_J) - (V_B - T_J) \bullet 1637\} - 221 \quad \text{(EQ. 8)}$$

TEMPERATURE MONITOR

V-Temp is an analog voltage that tracks the junction temperature.

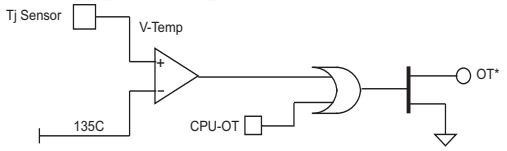


FIGURE 57.

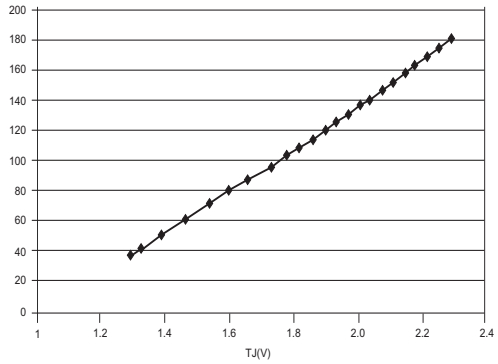


FIGURE 58. TJ TRANSFER FUNCTION

OT* is an open drain output that indicates when the junction temperature exceeds 135°C. The CPU port can directly force the over-temperature flag to be active.

TABLE 95.

CPU-OT	JUNCTION TEMPERATURE	$\overline{OT*}$
0	V-Temp < +135°C	HiZ
0	V-Temp > +135°C	Active. 100Ω to ground
1	X	Active. 100Ω to ground

Diagnostics

Each PMU has access to key internal nodes so that the voltage on these nodes may be monitored. This access is useful for both testing and diagnostic purposes. The CPU port controls the access to the diagnostic nodes.

TABLE 96.

SEL-MU#-DIAG	MI/$\overline{MV*}$#	V-SENSE-#
0	0	MVF-#
0	1	MI#
1	X	Test & Cal-#

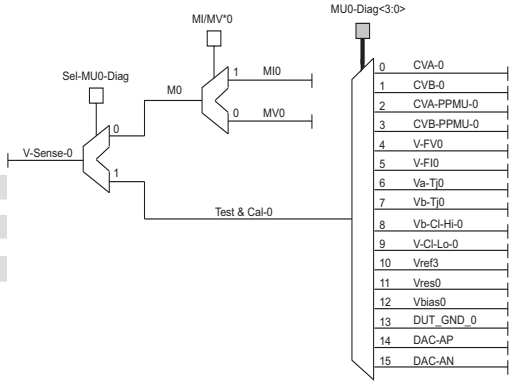


FIGURE 59. CHANNEL 0 DIAGNOSTIC SELECTION

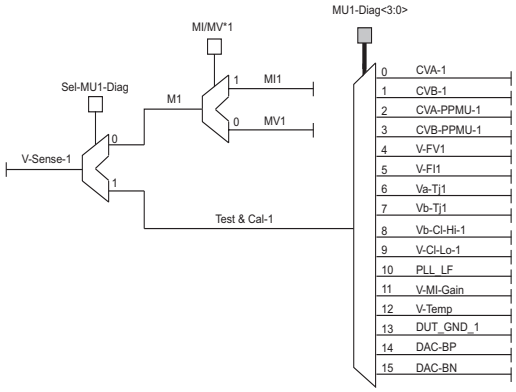


FIGURE 60. CHANNEL 1 DIAGNOSTIC SELECTION

External Force and Sense

EXT_FORCE and EXT_SENSE may be directly connected to either DOUT_0 or DOUT_1 or to each other. These paths are useful to completely bypass the pin electronics and provide for direct access to the DUT with no active circuitry in the path. This access is useful for:

- Connecting a central PMU to the DUT.
- Direct measurement of the DUT voltage.
- DC calibration.
- Establishing a Kelvin connection with an external PMU prior to contacting the DUT.

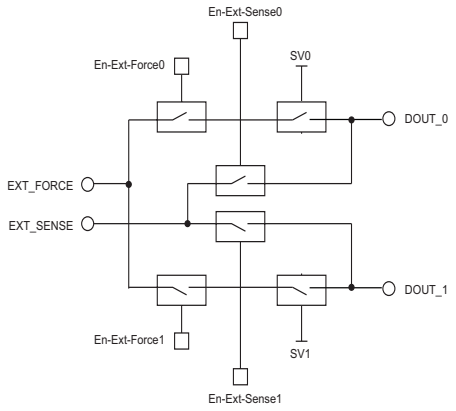


FIGURE 61.

TABLE 97.

SV#	EN-EXT-FORCE#	EXT_FORCE TO DOUT_#
0	X	Open
1	0	Open
1	1	Connected

TABLE 98.

SV#	EN-EXT-SENSE#	DOUT_# TO EXT_SENSE
X	0	Open
X	1	Connected

DC Levels

Every functional block requires a variety of DC voltage levels in order to function properly. These levels are all generated on chip with a 16-bit DAC that is programmed through the CPU port.

There are four voltage range options. Various DC levels are grouped together, and the selected voltage range is common for all levels within each group (see Table 99).

The realizable voltage range is restricted by the power supply levels and headroom limitations, especially in VR2. If a level is programmed beyond the recommended operating conditions, saturation will occur, and the actual DC level will not match the desired programmed level.

Voltage Range Options vs. Function

Within each DAC group, the voltage range selection is common and is programmed via the CPU port.

CVA-PPMU and CVB-PPMU should only use the IR range when measuring current (MI), and only use VR0, VR1, or VR2 when measuring a voltage (MV).

TABLE 99.

Range Select<1:0>	Voltage Range	Resolution (LSB)	Full Scale (FS)
0	VR0	61µV	4
1	VR1	122µV	8
2	VR2	244µV	16
3	VIR	30.5µV	2

Level Programming

Voltage ranges VR0, VR1 and VR2 use Equation 9:

$$V_{OUT} = (Value - V_{MID}) \bullet Gain + V_{MID} + Offset + DUT\_GND \quad \text{(EQ. 9)}$$

Programming Currents uses Equation 10:

$$V_{OUT} = (Value - V_{MID}) \bullet Gain + V_{MID} + Offset \quad \text{(EQ. 10)}$$

Value is described by Equation 11:

$$Value = \{(DAC\ Code)/(2^{**}N - 1)\} \bullet FS + V_{MIN} \quad \text{(EQ. 11)}$$

where:

N = 16; 2**N – 1 = 65,535

and:

Vmin = Vmid – (FS/2).

FI

FS = 2V

Vmin = -1V

Vmid = 0V

Vmax = +1V

Isource/Isink

FS = 1V

Vmin = 0V

Vmid = 0.5V

Vmax = +1V

Offset and Gain

Each individual DC level has an independent offset and gain correction. These correction values allow the desired output level to be programmed at their true post calibrated value and to be loaded simultaneously across multiple pins without having to correct for per pin errors. The range of possible offset voltage correction is a percentage of the full scale voltage range of each particular voltage group.

TABLE 100.

OFFSET CODE	OFFSET VALUE	GAIN CODE	GAIN VALUE
0000H	-5.4% of FS	0000H	0.875
7FFFH	0	7FFFH	1.0
FFFFH	+5.4% of FS	FFFFH	1.125

Device Under Test Ground

DUT_GND_# is a high impedance analog voltage input that provides a means of tracking the destination ground and making an additional offset to the programmed level so the programmed level is correct with respect to the DUT.

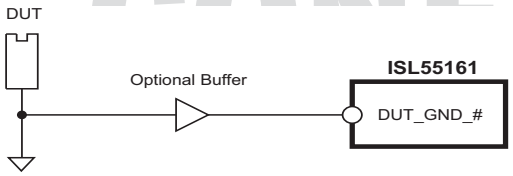


FIGURE 62.

The input at DUT_GND_# should be:

- Filtered for noise
- Stable
- Reflect the actual ground level at the DUT

VMID

The selected voltage range may be shifted up or down by the CPU port. Vmid does not affect current forcing and sensing DC levels. Vmid may be set independently per channel.

TABLE 101. V_{MID} VALUE

V_{MID}#<1:0>	VR0	VR1	VR2
00	+1.5V	+3.0V	+6.0V
01	+1.75V	+3.5V	+7.0V
10	+1.25V	+2.5V	+5.0V
11	+1.0V	+2.0V	+4.0V
Resolution	250mV	500mV	1V

TABLE 102. VOLTAGE RANGE

V_{MID}#<1:0>	VR0	VR1	VR2
00	-0.5V/+3.5V	-1V/+7V	-2V/+14V
01	-0.25V/+3.75V	-0.5V/+7.5V	-1V/+15V
10	-0.75V/+3.25V	-1.5V/+6.5V	-3V/+13V
11	-1V/+3V	-2V/+6V	-4V/+12V

Voltage Range Options vs. Function

Different functional blocks require different DC level voltage ranges. The allowed combinations are listed in Table 103.

DC Calibration

The part is designed and tested to meet its DC accuracy specifications after a two point, two iteration calibration. The actual calibration points are different for each voltage range, and may even be different for the same voltage range but for different functional blocks. In general, most calibration points will be at 20% and 80% of the full scale value for that range. (The actual calibration points are listed separately for each functional block in the DC specification section.)

The test points are broken into two categories:

- Inner test
- Outer test

The inner test is one specific test point (typically) at 50% of the full scale value of the particular range. The outer test is usually taken at the end points of the voltage range, or 0% and 100% of the full scale value.

In general, the inner test will be performed against tighter, more accurate limits. But every part shipped will be calibrated and tested against the limits in the specification section, and is guaranteed to perform within those limits under the documented calibration technique.

Typical Calibration andTest Point Set-up

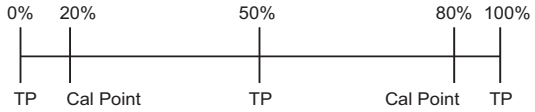


FIGURE 63.

TABLE 103. RANGE DECODE

GROUP	FUNCTIONAL BLOCK	VR0	VR1	VR2	VIR	RANGE SELECT
Drive	Driver (DVH, DVL, VTT)	√	√	√		Drive#<1:0>
Comp	Comparator Thresholds (CVA, CVB)	√	√	√		Comp#<1:0>
PPMU	PPMU Comparator Thresholds (CVA-PPMU, CVB-PPMU)	√	√	√	√	PPMU#<1:0>
FV	Voltage Clamps (V-Cl-Hi, V-Cl-Lo) PPMU Voltage Force (V-FV)	√	√	√		FV#<1:0>
FI	PPMU Current Force (V-FI)				√	N/A
	Tracks DUT_GND (FV, MV)					
	Does NOT Track DUT_GND (FI, MI)					

SYSTEM LEVEL DC ACCURACY

Other calibration schemes and techniques, using more or fewer calibration points or different test points, may also be employed. The resulting system level accuracy may be superior or inferior to the part's specified limits, and will be dependent on the details of the particular application.

Calibration Procedure

1. Calibrate the MONITOR
2. Calibrate the DAC using the DAC cal bits
3. Calibrate the MI Coarse Adjust
4. Calibrate the offset DAC
5. Calibrate the Gain DAC
6. Calibrate the DC Level

Level Calibration

Initialize

1. Select desired voltage range (VR0, VR1, VR2, VIR)
2. Set Gain = 1.0; Offset = 0.0V

Measure

1. Set Level 1 = Cal Point 1. Measure Output1'
2. Set Level 2 = Cal Point 2. Measure Output2'

Calculate

1. Gain' = (Output2' – Output1')/(Level 2 – Level1)
2. Offset' = (Output2' – Vmid) – Gain' • (Level2 – *Vmid*)

Finish

1. Set Offset = - Offset'/Gain'
2. Set Gain = 1.0/Gain'

DAC Calibration

The DAC supports the ability to independently calibrate the top five MSBs. The default condition of these adjustment bits is the zero correction state.

The magnitude of the bit correction is an integer count of LSB voltage added or subtracted from the individual bit weighting, and is therefore a function of the particular voltage range selected for each level. The DAC MSB adjustment is applied to the DC level prior to the gain correction.

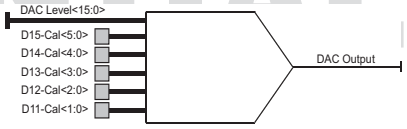


FIGURE 64.

TABLE 104. D15 CALIBRATION

D15-Cal<5>	D15-Cal<4>	D15-Cal<3>	D15-Cal<2>	D15-Cal<1>	D15-Cal<0>	D15 ADJUSTMENT
0	1	1	1	1	1	+93 LSB
			•			•
0	0	0	0	0	1	+3 LSB
0	0	0	0	0	0	No Adjustment
1	0	0	0	0	0	No Adjustment
1	0	0	0	0	1	-3 LSB
			•			•
1	1	1	1	1	1	-93 LSB

TABLE 105. D14 CALIBRATION

D14-Cal<4>	D14-Cal<3>	D14-Cal<2>	D14-Cal<1>	D14-Cal<0>	D14 ADJUSTMENT
0	1	1	1	1	+45 LSB
		•			•
0	0	0	0	1	+3 LSB
0	0	0	0	0	No Adjustment
1	0	0	0	0	No Adjustment
1	0	0	0	1	-3 LSB
		•			•
1	1	1	1	1	-45 LSB

TABLE 106. D13 CALIBRATION

D13-Cal<3>	D13-Cal<2>	D13-Cal<1>	D13-Cal<0>	D13 ADJUSTMENT
0	1	1	1	+21 LSB
	•			•
0	0	0	1	+3 LSB
0	0	0	0	No Adjustment
1	0	0	0	No Adjustment
1	0	0	1	-3 LSB
	•			•
1	1	1	1	-21 LSB

TABLE 107. D12 CALIBRATION

D12-Cal<2>	D12-Cal<1>	D12-Cal<0>	D12 ADJUSTMENT
0	1	1	+9 LSB
0	1	0	+6 LSB
0	0	1	+3 LSB
0	0	0	No Adjustment
1	0	0	No Adjustment
1	0	1	-3 LSB
1	1	0	-6 LSB
1	1	1	-9 LSB

TABLE 108. D11 CALIBRATION

D11-Cal<1>	D11-Cal<0>	D11 ADJUSTMENT
0	1	+3 LSB
0	0	No Adjustment
1	0	No Adjustment
1	1	-3 LSB

TABLE 109. CAL RANGE vs VOLTAGE RANGE vs DAC BIT

	D15	D14	D13	D12	D11
VR0	5.67mV	2.75mV	1.28mV	549µV	183µV
VR1	11.35mV	5.5mV	2.56mV	1.1mV	366µV
VR2	22.7mV	10.1mV	5.12mV	2.2mV	732µV
VIR	2.84mV	1.38mV	640.5µV	275µV	91.5µV

External References and Components

Many on-chip functional blocks reference a precision external:

- Voltage
- Resistance
- Frequency

By locking on-chip performance to an external reference, circuit performance will be more consistent over:

- Variations in ambient temperature
- Part to part distribution.

V_REF

V_REF is an analog input voltage that is used to program the on-chip DAC levels. V_REF should be held at +3.0V. Any noise or jitter on V_REF will contribute to the noise floor of the chip and therefore the V_REF should be filtered and be as quiet and stable as possible. There is one V_REF shared by both channels.

R_EXT

R_EXT is an external resistor used to control the output impedance of the driver. An external precision resistor with a low temperature coefficient will result in the driver output impedance remaining stable over changes in the ambient temperature.

R_EXT also determines the range of the output impedance adjustment for DVH, DVL and VTT with a total adjustment range of ± R_EXT/2000. There is one R_EXT pin shared by both channels.

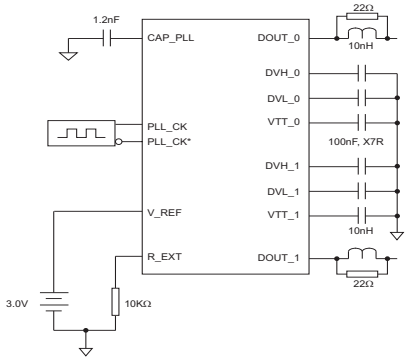


FIGURE 65.

Transmission Line Inductors and Resistors

Depending on the particular application and specific details of the PC board layout, a series inductor with a parallel resistor may or may not be placed at the DOUT pin to compensate for the capacitance on that node. The actual inductor and resistor value is application specific.

PLL Frequency

PLL_CK is an external frequency that establishes the range and resolution of all on-chip delay elements, as well as the propagation delay of all logic gates in series with the high speed driver and comparator signal paths. **For any applications that do not use any delay elements, PLL_CK must be placed in a low state. Do NOT leave PLL_CK/PLL_CK* floating.**

PLL FILTER CAPACITOR

A capacitor at pin CAP_PLL is used to compensate the op amp used in the PLL filter circuitry. The other end of the capacitor should be connected to ground.

Power Supply Restrictions

The following guidelines must be met to support proper operation:

- VCC_SV ≥ VCC
- VCC ≥ VDD; VEE ≤ GND
- VDD ≥ GND
- VDD ≥ V_REF

Schottky diodes are recommended on a once-per-board basis to protect against a power supply restriction violation.

Power Supply Sequence

Ideally, all power supplies would become active simultaneously while also meeting the power supply restrictions. However, since it is difficult to guaraqntee simultaneous levels, the following sequence is recommended:

- VEE
- VCC_SV
- VCC
- VDD
- V_REF

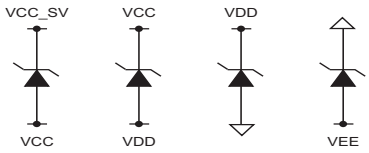


FIGURE 66.

ESD/EOS Protection

For the best Electrostatic Discharge (ESD) / Electrical Overstress (EOS) protection for the DOUT pins, please follow the guidelines below.

1. External Diodes on DOUT: Enhanced resistance to ESD can be improved by connecting 2 small signal diodes to the DOUT pin. One diode should be connected from VCC_SV to DOUT and the other from VEE to DOUT. These should be as close to the part and power planes as possible. Special attention should be paid to the leakage and AC performance specifications for these diodes. 1N914 silicon surface mount diodes are recommended.

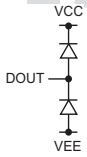


FIGURE 67.

2. Maximum Powered-On ESD Protection on pin DOUT_0 and DOUT_1
   a. Select Fast-HiZ. Set Fast-HiZ-En# in the Driver Configuration registers to 1.
   b. Program VTT_# to 2.5V or a voltage that meets the criteria listed in section 3 below.
   c. Select VTT Driver Mode. Set Dr-Mode# in the Driver Control registers to 1.
   d. Ensure SV# is low.
   e. Drive VTT. This can be accomplished two ways.
      1) Use the real time path through the part by driving pin pairs EN_#/EN_#* low.
      2) Use the CPU-En path. Set Sel-RT-En# in the Drive Control registers to 0.
      3) Set CPU-En0 and CPU-En1 in the CPU Force register to 0.

3. Driver Levels Programmed Values:
   a. Driver levels programming in driver mode:
      1) |DVH - DVL| <=8V
      2) |DVH - VTT| <=8V
      3) |DVL - VTT| <=8V
   b. When DOUT is in Hi-Z or PMU mode the driver levels should meet the following restrictions:
      1) |DOUT - DVH| <=8V
      2) |DOUT - DVL| <=8V
      3) |DOUT - VTT| <=8V

Optional PCB Layout Option

When designing new ATE systems, many times it is difficult to quantify exactly how much timing delay span will be needed in order to align timing edges of faster channels with the slowest one in the system. The ISL55161 includes on-chip timing deskew circuitry that can compensate for as much as 5ns of delay variation between channels in a system and align data edges to within 10 to 20ps of each other. In many systems, such a broad range of timing adjustment is not necessary so there are lower cost pin electronics alternatives available, like the ISL55163.

The ISL55163 is identical in function to ISL55161, except that the deskew circuitry is not present. It is software compatible with any software developed for ISL55161 and is packaged in the same package options. When used with a dual-option PCB layout, the pinout of the ISL55163 makes it possible to create an instrument that can accommodate either the ISL55161 (when deskew is needed) or the ISL55163 (when no deskew is needed).

The dual-option PCB layout employs the use of surface mount components so the same PCB will work with both ISL55163 and ISL55161 products. The schematic description of this idea is shown below for each device. The deskew circuitry included in the ISL55161 requires an external clock on pins 8 and 9, PLL_CLK/PLL_CLK*, to set the overall timing delay span, along with an external capacitor on pin 44 and ISL55163 does not use these pins for the same purpose. C1, R2, R3, and R4 are used to accommodate these differences.

External Component Implementation

When using ISL55161, R4 should be left unpopulated (open), and R2 and R3 should be populated with zero ohm resistors so that the external clock is routed to pins 8 and 9 of the device. Similarly, C1 should be populated with a 1.2nF capacitor.

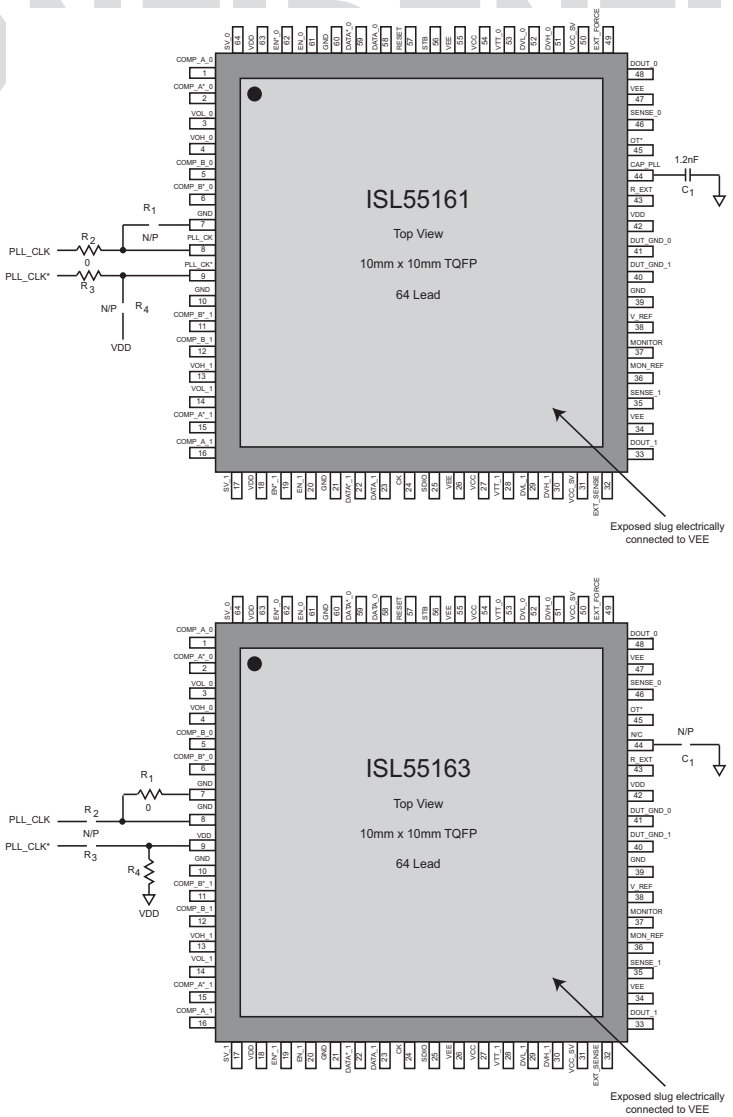


FIGURE 68.

CPU Port

All on-board DACs and registers are controlled through the CPU serial data port, which is capable of both writing to the chip as well as reading back from the chip (typically used for diagnostic purposes.)

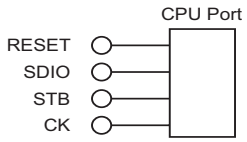


FIGURE 69.

Address

Address words for every CPU transaction are all 16 bits in length and contain the destination of the data word for a write cycle, or the source to be read back for a read cycle. Address bits are shifted in LSB first, MSB last.

Data

Data words for every CPU transaction are all 16 bits in length and are loaded or read back LSB first, MSB last. The timing for data is different for a read cycle vs. a write cycle, as the drivers on the SDIO alternate between going into high impedance and driving the line.

Control Signals

There are three CPU interface signals: SDIO, CK, and STB. SDIO is a bidirectional data pin through which information is either loaded or written back. CK is the CPU port clock signal that transfers data back and forth. When data is going into the part, SDIO is latched on a rising edge of CK. When data is coming out of the part, SDIO is again updated on a rising edge of CK. STB is the control signal that identifies the beginning of a CPU transaction. STB remains high for the duration of the transaction, and must go low for at least one CK cycle before another CPU transaction may begin.

CK must be running at all times even if no CPU transactions are occurring. CK is used on chip for other functions and MUST run continuously for correct chip operation.

Write Enable

Various register bits in the memory map tables (see tables in “Memory Space” section starting on page 74) require a write enable (WE) to allow those bits to be updated during a CPU write cycle. WE control allows some bits within an address to be changed, while others are held constant. Each WE applies to all lower data bits, until another WE is reached.

If WE = 1, the registers in the WE group will be written to. If WE = 0, the registers will not be updated. If WE = 0, the registers will not be updated but all data bits associated with that field must also be programmed to 0.

WE is read back as a don’t care (X) value.

Read vs. Write Cycle

The first SDIO bit latched by CK in a transaction identifies the transaction type.

TABLE 110.

1st SDIO BIT	CPU TRANSACTION TYPE
0	Read - Data flows out of the chip
1	Write - Data flows into the chip

Parallel Write

The second SDIO bit of a transaction indicates whether a parallel write occurs.

TABLE 111.

2nd SDIO BIT	CPU TRANSACTION TYPE
0	Data goes to the selected channel
1	Date goes to both channels

A parallel write ignores the particular channel address and writes the information into the same location on both channels.

Reset

RESET is an external hardware reset signal that places all internal registers and control lines into a low state. Reset must be executed independently after a power up sequence. **RESET does NOT place the DAC level memory into a known state, so this information must always be loaded after a power up sequence.**

RESET is active high.

FIGURE 70.

In addition, the CPU port can execute a reset (as a write only transaction). If the CPU-Reset address is written to, regardless of the value of any of the SDIO bits, CPU-Reset will fire off a one-shot pulse that performs the same function as an external RESET.

Chip ID

Chip ID (see tables in “Memory Space” section starting on page 74) is a read-only function that identifies the product and the die revision.

TABLE 112.

D15...D4	D3...D0
Prod-ID<11:0> 068 Hex (104)	Die-Rev<3:0>

NOTE: Product ID = 068 Hex = 104 Decimal.

DAC Sample and Hold (S/H) State Machine

The internal DACs used in the ISL55161 are S/H DACs. To update a single DAC level it takes 387 clock cycles. The clock used for this operation is the CPU interface clock. The first 256 clocks are used to select the desired level and let the DAC level settle. The next 128 clocks are needed to refresh the S/H. The 3 remaining

clocks are used to control the state machine. To calculate the time to refresh one DAC level, multiply the CPU clock time by the number of clocks needed to update one level. If using a 25MHz clock, the time needed is: 40nS * 387cycles = 15.48µS. There are 28 total internal levels to the S/H DAC; therefore, to update all levels, the time would be: 28 * 40nS * 387cycles = 433.44µS.

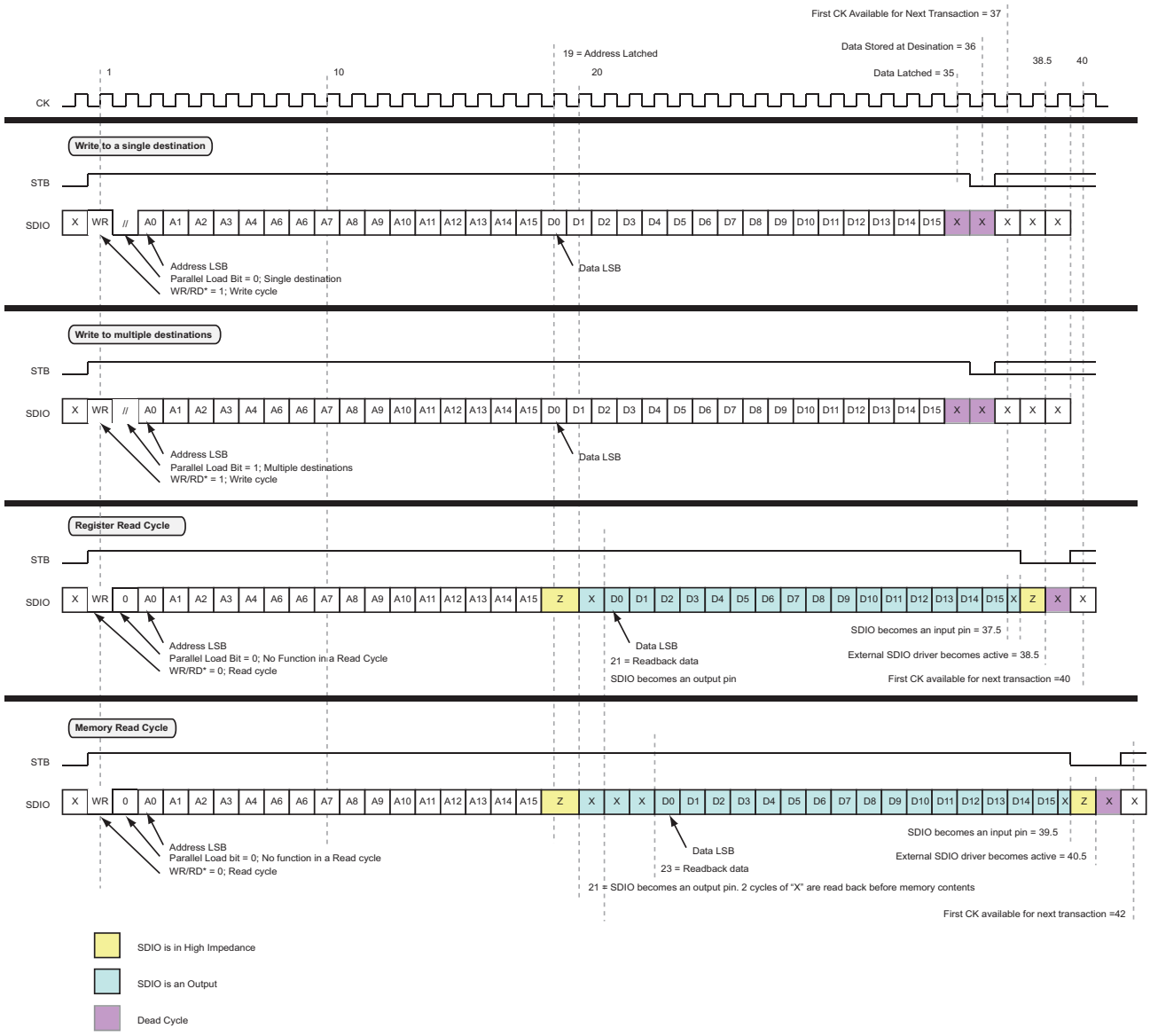
The sequence that the state machine uses to refresh the DAC matches the RAM address mapping: DVH-0, DVH-1, DVL-0, DVL-1, etc. This order allows both channels to update whenever a parallel write is performed for the same level on both channels.

When writing to a specific level, the state machine will complete the current level, then jump to the level which was just written. The state machine then proceeds in the normal order; it doesn't jump back. Therefore, you should assume, at worst case, it takes 774 clocks to update a single level after being written, 387 to complete the current level plus 387 to update the desired level. One caveat to this is with a parallel-channel write. There will still be, at worst case, 774 clocks to update channel 0 of the parallel-channel write. Channel 1 will be updated in sequence after channel 0. This means that if channel 0 and channel 1 are written as part of a parallel-channel write, channel 0 could take 774 clocks to update (worst case) and then channel 1 will update 387 clocks later.

There is another consideration when writing RAM location values. As stated above, there is a latency between when a new RAM value is written to a RAM location and when the actual voltage value will start to update due to the sample and hold. When a RAM value is written, its address is written to a "next address" stack so that it is the next address to be updated by the sample and hold DAC after the current location is finished. This "next address" stack is only 1 address deep; therefore, if you push another address on the stack before the current one is popped, you will lose the current "next address" to be written. This does not mean the RAM location will not be updated, it will just take a longer time to update. With this in mind, for the fastest update when writing several levels, the user should write the various levels in the reverse order that the S/H loop goes through them. This way, after completing the last write, all levels will update in order. For example, if you want to update DVH, DVL, and VTT, you would write VTT first, then DVL, then DVH.

The user also needs to be aware that when continuously writing to a particular level, other levels may be starved of being refreshed by the CPU clock. If this happens, levels can droop out of specification.

Protocol Timing Diagram



Memory Space

Information is stored on-chip in two ways:

- RAM
- Registers

Each storage mechanism is then broken into two categories:

- Per pin resources
- Central resources

TABLE 113.

ADDRESS RANGE	FUNCTION
0 to 63	Channel 0 RAM (DC Levels)
64 to 111	Channel 0 registers
112 to 127	Central registers
128 to 191	Channel 1 RAM (DC Levels)
192 to 239	Channel 1 registers
240 to 255	Central registers
256+	Unused

RAM Storage

CHANNEL 0 ADDRESS	CHANNEL 1 ADDRESS	RESOURCE	D15 – D0
0	128	DVH-#	DAC Level
1	129	DVL-#	DAC Level
2	130	VTT-#	DAC Level
3	131	CVA-#	DAC Level
4	132	CVB-#	DAC Level
5	133	CVA-PPMU-#	DAC Level
6	134	CVB-PPMU-#	DAC Level
7	135	V-FV-#	DAC Level
8	136	V-FI-#	DAC Level
9	137	V-CI-Hi-#	DAC Level
10	138	V-CI-Lo-#	DAC Level
11	139	I-Source-#	DAC Level
12	140	I-Sink-#	DAC Level
13 – 15	141 - 143	Not Used	
16	144	DVH-#	DAC Level Offset
17	145	DVL-#	DAC Level Offset
18	146	VTT-#	DAC Level Offset
19	147	CVA-#	DAC Level Offset
20	148	CVB-#	DAC Level Offset
21	149	CVA-PPMU-#	DAC Level Offset
22	150	CVB-PPMU-#	DAC Level Offset
23	151	V-FV-#	DAC Level Offset
24	152	V-FI-#	DAC Level Offset
25	153	V-CI-Hi-#	DAC Level Offset
26	154	V-CI-Lo-#	DAC Level Offset
27	155	I-Source-#	DAC Level Offset
28	156	I-Sink-#	DAC Level Offset
29 – 31	157 - 159	Not Used	
32	160	DVH-#	DAC Level Gain

RAM Storage (Continued)

CHANNEL 0 ADDRESS	CHANNEL 1 ADDRESS	RESOURCE	D15 – D0
33	161	DVL-#	DAC Level Gain
34	162	VTT-#	DAC Level Gain
35	163	CVA-#	DAC Level Gain
36	164	CVB-#	DAC Level Gain
37	165	CVA-PPMU-#	DAC Level Gain
38	166	CVB-PPMU-#	DAC Level Gain
39	167	V-FV-#	DAC Level Gain
40	168	V-FI-#	DAC Level Gain
41	169	V-CI-Hi-#	DAC Level Gain
42	170	V-CI-Lo-#	DAC Level Gain
43	171	I-Source-#	DAC Level Gain
44	172	I-Sink-#	DAC Level Gain
45 – 63	173 – 191	Not Used	

Per Channel Registers - Driver

ADDRESS	RESOURCE	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
64 0040H 192 00C0H	Driver Terminations							WE	Sel-En#-BP	WE	Sel-D#-BP	WE	EZ#<1>	EZ#<0>	WE	DZ#<1>	DZ#<0>
65 0041H 193 00C1H	Driver Configuration	WE	CPU-XOR#					WE	HiZ-Override#	WE	Fast-HiZ-En#	WE	Sel-SV#-En	WE		Sel-En#	Sel-D#
66 0042H 194 00C2H	Driver Control	WE	Hold-SV#					WE	Dr-Mode#<1>	WE	Dr-Mode#<0>	WE	Sel-RT-SV#	WE	Sel-RT-En#	WE	Sel-RT-D#
67 0043H 195 00C3H	Data Deskew	WE	Sel-D#-CD	WE	0	D#-CD<3>	D#-CD<2>	D#-CD<1>	D#-CD<0>	WE	Sel-D#-FD		WE	D#-FD<3>	D#-FD<2>	D#-FD<1>	D#-FD<0>
68 0044H 196 00C4H	Data Falling Edge Adjust	WE	Sel-D#-CFEA		WE	D#-CFEA<3>	D#-CFEA<2>	D#-CFEA<1>	D#-CFEA<0>	WE	Sel-D#-FFEA		WE	D#-FFEA<3>	D#-FFEA<2>	D#-FFEA<1>	D#-FFEA<0>
69 0045H 197 00C5H	Enable Deskew	WE	Sel-En#-CD	WE	0	En#-CD<3>	En#-CD<2>	En#-CD<1>	En#-CD<0>	WE	Sel-En#-FD		WE	En#-FD<3>	En#-FD<2>	En#-FD<1>	En#-FD<0>
70 0046H 198 00C6H	Enable Falling Edge Adjust	WE	Sel-En#-CFEA		WE	En#-CFEA<3>	En#-CFEA<2>	En#-CFEA<1>	En#-CFEA<0>	WE	Sel-En#-FFEA		WE	En#-FFEA<3>	En#-FFEA<2>	En#-FFEA<1>	En#-FFEA<0>

Per Channel Registers - Driver (Continued)

ADDRESS	RESOURCE	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
71 0047H 199 00C7H	Output Impedance		WE	RO-VTT#<3>	RO-VTT#<2>	RO-VTT#<1>	RO-VTT#<0>	WE	RO-DVH#<3>	RO-DVH#<2>	RO-DVH#<1>	RO-DVH#<0>	WE	RO-DVL#<3>	RO-DVL#<2>	RO-DVL#<1>	RO-DVL#<0>
72 0048H 200 00C8H	Power Options													WE	PMU-MI-Off#	PMU-Comp-Off#	Comp-Off#
73 – 79 201 - 207	Not Used																

NOTE: Channel 0 addresses are listed on the top and Channel 1 addresses are listed on the bottom of each address entry.

Per Channel Registers - Comparator

ADDRESS	RESOURCE	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
80 0050H 208 00D0H	Comparator Configuration				WE	Sel-C#-BP	WE	CPU-CB#	CPU-CA#	WE	Sel-CPU-C#				WE	Sel-MU-B#	Sel-MU-A#
81 0051H 209 00D1H	Comp A Deskew	WE	Sel-CA#-CD	WE	0	CA#-CD<3>	CA#-CD<2>	CA#-CD<1>	CA#-CD<0>	WE	Sel-CA#-FD		WE	CA#-FD<3>	CA#-FD<2>	CA#-FD<1>	CA#-FD<0>
82 0052H 210 00D2H	Comp A Falling Edge Adjust								WE	Sel-CA#-FFEA		WE	CA#-FFEA<4>	CA#-FFEA<3>	CA#-FFEA<2>	CA#-FFEA<1>	CA#-FFEA<0>
83 0053H 211 00D3H	Comp B Deskew	WE	Sel-CB#-CD	WE	0	CB#-CD<3>	CB#-CD<2>	CB#-CD<1>	CB#-CD<0>	WE	Sel-CB#-FD		WE	CB#-FD<3>	CB#-FD<2>	CB#-FD<1>	CB#-FD<0>
84 0054H 212 00D4H	Comp B Falling Edge Adjust								WE	Sel-CB#-FFEA		WE	CB#-FFEA<4>	CB#-FFEA<3>	CB#-FFEA<2>	CB#-FFEA<1>	CB#-FFEA<0>
85 0055H 213 00D5H	Comparator Diagnostics (Read Only in Red) (Write Only in Blue)	PMU-CB#	PMU-CA#	RT-CB#	RT-CA#				WE	CPU-Pulse#	WE	D#-Diag	En#-Diag	Edge#-Par	En-SV#	Sel-C#-Diag	Ring#-En
86 – 95 216 - 223	Not Used																

NOTE: Channel 0 addresses are listed on the top and channel 1 addresses are listed on the bottom of each address entry.

Per Channel Registers - PMU

ADDRESS	RESOURCE	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
96 0060H 224 00E0H	PPMU Configuration	WE	Sel-Mon-Ref#	WE	PPMU-En#	WE	V-Cl-En#	WE	Sel-MV#	WE	Sel-MU#	WE	Loop#	WE	MI/MV*#	WE	FI/FV*#
97 0061H 225 00E1H	PPMU Current Ranges								WE	IR#<7>	IR#<6>	IR#<5>	IR#<4>	IR#<3>	IR#<2>	IR#<1>	IR#<0>
98 0062H 226 00E2H	Ext Force/Sense									WE	Sel-Ext-DAC#	WE	Sel-Ext-Sense#	WE	En-Ext-Sense#	WE	En-Ext-Force#
99 0063H 227 00E3H	PPMU Diagnostics									WE	Sel-MU#-Diag		WE	MU#-Diag<3>	MU#-Diag<2>	MU#-Diag<1>	MU#-Diag<0>
100 0064H 228 00E4H	DC Level Range Select		WE	Vmid#<1>	Vmid#<0>	WE	PPMU#<1>	PPMU#<0>	WE	FV#<1>	FV#<0>	WE	Comp#<1>	Comp#<0>	WE	Drive#<1>	Drive#<0>
101 0065H 229 00E5H	Load									WE	Sink-Adj#<2>	Sink-Adj#<1>	Sink-Adj#<0>	WE	Source-Adj#<2>	Source-Adj#<1>	Source-Adj#<0>
102 – 111 230 – 239	Not Used																

NOTE: Channel 0 addresses are listed on the top and channel 1 addresses are listed on the bottom of each address entry.

Central Registers

ADDRESS	RESOURCE	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
112 0070H	Monitor/ Over-temperature									WE	CPU-OT			WE	Sel-Mon	WE	Mon-OE
113 0071H	CPU Force				WE	CPU-SV1	WE	CPU-En1	WE	CPU-D1		WE	CPU-SV0	WE	CPU-En0	WE	CPU-D0
114 0072H	PLL						WE	PLL-Dis	WE	Fclamp<1>	Fclamp<0>	WE	Vswing<1>	Vswing<0>	WE	PLL-Z<1>	PLL-Z<0>

Central Registers (Continued)

ADDRESS	RESOURCE	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
115 0073H	CPU-Reset (Write Only)	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X
116 0074H	Differential Comparator											WE	Diff-B<1>	Diff-B<0>	WE	Diff-A<1>	Diff-A<0>
117 – 126 0075H -	Not Used																
127 007FH	Die ID (Read Only)	Prod-ID<11>	Prod-ID<10>	Prod-ID<9>	Prod-ID<8>	Prod-ID<7>	Prod-ID<6>	Prod-ID<5>	Prod-ID<4>	Prod-ID<3>	Prod-ID<2>	Prod-ID<1>	Prod-ID<0>	Die-Rev<3>	Die-Rev<2>	Die-Rev<1>	Die-Rev<0>
- 214 00D6H	Upper DAC Bit Calibration	WE	Coarse-Adj<1>	Coarse-Adj<0>	WE	D14-Cal<4>	D14-Cal<3>	D14-Cal<2>	D14-Cal<1>	D14-Cal<0>	WE	D15-Cal<5>	D15-Cal<4>	D15-Cal<3>	D15-Cal<2>	D15-Cal<1>	D15-Cal<0>
- 215 00D7H	Mid DAC Bit Calibration					WE	D11-Cal<1>	D11-Cal<0>	WE	D12-Cal<2>	D12-Cal<1>	D12-Cal<0>	WE	D13-Cal<3>	D13-Cal<2>	D13-Cal<1>	D13-Cal<0>
240 – 254 00F0H – 00FEH	Not Used																
255 00FFH	Null Command	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X

Manufacturing Information

Moisture Sensitivity

The ISL55162 is a Level 3 (JEDEC Standard 033A) moisture sensitive part. All Pre Production and Production shipments will undergo the following process post final test:

- Baked @ +125°C ± 5°C for a duration ≥ 16 hours
- Vacuum sealed in a moisture barrier bag (MBB) within 30 minutes after being removed from the oven.

PCB Assembly

The floor life is the time from the opening of the MBB to when the unit is soldered onto a PCB.

- Product Floor Life ≤ 168 Hours

Units that exceed this floor life must be baked before being soldered to a PCB.

Solder Profile

The recommended solder profile is dependent upon whether the PCB assembly process is lead-free or not.

TABLE 114. Solder Profile

Profile Feature	Pb-Free Assembly
Average ramp up rate (T_L to T_P)	3°C/sec (max)
Preheat • Min Temp (Ts min) • Max Temp (Ts max) • Time (min to max) (ts)	 150°C 200°C 60 – 180 sec
Ts max to T_L • Ramp Up Rate	 3°C/sec (max)
Time above • Temperature (T_L) • Time (t_L)	 217°C 60 – 150 sec
Peak Temperature (T_P)	260°C
Time within 5°C of actual peak temp (tp)	20 sec – 40 sec
Ramp down rate	6°C/sec (max)
Time 25°C to peak temperature	8 minutes (max)

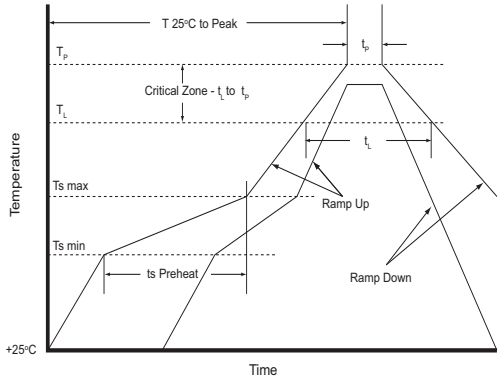


FIGURE 71.

Package Thermal Analysis

Junction Temperature

Maintaining a low and controlled junction temperature is a critical aspect of any system design. Lower junction temperatures translate directly into superior system reliability. A more stable junction temperature translates directly into superior AC and DC accuracy.

The junction temperature follows Equation 12:

$$T_J = P_D \bullet \Theta_{JA} + T_A \quad \text{(EQ. 12)}$$

where:

T_J = Junction Temperature

P_D = Power Dissipation

θ_{JA} = Thermal Resistance (Junction to Ambient)

T_A = Ambient Temperature

Heat can flow out of the package through two mechanisms:

- Conduction
- Convection

Conduction

Conduction occurs when power dissipated inside the chip flows out through the leads of the package and into the printed circuit board. While this heat flow path exists in every application, most of the heat flow will NOT occur with thermal conduction into the PCB.

Conduction also occurs in applications using liquid cooling, in which case most of the heat will flow directly out of the top of the package through the exposed heat slug and into the liquid cooled heat sink. The heat sink represents a low thermal resistance path to a large thermal mass with a controlled temperature.

The total thermal resistance is the series combination of the resistance from the junction to case (exposed paddle) (θ_{JC}) plus the resistance from the case to ambient (θ_{CA}).

Convection

The most common cooling scheme is to use airflow and (potentially) a heat sink on each part. In this configuration, most of the heat will exit the package via convection, as it flows through the die, into the paddle, and off the chip into the surrounding air flow.

Thermal Resistance

Each system will have its own unique cooling strategy and overall θ_{JA}. However, the resistance between the junction and the case is a critical and common component to the thermal analysis in all designs.

$$\Theta_{JA} = \Theta_{JC} + \Theta_{CA} \quad \text{(EQ. 13)}$$

θ_{CA} is determined by the system environment of the part and is therefore application specific. θ_{JC} is determined by the construction of the part.

q_{JC} Calculation

$$\Theta_{JC} = \Theta(\text{silicon}) + \Theta(\text{dieattach}) + \Theta(\text{paddle}) \quad \text{(EQ. 14)}$$

The thermal resistance of any material is defined by Equation 15:

$$\Theta = (\text{Intrinsic material resistivity}) \bullet \text{Thickness}/\text{Area} \quad \text{(EQ. 15)}$$

or

$$\Theta = \text{Thickness}/(\text{Intrinsic material conductivity} \bullet \text{Area})$$

Intrinsic Thermal Conductivity

Die Attach Thermal Conductivity = 1.4 W/M°K

Silicon Thermal Conductivity = 141.2 W/M°K

Paddle Thermal Conductivity = 263 W/M°K

Plastic Thermal Conductivity = 0.88 W/M°K

(Although some heat will flow throw the plastic package, the molding compound conductivity is not specifically used in the calculation of θ_{JC} through the paddle.)

TQFP Thermal Resistance Calculation

$$\Theta_{JC} = 0.12°C/W + 0.6°C/W + 0.01°C/W \quad \text{(EQ. 16)}$$

$$\Theta_{JC} = 0.73°C/W$$

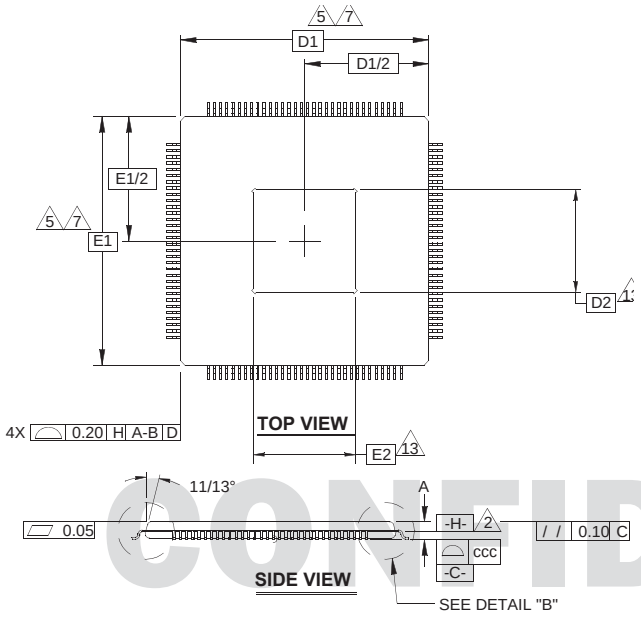
QFN Thermal Resistance Calculation

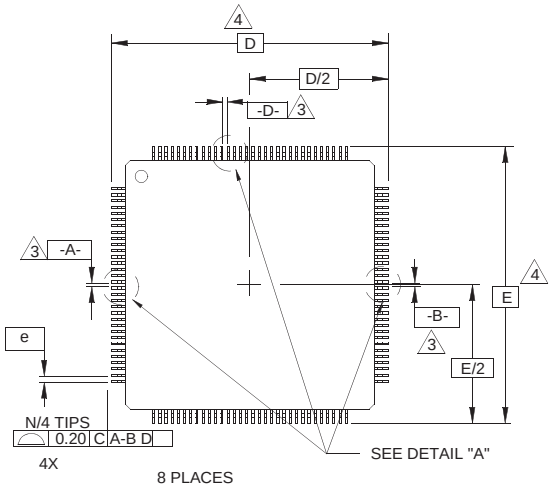
$$\Theta_{JC} = 0.06°C/W + 0.6°C/W + 0.01°C/W \quad \text{(EQ. 17)}$$

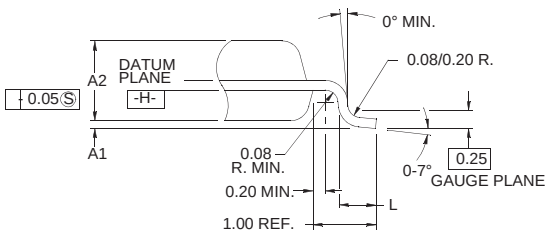
$$\Theta_{JC} = 0.67°C/W$$

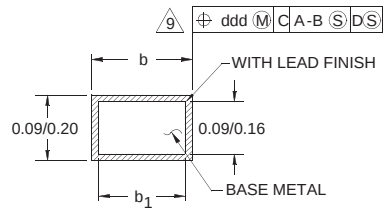
Package Outline Drawings

THIN PLASTIC QUAD FLATPACK PACKAGE WITH TOP EXPOSED PAD (TQFP-TEP)









64 LEAD THIN PLASTIC QUAD FLATPACK PACKAGE WITH TOP EXPOSED PAD (TQFP-TEP)

SYMBOL	ACD MIN	ACD NOM.	ACD MAX	NOTES
A			1.20	
A1	0.05		0.15	12
A2	0.95	1.00	1.05	
D		12.00 BSC		4
D1		10.00 BSC		7, 8
D2		7.49 BSC		13
E		12.00 BSC		4
E1		10.00 BSC		7, 8
E2		7.49 BSC		13
L	0.45	0.60	0.75	
N		64		
e		0.50 BSC		
b	0.17	0.22	0.27	9
b1	0.17	0.20	0.23	
ccc			0.08	
ddd			0.08	

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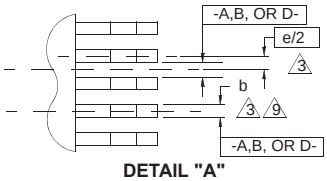
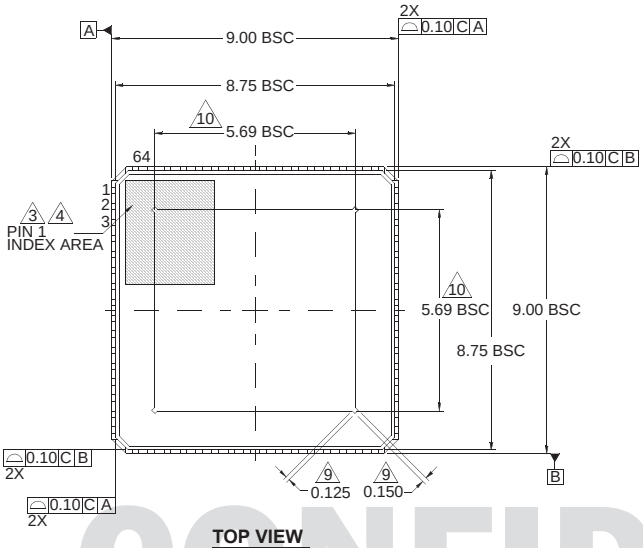
NOTES:

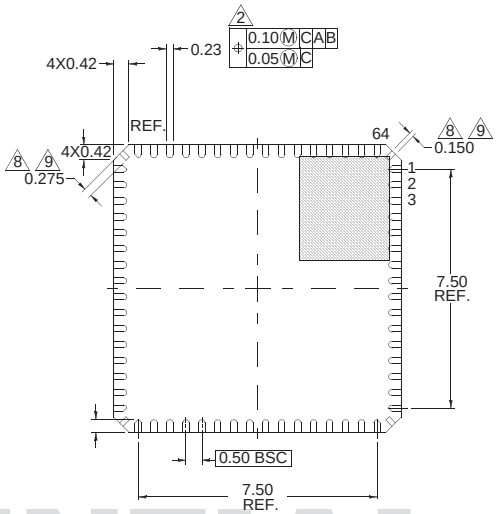
1. All dimensions and tolerances per ANSI Y14.5-1982.
2. Datum plane -H- located at mold parting line and coincident with lead, where lead exits plastic body at bottom of parting line.
3. Datums A-B and -D- to be determined at center line between leads where leads exit plastic body at datum plane -H- .
4. To be determined at seating plane -C- .
5. Dimensions D1 and E1 do not include mold protrusion. Allowable mold protrusion is 0.254 mm on D1 and E1 dimensions.
6. "N" is the total number of terminals.
7. These dimensions to be determined at datum plane -H- .
8. The top of package is smaller than the bottom of package by 0.15 millimeters.
9. Dimension b does not include dambar protrusion. allowable dambar protrusion shall be 0.08mm total in excess of the b dimension at maximum material condition. Dambar cannot be located on the lower radius or the foot.
10. Controlling dimension: millimeter.
11. This outline conforms to jedec publication 95 registration MS-026, variations ACB, ACC, ACD & ACE.
12. A1 is defined as the distance from the seating plane to the lowest point of the package body.
13. Dimension D2 and E2 represent the size of the exposed pad.
14. Exposed pad shall be coplanar with bottom of package within 0.05.
15. JEDEC variation.



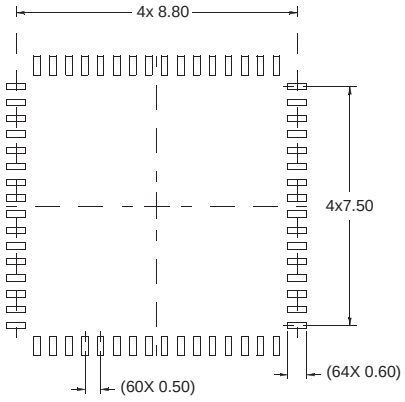
64 LEAD QUAD FLAT NO-LEAD PLASTIC PACKAGE WITH TOP EXPOSED PAD (QFN-TEP)



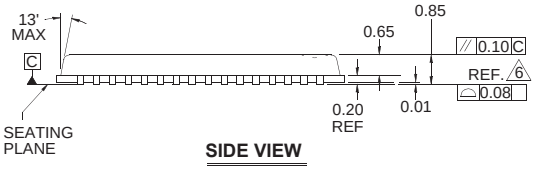
TOP VIEW



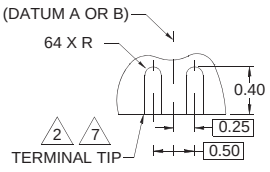
BOTTOM VIEW

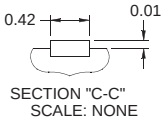


TYPICAL RECOMMENDED LAND PATTERN



SIDE VIEW





NOTES:

1. Dimensioning & tolerancing conform to ASME Y14.5M-1994.
2. Dimension b applies to metallized terminal and is measured between 0.15 and 0.30mm from terminal tip.
3. The pin #1 identifier must be existed on the top surface of the package by using indentation mark or other feature of package body.
4. Exact shape and size of this feature is optional.
5. All dimensions are in millimeters.
6. Bilateral coplanarity zone applies to the exposed pad as well as the terminals.
7. Applied only for terminals.
8. The shape shown on four corners are not actual I/O.
9. R, T or S, U applies only for straight tiebar shapes. Any mold flash on the exposed tiebar area shall be allowable.
10. D2, E2 dimensions : Nominal exposed pad size.

Revision History

DATE	REVISION	CHANGE
January 7, 2016	8	• Page 69: Power Supply Sequence section - change order of sequence • Page 79: Table 114 - change Peak Temperature to 260°C
April 1, 2015	8	• Change from Intersil to Elevate format • Page 8: ROC - Delete PPMU Levels heading and change V-FV to PPMU • Page 9: Power Supplies table : - Static; PLL_CK = 156.25MHz section - change all spec numbers - Dynamic- Ring Oscillator Configuration; PLL_CK=100MHz section - change all spec numbers • Pages 15 & 16: Load table: - Source Current Adjust section - change all spec numbers - Sink current Adjust section - change all spec numbers • Page 19: Force Current Table: change all spec numbers • Page 27: Fine Falling Edge Adjust table: - PLL_CK = 256.25MHz section - change all spec numbers • Page 28: Coarse Falling Edge Adjust table - add spec number 25221 • Page 67: Add Optional PCB Layout Option section
June 18, 2014	7	• Pages 30, 31, 32, 35, 38, 47, 55, 61: Diagrams updated to correct typos • Page 49: Figure 34 - Add Figure Name • Page 50: Figure 36 - Change Figure Name • Page 53: Figure 43 - Change <3:0> to <4:0> • Page 58: Table 88: Change SV+# to RT-En*#; change EN*_# to SV_#
February 3, 2014	6	• Page 15: Spec #14900 - Add new sentence to Test Conditions. • Page 16: Table 5: Change 0mA to 0mA to 1.6mA in 80µA steps. • Page 45: Current Source Enable Section - Add new paragraph after Table 48.
December 6, 2013 July 31, 2013 June 6, 2013	5	• Page 8: ROC - EXT_SENSE and EXT_FORCE: change VEE to VCC to VEE to VCC_SV. • Page 15: Spec # 14900, Test Conditions, add FS = 32mA. • Page 75: Add Solder Profile Section
February 7, 2013	4	• Page 48: Figure 32: change DOUT_# to V-MU# • Page 32: Updated PMU Block Diagram
October 30, 2012	3	• Page 52, Bypass Mode - Add sentence to end of paragraph • Page 66, add ESD/EOS Protection section • Page 68 - add DAC Sample and Hold Section
April 19, 2012	FN7923.2	• Page 8, Recommended Operating Conditions - Comparator Output Supplies: Changed VOH from VDD to <VDD; Changed VOL from GND to >GND Driver Levels: Changed ±8V to <8V FI V-Clamp Levels: Changed V-Cl-Hi - C-Cl-Lo....1V to V-Cl-Hi - V-Cl-Lo....>1V External Load Capacitance 1nF changed to <1nF • Page 13 - DC Electrical Specs - Driver: - Spec #13322 - changed Max from 50 to 45, Spec #13323 - changed Min from 45 to 50, Spec #13324 - changed Max from 50 to 45, Spec #13325 - changed Min from 45 to 50 • Page 13 - "Driver Output Impedance" section - Changed all references of Note 14 to Note 12 • Pages 31 and 47 - Comparator diagrams updated • Page 35 - Driver Detailed Block Diagram updated • Page 46 - Table 50, SV# Column: Swapped SV_# and EN*_#.Figure 29: Sel-SV#-En MUX: Swapped 0 and 1 • Page 58 - Table 88, as Swapped SV_# and EN*_#. Figure 51 - swapped 0 and 1

DATE	REVISION	CHANGE
November 22, 2011	FN7923.1	• page 4: Pin Configuration: Add "connected to VEE" tag to QFN pinout • page 6: Thermal Information: Add TQFP information • page 6: ROC: Power Supplies, VDD-VEE +7.5V changed to <+7.5V • page 6: ROC: Driver Level Restrictions: - Change VCC_SV-(DVH,DVL,VTT) 1V to 8V to |DOUT-DVH| <8V - Change VEE - (DVH,DVL,VTT) -1V to -8V to |DOUT-DVL| < 8V - Add |DOUT-VTT| <8V • page 17:, DC Electrical Spec - Load, Spec #s 15100, 15200 & 15300: Remove notes 19, 20, 21. Add "ISINK and ISRC set to 3.2mA" to Test Conditions. • page 24 - DC Elec Spec, Resistor Values/Switch Impedances, change "W" in Units to "Ω" • page 33 - Driver/VTT/Load Block Diagram: Add Data0/1, En0/1, SV0, SV1, Dr-Mode-1 labels • page 35 - PMU Block Diagram: Add RT-SV0/1 and PPMU-F1 labels, Add 1, 0 to Sel_Ext_Sense Mux • page 36- Measurement Unit Block Diagram: changes typos in labels as follows: - V-EI0/I1 changed to V-FI0/I1 - Va-Ti0/i1 changed to Va-Tj0/1 - Vb-ti0/i1 changed to Vb-Tj0/1 • page 41 - Figure 14: Correct typos in labels • page 46 - Output Impedance: R_EXT = 10.00kW changed to 10.00kΩ • page 47 - Figure 26: Add line between Rnom and Radj boxes • page 49 - correct typo in labels • page 53 - Equation 3 and 4: VCM + (VDIFF/2) changed to VCM - (VDIFF/2) • page 54 - Equation 5 and 6: Change VREF to VDIFF. Change Vref bullet to: Vdiff - Desired effective differential threshold level. • page 62 - Figure 52: changed Mux that has signal Test&Cal-1 as input from Sel-MU0-Diag as its control signal to Sel-MU1-Diag. Figure 53: correct typos in labels as in #6 above. • page 64 - Figures 59 and 60: correct typos in labels as in #6 above • page 71 - Write Enable section: added new paragraph, “WE is read back as a don’t care (X) value.” Table 112: change 069 Hex = 105 Decimal in note to 068 Hex and 104 Decimal • page 74 through page 77 - remove purple boxes from tables
09/16/ 2011	FN7923.0	Initial Release

Ordering Information

PART NUMBER (NOTE 1)	PART MARKING	TEMP. RANGE (°C)	PACKAGE (Pb-free)
ISL55161CNEZ	ISL55161CNEZ	+25 to +100	64 Lead, 10x10mm TQFP w/top exposed heat slug
ISL55161CRSZ	ISL55161CRSZ	+25 to +100	64-Lead, 9x9mm QFN w/top exposed heat slug
ISL55161-LB	Evaluation Board		
ISL55161-SYS	Evaluation Board		

NOTE:

1. These Elevate Semiconductor Pb-free plastic packaged products employ special Pb-free material sets), molding compounds/die attach materials, and 100% matte tin plate plus anneal (e3 termination finish, which is RoHS compliant and compatible with both SnPb and Pb-free soldering operations). Elevate Semiconductor Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020.