SOC Dual Channel 300MHz Pin Electronics/DAC/PMU/Deskew

ISL55162

The ISL55162 is a highly integrated System-on-a-Chip (SOC) pin electronics solution aimed at incorporating every analog function, along with some digital support circuitry, required on a per channel basis for Automated Test Equipment. The interface, control and I/O of the chip are all digital; all analog circuitry is inside the chip. Two complete tester channels are integrated into each chip.

ISL55162 is pin and functionally compatible with Venus, Venus Plus and Venus 2.

Features

- Pin Electronics Driver/Comparator
  - 3 Level Driver (DVH/DVL/VTT)
  - 8V Driver Output Swings
  - 16V Comparator Input Voltage Range
  - Extremely Low HiZ Leakage over 16V Range
- Per Pin PMU
  - FV, FI, MV, MI
  - 4 Quadrant Operation
  - 8 Current Ranges (32mA, 8mA, 2mA, 512µA, 128µA, 32µA, 8mA, 2µA)
  - +13V Super Voltage Capability
  - FI Voltage Clamps
  - Resistive Load (8 selectable resistor values)
- Deskew
  - Propagation Delay Adjustment
  - Falling Edge Adjustment
  - Delay Range set by PLL Clock
- On-Chip DC Levels
  - 11 Levels/Channel
  - Gain and Offset Correction/Level
  - DUT Ground Sensing and Correction
- 3-Bit Serial CPU Port
- Flexible High Speed Digital Inputs and Outputs
  - Selectable On-Chip Terminations for Inputs
  - 50Ω Series Termination for Comparator Outputs
- Lead Free Package
  - 64-Lead, 10mmx10mm TQFP with Top Exposed Heat Slug
  - Pdq < 1.1W/Channel

Applications

- Automated Test Equipment
- Instrumentation
- ASIC Verifiers

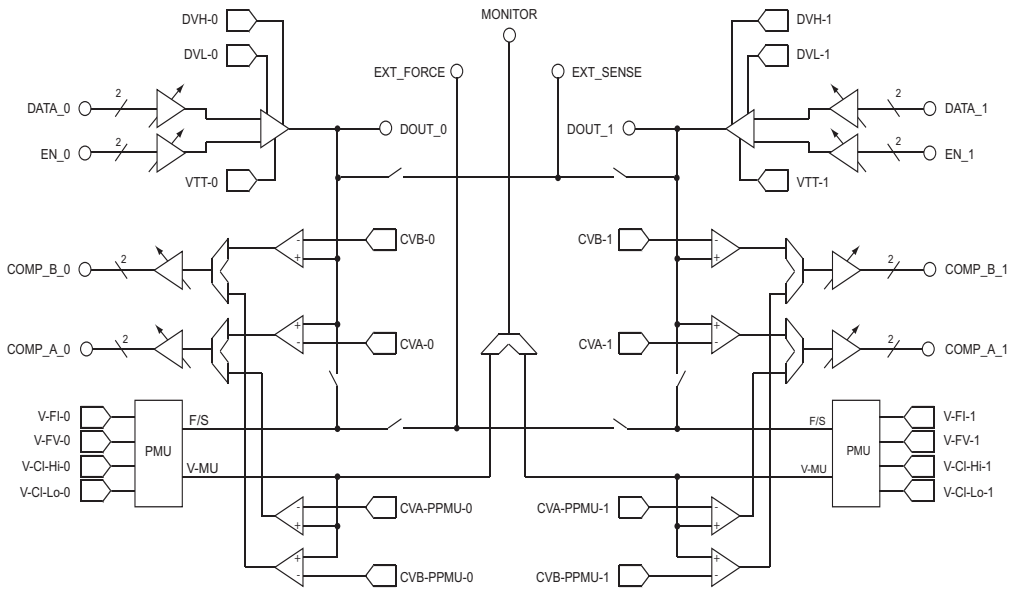


FIGURE 1. BLOCK DIAGRAM

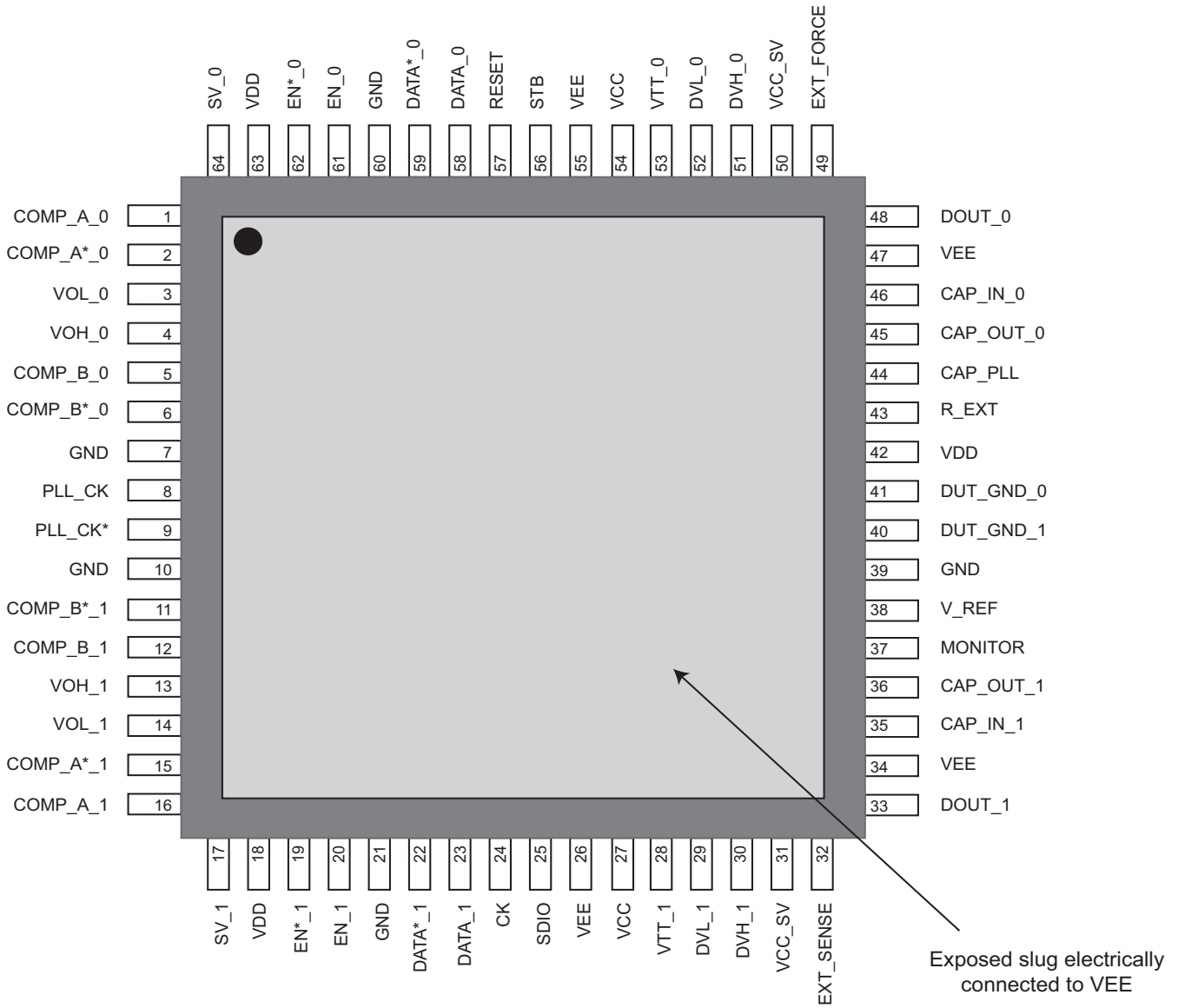
Table of Contents

Pin Descriptions

PIN #	PIN NAME	DESCRIPTION
Digital Inputs		
58, 59	DATA_0; DATA*_0	Channel 0 driver data.
61, 62	EN_0, EN*_0	Channel 0 driver enable.
64	SV_0	Channel 0 super voltage enable
23, 22	DATA_1; DATA*_1	Channel 1 driver data.
20, 19	EN_1, EN*_1	Channel 1 driver enable.
17	SV_1	Channel 1 super voltage enable.
8, 9	PLL_CK, PLL_CK*	Differential PLL reference signal.
Digital Outputs		
1, 2	COMP_A_0; COMP_A*_0	Channel 0, comparator A outputs
5, 6	COMP_B_0, COMP_B*_0	Channel 0, comparator B outputs
16, 15	COMP_A_1; COMP_A*_1	Channel 1, comparator A outputs
12, 11	COMP_B_1, COMP_B*_1	Channel 1, comparator B outputs
DUT Pins		
48, 33	DOUT_0, DOUT_1	Analog I/O pin which connects to the Device Under Test
Analog Pins		
51, 52, 53	DVH_0, DVL_0, VTT_0	Driver levels for Channel 0
30, 29, 28	DVH_1, DVL_1, VTT_1	Driver levels for Channel 1
38	V_REF	External precision voltage reference
43	R_EXT	External precision resistor.
46, 45	CAP_IN_0, CAP_OUT_0	Compensation capacitor for channel 0 PPMU
35, 36	CAP_IN_1, CAP_OUT_1	Compensation capacitor for Channel 1 PPMU
44	CAP_PLL	PLL Filter capacitor
41, 40	DUT_GND_0, DUT_GND_1	Analog voltage input used to track GND at the DUT.
49, 32	EXT_FORCE, EXT_SENSE	External PMU connection pins.
37	MONITOR	PMU Monitor output pin.
CPU Interface		
24, 25, 56	CK, SDIO, STB	3-bit serial port (Clock, Data, and Strobe).
57	RESET	Chip reset.
Power Supplies		
18, 42, 63	VDD	Digital power supply.
7, 10, 21, 39, 60	GND	Device ground
27, 54	VCC	Positive analog voltage supply
26, 34, 47, 55	VEE	Negative analog voltage supply
31, 50	VCC_SV	Highest positive analog voltage supply
4, 3	VOH_0, VOL_0	Channel 0 comparator output level supplies
13, 14	VOH_1, VOL_1	Channel 1 comparator output level supplies

Pin Configuration

ISL55162
(64 LD TQFP)
TOP VIEW



Absolute Maximum Ratings

Parameter	Min	Typ	Max	Units
Power Supplies				
VCC_SV	VCC – 0.5		VEE + 16.75	V
VCC	VDD – 0.5		+10	V
VEE	–6		+0.5	V
VDD	–0.5		+5	V
VDD – VEE			+8	V
VOH	GND – 0.5		VDD + 0.5	V
VOL	GND – 0.5		VDD + 0.5	V
Output Voltage				
DOUT	VEE – 0.5		VCC_SV + 0.5	V
Output Currents				
COMP_A, COMP_B	–80		80	mA
SDIO	–20		20	mA
External References				
V_REF	GND – 0.25V		VCC + 0.25	V
EXT_SENSE	VEE – 0.5		VCC_SV + 0.5	V
EXT_FORCE	VEE – 0.5		VCC_SV + 0.5	V
Thermal Information				
Typical Thermal Resistance θJA (Note 1) - TQFP Package		39		°C/W
Typical Thermal Resistance θJC (Note 2) - TQFP Package		0.73		°C/W
Junction Temperature	–55		150	°C

CAUTION: Do not operate at or near the maximum ratings listed for extended periods of time. Exposure to such conditions may adversely impact product reliability and result in failures not covered by warranty.

NOTES:

1. θJA is measured with the component mounted on a high effective thermal conductivity test board in free air.
2. For θJC, the “case temp” location is taken at the package top center.

Recommended Operating Conditions

Parameter	Min	Typ	Max	Units
Power Supplies				
VCC_SV	VCC		+14	V
VCC	+7.75		+8.5	V
VEE	–3.5		–2	V
VDD	+3.25		+3.5	V
GND		0		V
VCC_SV – VEE	+10		16.2	V
VCC – VEE	+8		+12	V
VDD – VEE	+5.25		+7.0	V
Comparator Output Supplies				
VOH		VDD		V
VOL		GND		V
VOH – VOL	0.4		VDD – GND	V
Digital Inputs (DATA/*; EN/*)				
CK, SDIO, STB, RESET	GND		VDD	V
Driver Levels				
DVH, DVL, VTT	VEE + 1		VCC – 1	V
|DVH – DVL|, |DVH – VTT|, |DVL – VTT|		<8		V
Driver Level Restrictions in HiZ and PMU Mode				
|DOUT – DVH|		<8		V
|DOUT – DVL|		<8		V
|DOUT – VTT|		<8		V
Threshold Levels				
CVA, CVB	VEE + 1		VCC	V
CVA_PPMU, CVB_PPMU	VEE + 1		VCC_SV – 1	V
FI V-Clamp Levels				
V-Cl-Lo	VEE + 1		VCC_SV – 3	V
V-Cl-Hi	VEE + 3	>1	VCC_SV – 3	V
V-Cl-Hi – V-Cl-Lo	1			V
PPMU Levels				
V-FV	VEE + 1		VCC_SV – 1	V
External Load Capacitance			1	nF
External References				
V_REF	+2.99		+3.01	V
R_EXT	9.99		10.01	KΩ
PLL-CK	78.125		125	MHz
EXT_SENSE	VEE		VCC_SV	V
EXT_FORCE	VEE		VCC-SV	V
DUT_GND	–300		+300	mV
Miscellaneous				
Junction Temperature Range	+25		85	°C
CPU Port CK Frequency	10		25	MHz

DC Characteristics

NOTE: For all of the following DC Electrical specifications, compliance to datasheet limits is assured by one or more methods: production test, characterization and/or design.

DC Electrical Specifications - Power Supplies/Junction Temperature

VCC_SV = +13.25V, VCC = +8.5V, VEE = –3.25V, VDD = +3.5V, V_REF = +3V, DUT_GND = 0V unless otherwise specified.

Spec #	PARAMETER	TEST CONDITIONS	MIN (Note 1)	TYP	MAX (Note 1)	UNITS	Pd (TYP)
Static (PLL Disabled, All Deskew Elements Bypassed)							**2.2W/Chip**
11420	VCC_SV		30	45	60	mA	585mW
11120	VCC		15	22	35	mA	176mW
11220	VEE		60	80	100	mA	240mW
11320	VDD	VDD = +3.3V	275	350	425	mA	1155mW
Static – PLL_CK = 78.125MHz (All Deskew Elements Selected)							**2.3W/Chip**
11400	VCC_SV		30	45	60	mA	585mW
11100	VCC		15	22	35	mA	176mW
11200	VEE		60	80	100	mA	240mW
11300	VDD		300	400	500	mA	1320mW
Static – PLL_CK = 125MHz (All Deskew Elements Selected)							**2.5W/Chip**
11410	VCC_SV		30	45	60	mA	585mW
11110	VCC		15	22	35	mA	176mW
11210	VEE		60	80	100	mA	240mW
11310	VDD		340	440	540	mA	1452mW
Dynamic – Ring Oscillator Configuration – PLL_CK = 78.125MHz (All Deskew Elements Selected)							**2.5W/Chip**
12400	VCC_SV	Channels 0 and 1 configured as ring oscillators	30	45	60	mA	585mW
12100	VCC	Channels 0 and 1 configured as ring oscillators	31	41	51	mA	328mW
12200	VEE	Channels 0 and 1 configured as ring oscillators	68	88	108	mA	264mW
12300	VDD	Channels 0 and 1 configured as ring oscillators	310	410	510	mA	1352mW
Dynamic – Ring Oscillator Configuration – PLL_CK = 125MHz (All Deskew Elements Selected)							**2.7W/Chip**
12410	VCC_SV	Channels 0 and 1 configured as ring oscillators	30	45	60	mA	585mW
12110	VCC	Channels 0 and 1 configured as ring oscillators	34	44	54	mA	352mW
12210	VEE	Channels 0 and 1 configured as ring oscillators	68	88	108	mA	264mW
12310	VDD	Channels 0 and 1 configured as ring oscillators	350	450	550	mW	1485mW
Junction Temperature							
11000	Junction Temperature	PLL_CK = 125MHz; Channels 0 and 1 configured as ring oscillators; thermal equilibrium	45	78	110	°C	

NOTE:

1. Compliance to datasheet limits is assured by one or more methods: production test, characterization and/or design.

DC Electrical Specifications - CPU Port

VCC_SV = +13V, VCC = +8V, VEE = –3V, VDD = +3.3V, V_REF = 3.0V, DUT_GND = 0V

Spec #	PARAMETER	TEST CONDITIONS	MIN (Note 2)	TYP	MAX (Note 2)	UNITS
SDIO, CK, STB, RESET						
17100	VIH		2.0			V
17110	VIL				0.8	V
17120	Input Leakage Current	Tested at 0V and VDD	–100	0	+100	nA
17200	VOH (SDIO Only)	Output Current = 8mA	2.4			V
17210	VOL (SDIO Only)	Input Current = 8mA			0.4	V

NOTE:

2. Compliance to datasheet limits is assured by one or more methods: production test, characterization and/or design.

DC Electrical Specifications - Analog Pins

VCC_SV = +13V, VCC = +8V, VEE = –3V, VDD = +3.3V, V_REF = 3.0V, DUT_GND = 0V

Spec #	PARAMETER	TEST CONDITIONS	MIN (Note 4)	TYP	MAX (Note 4)	UNITS
10999	V_REF Input Current		–1	0	+1	µA
10998	DUT_GND Input Current	Tested at 0V and +3V	–20	0	+20	nA
10997	EXT_FORCE, EXT_SENSE HiZ Leakage	Tested at 0V, tested at VCC_SV and VEE	–20	0	+20	nA
	Capacitance on EXT_FORCE	All other switches open; Note 3		25		pF
	Capacitance on EXT_SENSE	All other switches open; Note 3		8		pF

NOTES:

3. Limits established by characterization and are not production tested.
4. Compliance to datasheet limits is assured by one or more methods: production test, characterization and/or design.

DC Electrical Specifications - PLL

Spec #	PARAMETER	TEST CONDITIONS	MIN (Note 8)	TYP	MAX (Note 8)	UNITS
	Differential Input Swing PLL_CK/PLL_CK*					
	VIH	PLL_CK = 78.125MHz; Notes 6 and 6	0.2		VDD	V
	VIL	PLL_CK = 78.125MHz; Notes 6 and 6	0		VDD	V
	Crossing Voltage	PLL_CK = 78.125MHz; Notes 6 and 7	0.5		2.25	V
18100	Input Leakage Current	PLL-ZA = 0, PLL-ZB = 0; Tested at 0V and VDD	–100	0	+100	nA
18110	Differential Input Resistance	PLL-ZA = 1, PLL-ZB = 0 or PLL-ZA = 0, PLL-ZB = 1; PLL_CK = 78.12MHz		105		Ω

NOTES:

5. Limits established by characterization and are not production tested.
6. VIH = 2.1V, VIL = 1.9V
7. VIH = 1.2V, VIL = 0.9V.
8. Compliance to datasheet limits is assured by one or more methods: production test, characterization and/or design.

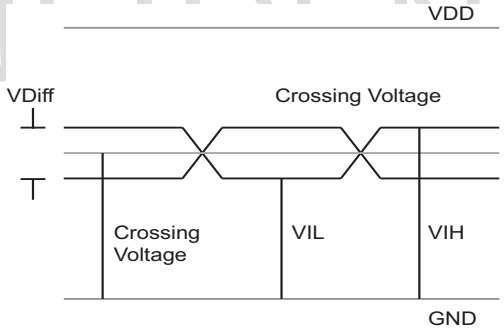


FIGURE 2.

DC Electrical Specifications– DAC Calibration

VCC_SV = +12.75V, VCC = +7.75V, VEE = –2.75V, VDD = +3.2V, V_REF = 3.00V, DUT_GND = 0V; VR1.

All DAC tests are performed after the DAC is first calibrated. The upper 5 bits of the DAC are calibrated in the sequence D11 to D15. The DAC cal bits are adjusted to make the major carries as small as possible.

Spec #	PARAMETER	TEST CONDITIONS	MIN (Note 9)	TYP	MAX (Note 9)	UNITS
16610	D15 Step Error	Cal Point: (DAC @ 8000 – 7000) – DAC LSB Test Point: Code 8000 – Code 7FFF – LSB;	–5		+5	mV
16620	D14 Step Error	Cal Point: (DAC @ 7000 – 3000) – DAC LSB; Test Point: Code 4000 – Code 3FFF – LSB;	–5		+5	mV
16630	D13 Step Error	Cal Point: (DAC @ 7000 – 5000) – DAC LS; Test Point: Code 6000 – Code 5FFF – LSB;	–5		+5	mV
16640	D12 Step Error	Cal Point: (DAC @ 7000 – 6000) – DAC LSB Test Point: Code 7000 – Code 6FFF – LSB	–5		+5	mV
16650	D11 Step Error	Cal Point: (DAC @ 7800 – 7000) – DAC LSB Test Point: Code 7800 – Code 77FF – LSB	–5		+5	mV

NOTE:

9. Compliance to datasheet limits is assured by one or more methods: production test, characterization and/or design.

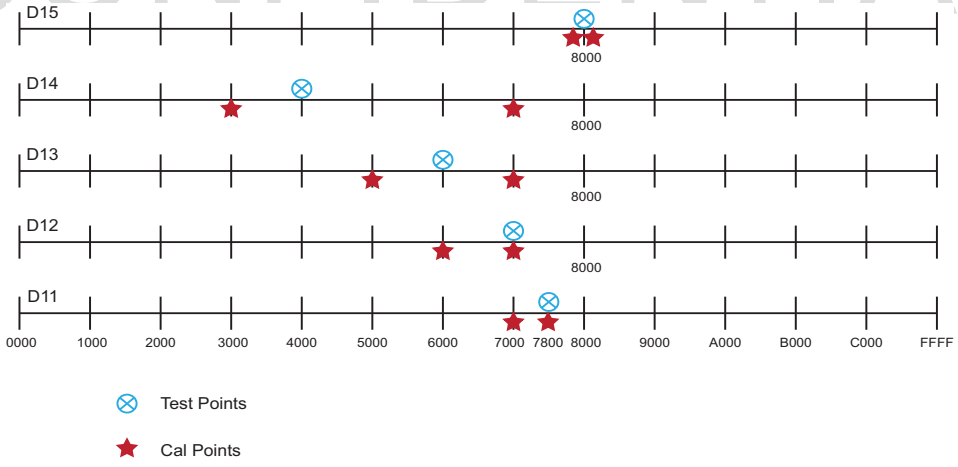


FIGURE 3.

DC Electrical Specifications - DAC

VCC_SV = +12.75V, VCC = +7.75V, VEE = –2.75V, VDD = +3.2V, V_REF = –3.0V, DUT_GND = 0V.

There are 3 on-chip internal DACs used for DC Level, DC Level Offset Correction, and DC Level Gain Correction. These on-chip DACs are not used off-chip explicitly as stand-alone outputs. Rather, they are internal resources that are used by every functional block. The DACs are tested many times over by the DC tests for driver, comparator and PMU. However, the DACs are specifically tested independently from all other functional blocks to verify basic functionality.

Spec #	PARAMETER	TEST CONDITIONS	MIN (Note 20)	TYP	MAX (Note 20)	UNITS
Level DAC Test						
16100	Span	Notes 10, 11 and 13	7.5	8.0	8.5	V
16110	Linearity Error	Notes 10, 11 and 12	–10	0	+10	mV
16120	Bit Test Error	Notes 10, 11 and 19	–10	0	+10	mV
16190	Droop Test	Note 15			2	mV/ms
16400	DAC Noise Test	Note 14			1	mV
Offset DAC Test						
16200	+Adjustment Range	Notes 10, 16 and 17	+4.8	+5.4	+6.0	% of Span
16210	–Adjustment Range	Notes 10, 16 and 17	–6.0	–5.4	–4.8	% of Span
16220	Linearity Error	Notes 10, 12 and 17	–10	0	+10	mV
16230	Bit Test Error	Notes 10, 17 and 19	–10	0	+10	mV
Gain DAC Test						
16300	+Adjustment Range	Notes 10, 16 and 18	1.07	1.125	1.15	V/V
16310	–Adjustment Range	Notes 10, 16 and 18	0.850	0.875	0.922	V/V
16320	Linearity Error	Notes 10, 12 and 18	–5	0	+5	mV/V
16330	Bit Test Error	Notes 10, 18 and 19	–5	0	+5	mV/V

NOTES:

10. DAC tests performed using the PMU in FV mode.Channel 0, VR1 measured at the monitor **output in MV mode**.
11. Offset and Gain DACs both programmed to mid-scale (Code 7FFF)
12. Linearity Test: 17 equal spaced codes relative to a straight line determined by 3/17 and 15/17 measurement points: 0000, 0FFF, **1FFF**, 2FFF, 3FFF ... CFFF, **DFFF**, EFFF, FFFF
13. Span = DAC(FFFF) - DAC (0000)
14. FV = 0V, VR2, measured at DOUT_0, RMS value
15. CPU CK turned off. 66mS delay between measurements. All DC levels tested one at a time.
16. Code 0000, FFFF relative to mid-scale (8000)
17. Level and gain DACs both programmed to mid-scale (Code 7FFF).
18. Level DAC programmed to FFFF and Offset DAC programmed to mid-scale (Code 7FFF).
19. Bit Test - Walking 1 and walking 0 to determine the correct bit weight: 1's: 8000, 4000, 2000, 2000, 0800,0400, 0200, 0100, 0080, 0040, 0020, 0010, 0008, 0004, 0002, 0001 0's: EFFF, DFFF, BFFF, 7FFF, ... FFF7, FFFB, FFFD, FFFE
20. Compliance to datasheet limits is assured by one or more methods: production test, characterization and/or design.

DC Electrical Specifications - Pin Electronics - Driver

Spec #	PARAMETER	TEST CONDITIONS	MIN (Note 23)	TYP	MAX (Note 23)	UNITS
13300	HiZ Leakage	Tested @DOUT = 0V	–5		+5	nA
13310	HiZ Leakage	Tested @ DOUT = VCC_SV – 1, VEE + 1	–15		+15	nA
13100	DVH, DVL, VTT Post Cal Error (Range 0)	VR0; Cal Points 0V, +3V; Test Points –0.5V, +1.5V, +3.5V	–10		+10	mV
13120	DVH, DVL, VTT Post Cal Error (Range 1)	VR1; Cal Points 0V, +5V; Test Points –1V, +3V, +7V	–15		+15	mV
13140	DVH, DVL, VTT Post Cal Error (Range 2)	VR2; Cal Points 0V, +5V; Test Points –2V, +3V, +7V	–25		+25	mV
	Driver Level DC PSRR	VR1; Note 22		10		mV/V
	Driver Level DC PSRR	VR2; Note 22		20		mV/V
Driver Output Impedance						
13320	DVH, DVL, VTT Nominal Output Impedance	Note 21; Rout adjust programmed to the nominal value.		50		Ω
13322	DVH, DVL Minimum Rout Adjust Output Impedance	Note 21; Rout adjust programmed to the minimum value			50	Ω
13323	DVH, DVL Maximum Rout Adjust Output Impedance	Note 21; Rout adjust programmed to the maximum value	45			Ω
13324	VTT Minimum Rout Adjust Output Impedance	Note 21; Rout adjust programmed to the minimum value			50	Ω
13325	VTT Maximum Rout Adjust Output Impedance	Note 21; Rout adjust programmed to the maximum value	45			Ω
Driver Output Current						
13321	DC Output Current	Driver at 5V shorted to 0V Driver at 0V shorted to 5V	+35 –35			mA mA
	AC Output Current	Note 22	±70			mA
Differential Inputs DATA & EN						
	VIH	VIH = 2.1V, VIL = 1.9V VIH = 1.1V, VIL = 0.9V Note 22			VDD	V
	VIL	VIH = 2.1V, VIL = 1.9V VIH = 1.1V, VIL = 0.9V Note 22	0			V
13200	Input Leakage Current	Data0(1)-ZA = 0; Data0(1)-ZB = 0; En0(1)-ZA = 0; En0(1)-ZB = 0; tested at 0V and VDD	–100	0	+100	nA
	Differential Input Resistance	Data0(1)-ZA = 1; Data0(1)-ZB = 0; En0(1)-ZA = 1; En0(1)-ZB = 0 *or* Data0(1)-ZA = 0; Data0(1)-ZB = 1; En0(1)-ZA = 0; En0(1)-ZB = 1		105		Ω
SV Input						
13210	VIH		2.0			V
13220	VIL				0.8	V
13230	Input Leakage Current	Tested at 0V and VDD	–100	0	+100	nA

NOTE:

21. DVH = 3.0V, 19.2mA sourced @ DOUT; VTT = 1.5V, 19.2mA sunk @ DOUT; DVL = 0V, 19.2mA sunk @ DOUT
22. Limits established by characterization and are not production tested.
23. Compliance to datasheet limits is assured by one or more methods: production test, characterization and/or design.

DC Electrical Specifications – Pin Electronics - Comparator

VCC_SV = +12.75V, VCC = +7.75V, VEE = –2.75V, VDD = +3.2V, VREF = 3.00V, DUT_GND = 0V unless otherwise specified.

The window comparator thresholds are tested using a binary search algorithm at the digital outputs COMP_A and COMP_B.

Spec #	PARAMETER	TEST CONDITIONS	MIN (Note 25)	TYP	MAX (Note 25)	UNITS
14500	Post Calibration Threshold Error, VR0	See Table 1, VR0. Test the comparator outputs using a binary search	–10		+10	mV
14510	Post Calibration Threshold Error, VR1	See Table 1, VR1. Test the internal references via Test & Cal Mux	–15		+15	mV
14520	Post Calibration Threshold Error, VR2	See Table 1, VR2. Test the comparator outputs using a binary search	–25		+25	mV
13360	Comparator Output Impedance	VCC_SV = +13V, VCC = +8V, VEE = –3.00V, VDD = +3.2V, V_REF = 3.0V, DUT_GND = 0V; Sourcing 20mA; Sinking 20mA		50		Ω
	Input Capacitance	Note 24		4		pF

NOTE:

24. Limits established by characterization and are not production tested.

25. Compliance to datasheet limits is assured by one or more methods: production test, characterization and/or design.

TABLE 1. Comparator Threshold

V Range	Cal Points	Test Points
VR0	0V +3V	–.5V +1.5V +3.5V
VR1	0V +5V	–1V +3V +7V
VR2	0V +5V	–1V +5V +7V

DC Electrical Specifications– PMU (Force Voltage)

The sequence of events performed for FV Testing is:

1. Program FV
2. Force current at DOUT_# using tester PMU
3. Measure the voltage at DOUT_#.

FV Tests:

1. VR0 tested in IR5 (no load)
2. VR1 tested in IR5 (no load)
3. VR2 tested in IR6 and IR7 (no load)
4. VR2 tested in IR0 – IR7 (at maximum load).

VCC_SV = +12.75V, VCC = +7.75V, VEE = –2.75V, VDD = +3.2V, V_REF = 3.0V, DUT_GND = 0.

Spec #	PARAMETER	TEST CONDITIONS	MIN (Note 28)	TYP	MAX (Note 28)	UNITS
14250	Output Force Error, VR0	FV VR0 test points	–10		+10	mV
14252	Output Force Error, VR1	FV VR1 test points	–15		+15	mV
14265	Output Force Error, VR2	FV VR2 test points	–25		+25	mV
	FV Temperature Coefficient	Note 29		–200		µA/°C
14208	PMU Short Circuit Test	Note 26; FV VR1, IR7	85		180	mA
14209	PMU Short Circuit Test	Note 27; FV VR1, IR7	–85		–180	mA

NOTE:

26. FV = 10V, Tester PMU = 0V
27. FV = 0V, Tester PMU = 10V
28. Compliance to datasheet limits is assured by one or more methods: production test, characterization and/or design.
29. Limits established by characterization and are not production tested.

TABLE 2. Force Voltage

Range	Cal Points	FV Test Points
VR0 IR5	0V/0µA +3V/0µA	–.5V/0µA +1.5V/0µA +3.5V/0µA
VR1 IR5	0V/0µA +5V/0µA	–1V/0µA +3V/0µA +7V/0µA
VR2 IR6, IR7	0V/0µA +10V/0µA	–1V/0µA +6V/0µA +11V/0µA
VR2 IR0 – IR7	0V/0µA +10V/0µA	+2V/–Imax +8V/+Imax

DC Electrical Specifications – PMU (Measure Current)

MI tested in VR2, IR0 –IR7. MI tested post 2-point software calibration.

VCC_SV = +12.75V, VCC = +7.75V, VEE = –2.75V, VDD = +3.2V, VREF = 3.00V, DUT_GND = 0V.

Spec #	PARAMETER	TEST CONDITIONS	MIN (Note 32)	TYP	MAX (Note 32)	UNITS
MI (Post Calibration)						
14100	Measure Current Error, IR0	See Table 3; Note 30	–25		+25	nA
14110	Measure Current Error, IR1	See Table 3; Note 30	–80		+80	nA
14120	Measure Current Error, IR2	See Table 3; Note 30	–320		+320	nA
14130	Measure Current Error, IR3	See Table 3; Note 30	–1.25		+1.25	µA
14140	Measure Current Error, IR4	See Table 3; Note 30	–5		+5	µA
14150	Measure Current Error, IR5	See Table 3; Note 30	–20		+20	µA
14160	Measure Current Error, IR6	See Table 3; Note 30	–80		+80	µA
14170	Measure Current Error, IR7	See Table 3; Note 30	–320		+320	µA
MI Temperature Coefficient						
	IR0	Note 31		225		pA/°C
	IR1	Note 31		1		nA/°C
	IR2	Note 31		4		nA/°C
	IR3	Note 31		16		nA/°C
	IR4	Note 31		64		nA/°C
	IR5	Note 31		250		nA/°C
	IR6	Note 31		1		µA/°C
	IR7	Note 31		4		µA/°C

NOTE:

30. 2-point software CMRR calibration.
31. Limits established by characterization and are not production tested.
32. Compliance to datasheet limits is assured by one or more methods: production test, characterization and/or design.

TABLE 3. Measure Current

Range	Cal Points	Test Points
VR2	+5V/+0.8 x Imax +5V/–0.8 x Imax	–1V/0µA +11V/0µA +2V/–Imax +8V/+Imax

DC Electrical Specifications –PMU (Force Current)

The sequence of events performed for FI Testing is:

1. Program FI to the desired current.
2. Force voltage with external PMU at DOUT_#.
3. Measure the current at DOUT_#.

FI is tested in all 8 current ranges.

VCC_SV = +12.75V, VCC = +7.75V, VEE = –2.75V, VDD = +3.2V, VREF = 3.00V, DUT_GND = 0V.

Spec #	PARAMETER	TEST CONDITIONS	MIN (Note 35)	TYP	MAX (Note 35)	UNITS
Post Calibration FI Error						
14101	Force Current Error, IR0	See Table 4; Note 33	–20		+20	nA
14111	Force Current Error, IR1	See Table 4; Note 33	–80		+80	nA
14121	Force Current Error, IR2	See Table 4; Note 33	–320		+320	nA
14131	Force Current Error, IR3	See Table 4; Note 33	–1.25		+1.25	µA
14141	Force Current Error, IR4	See Table 4; Note 33	–5		+5	µA
14151	Force Current Error, IR5	See Table 4; Note 33	–20		+20	µA
14161	Force Current Error, IR6	See Table 4; Note 33	–80		80	µA
14171	Force Current Error, IR7	See Table 4; Note 33	–320		+320	µA
FI Temperature Coefficient						
	IR0	Note 34		225		pA/°C
	IR1	Note 34		1		nA/°C
	IR2	Note 34		4		nA/°C
	IR3	Note 34		16		nA/°C
	IR4	Note 34		64		nA/°C
	IR5	Note 34		250		nA/°C
	IR6	Note 34		1		µA/°C
	IR7	Note 34		4		µA/°C

NOTE:

33. Post CMRR calibration for FI.
34. Limits established by characterization and are not production tested.
35. Compliance to datasheet limits is assured by one or more methods: production test, characterization and/or design.

TABLE 4. Force Current

FI Testing	Cal Points	FI Test Points
IR0 – IR7	+5V/+0.8 • Imax +5V/–0.8 • Imax	–1V/0µA +11V/0µA +2V/–Imax +8V/+Imax

DC Electrical Specifications – Measure Voltage (Monitor)

The sequence of events performed for the MONITOR is:

1. Program FV to the desired voltage (in VR2, IR5, Iload = 0)
2. Measure the voltage at DOUT_#.
3. Measure the voltage at MONITOR
4. Calculate the difference to determine the error.

MONITOR is tested post 2-point software calibration.

Spec #	PARAMETER	TEST CONDITIONS	MIN (Note 38)	TYP	MAX (Note 38)	UNITS
14710	HiZ Leakage Current	Note 36; Tested at MONITOR = 0V, VCC_SV, VEE	–20	0	+20	nA
14700	Output Impedance	Note 37; Tested at +5V, Iout = 0µA, 2mA		0.6	1.0	kΩ
14720	Voltage Error	See Table 5; Note 37	–10		+10	mV
14741	DUT_GND Error	Note 37; DUT_GND = ±300mV, FV Mode, V-FV = +3V, measured at Test & Cal relative to GND	–5		+5	mV

NOTES:

36. VCC_SV = +13V, VCC = +8V, VEE = –3V, VDD = 3.3V, V_REF = 3.0V, DUT_GND = 0V.
37. VCC_SV = +12.75V, VCC = +7.75V, VEE = –2.75V, VDD = +3.2V, VREF = 3.00V, DUT_GND = 0V.
38. Compliance to datasheet limits is assured by one or more methods: production test, characterization and/or design.

TABLE 5. Measure Voltage

MV Testing	Cal Points	MV Test Points
IR5	0V/0µA +10V/0µA	–1V/0µA +5V/0µA +11V/0µA

DC Electrical Specifications – Measure Voltage (Comparator)

VCC_SV = +12.75V, VCC = +7.75V, VEE = –2.75V, VDD = +3.2V, VREF = 3.00V, DUT_GND = 0V.

Spec #	PARAMETER	TEST CONDITIONS	MIN (Note 43)	TYP	MAX (Note 43)	UNITS
14600	Threshold Error, VR0	See Table 6; Notes 39	–10		+10	mV
14620	Threshold Error, VR1	See Table 6; Notes 40	–15		+15	mV
14640	Threshold Error, VR2	See Table 6; Notes 41	–25		+25	mV
14660	Threshold Error, VIR	See Table 6; Notes 42	–8		+8	mV
	Threshold Temperature Coefficient	VR1; Note 44		100		µV/°C

NOTES:

39. PMU comparator threshold test points, VR0, test the comparator outputs using a binary search.
40. PMU comparator threshold test points, VR1, test the internal references via Test & Cal Mux.
41. PMU comparator threshold test points, VR2, test the comparator outputs using a binary search.
42. PMU comparator threshold test points, VIR, test the internal references via Test & Cal Mux.
43. Compliance to datasheet limits is assured by one or more methods: production test, characterization and/or design.
44. Limits established by characterization and are not production tested.

TABLE 6. PPMU Comparator Threshold

V Range	Cal Points	Test Points
VR0	0V +3V	–.5V +1.5V +3.5V
VR1	0V +5V	–1V +3V +7V
VR2	0V +10V	–1V +6V +11V
VIR	–.8V +.8V	–1V 0V +1V

DC Electrical Specifications – Voltage Clamp Low

VCC_SV = +12.75V, VCC = +7.75V, VEE = –2.75V, VDD = +3.2V, VREF = 3.00V, DUT_GND = 0V.

Spec #	PARAMETER	TEST CONDITIONS	MIN (Note 45)	TYP	MAX (Note 45)	UNITS
14400	Low Voltage Clamp Error, VR0	See Table 7, VR0	–100		+100	mV
14410	Low Voltage Clamp Error, VR1	See Table 7, VR1	–100		+100	mV
14420	Low Voltage Clamp Error, VR2	See Table 7, VR2	–100		+100	mV

NOTE:

45. Compliance to datasheet limits is assured by one or more methods: production test, characterization and/or design.

TABLE 7. Low Voltage Clamps

V Range	Cal Points	Test Points
VR0	0V +2V	–.5V +1.5V +2.5V
VR1	0V +5V	–1V +3V +6V
VR2	0V +9V	–1V +6V +10V

DC Electrical Specifications – Voltage Clamp High

VCC_SV = +12.75V, VCC = +7.75V, VEE = –2.75V, VDD = +3.2V, VREF = 3.00V, DUT_GND = 0V.

Spec #	PARAMETER	TEST CONDITIONS	MIN (Note 46)	TYP	MAX (Note 46)	UNITS
14440	High Voltage Clamp Error, VR0	See Table 8, VR0	–100		+100	mV
14450	High Voltage Clamp Error, VR1	See Table 8, VR1	–150		+150	mV
14460	High Voltage Clamp Error, VR2	See Table 8, VR2	–200		+200	mV

NOTE:

46. Compliance to datasheet limits is assured by one or more methods: production test, characterization and/or design.

TABLE 8. High Voltage Clamps

V Range	Cal Points	Test Points
VR0	+1V +3V	+1V +1.5V +3.5V
VR1	+1V +5V	+1V +3V +7V
VR2	+1V +8V	+1V +5V +11V

DC Electrical Specifications – CMRR

VCC_SV = +12.75V, VCC = +7.75V, VEE = –2.75V, VDD = +3.2V, VREF = 3.00V, DUT_GND = 0V. FV Mode, VR2, Iout = 0 (open switch), tight loop, measure MI @ MONITOR, test @ +1V and +9V.

Spec #	PARAMETER	TEST CONDITIONS	MIN (Note 47)	TYP	MAX (Note 47)	UNITS
14203	Uncalibrated CMRR, IR0	IR0	–4		+4	nA/V
14213	Uncalibrated CMRR, IR1	IR1	–16		+16	nA/V
14223	Uncalibrated CMRR, IR2	IR2	–64		+64	nA/V
14233	Uncalibrated CMRR, IR3	IR3	–256		+256	nA/V
14243	Uncalibrated CMRR, IR4	IR4	–1024		+1024	nA/v
14253	Uncalibrated CMRR, IR5	IR5	–4		+4	µA/V
14263	Uncalibrated CMRR, IR6	IR6	–16		+16	µA/V
14273	Uncalibrated CMRR, IR7	IR7	–64		+64	µA/V

NOTE:

47. Compliance to datasheet limits is assured by one or more methods: production test, characterization and/or design.

DC Electrical Specifications – Resistor Values

VCC_SV = +13V, VCC = +8V, VEE = –3V, VDD = 3.3V, V_REF = 3.0V, DUT_GND = 0V.

Spec #	PARAMETER	TEST CONDITIONS	MIN (Note 48)	TYP	MAX (Note 48)	UNITS
Sense Resistors						
19000	IR0			500		kΩ
19010	IR1			125		kΩ
19020	IR2			31.25		kΩ
19030	IR3			7.81		kΩ
19040	IR4			1.95		kΩ
19050	IR5			500		Ω
19060	IR6			125		Ω
19070	IR7			31.25		Ω
On-Chip FET Switches						
19100	RT PMU (SV) Switch		30	50	85	Ω
19110	External Force Switch		30	50	85	Ω
19120	External Sense Switch		4.3	8	11	kΩ

NOTE:

48. Compliance to datasheet limits is assured by one or more methods: production test, characterization and/or design.

AC Characteristics

NOTE: For all of the following AC Electrical specifications, compliance to datasheet limits is assured by one or more methods: production test, characterization and/or design.

AC Electrical Specifications – CPU Port

VCC_SV = +12.75V, VCC = +7.75V, VEE = –2.75V, VDD = +3.2V, V_REF = 3.0V, DUT_GND = 0V

Spec #	PARAMETER	TEST CONDITIONS	MIN (Note 49)	TYP	MAX (Note 49)	UNITS
	Set-Up Time					
27100	SDIO to Rising CK		7			ns
27110	STB to Rising CK		7			ns
	Hold Time					
27120	Rising CK to SDIO		7			ns
27130	Rising CK to STB		7			ns
27140	CK Minimum Pulse Width High		20			ns
27150	CK Minimum Pulse Width Low		18			ns
27160	CK Period		40		100	ns
	Propagation Delay Rising CK to SDIO Out - Tpd				7	ns
27170	Reset Minimum Pulse Width		100			ns

NOTE:

49. Compliance to datasheet limits is assured by one or more methods: production test, characterization and/or design.

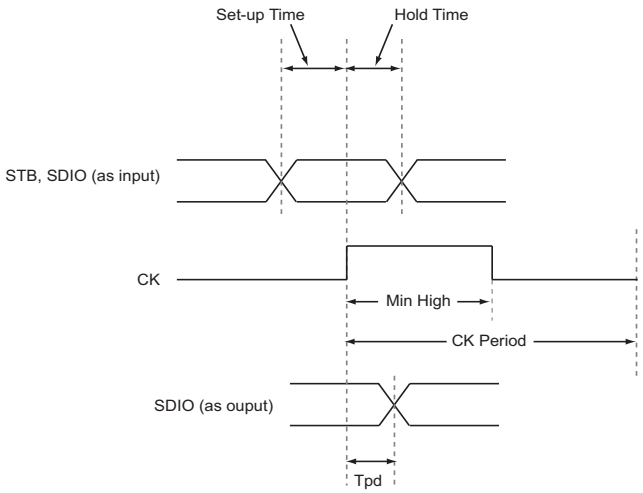


FIGURE 4.

AC Electrical Specifications – Pin Electronics - Driver

DVH = 3V, DVL = 0V, ≤ 12; 50Ω to ground; 20% - 80% unless otherwise specified.

Spec #	PARAMETER	TEST CONDITIONS	MIN (Note 51)	TYP	MAX (Note 51)	UNITS
22200	**Rise/Fall Times** 2V Swing	DVH = 2V, DVL = 0V, ≤ 12 inches; 50Ω to ground; 20% - 80%	0.5	0.8	1.1	ns
	Minimum Pulse Width	Bypass mode; PLL Disabled, Note 50		1.25		ns
	Minimum Pulse width	All deskew elements selected; PLL_CK = 100MHz; Note 50		1.5		ns
	Propagation Delay DATA to DOUT	All deskew elements bypassed; Note 50		8.6		ns
	EN to DOUT	EN to DOUT; tested at 2.25V and 0.75V; Dr-Mode = 1; all deskew elements bypassed; Note 50		8.4		ns
	SV to DOUT	Note 50		16		ns
	Bypass Mode DATA to DOUT EN to DOUT	 Bypass mode. Bypass mode.		 4.5 4.5		 ns ns
	Output Capacitance @ DOUT	VCC_SV = +13V, VCC = +8V, VEE = -3V, VDD = +3.3V, V_REF = 3.0V, DUT_GND = 0V; Note 50		5		pF
	ΔTpd vs. Temperature	All deskew elements bypassed, PLL_CK = 100MHz; Note 50		4.2		ps/°C
	ΔTpd vs. Duty Cycle	T = 100ns, duty cycle varies from 1.65% to 98.35%; Bypass mode; Note 50		100		ps
	ΔTpd vs. Duty Cycle	T = 100ns, duty cycle varies from 2% to 98%; Bypass mode; Note 50		100		ps
	ΔTpd vs. Duty Cycle	T = 100ns, duty cycle varies from 2% to 98%; All delay elements invoked and programmed to maximum delay; PLL_CK = 100MHz; Note 50		200		ps
	ΔTpd vs. Duty Cycle	T = 100ns, duty cycle varies from 2.5% to 97.5%; All delay elements invoked and programmed to maximum delay; PLL_CK = 100MHz; Note 50		250		ps
	Driver Path Jitter (DATA to DOUT) 1σ	Bypass mode; Note 50 All delay elements invoked and programmed to maximum delay; Note 50		8 12		ps ps

NOTES:

50. Limits established by characterization and are not production tested.

51. Compliance to datasheet limits is assured by one or more methods: production test, characterization and/or design.

AC Electrical Specifications – Pin Electronics (COMPARATOR)

Limits established by characterization and are not production tested.

Spec #	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
	Minimum Pulse Width	Bypass mode		1.25		ns
	Minimum Pulse Width	All delay elements programmed to maximum value		1.5		ns
	Comparator Equivalent Bandwidth	Note 52; VTT Active, VTT = 0V		600		MHz
	Comparator Equivalent Bandwidth	Note 52; VTT HiZ		750		MHz
	Propagation Delay (DOUT to COMP_A, COMP_B)	All deskew elements bypassed. No elements selected.		8		ns
	Propagation Delay (DOUT to COMP_A, COMP_B)	Bypass mode		5		ns
	Output Rise Time (COMP_A, _B)			800		ps
	ΔTpd vs. Duty Cycle	3V input, 100 ns period, 1.25% to 98.75%, VR2; Bypass mode		100		ps
	ΔTpd vs. Duty Cycle	3V input, 100 ns period, 1.65% to 98.35%, VR2; All delay elements programmed to maximum value; PLL_CK = 100MHz		450		ps
	ΔTpd vs. Duty Cycle	3V input; 100 ns period, 2% to 98%, VR2, All delay elements programmed to maximum value; PLL_CK = 100MHz		200		ps
	ΔTpd vs. Temperature	All delay elements programmed to maximum value; PLL_CK = 100MHz		2		ps/°C
	Comparator Path Jitter (DOUT to COMP_A, _B) 1σ	Bypass mode		8		ps
	Comparator Path Jitter (DOUT to COMP_A, _B) 1σ	All delay elements programmed to maximum value; PLL_CK = 100MHz		12		ps

NOTE:

52. 10% - 90% BW = 0.35/((Tr-input)*2 – (Tr-measured)*2)*0.5; 3V input; Tr/Tf(input) = 1.2ns

AC Electrical Specifications – PPMU

Limits established by characterization and are not production tested.

Spec #	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Voltage Force Settling Time						
	IR0	Note 53		4		ms
	IR1	Note 53		1		ms
	IR2	Note 53		400		µs
	IR3	Note 53		100		µs
	IR4	Note 53		25		µs
	IR5	Note 53		20		µs
	IR6	Note 53		20		µs
	IR7	Note 53		20		µs
Current Force Settling Time						
	IR0	Note 54		350		µs
	IR1	Note 54		170		µs
	IR2	Note 54		130		µs
	IR3	Note 54		130		µs
	IR4	Note 54		130		µs
	IR5	Note 54		130		µs
	IR6	Note 54		130		µs
	IR7	Note 54		130		µs
MI Settling Time (through MONITOR)						
	IR0	Note 54		250		µs
	IR1	Note 54		130		µs
	IR2	Note 54		130		µs
	IR3	Note 54		130		µs
	IR4	Note 54		130		µs
	IR5	Note 54		130		µs
	IR6	Note 54		130		µs
	IR7	Note 54		130		µs
MV Settling Time (through MONITOR)		0V to 5V input at DOUT, Tr = 2ns		5		µs

NOTES:

53. 1nF load. 0V to 5V input signal. PMU Sense = DOUT

54. -Imax to +Imax into an external resistive load equal to Rsense for each current range.

AC Electrical Specifications – Ring Oscillator Delay/PLL Lock

All deskew elements bypassed. No elements selected. PLL_CK = 100MHz. Channel 0 and Channel 1 configured as ring oscillators.

Spec #	PARAMETER	TEST CONDITIONS	MIN (Note 57)	TYP	MAX (Note 57)	UNITS
20000	Ring Oscillator Loop Delay	Note 55 Ring triggered on a rise edge. Ring triggered on a falling edge.	16	22	28	ns

NOTES:

55. Ring configured:
    1) DATA through Comp A
    2) DATA through Comp B
    3) EN through Comp A
    4) EN through Comp B
56. The loop time measured when the channel is configured as a ring oscillator does *not* indicate the total round trip time of the pin electronics as some circuitry in the driver signal paths are bypassed, and the circuitry of the ring oscillator control logic is inserted into the overall loop. The total delay measured in this configuration is used as a figure of merit to verify part-to-part AC performance.
57. Compliance to datasheet limits is assured by one or more methods: production test, characterization and/or design.

AC Electrical Specifications – Delay Elements (Fine Delay)

VCC_SV = +13V, VCC = +8V, VEE = –3V, VDD = +3.3V, V_REF = 3.0V, DUT_GND = 0V. PLL_CK = 100MHz; Channel 0 and Channel 1 configured as ring oscillators

Spec #	PARAMETER	TEST CONDITIONS	MIN (Note 59)	TYP	MAX (Note 59)	UNITS
DATA, EN Delay Blocks						
25300	Tmin (Tpd+, Tpd– with FD = 0)		1.5	2.5	3.5	ns
25310	Full Scale Delay (Tpd+, Tpd–)		350	650	950	ps
	Resolution	Note 58		40		ps
COMP A, B Delay Blocks						
25320	Tmin (Tpd+, Tpd– with FD = 0)		1.5	2.5	3.5	ns
25330	Full Scale Delay (Tpd+, Tpd–)		350	600	850	ps
	Resolution	Note 58		40		ps

NOTES:

58. Limits established by characterization and are not production tested.
59. Compliance to datasheet limits is assured by one or more methods: production test, characterization and/or design.

AC Electrical Specifications – Delay Elements (Coarse Delay)

VCC_SV = +13V, VCC = +8V, VEE = –3V, VDD = +3.3V, V_REF = 3.0V, DUT_GND = 0V. PLL_CK = 100MHz; Channel 0 and Channel 1 configured as ring oscillators

Spec #	PARAMETER	TEST CONDITIONS	MIN (Note 61)	TYP	MAX (Note 61)	UNITS
DATA, EN						
25100	Tmin (Tpd+, Tpd– with CD = 0)		1.5	2.5	3.5	ns
25110	Full Scale Delay (Tpd+, Tpd–)		8.0	9.6875	12.0	ns
	Resolution	Note 60		312.5		ps
COMP A, B						
25120	Tmin (Tpd+, Tpd– with CD = 0)		1.5	2.5	3.5	ns
25130	Full Scale Delay (Tpd+, Tpd–)		8.0	9.6875	12.0	ns
	Resolution	Note 60		312.5		ps

NOTES:

60. Limits established by characterization and are not production tested.

61. Compliance to datasheet limits is assured by one or more methods: production test, characterization and/or design.

AC Electrical Specifications – Fine Falling Edge Adjust

VCC_SV = +13V, VCC = +8V, VEE = –3V, VDD = +3.3V, V_REF = 3.0V, DUT_GND = 0V. PLL_CK = 100MHz; Channel 0 and channel 1 configured as ring oscillators

Spec #	PARAMETER	TEST CONDITIONS	MIN (Note 63)	TYP	MIN (Note 63)	UNITS
Driver (DATA, EN)						
25400	Tmin (Tpd+, Tpd–; Sel-XX-FFEA = 0; Code = 1000)		2.8	3.8	4.8	ns
25410	ΔTpd– Full Scale Acceleration (Code 0000 relative to 1000)		–550	–350	–150	ps
25420	ΔTpd– Full Scale Delay (Code 1111 relative to 1000)		150	350	550	ps
	Resolution	Note 62		40		ps
	Tpd+ Error (ΔTpd+ vs. all FFEA codes)	Note 62		<20		ps
Comparator (COMP_A, COMP_B)						
25430	Tmin (Tpd+, Tpd–; Sel-XX-FFEA = 0; Code = 01000)		4.3	5.3	6.3	ns
25440	ΔTpd– Full Scale Acceleration (Code 00000 relative to 01000)		–950	–650	–350	ps
25450	ΔTpd– Full Scale Delay (Code 11111 relative to 01000)		350	650	950	ps
	Resolution	Note 62		40		ps
	Tpd+ vs. all FFEA	Note 62		<30		ps

NOTES:

62. Limits established by characterization and are not production tested.

63. Compliance to datasheet limits is assured by one or more methods: production test, characterization and/or design.

AC Electrical Specifications – Coarse Falling Edge Adjust

VCC_SV = +13V, VCC = +8V, VEE = –3V, VDD = +3.3V, V_REF = 3.0V, DUT_GND = 0V. PLL_CK = 100MHz; Channel 0 and Channel 1 configured as ring oscillators

Spec #	PARAMETER	TEST CONDITIONS	MIN (Note 65)	TYP	MAX (Note 65)	UNITS
DATA, EN						
25200	Tmin (Tpd+, Tpd–; Sel-XX-CFEA = 0; Code = 1000)		3.0	4.3	5.6	ns
25210	ΔTpd– Full Scale Acceleration (Code 0000 relative to 1000)		–3.3	–2.7	–2.1	ns
25220	ΔTpd– Full Scale Delay (Code 1111 relative to 1000)		+1.6	+2.3	+3.0	ns
	Resolution	Note 64		312.5		ps
	ΔTpd+ vs. CFEA Codes (all codes except 8 and 9)	Note 64		<50		ps
	ΔTpd+ vs. CFEA Codes (Codes 8 and 9)	Note 64		<200		ps

NOTES:

64. Limits established by characterization and are not production tested.

65. Compliance to datasheet limits is assured by one or more methods: production test, characterization and/or design.

Chip Overview

The ISL55162 (Venus 3) is a highly integrated System-on-a-Chip pin electronics solution aimed at incorporating every analog function, along with some digital support circuitry, required on a per channel basis for Automated Test Equipment (see picture below.) The interface, control and I/O of the chip are all digital; all analog circuitry is inside the chip. Two complete tester channels are integrated into each chip.

ISL55162 is pin and functionally compatible with Venus and Venus 3.

CPU Control

All chip set up, configuration control, the writing to and reading back of the internal registers and memory is controlled through the 3 bit serial data CPU port. The CPU port is typically used to set up the operating mode of the chip prior to executing a test, or to change modes during a test.

An internal register chart (Memory Map - listed later in the data sheet) documents all programmable control signals and their addresses, and shows how to program each internal signal.

High Speed Control

All real time control and observation is accomplished via the real time input and output signals:

- DATA_0, DATA_1 (Differential Inputs)
- EN_0, EN_1 (Differential Inputs)
- SV_0, SV_1 (Single Ended Inputs)
- COMP_A_0, COMP_B_0 (Differential Outputs)
- COMP_A_1, COMP_B_1 (Differential Outputs)

Analog Reference

All on chip analog functions are related to one of several off chip precision reference inputs:

- PLL_CK
- R_EXT
- V_REF.

These external references are used to provide accurate and stable analog circuit performance that does not vary over time, temperature, supply voltage, or process changes.

External Signal Nomenclature

All input and output pins, when referred to in the data sheet or in any circuit diagram, use the following naming conventions:

1) all capital letters (i.e. DATA, CK, SDIO)

2) underscores for clarity (i.e. EXT_SENSE, EN_0)

3) shown next to an I/O circle in any schematic.

CPU Programmed Control Line Nomenclature

Any internal signal, DAC level, or control signal which is programmed via the CPU port uses a different nomenclature:

1) the first letter in a word is always a capital letter

2) subsequent letters within the same word are small

3) dashes (but never an underscore) for clarity

4) NOT shown with an I/O circle in any schematic.

Control lines, internal registers, and other internal signals, which are programmable by the CPU port, are listed in the Memory Map table.

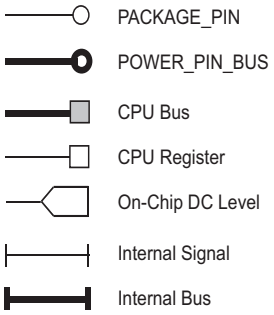


FIGURE 5.

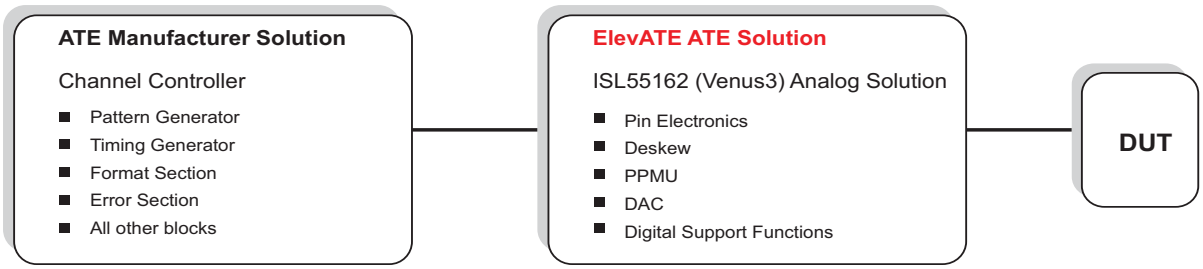
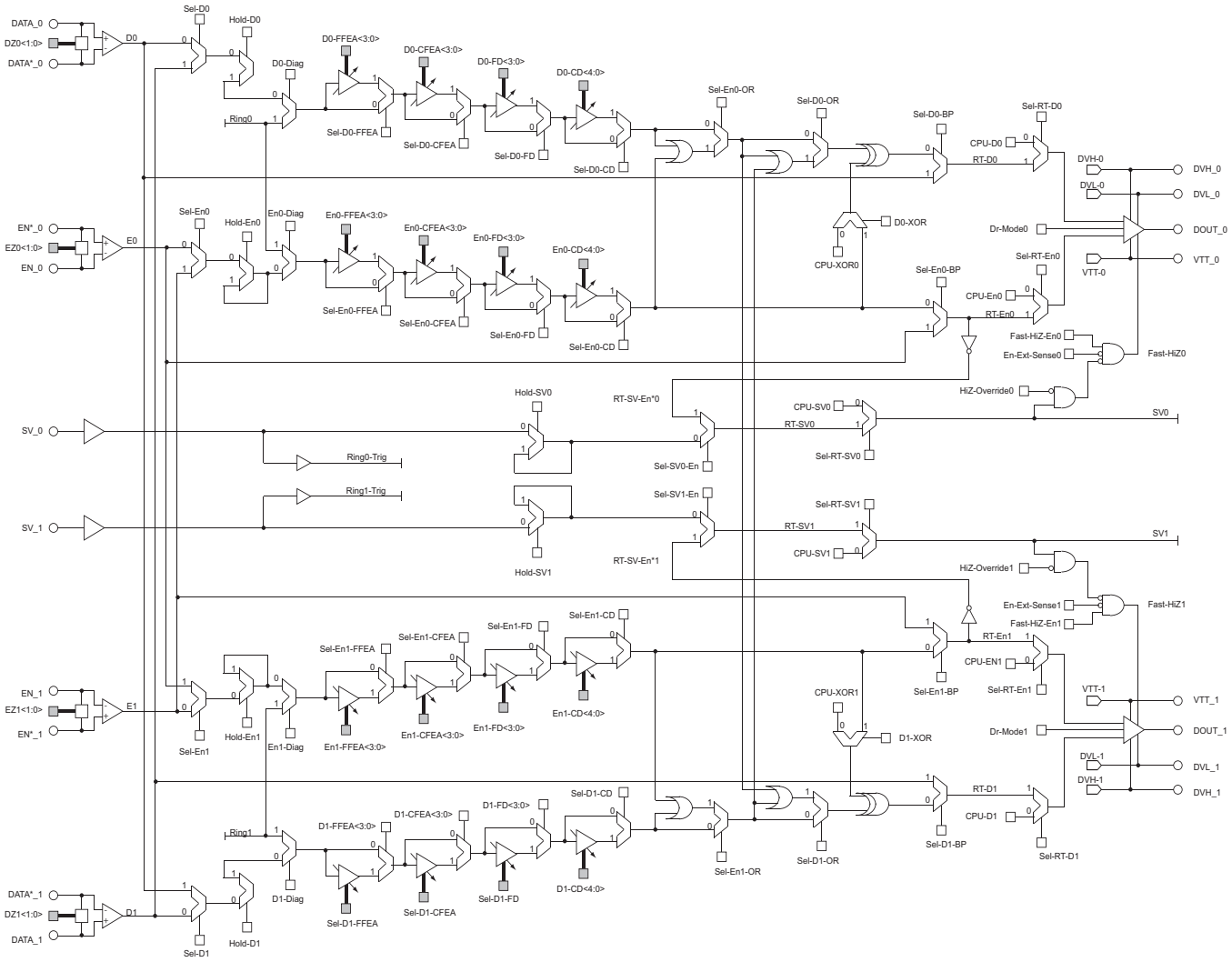


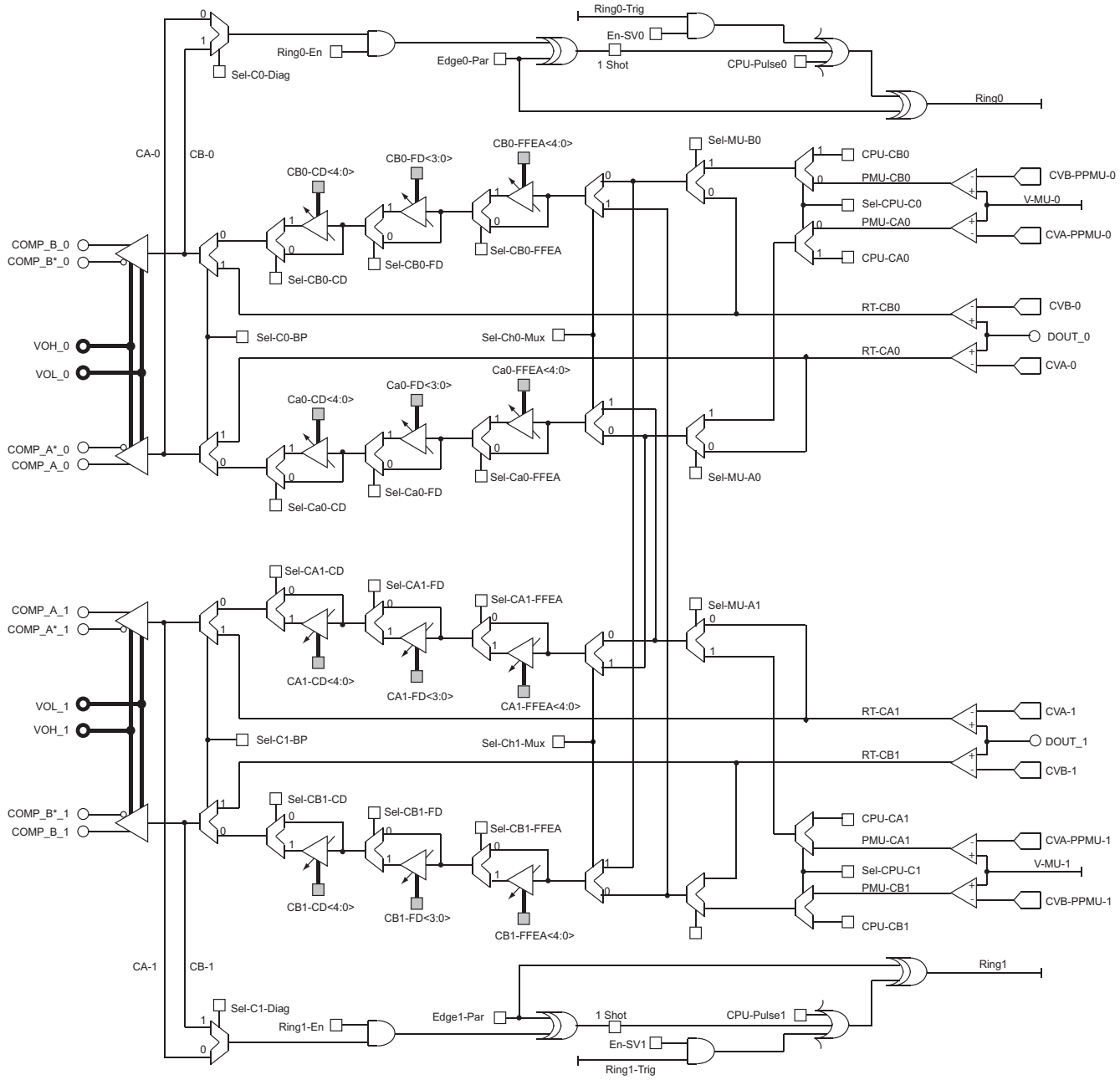
FIGURE 6.

Block Diagrams

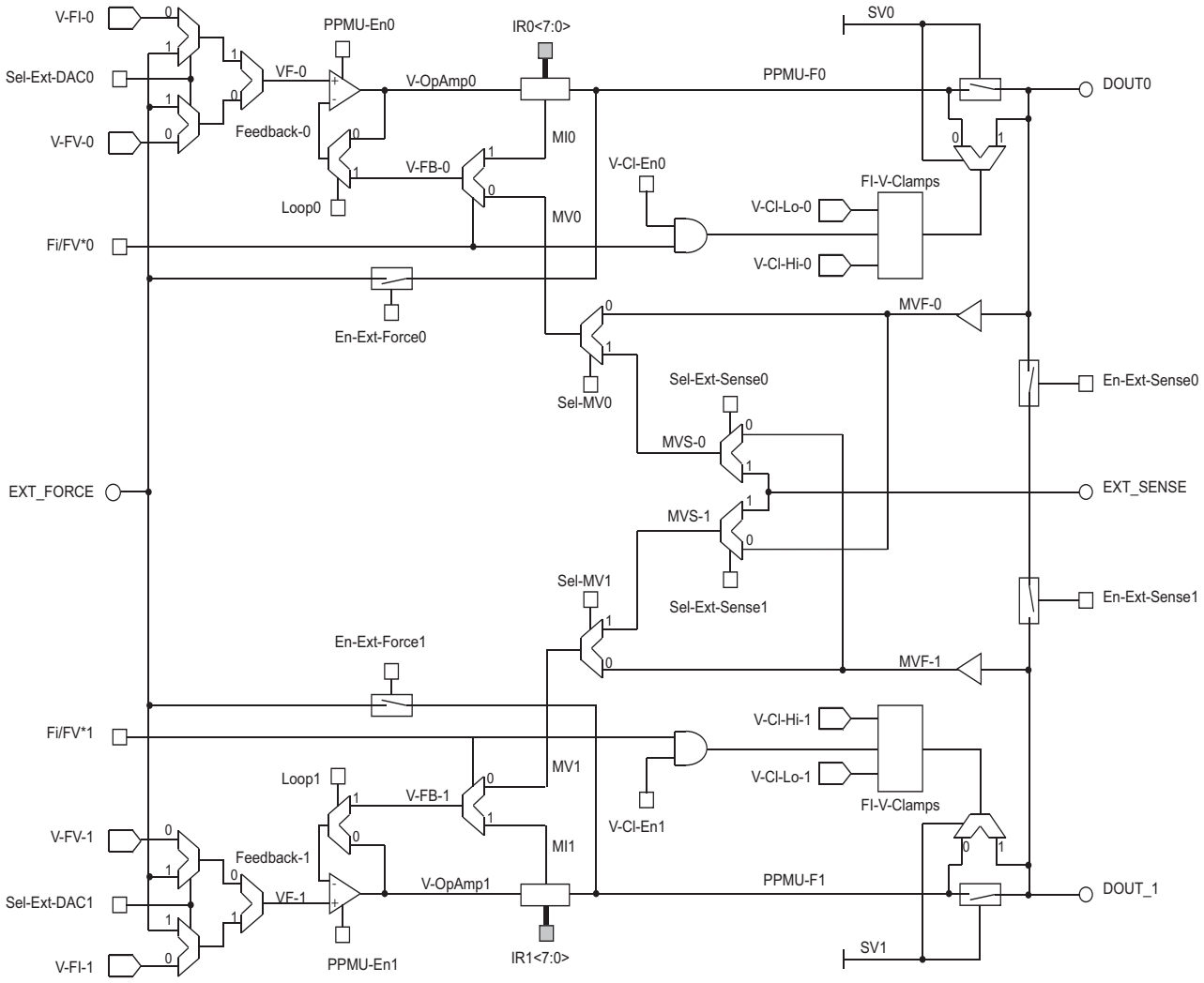
Driver Path



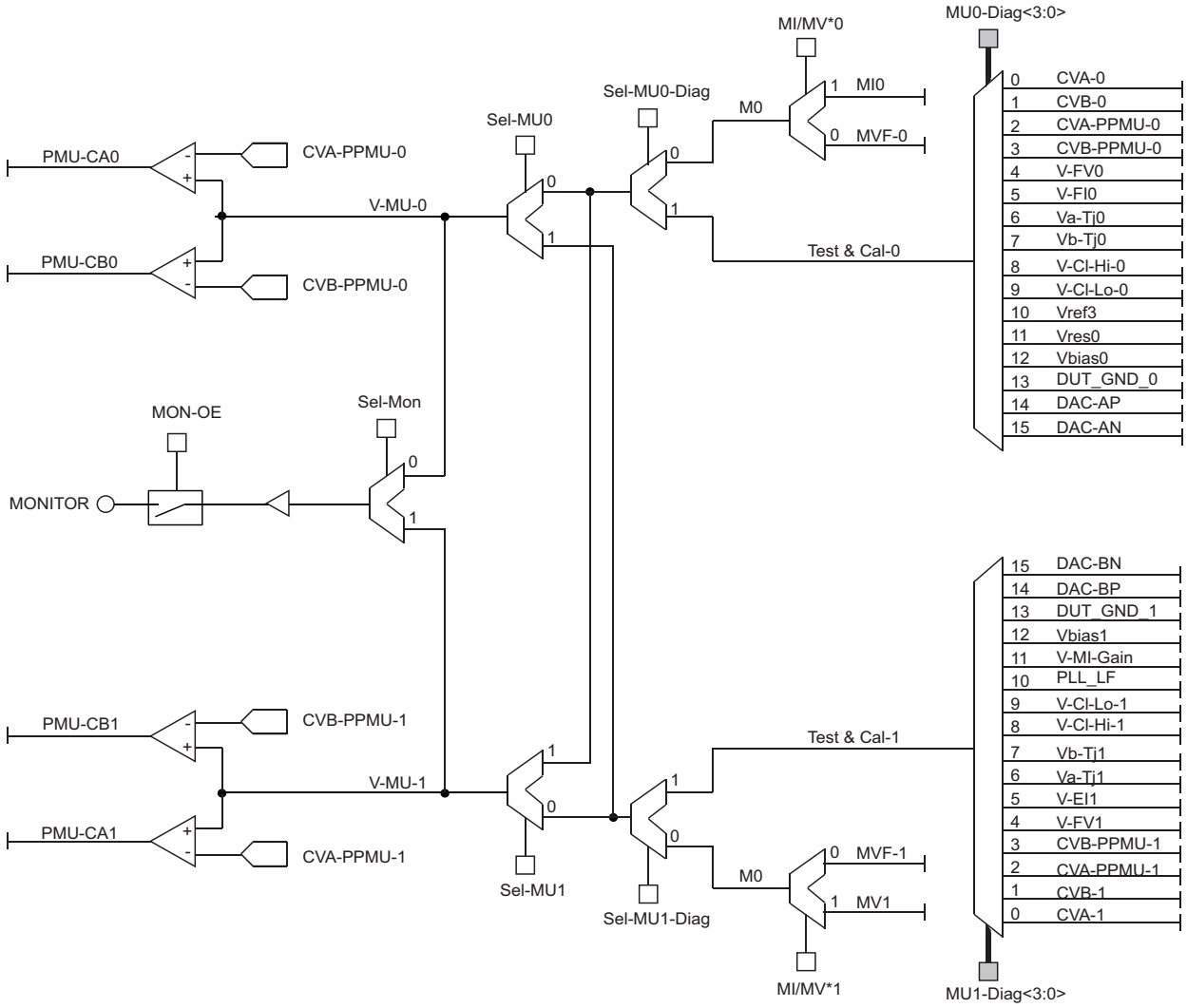
Comparator Path



PMU


V-FI-0
Sel-Ext-DAC0
V-FV-0
Fi/FV*0
VF-0
Feedback-0
PPMU-En0
V-OpAmp0
IR0<7:0>
MI0
V-FB-0
Loop0
MV0
SV0
PPMU-F0
DOUT0
V-Cl-En0
FI-V-Clamps
V-Cl-Lo-0
V-Cl-Hi-0
En-Ext-Force0
MVF-0
Sel-MV0
Sel-Ext-Sense0
En-Ext-Sense0
MVS-0
EXT_FORCE
EXT_SENSE
MVS-1
Sel-MV1
Sel-Ext-Sense1
En-Ext-Sense1
En-Ext-Force1
MVF-1
Fi/FV*1
V-Cl-Hi-1
V-Cl-Lo-1
FI-V-Clamps
MV1
Loop1
V-FB-1
V-Cl-En1
MI1
V-FV-1
Feedback-1
Sel-Ext-DAC1
VF-1
V-OpAmp1
PPMU-F1
DOUT_1
V-FI-1
PPMU-En1
IR1<7:0>
SV1

Measurement Unit



PLL Overview

There is an on chip PLL that sets the full scale delay range and resolution of all internal deskew elements.

$$78.125\ MHz \leq PLL\_CK\ Frequency \leq 125\ MHz$$

PLL_CK is required only if any deskew element is used. If no delay elements are used, PLL_CK may be left in a static low state.

Lock Range

The PLL lock range is total span of PLL_CK frequencies for which the PLL can capture and lock to the input signal.

Track Range

The track range of the PLL is the span of PLL_CK frequencies that the PLL can track, once lock has already been achieved. The track range is wider than the lock range.

Frequency Clamps

A frequency clamp exists which limits the lower end of the frequency range for which the PLL will lock. If no signal is on PLL_CK, or the frequency of PLL_CK is too low, the clamps will limit the effective locking frequency to the clamping frequency.

TABLE 9. Frequency Clamps

Fclamp1	Fclamp0	Fmin
0	0	40MHz
0	1	50MHz
1	0	60MHz
1	1	80MHz

The frequency clamps are programmed via the CPU port, and should be established prior to executing any real time patterns. As long as PLL_CK is faster than the Fclamp limit, the frequency clamps have no function or effect on PLL operation.

The recommended clamp setting for all PLL_CK inputs is the default condition:

Fclamp1 = 0

Fclamp0 = 0.

Internal Swing Settings

There are two CPU register bits that slightly alter the internal behavior of the delay cells and the logic gates in the high-speed timing path by changing the amplitude of the internal swings.

The recommended setting is:

Vswing1 = 0

Vswing0 = 1

PLL Disable

The CPU port may connect the PLL output voltage to ground through an on-chip switch. This connection may be used to place the PLL in a known state prior to locking.

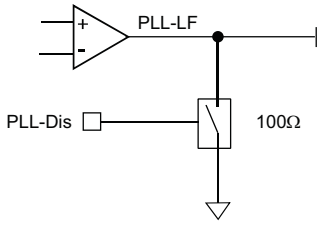


FIGURE 7.

TABLE 10. PLL Disable

PLL-Dis	PLL-LF
0	Active
1	Disabled (100Ω to GND)

On-Chip Terminations

PLL_CK / PLL_CK* inputs have on chip termination options which support 3 different termination schemes:

1. No termination (open circuit)
2. 100Ω across the differential inputs
3. 50Ω single ended termination.

All of these termination schemes may be realized without requiring any external resistors.

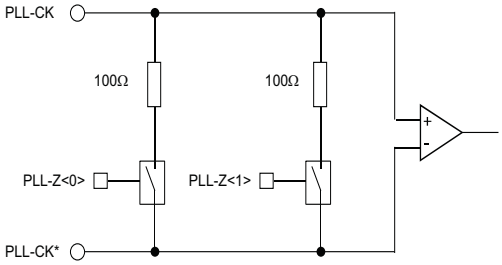


FIGURE 8.

The selection of any on chip termination is made through the CPU port. PLL-Z<1:0> are internal control bits which select the termination option. Their addresses are listed in the memory map tables.

TABLE 11. On-chip Terminations

PLL-Z<1:0>	Termination Option
00	No Termination
01	100Ω Differential
10	100Ω Differential
11	50Ω Single-Ended

Driver

Driver Detailed Block Diagram

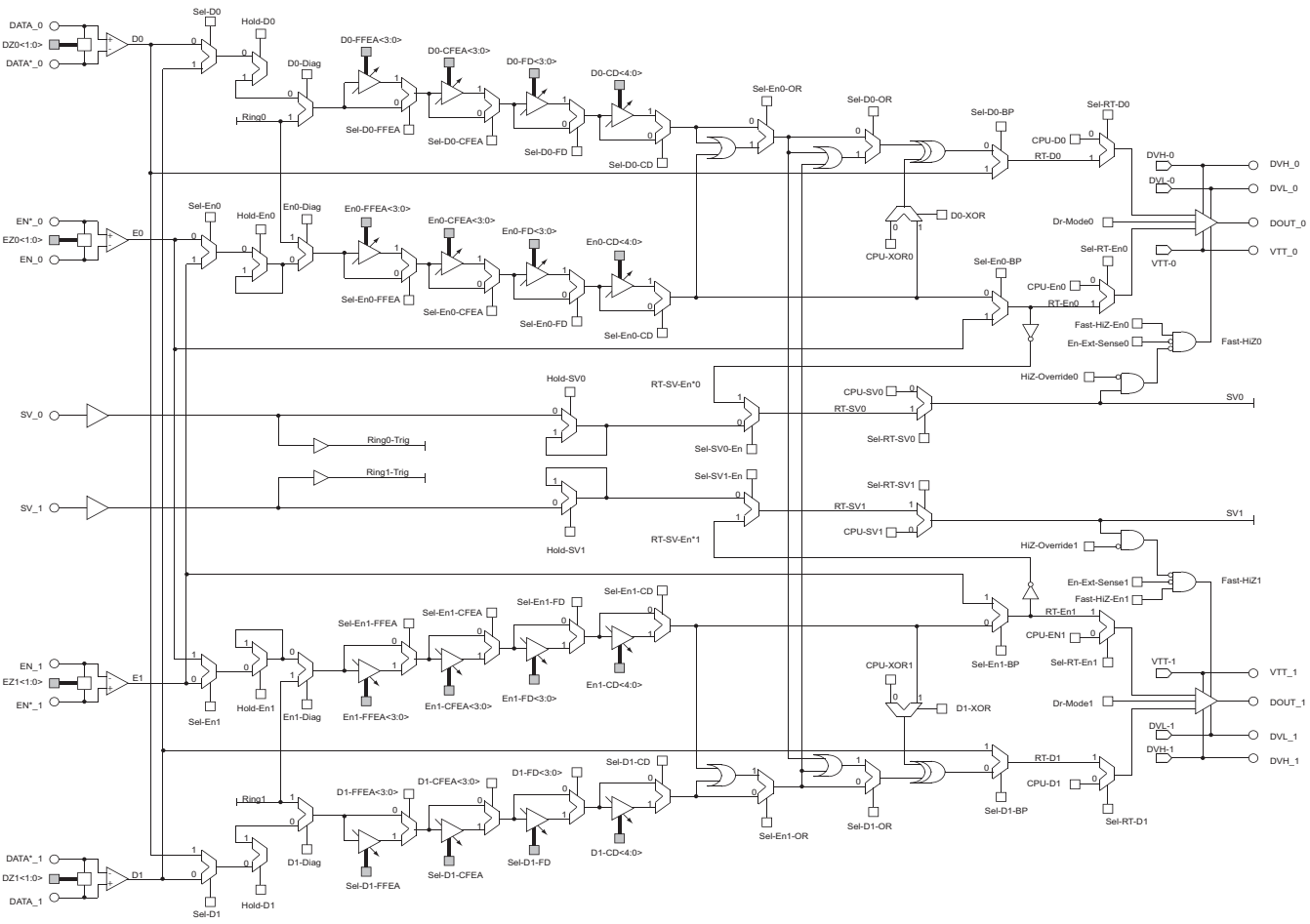


FIGURE 9.

Real-Time Digital Inputs

Each channel has high speed differential digital inputs DATA and EN which control the real time operation of the driver.

Universal Inputs

DATA_0 / DATA*_0, DATA_1 / DATA*_1, EN_0 / EN*_0, and EN_1 / EN*_1 are differential inputs that directly accept most standard technologies which operate between VDD (+3.3V) and ground without requiring any external translation.

On-Chip Terminations

Each channel's DATA and EN inputs have independent on chip termination options which support 3 different termination schemes:

1. No termination (open circuit)
2. 100Ω across the differential input
3. 50Ω single ended termination.

All of these termination schemes may be realized without requiring any external resistors. Access and control of these termination resistors is accomplished via the CPU port, through which the individual enable bits can be set or cleared.

TABLE 12. On-Chip Terminations

EZ#<1:0> DZ#<1:0>	Input Termination
00	No Termination
01	100Ω
10	100Ω
11	50Ω

50Ω Single Ended Termination

Selecting both 100Ω terminators creates a single ended 50Ω termination. The inverting input then becomes the termination voltage for the input signal, and the appropriate termination voltage level must be applied to this pin. Vterm must be able to handle any current flow required for proper termination.

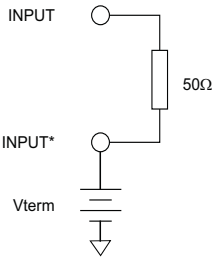


FIGURE 10.

100Ω Differential Termination

By selecting either, but not both, 100Ω terminators, a 100Ω resistance is connected between the differential inputs, thus cleanly terminating differential inputs connected by 50Ω transmission lines on the PCB.

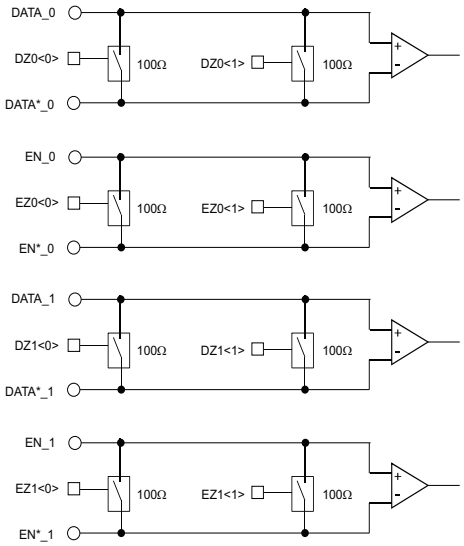


FIGURE 11.

Pre Deskew Signal Processing

DATA & ENABLE CROSS POINT SWITCH

The DATA and EN inputs for each channel may be routed independently to either channel. This up front 2X2 cross point switch is extremely useful in creating a 1:2 fanout tree for these two high speed digital inputs without requiring any external circuitry.

There are no restrictions between the selected DATA or EN signals on channel 0 and channel 1 in that either channel's signals may drive either, or both, channel's signal paths. The various mux select control lines are internal registers controlled via the CPU port and are documented in the memory map tables.

TABLE 13. High Speed Input Signal Selection

Sel-D#	Data # Source	Sel-En#	Enable # Source
0	DATA_#	0	EN_#
1	DATA_(1-#)	1	EN_(1-#)

DATA & ENABLE HOLD

Both high speed driver inputs DATA and EN have a hold feature where an existing state may be stored and held, allowing the input source to change without affecting the state of the driver.

TABLE 14. Data & Enable Hold

Hold-D# Hold-En#	Driver Control
0	Real Time Inputs
1	Latched State

The hold feature is useful in situations where one pattern resource is shared over multiple test heads or multiple sites and one site wishes to remain in a constant and known state while the other site requires a change in status.

Ring Oscillator Mode

The data and enable paths may be used to configure the channel as a ring oscillator. This configuration is useful for calibration of the delay elements.

TABLE 15. Ring Oscillator Mode

D#-Diag En#-Diag	Data Path Source Enable Path Source
0	DATA_#, EN_#
1	Ring#

Bypass Mode

All DATA and EN digital processing and deskew options may be bypassed completely with DATA and EN having direct control over the driver. This mode results in the shortest Tpd across the chip and is useful in applications where the digital features and channel deskew are performed in an external IC.

TABLE 16. Bypass Mode

Sel-D#-BP Sel-En#-BP	RT-D# RT-EN#I
0	Full Digital Feature Capability
1	Bypassed

Ring Oscillator

Each channel may be placed into a ring oscillator configuration where the comparator outputs are fed back into the pattern inputs. This mode is used primarily for test and characterization and it may also be used for calibration purposes.

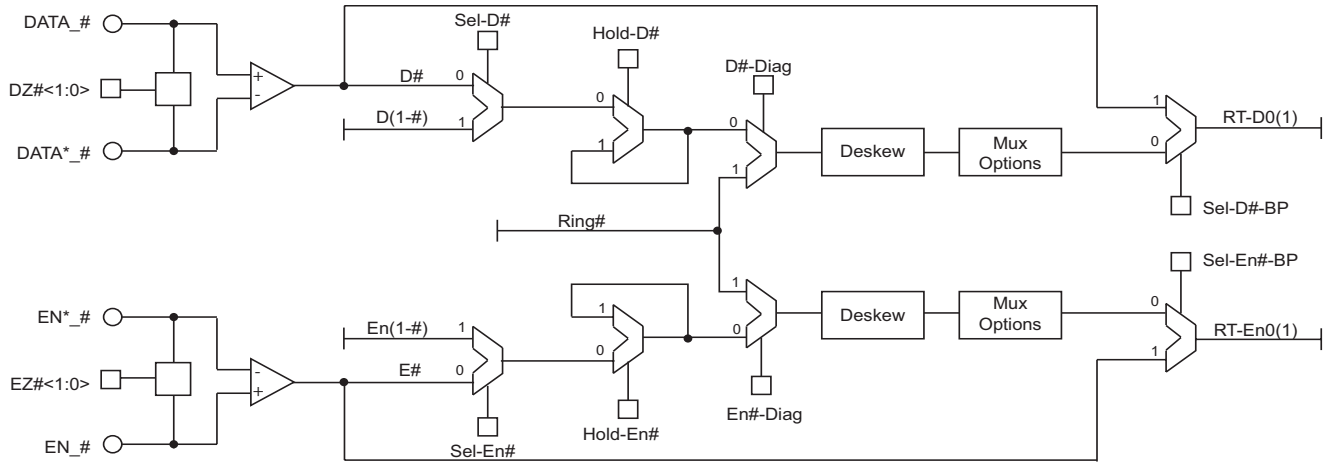


FIGURE 12.

Ring Oscillator - Driver Path Selection

Either the Data or Enable path may be chosen as the source of the driver input and is determined by the CPU port.

TABLE 17. Driver Path Selection

D#-Diag	En#-Diag	Channel # Configuration
0	0	Driver Configuration
0	1	Enable path as a ring oscillator
1	0	Data path as a ring oscillator
1	1	NOT ALLOWED

It is important to choose either the driver or the enable path, but not both.

Ring Oscillator - Comparator Path Selection

Either comparator path A or B may be selected as the return path for the ring oscillator.

TABLE 18. Comparator Path Selection

Sel-C#-Diag	Comparator Path
0	Comp A
1	Comp B

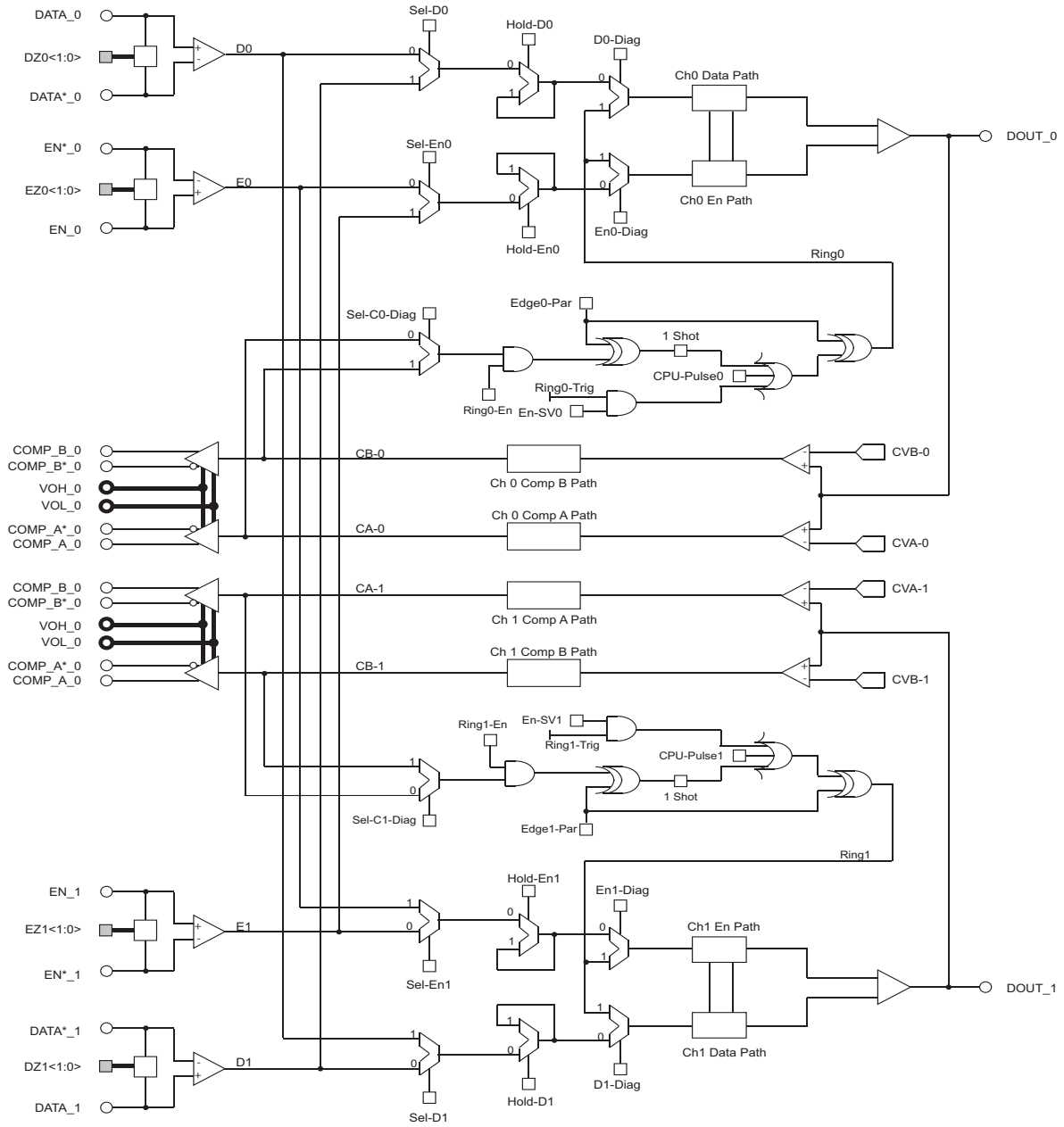


FIGURE 13.

Ring Oscillator - Edge Parity

The ring oscillator may be triggered by either a positive or negative driver transition. This flexibility is useful when measuring the affects of the Falling Edge Adjust delay elements as well as falling edge timing errors due to duty cycle or pulse width.

TABLE 19. Edge Parity

Edge#-Par	Ring # Trigger Polarity
0	Positive Edge
1	Negative Edge

Ring Oscillator - Enable

Once the ring is configured it will not oscillate until the enable signal is set high by the CPU port.

TABLE 20.

Ring#-En	Ring # Oscillator Status
0	Ring Disabled
1	Ring Enabled

Ring Oscillator Start Up

There are two methods to start up the ring oscillator.

1. CPU port
2. SV input pin

CPU Port Start-Up

The ring starts up by the CPU port executing a CPU-Pulse# transaction. This write-only function fires off a one shot pulse that initiates the ring oscillating.

Only 1 CPU transaction is needed to start up the ring.

SV Start-Up

SV_# may be used to initiate the ring oscillator by injecting 1 narrow positive pulse (~ 10 ns) into this pin. En-SV# enables and disables this start-up path.

TABLE 21. SV Start-Up

En-SV#	SV# Start-Up Path
0	Disabled
1	Enabled

Enable Path Configuration

In order to use the enable path for the ring oscillator the enable signal must be routed into the driver's data input through either the XOR or the OR option multiplexer. The following steps should be taken to set up the configuration correctly:

- CPU control over the enable signal, driver on.
  - Sel-RT-En0(1) = 0
  - CPU-En0(1) = 1

XOR Gate Option

- Enable path connected as the driver data.
  - Sel-RT-D0(1) = 1
  - Sel-D0(1)-OR = 0
  - D0-XOR = 1

OR Gate Option

- Enable path connected as the driver data.
  - Sel-RT-D0(1) = 1
  - D0(1)-XOR = 0
  - CPU-XOR0(1) = 0
  - Sel-D0(1)-OR = 1.

Either the XOR path or the OR path may be used to configure the ring to use the enable signal path to force the driver, but NOT both at the same time. In either case, D0(1) must be placed in a static low state otherwise this signal will affect proper ring oscillator operation.

Deskew

Each channel's high-speed DATA and EN inputs have timing adjustment capability with the following characteristics:

1. Separate and independent delay circuitry for the DATA and EN paths
2. Separate and independent delay circuitry for channel 0 and channel 1
3. Propagation delay adjust (both rising (Tpd+) and falling (Tpd-) edge are delayed equally)
4. Falling edge adjust (FEA) (falling edge may be adjusted, rising edge Tpd remains constant)
5. Timing delay range and resolution established by an external frequency
6. If bypassed, the delay element shuts down and consumes no power.

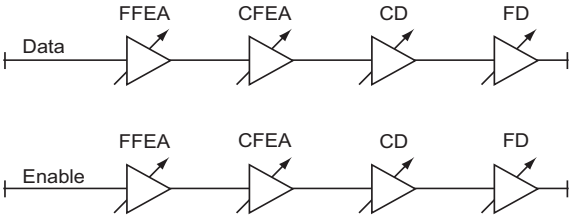


FIGURE 14.

Full Scale Delay Range

Each element's delay range is established by an off-chip PLL_CK frequency with a period of T.

PLL_CK Frequency Range

PLL_CK locks over a 2:1 input frequency range.

8 ns ≤ T ≤ 13.3 ns

125 MHz ≥ F ≥ 75 MHz

Propagation Delay Adjust

The propagation delay circuitry adds timing delay to the rising edge (Tpd+) and the falling edge (Tpd-) in equal amounts. Propagation delay adjustment is typically used for aligning the timing of multiple channels inside a tester.

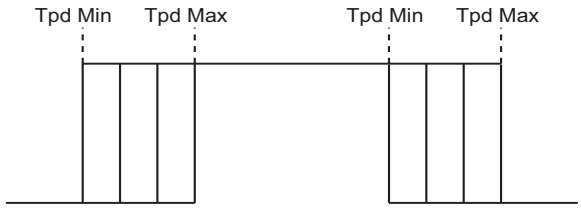


FIGURE 15.

The delay circuitry is divided into two separate blocks:

1. Coarse Delay
2. Fine Delay.

Propagation Delay Falling Edge Adjust

The falling edge delay circuitry adds or subtracts timing delay to or from the falling edge (Tpd-) while having no effect on the rising edge (Tpd+). Propagation delay adjustment is typically used for removing any pulse width distortion inside a tester.

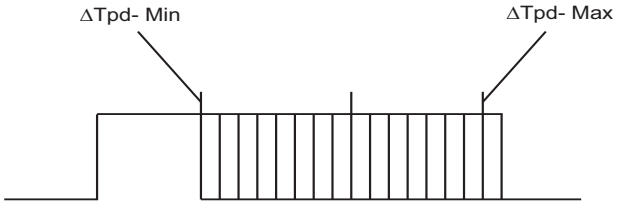


FIGURE 16.

The delay circuitry is divided into two separate blocks:

1. Coarse Falling Edge Adjust
2. Fine Falling Edge Adjust.

Coarse Delay

Coarse delay divides the overall delay range (established by the period of PLL_CK) into 32 equal segments and then selects one of those delays.

Tspan (CD) = (31/32) x T

Resolution = T/32

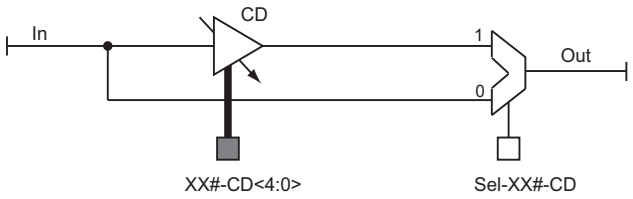


FIGURE 17.

Coarse delay is programmed by the CPU port and may be bypassed. If bypassed, the circuitry powers down.

TABLE 22. Coarse Delay

PLL_CK	T = 8ns	T = 10ns	T = 12.8ns
Tspan	7.75ns	9.6875ns	12.4ns
Resolution	250ps	312.5ps	400ps
CD<4:0>	**ΔTpd+,–**	**ΔTpd+,–**	**ΔTpd+,–**
00000	0ps	0ps	0ps
00001	+250ps	+312.5ps	+400ps
00010	+500ps	+625ps	+800ps
⋮	⋮	⋮	⋮
11101	+7.25ps	+9.0625ns	+11.6ns
11110	+7.5ns	+9.375ns	+12.0ns
11111	+7.75ns	+9.6875ns	+12.4ns

Fine Delay

Fine delay adjust makes very small corrections to Tpd+ and Tpd– and affects both rising and falling edges equally. FD allows edge placement between coarse delay LSB steps.

Tspan (FD) = 15 x T/512

Resolution = T/512

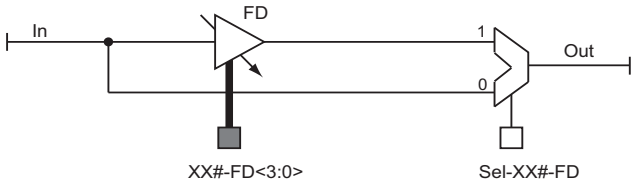


FIGURE 18.

Fine delay is programmed by the CPU port and may be bypassed. If bypassed, the circuitry powers down.

TABLE 23. Fine Delay

PLL_CK	T = 8ns	T = 10ns	T = 12.8ns
Tspan	234.375ps	292.96875ps	375ps
Resolution	15.625ps	19.53125ps	25ps
FD<3:0>	**ΔTpd+,–**	**ΔTpd+,–**	**ΔTpd+,–**
0000	0ps	0ps	0ps
0001	+15.625ps	+19.53125ps	+25ps
0010	+31.25ps	+39.0625ps	+50ps
⋮	⋮	⋮	⋮
1101	+203.125ps	+253.90625ps	+325ps
1110	+218.75ps	+273.4375ps	+350ps
1111	+234.375ps	+292.96875ps	+375ps

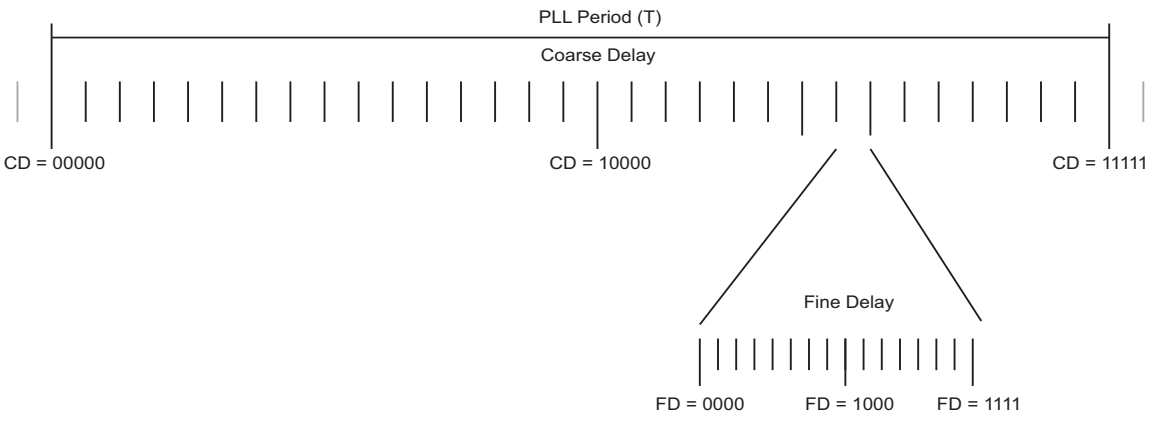


FIGURE 19.

Coarse Falling Edge Adjust

CFEA offers a selection of 16 different falling edge adjustments as selected by the CPU port. The total range for CFEA is related to the PLL_CK period by the relationship:

Tpd– Min = - (1/4) • T

Tpd–Max = + (7/32) • T

Resolution = T / 32

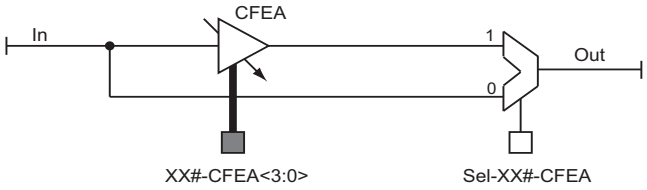


FIGURE 20.

CFEA may be bypassed via the CPU port. If bypassed, the circuitry powers down.

TABLE 24. Coarse Falling Edge Adjust

PLL_CK	T = 8ns	T = 10ns	T = 12.8ns
Tpd–(min)	–2ns	–2.5ns	–3.2ns
Tpd–(max)	+1.75ns	+2.1875ns	+2.8ns
Resolution	+250ps	+312.5ps	+400ps

CFEA<3:0>	ΔTpd–	ΔTpd–	ΔTpd–
0000	–2ns	–2.5ns	–3.2ns
0001	–1.75ns	–2.1875ns	–2.8ns
0010	–1.5ns	–1.875ns	–2.4ns
0011	–1.25ns	–1.5625ns	–2.0ns
0100	–1.0ns	–1.25ns	–1.6ns
0101	–750ps	–937.5ps	–1.2ns
0110	–500ps	–625ps	–800ps
0111	–250ps	+312.5ps	–400ps
1000	0ps	0ps	0ps
1001	+250ps	+312.5ps	+400ps
1010	+500ps	+625ps	+800ps
1011	+750ps	+937.5ps	+1.2ns
1100	+1.0ns	+1.25ns	+1.6ns
1101	+1.25ns	+1.5625ns	+2.0ns
1110	+1.5ns	+1.875ns	+2.4ns
1111	+1.75ps	+2.1875ns	+2.8ns

Fine Falling Edge Adjust

FFEA offers a selection of 16 different falling edge adjustments as selected by the CPU port. The total range for FFEA is related to the PLL_CK period by the relationship:

Tpd- Min = - T / 64

Tpd- Max = + 7 • T / 512

Resolution = T / 512

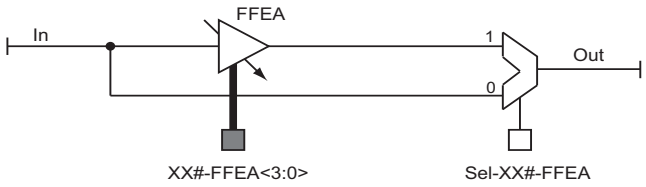


FIGURE 21.

FFEA may be bypassed via the CPU port. If bypassed, the circuitry powers down.

TABLE 25. Fine Falling Edge Adjust

PLL_CK	T = 8ns	T = 10ns	T =12.8ns
Tpd–(min)	–125ps	–2.5ns	–3.2ns
Tpd–(max)	+109.375ps	+136.71875ps	+175ps
Resolution	+15.625ps	+19.53125ps	+25ps

CFEA<3:0>	ΔTpd–	ΔTpd–	ΔTpd–
0000	–125ps	–125.25ns	–200ps
0001	–109.375ps	–136.71875ps	–175ps
0010	–93.75	–117.1875ps	–150ps
0011	–78.125ps	–97.65625ps	–125ps
0100	–62.5ps	–78.125ps	–100ps
0101	–46.875ps	–58.59375ps	–75ps
0110	–31.25ps	–39.0625ps	–50ps
0111	–15.625ps	–19.53125ps	–25ps
1000	0ps	0ps	0ps
1001	+15.625ps	+19.53125ps	+25ps
1010	+31.25ps	+39.0625ps	+50ps
1011	+46.875ps	+58.59375ps	+75ps
1100	+62.5ps	+78.125ps	+100ps
1101	+78.125ps	+97.65625ps	+125ps
1110	+93.75ps	+117.1875ps	+150ps
1111	+109.375ps	+136.71875ps	+175ps

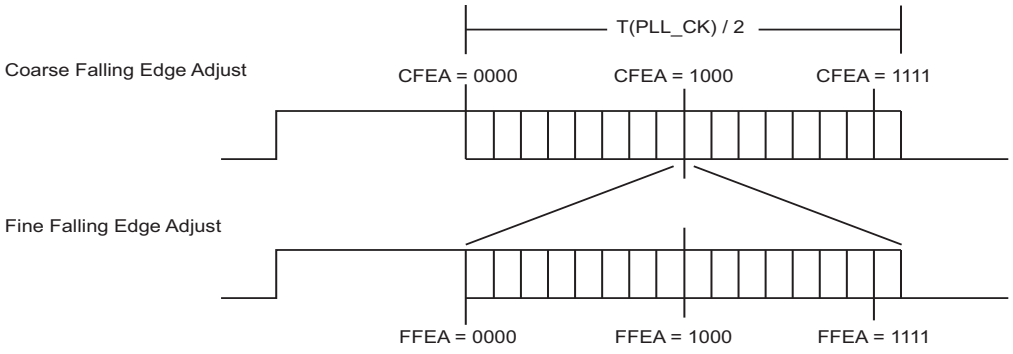


FIGURE 22.

Post Deskew Processing Options

Once the driver Data and Enable signals have been selected and calibrated by the deskew elements, additional processing options exist for the Data signal:

1. Data and Enable from the same channel ORed together
2. Data and Data from the channels ORed together
3. Data and Enable from the same channel XORed
4. Data inversion per channel
5. CPU over-ride.

Same Channel Multiplexing - Data OR Enable

The DATA and EN signals of each channel are combined in an OR gate, and that gate's output may be selected as that channel's data signal to the driver.

TABLE 26. Same Channel Multiplexing

Sel-En#-OR	Ch# Data Signal
0	Data#
1	Data# OR En#

In this mode, the CPU port should take control over the driver enable signal and keep the driver active so that any real time changes in the EN input will affect only the driver data pattern.

- Sel-RT-En = 0
- CPU-En = 1
- Sel-En-OR = 1

Channel-to-Channel Multiplexing - Data0 OR Data1

The data signals of each channel are combined in an OR gate, and that gate's output can be selected as either channel's data signal to the driver.

TABLE 27. Channel-to-Channel Multiplexing

Sel-En#-OR	Ch# Data Signal
0	Data#
1	Data0 OR Data1

Same Channel Formatting — Data XOR

The Data and Enable signals from one channel may be combined via an XOR gate, which allows the timing resources behind the Data and Enable inputs to combine into more complex patterns.

TABLE 28. Same Channel Formatting

D#-XOR	CPU-XOR#	Ch# Data Source
0	0	Ch #Data Pattern
0	1	Ch# Data Pattern*
1	X	Ch# Data Pattern XOR En#

Data Inversion

After all OR combination options are selected, but before the processed data signal enters the driver, it passes through an XOR gate, which provides a convenient method of inverting the data pattern. Selecting the CPU-XOR bit and programming it to a zero state results in no signal inversion or alteration.

CPU Control

After all driver control signal processing is performed, Data and Enable enter one last control stage, where the real time signals may be bypassed and the CPU port can take direct control over the driver. This final logic stage allows the CPU port to exercise driver control regardless of any real time inputs.

TABLE 29. CPU Control

Sel-RT-D# Sel-RT-En#	RT-D# / RT-En#
0	CPU-D# / CPU-En#
1	RT-D# / RT-En#

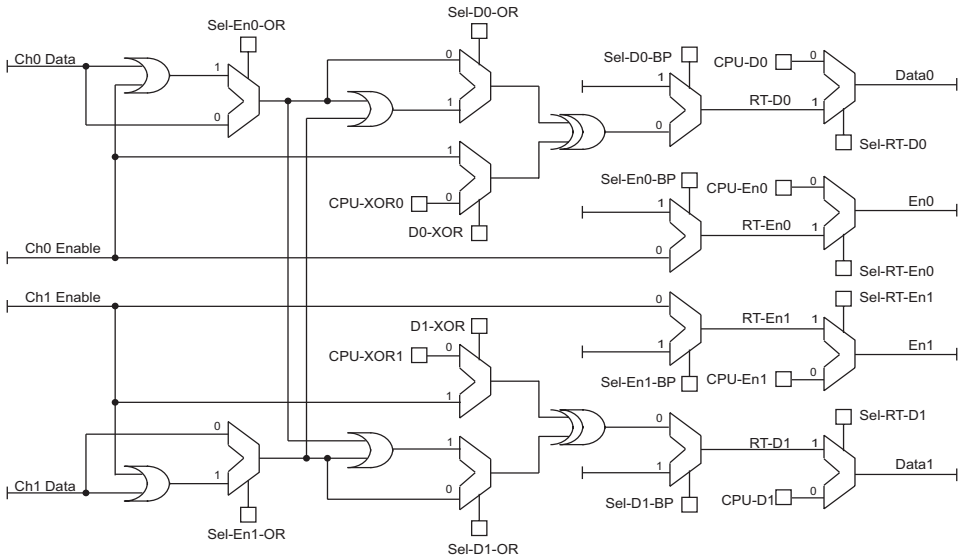


FIGURE 23.

Driver Output Control

The driver has a 50Ω output impedance and is capable of forcing 3 voltage levels - DVH, DVL, and VTT - and can go into a high impedance state. The high, low, and termination voltages are all supported by on chip DC level generators and buffers, and are programmed through the CPU port. The DAC addresses are listed in the memory map tables.

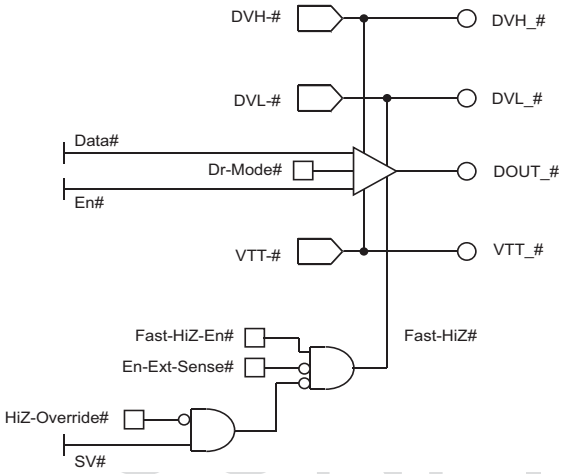


FIGURE 24.

Driver Mode

The Dr-Mode bit establishes the driver mode. When low, the driver is a traditional 2 level driver with HiZ. When high, the driver supports an additional termination level and no HiZ.

TABLE 30. High Speed Driver Control

Dr-Mode#	En#	Data#	DOUT_#
0	0	X	HiZ
0	1	0	DVL
0	1	1	DVH
1	0	X	VTT
1	1	0	DVL
1	1	1	DVH

High Impedance

There are two distinct driver HiZ modes:

1) Fast HiZ

2) Slow Hiz

FAST HiZ

Fast HiZ is used during high-speed functional test patterns when the driver is forcing DVH and DVL. In Fast HiZ, the driver maintains low leakage between VEE and VCC. For DOUT voltages more positive than VCC, the high speed driver starts to turn on. Driver transition times going into and out of high impedance are quicker and more accurate when the driver is in Fast HiZ mode than when in Slow HiZ mode.

It is acceptable and legal for the DUT to exceed VCC in Fast HiZ mode, but the DUT will see a 50Ω load to VCC + 1.25V, once that voltage is exceeded. But no damage will be done to the driver.

SLOW HiZ

Slow HiZ is used primarily during wide voltage PPMU operation, and is the default mode upon power up or reset. In Slow HiZ, the driver maintains a very low leakage when tracking any voltage between VEE and VCC_SV, and therefore the DOUT pin has a wider input compliance voltage range.

Slow HiZ is automatically selected anytime the PPMU or external FET switches are enabled unless overridden by the HiZ-Override function. In addition, this wider voltage mode may be forced by the CPU port setting Fast-HiZ-En = 0. It may be desirable to force Slow HiZ when the Comparator is testing a large positive voltage in excess of VCC. In Slow HiZ, the driver functions the same as in Fast HiZ, but the driver transition times into and out of HiZ, as well as driver minimum pulse widths, will be slightly slower.

TABLE 31. HI-Z

Fast-HIZ-En#	En-Ext-Sense#	SV#	HIZ-Override	Channel # HIZ Mode
0	X	X	X	Slow HiZ
X	1	X	X	Slow HiZ
X	X	1	0	Slow HiZ
1	0	0	X	Fast HiZ
1	0	X	1	Fast HiZ

Driver Level Restrictions in HiZ and PMU Mode

The ISL55162 driver levels (DVH, DVL, VTT) should be programmed to the midpoint between VCC_SV and VEE when in HiZ or PMU Mode.

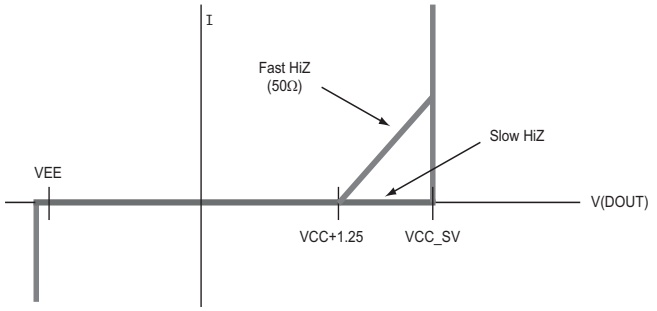


FIGURE 25.

Output Impedance

The driver is designed to maintain constant output impedance regardless of any changes due to:

1. ambient temperature
2. part-to-part variation

by tracking a precision and temperature compensated off chip resistor (R_EXT) with a ratio of 204:1. Nominal conditions are:

R_EXT = 10.00kΩ

Rout = 49Ω.

Rout may be adjusted over a limited range by varying R_EXT.

Output Impedance Adjustments

The driver tracks R_EXT equally for DVH, DVL, and VTT levels. However, it is possible to make fine adjustments to Rout for each drive level separately. This independent adjustment is useful for calibrating waveforms in precision applications and may be used to accommodate any transmission line impedance errors on a load board, as well as to adjust a characteristic in a waveform's DVH, DVL, or VTT performance, without affecting its characteristics when driving the other two levels.

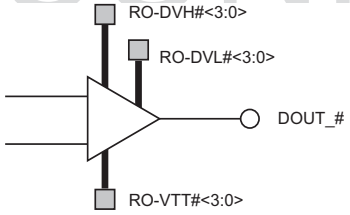


FIGURE 26.

Fine control is programmed through the CPU port, and is normally set up before the execution of any real time patterns. The default condition (Reset, Power up) is Radj = 0Ω.

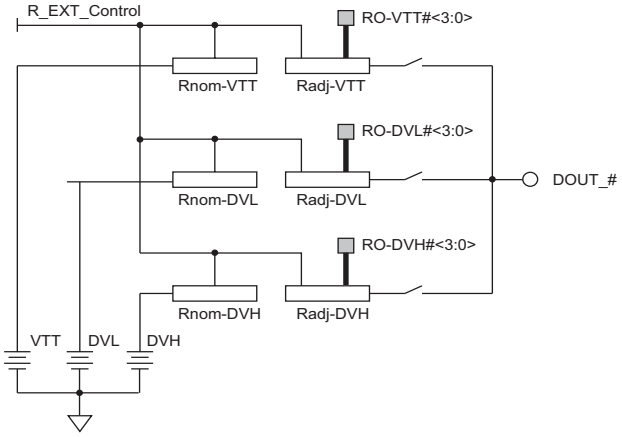


FIGURE 27.

Fine Adjustment Range

Each level has a fine adjustment range of ± 10%, or ± 5Ω for R_EXT = 10kΩ. The total output impedance of the driver is the nominal output impedance plus the fine adjustment.

Rnom = R_EXT / 204

Radj = ±10% = ± R_EXT/2,000

Rout = Rnom + Radj = R_EXT/204 ± R_EXT/2000

TABLE 32. Fine Adjustment Range

RO-DVH<3:0> RO-DVL<3:0> RO-VTT<3:0>	Radj-DVH Radj-DVL Radj-VTT (Ω)	Radj-DVH Radj-DVL Radj-VTT (%)
0111	+4.375	+8.92
0110	+3.75	+7.65
0101	+3.125	+6.38
0100	+2.5	+5.1
0011	+1.875	+3.83
0010	+1.25	+2.55
0001	+0.625	+1.28
0000	0	0
1111	-0.625	-1.28
1110	-1.25	-2.55
1101	-1.875	-3.83
1100	-2.5	-5.1
1011	-3.125	-6.38
1010	-3.75	-7.65
1001	-4.375	-8.92
1000	-5.0	-10.2

The numbers in the above table are based upon R_EXT = 10.0kΩ

Comparator

Block Diagram

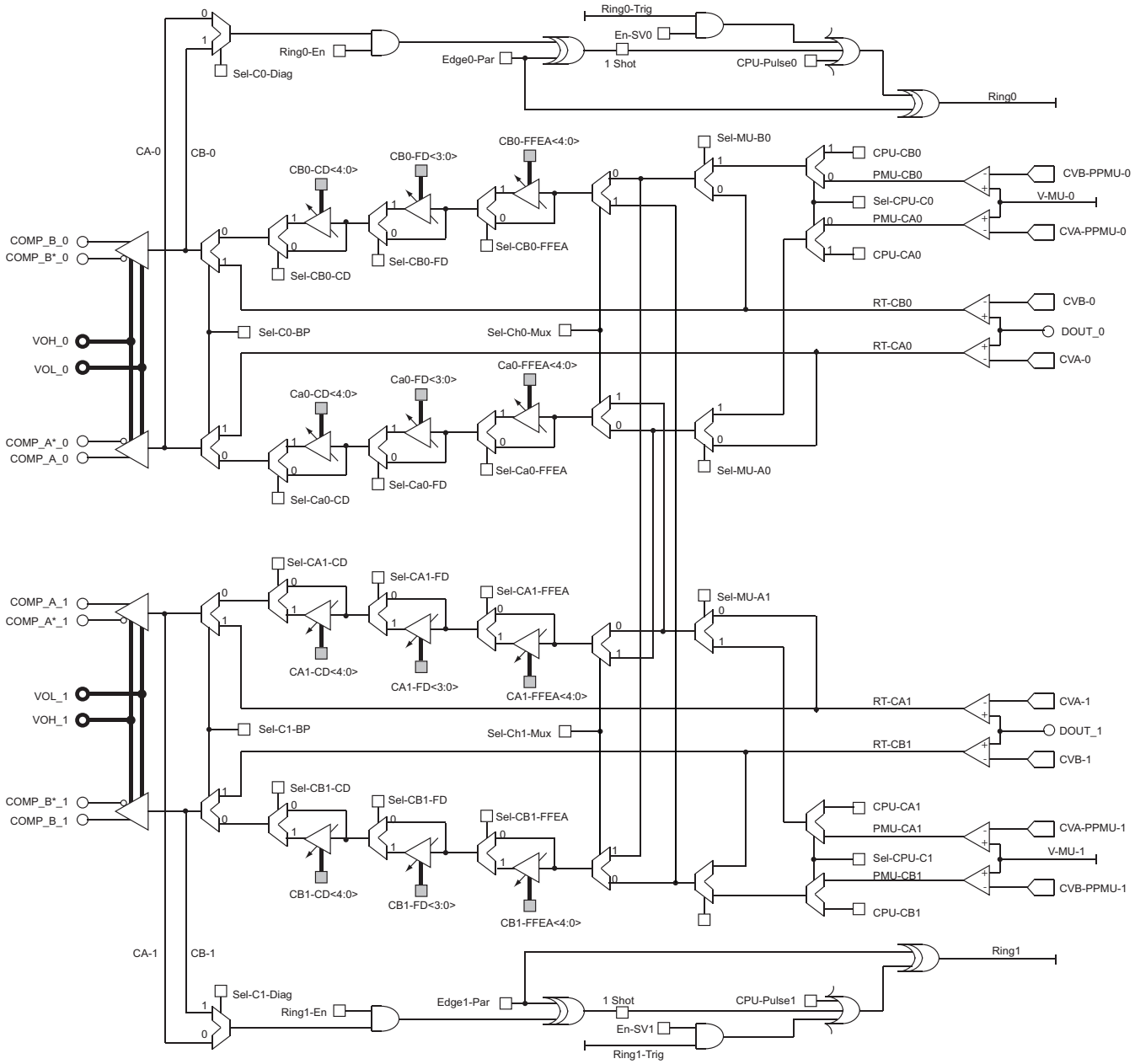


FIGURE 28.

Overview

Each channel supports 2 comparator output signals COMP_A_# and COMP_B_#. Through a series of multiplexers each comparator output signal may be driven by a variety of signal sources:

1. Functional comparators
2. PMU comparators
3. CPU port
4. The same 3 sources from the other channel.

Functional Comparator

The functional comparator is a high-speed window comparator with extremely low input leakage current when DOUT is between the power supply rails VEE and VCC_SV. It is normally selected for real time functional testing of the Device Under Test.

PMU Comparator

The parametric measurement comparator is a window comparator with its input (V-MU) generated by the PPMU. The parametric comparator is normally selected for parametric testing of the Device Under Test.

Threshold Generation

The DC threshold reference levels per channel:

CVA-0(1), CVB-0(1)

CVA-PPMU-0(1),CVB-PPMU-0(1)

are independent on-chip DC levels programmed through the CPU port. Their addresses are listed in the memory space tables.

Internal State Readback

Real time access to all internal comparator states is available. The CPU port can read back the internal nodes:

RT-CA#, RT-CB#

PPMU-CA#, PPMU-CB#

The addresses of these nodes are listed in the memory map tables.

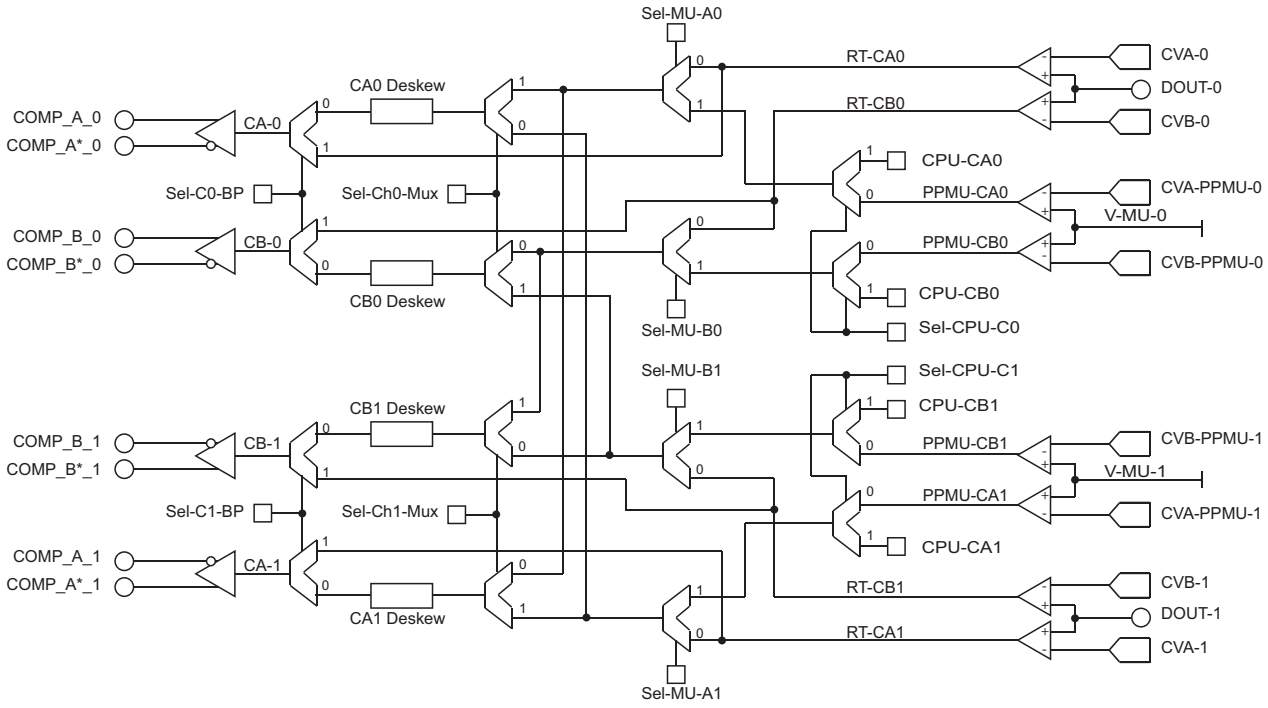


FIGURE 29.

Comparator Source Selection

CPU SOURCE CONTROL

The CPU port can set the Comparator A and B status and override any real time status from the measurement unit. This CPU control allows the comparator outputs to be placed in a known state, typically for diagnostic and debugging purposes within a tester. Each channel has separate comparator source selection capability.

TABLE 33. CPU Source Control

Sel-C#-BP	Sel-Ch#-Mux	Sel-MU-A(B)#	Sel-CPU-C#	CompA(B)_#Source
1	X	X	X	C#A(B)
0	1	X	X	Ch(1-#)Source
0	0	0	X	RT-CA(B)#
0	0	1	0	PMU-CA(B)#
0	0	1	1	CPU-CA(B)#

FUNCTIONAL VS. MEASUREMENT UNIT CONTROL

Once the source of the measurement unit is selected, each channel may then select either the functional or the measurement unit comparator for that channel's COMP_A and COMP_B sources. This source selection is performed separately for comparators A and B of the same channel to allow both functional and parametric information to be simultaneously present at the real time comparator outputs.

COMPARATOR CHANNEL MULTIPLEXING

Either channel's comparator signals may be routed through either channel's delay circuitry and output pins. A dual 2X2 cross point switch allows full flexibility of routing comparator signals with no restrictions.

BYPASS MODE

The deskew and channel multiplexing circuitry may be bypassed completely, resulting in the shortest Tpd across the chip. Bypass is useful in applications where these functions are performed in an external IC.

TABLE 34. Bypass Mode

Sel-C#-BP	COMP_A(B)_#
0	Full Feature Capability
1	Bypassed

Comparator Deskew

Each channel's high-speed COMP_A and COMP_B outputs have timing adjustment capability with the following characteristics:

1. Separate and independent delay circuitry for the COMP_A and COMP_B paths
2. Separate and independent delay circuitry for channel 1 and channel 2
3. Propagation delay adjust (both rising (Tpd+) and falling (Tpd-) edge are delayed equally)
4. Falling edge adjust (FEA) (falling edge may be adjusted, rising edge Tpd remains constant)
5. Timing delay range and resolution established by an external frequency
6. If bypassed, the delay element shuts down and consumes no power.

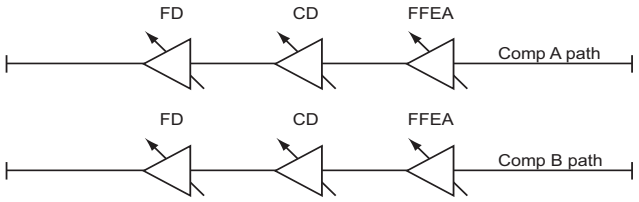


FIGURE 30.

FULL SCALE DELAY RANGE

Each element's delay range is established by an off-chip PLL_CK frequency with a period of T.

PLL_CK FREQUENCY RANGE

PLL_CK locks over a 2:1 input frequency range.

$$8\ ns \leq T \leq 13.3\ ns$$

$$125\ MHz \geq F \geq 75\ MHz$$

PROPAGATION DELAY ADJUST

The propagation delay circuitry adds timing delay to the rising edge (Tpd+) and the falling edge (Tpd-) in equal amounts. Propagation delay adjustment is typically used for aligning the timing of multiple channels inside a tester.

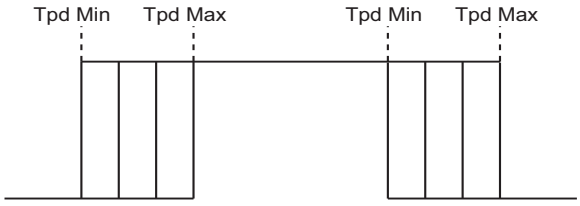


FIGURE 31.

The delay circuitry is divided into two separate blocks:

1) Coarse Delay

2) Fine Delay

PROPAGATION DELAY FALLING EDGE ADJUST

The falling edge delay circuitry adds or subtracts timing delay to or from the falling edge (Tpd-) while having no effect on the rising edge (Tpd+). Propagation delay adjustment is typically used for removing any pulse width distortion inside a tester.

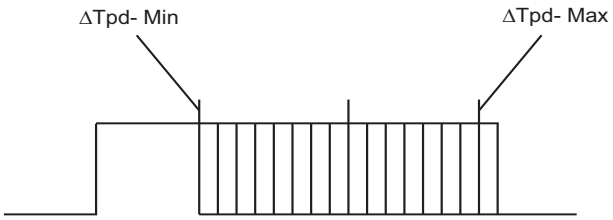


FIGURE 32.

COARSE DELAY

Coarse delay divides the overall delay range (established by the period of PLL_CK) into 32 equal segments, and then selects one of those delays.

Tspan (CD) = (31 / 32) • T

Resolution = T / 32

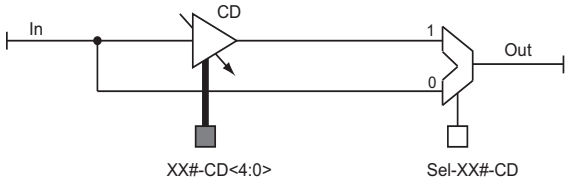


FIGURE 33.

Coarse delay is programmed by the CPU port and may be bypassed. If bypassed, the circuitry powers down.

TABLE 35. Coarse Delay

PLL_CK	T = 8ns	T = 10ns	T = 12.8ns
Tspan	7.75ns	9.6875ns	12.4ns
Resolution	250ps	312.5ps	400ps
CD<4:0>	**ΔTpd+,–**	**ΔTpd+,–**	**ΔTpd+,–**
00000	0ps	0ps	0ps
00001	+250ps	+312.5ps	+400ps
00010	+500ps	+625ps	+800ps
⋮	⋮	⋮	⋮
11101	+7.25ns	+9.0625ns	+11.6ns
11110	+7.5ns	+9.375ns	+12.0ns
11111	+7.75ns	+9.6875ns	+12.4ns

FINE DELAY

Fine delay adjust makes very small corrections to Tpd+ and Tpd- and affects both rising and falling edges equally. FD allows edge placement between coarse delay LSB steps.

Tspan (FD) = 15 • T / 512

Resolution = T / 512

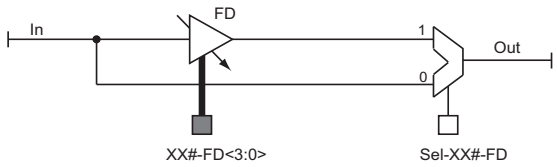


FIGURE 34.

Fine delay is programmed by the CPU port and may be bypassed. If bypassed, the circuitry powers down.

TABLE 36. Fine Delay

PLL_CK	T = 8ns	T = 10ns	T = 12.8ns
Tspan	234.375ps	292.96875ps	375ps
Resolution	15.625ps	19.53125ps	25ps
FD<3:0>	**ΔTpd+,–**	**ΔTpd+,–**	**ΔTpd+,–**
0000	0ps	0ps	0ps
0001	+15.625ps	+19.53125ps	+25ps
0010	+31.25ps	+39.0625ps	+50ps
⋮	⋮	⋮	⋮
1101	+203.125ps	+253.90625ps	+325ps
1110	+218.75ps	+273.4375ps	+350ps
1111	+234.375ps	+292.96875ps	+375ps

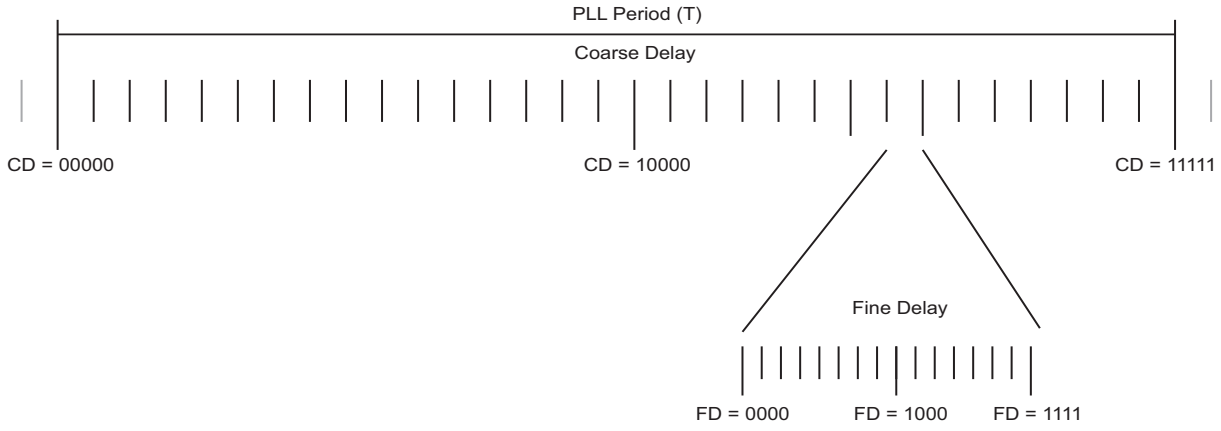


FIGURE 35.

FINE FALLING EDGE ADJUST

FFEA offers a selection of 32 different falling edge adjustments as selected by the CPU port. The total range for FFEA is related to the CFEA by the relationship:

Tpd- Min = - T / 32

Tpd- Max = + (15 / 512) • T

Resolution - T / 512

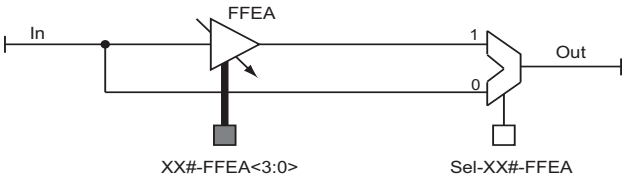


FIGURE 36.

FFEA may be bypassed via the CPU port. If bypassed, the circuitry powers down.

TABLE 37. Fine Falling Edge Adjust

PLL_CK	T = 8ns	T = 10ns	T = 12.8ns
Tpd–(min)	–250ps	–312.5ps	–400ps
Tpd–(max)	+234.375ps	+292.96875ps	+375ps
Resolution	15.6255ps	19.5313ps	25ps
FFEA<4:0>	**ΔTpd+,–**	**ΔTpd+,–**	**ΔTpd+,–**
00000	–250ps	–312.5ps	–400ps
00001	–234.375ps	–292.96875ps	–375ps
00010	–218.75	+275.4375ps	–350ps
00011	–203.125ps	+253.90625ps	–325ps
00100	–187.5ps	–234.375ps	–300ps
00101	–171.875ps	–214.84375ps	–275ps
00110	–156.25ps	–195.3125ps	–250ps
00111	–140.625ps	–175.78125ps	–225ps
01000	–125ps	–156.25ps	–200ps
01001	–109.375ps	–136.71875ps	–175ps
01010	–93.75ps	–117.1875ps	–150ps
01011	–78.125ps	–97.65625ps	–125ps
01100	–62.5ps	–78.125ps	–100ps
01101	–46.875ps	–58.59375ps	–75ps
01110	–31.25ps	–39.0625ps	–50ps
01111	–15.625ps	–19.53125ps	–25ps
10000	0ps	0ps	0ps
10001	+15.625ps	+19.53125ps	+25ps
10010	+31.25ps	+39.0625ps	+50ps
10011	+46.875	+58.59375ps	+75ps
10100	+62.5ps	+78.125ps	+100ps
10101	+78.125ps	+97.65625ps	+125ps
10110	+93.75ps	+117.1875ps	+150ps
10111	+109.375ps	+136.71875ps	+175ps
11000	+125ps	+256.25ps	+200ps
11001	+140.625ps	+175.78125ps	+225ps
11010	+156.25ps	+195.3125ps	+250ps
11011	+171.875ps	+214.84375ps	+275ps
11100	+187.5ps	+234.375ps	+300ps
11101	+203.125ps	+253.90625ps	+325ps
11110	+218.75ps	+273.4375ps	+350ps
11111	+234.375ps	+292.96875ps	+375ps

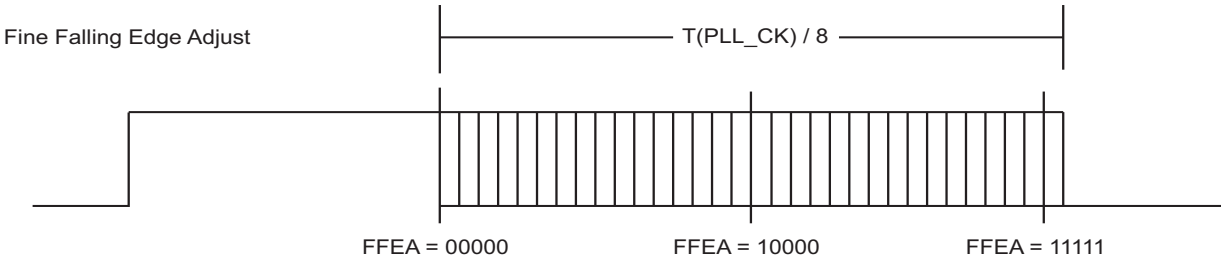


FIGURE 37.

Comparator Output Stage

Each channel supports two comparator outputs with the following characteristics:

1. Differential outputs
2. 50Ω series terminated outputs
3. Programmable high and low levels
4. Separate high and low levels per channel.

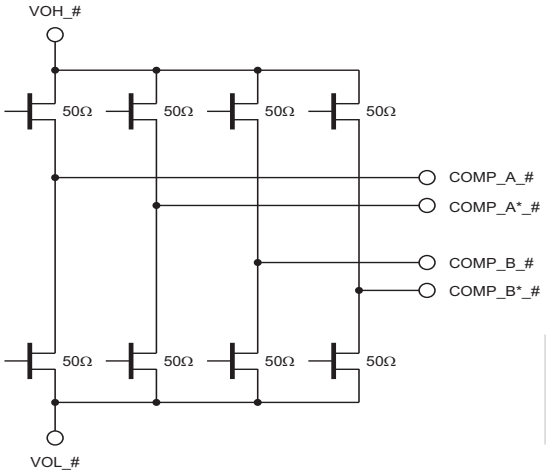


FIGURE 38.

COMPARATOR OUTPUT SUPPLY LEVELS

VOH_# and VOL_# are power supply inputs that set the high and low level of each channel. There are no restrictions between the two channels. VOH_# and VOL_# provide the current required to drive the off-chip transmission line and any DC current associated with any termination used. Therefore, these voltage inputs should be driven by a low impedance and low inductance source with ample current drive.

Comparator Source Termination

No external components are required and full amplitude at the destination is achieved with source termination.

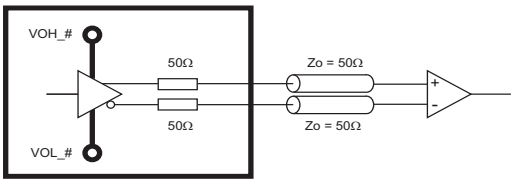


FIGURE 39.

SOURCE AND DESTINATION (DOUBLE) TERMINATION

One external component is required and one half the signal amplitude is realized at the destination with double termination.

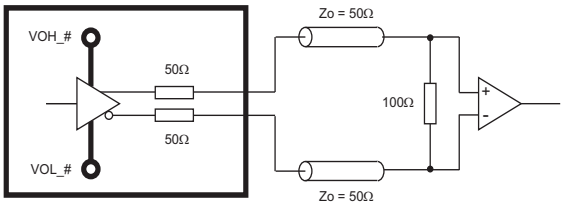


FIGURE 40.

PMU

Overview

Each channel has a per pin parametric measurement unit with the ability to:

- Force Current (FI)
- Force Voltage (FV)
- Measure Current (MI)
- Measure Voltage (MV)

The current or voltage measured may be tested via two different mechanisms:

- On board PMU window comparator
- MONITOR analog output voltage.

PMU Operating Mode

The decision whether to force current or voltage, or to measure current or voltage, is controlled by the CPU port. There are no restriction between FI / FV* and MI / MV* in that all combinations are legal modes.

TABLE 38. PMU Operating Mode

FI/FV*#	Ch# Force Function
0	FV
1	FI

MI/MV*#	Ch# Measure Function
0	MV
1	MI

High Impedance

The PMU may be placed in an off state where it maintains a high impedance between the supply voltages VCC_SV and VEE. In addition, there is the ability to turn off the forcing op amp, although care should be exercised when doing this due to the large transient response possible when turning the op amp back on.

TABLE 39. High Impedance

PPMU-En#	Ch# Forcing Op Amp Status
0	HiZ
1	Active

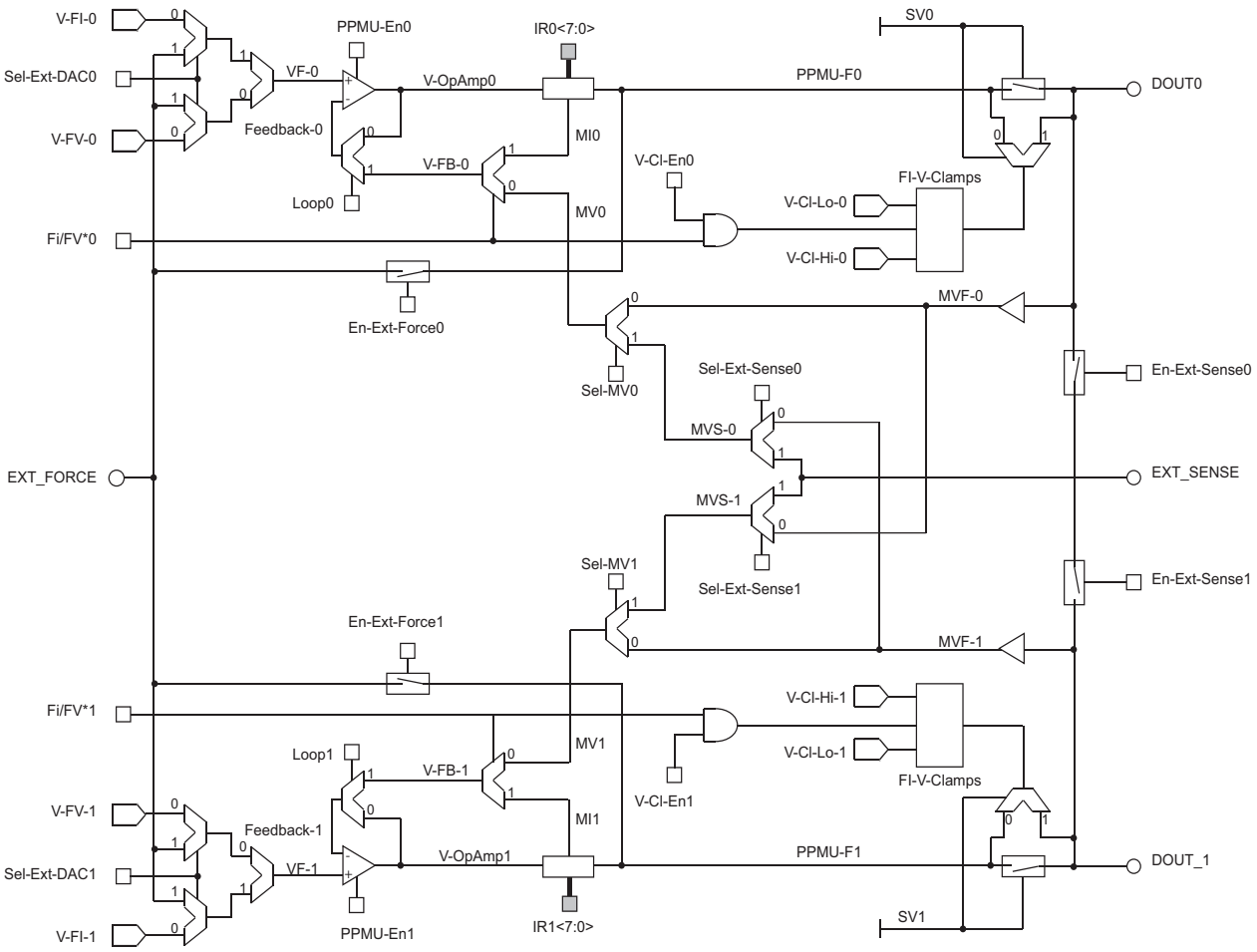


FIGURE 41.

Current Force

FI mode has the following transfer function translating the voltage input to a current output.

TABLE 40. Current Force

V-FI	Current at DOUT
–1V	–Imax
0V	0
+1V	+Imax

Current Ranges

The PMU can force and sense current up to a maximum of 32mA. In order to achieve the maximum accuracy while measuring smaller currents, 8 current ranges are supported.

TABLE 41. Current Ranges

Current Range	Imax	Rsense
IR0	2µA	500kΩ
IR1	8µA	125kΩ
IR2	32µA	31.25kΩ
IR3	128µA	7.81kΩ
IR4	512µA	1.95kΩ
IR5	2mA	500Ω
IR6	8mA	125Ω
IR7	32mA	31.25Ω

The CPU selects the current range by setting the range select bit high. Each range select bit is independent in that it is possible to select more than one range simultaneously. However, this option should be used only when changing ranges as a means of controlling the transient response associated with a range change.

It is NOT recommended that more than one range be active at the same time when taking a measurement.

FI Voltage Clamps

Each PMU has a set of programmable voltage clamps that limit the voltage swing at forcing op amp feedback voltage (V-FB) when the PMU is forcing current. These clamps protect the DUT when current is being forced into a high impedance node at the DUT.

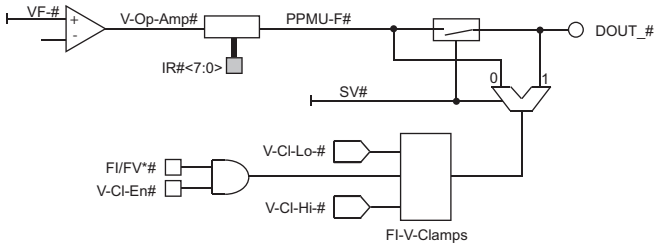


FIGURE 42.

The clamps may be turned off by setting V-Cl-En# = 0, in which case the clamps have no effect while DOUT varies between the supply voltages VCC-SV and VEE.

TABLE 42. FI Voltage Clamps

V-Cl-En#	V-FB	Ch# Clamps
0	X	Not Active
1	V-FB > V-Cl-Hi	DOUT = V-Cl-Hi
1	V-FB < V-Cl-Lo	DOUT = V-Cl-Lo
1	V-Cl-Lo < V-FB < V-Cl-Hi	Not Active

If the sensed voltage exceeds the high or low voltage clamp, the PMU reduces the output current in order for the output voltage to not exceed the clamp. If the voltage subsequently returns back to within the clamp thresholds, the PMU resumes forcing the programmed current.

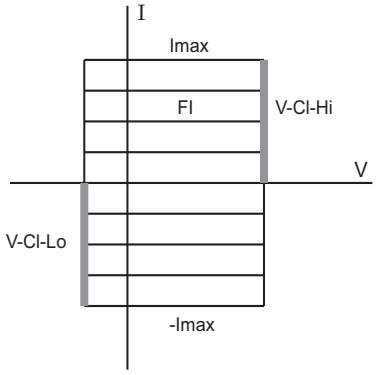


FIGURE 43.

Local Sense

Local sense changes the voltage clamp sense point automatically whenever the real time PMU switch is open to guarantee that the voltage clamps do not false activate whenever the switch is opened.

Voltage Force

In FV mode the source of the forced voltage may be selected from either on-chip DC level V-FV or the voltage on the EXT_FORCE pin.

TABLE 43. Voltage Force

Sel-Ext-DAC#	Ch# FV Source	DOUT_#
0	V-FV-#	V-FV-#
1	EXT_FORCE	EXT_FORCE

Feedback Options

When forcing a voltage, the PMU has a variety of configurations with different voltage feedback points:

1. Forcing op amp output
2. PMU force node
3. DOUT_#
4. Other channel's feedback point
5. EXT_SENSE.

TABLE 44.

Loop#	FI/FV#	Sel-MV#	Sel-Ext-Sense	Mode	Feedback#
0	X	X	X	FV	V Op Amp#
1	1	X	X	FI	MI#
1	0	0	X	FV	MVF-#
1	0	1	0	FV	MV(1-#)
1	0	1	1	FV	EXT_SENSE

Tight Loop Option

With Loop = 0, the forcing op amp will be configured as a unity gain amplifier tracking either V-FV or V-FI. This tight loop is the default condition upon reset or power up.

The tight loop configuration is NOT used for any traditional PMU FI or FV function. It is used mainly for:

1. A stable default condition
2. Resistive load applications
3. Super voltage applications.

Real Time Control Options

The PMU may be connected and disconnected to DOUT under real time pattern control. Being able to switch the PMU in and out at test rate speeds, rather than at CPU speeds, may be useful for:

1. Faster tester throughput
2. Resistive load applications
3. Super voltage applications
4. HiZ force situations.

TABLE 45. Real Time Control Options

SV#	PMU to DOUT_#
0	Disconnected
1	Connected

There are two high-speed inputs that can be used to control this option:

1. SV
2. EN

TABLE 46.

Sel-SV#-En	SV#	Control
X	CPU-SV#	CPU
0	SV_#	Real Time
1	RT-En#	Real Time

SV is a real time input dedicated to connecting and disconnecting the PMU and DOUT independent of the state of the driver. When EN is used, the PMU is connected whenever the driver is into HiZ and is disconnected whenever the driver is active. In addition, the CPU port can drive the SV switch directly.

Hold Function

The SV signal may be held at a constant level regardless of any real time changes present at the SV pin.

TABLE 47. Hold function

Hold-SV#	SV# Source
0	SV_#
1	Latched State

CPU Control

SV may be controlled directly by the CPU port which can then override any real time changes in either SV or RT-En*.

TABLE 48. CPU Control

Sel-RT-SV#	SV#
0	CPU-SV
1	RT-SV

Measurement Unit

The measurement unit is the circuitry that translates the voltage or the current being sensed into an output voltage (V-MU-#) that can be measured or compared against an upper and lower limit. In addition to measuring the voltage or current at a channel's DOUT pin, the measurement unit may also monitor the V-MU from the other channel or a variety of internal test nodes.

TABLE 49. Measurement Unit

Sel-MU#	Sel-MU#-Diag	MI/MV*#	V-MU#
1	X	X	V-Sense-(1-#)
0	1	X	Test & Cal-#
0	0	0	MV#
0	0	1	MI#

An on-chip window comparator supports a 2-bit "go/no-go" test. V-MU is the input voltage to the comparators and the thresholds are set via on-chip DC level generators through the CPU port. The window comparator outputs PPMU-CA and PPMU-CB may be read back directly through the CPU port, providing direct access to the actual comparator status at any time, or they may be routed off chip through the COMP_A and COMP_B pins.

Current Measure

When MI / MV* = 1, V-Sense will be an analog voltage that is proportional to the current flowing through DOUT. Imax is determined by the current range selection.

TABLE 50.

V-Sense	Iout
–1V	–Imax
0V	0
+1V	+Imax

Voltage Measure

When MI / MV* = 0, V-Sense will be an analog voltage equal to the voltage present at MV#.

V-Sense-# = MV#

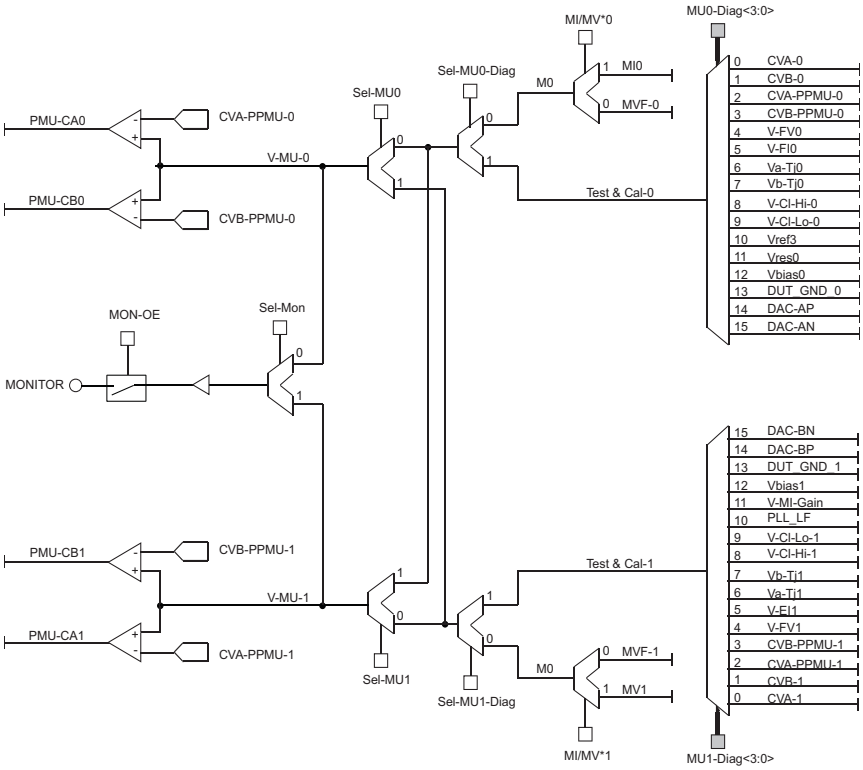


FIGURE 44.

Monitor

MONITOR_# is an analog voltage output whose voltage source is the measurement unit output from either channel (V-MU-0 or V-MU-1).

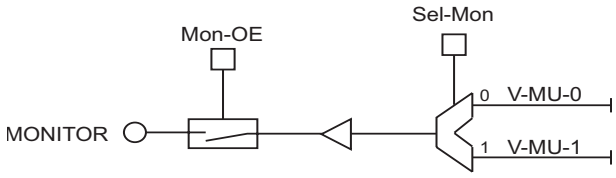


FIGURE 45.

Monitor Transfer Function

When measuring voltage, MONITOR_# has a 1:1 transfer function with DOUT. When measuring current, MONITOR_# varies between -1V and +1V for -Imax and +Imax.

TABLE 51. Monitor Transfer Function

Mode	MONITOR	DOUT
MV	Voltage at DOUT	DOUT
MI	–1V	–Imax
MI	0V	0
MI	+1V	+Imax

Monitor High Impedance

The monitor outputs may be placed into a high impedance state. This HiZ feature is useful when connecting multiple MONITOR pins from multiple ICs to one A to D converter.

TABLE 52. Monitor High Impedance

Mon-OE	Sel-Mon	MONITOR
0	X	HiZ
1	0	V-MU-0
1	1	V-MU-1

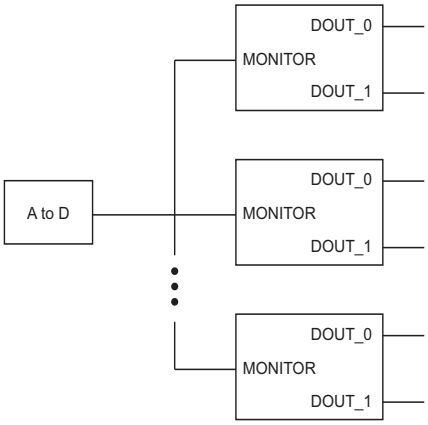


FIGURE 46.

Resistive Load

The PMU may be configured as a resistive load that acts like a selectable resistor to a programmable voltage level.

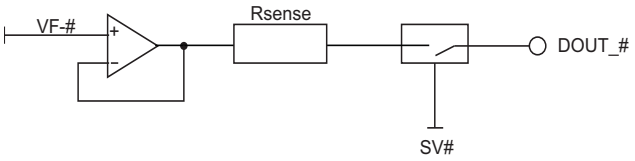


FIGURE 47.

Load Voltage

To establish the load voltage source, select V-FV, program it to the desired voltage level and set Loop = 0. In this configuration the forcing op amp will be a low impedance voltage source.

- FI / FV* = 0 (FV mode)
- V-FV = Desired Load Voltage
- Loop = 0 (Tight Loop).

Load Resistor

The resistance between the load voltage and DOUT will be the series combination of the sense resistor inside the PMU and the on resistance of the real time super voltage controlled isolation switch.

Rload = Rsense + R(SV Switch)

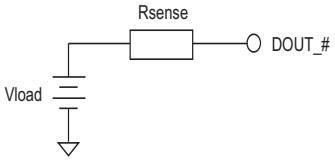


FIGURE 48.

Rsense

The value of the sense resistor is determined by the current range selection.

TABLE 53. RSense

Current Range	Imax	Rsense
IR0	2µA	500kΩ
IR1	8µA	125kΩ
IR2	32µA	31.25kΩ
IR3	128µA	7.81kΩ
IR4	512µA	1.95kΩ
IR5	2mA	500Ω
IR6	8mA	125Ω
IR7	32mA	31.25Ω

HiZ Force

HiZ force uses a similar configuration as does the resistive load. However, in this case, the PMU is placed into a low current mode (high Rsense value) and is connected whenever the driver goes into HiZ. The PMU will pull the transmission line between the pin electronics and the DUT to a known and programmed state, rather than let it float.

Super Voltage

Super Voltage is a large positive voltage typically used during the testing and characterization of flash memory devices and it is realized by using the PMU as a very slow driver. The PMU is again configured in the same manner as for a resistive load but the programmed voltage is much higher.

Super voltage may be forced when the driver is in either a high or a low state with no restrictions. The value of the sense resistor, in conjunction with the capacitance on the output node, will determine the rise time of the super voltage waveform.

Diagnostics

Each PMU has access to key internal nodes so that the voltage on these nodes may be monitored. This access is useful for both testing and diagnostic purposes. The CPU port controls the access to the diagnostic nodes.

TABLE 54. Diagnostics

Sel-MU#-Diag	MI/MV*#	V-Sense-#
0	0	MVF-#
0	1	MI#
1	X	Test & Cal-#

CHANNEL 0 DIAGNOSTIC SELECTION

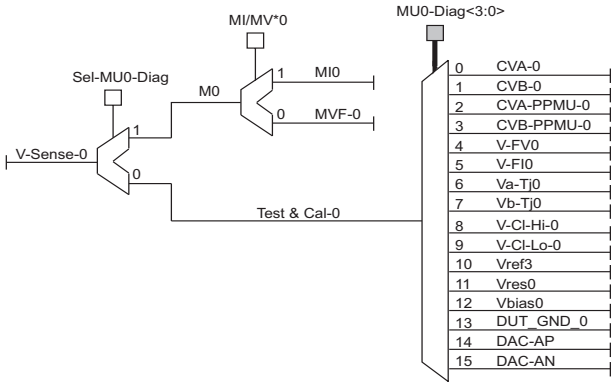


FIGURE 49.

CHANNEL 1 DIAGNOSTIC

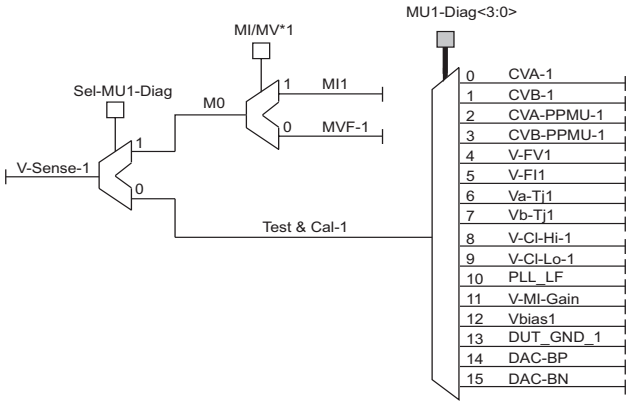


FIGURE 50.

Temperature Sensing

Each channel has its own independent temperature sense capability. There are two internal voltages: Va-Tj and Vb-Tj.

Which, when measured, may be used to calculate the junction temperature associated with each channel.

$Tj[^\circ C] = [\{(Va\text{-}Tj) - (Vb\text{-}Tj)\}] * 1{,}634 \} - 234$

External Force and Sense

EXT_FORCE and EXT_SENSE may be directly connected to either DOUT_0 or DOUT_1 or to each other. These paths are useful to completely bypass the pin electronics and provide for direct access to the DUT with no active circuitry in the path. This access is useful for:

- Connecting a central PMU to the DUT
- Direct measurement of the DUT voltage
- DC calibration.
- Establishing a Kelvin connection with an external PMU prior to contacting the DUT.

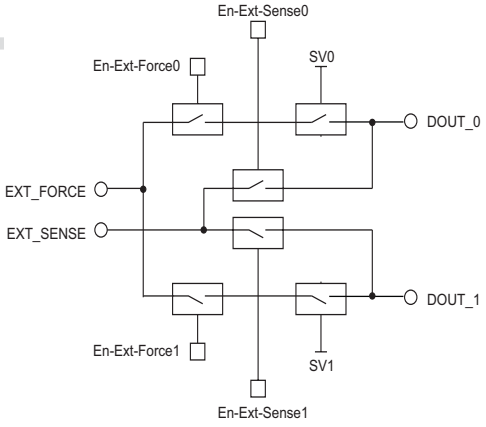


FIGURE 51.

TABLE 55. External Force and Sense

SV#	En-Ext-Force#	EXT_FORCE to DOUT#
0	X	Open
1	0	Open
1	1	Connected

SV#	En-Ext-Sense#	DOUT_# to EXT_SENSE
X	0	Open
X	1	Connected

DC Levels

Every functional block requires a variety of DC voltage levels in order to function properly. These levels are all generated on chip with a 16-bit DAC that is programmed through the CPU port.

There are 4 voltage range options. Various DC levels are grouped together, and the selected voltage range is common for all levels within each group. (See Table 56)

The realizable voltage range is restricted by the power supply levels and headroom limitations, especially in VR2. If a level is programmed beyond the recommended operating conditions, saturation will occur and the actual DC level will not match the desired programmed level.

Voltage Range Options vs. Function

Within each DAC group, the voltage range selection is common and is programmed via the CPU port.

CVA-PPMU and CVB-PPMU should only use the IR range when measuring current (MI), and only use VR0, VR1, or VR2 when measuring a voltage (MV).

TABLE 56. Voltage Range Options vs. Function

Range Select<1:0>	Voltage Range	Output Voltage Swing	Resolution (LSB)	Scale Factor (SF)	Vmid
0	VR0	–0.5V to +3.5V	61µV	2	+1.5V
1	VR1	–1V to +7V	122µV	4	+3.0V
2	VR2	–2V to +14V	244µV	8	+6.0V
3	VIR	–1V to +1V	30.5µV	1	0V

Level Programming

Voltage ranges VR0, VR1 and VR2 use the equation:

$$Vout = (Value - Vmid) \bullet Gain + Offset + Vmid + DUT\_GND$$

Programming Currents (VIR) uses the equation:

$$Vout = (Value - Vmid) \bullet Gain + Offset + Vmid$$

Value is described by the equation:

$$Value = \{(DAC\ Code) / (2^{**}N - 1)\} \bullet FS + Vmin,$$

where

$$N = 16;\ 2^{**}N - 1 = 65,535$$

and

$$Vmin = Vmid - (FS / 2)$$

FI

FS = 2V

Vmin = –1V

Vmid = 0V

Vmax = +1V.

Offset and Gain

Each individual DC level has an independent offset and gain correction. These correction values allow the desired output level to be programmed at their true post calibrated value and to be loaded simultaneously across multiple pins without having to correct for per pin errors. The range of possible offset voltage correction is a percentage of the full scale voltage range of each particular voltage group.

TABLE 57. Offset and Gain

Offset Code	Offset Value	Gain Code	Gain Value
0000H	–5.4% of FS	0000H	0.875
7FFFH	0	7FFFH	1.0
FFFFH	+5.4% of FS	FFFFH	1.125

Device Under Test Ground

DUT_GND_# is a high impedance analog voltage input that provides a means of tracking the destination ground and making an additional offset to the programmed level so the programmed level is correct with respect to the DUT.

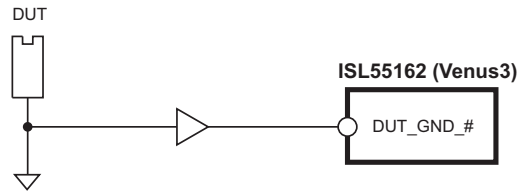


FIGURE 52.

The input at DUT_GND_# should be:

1) filtered for noise

2) stable

3) reflect the actual ground level at the DUT.

TABLE 58. Range Decode

Group	Functional Block	VR0	VR1	VR2	VIR	Range Select Bits <1:0>
Drive	Driver **DVH, DVL, VTT**	√	√	√		Drive#<1:0>
Comp	Comparator Thresholds **CVA, CVB**	√	√	√		Comp#<1:0>
PPMU	PPMU Comparator Thresholds **CVA-PPMU, CVB-PPMU**	√	√	√	√	PPMU#<1:0>
FV	Voltage Clamps **V-Cl-HI, V-Cl-Lo** PPMU Voltage Force **V-FV**	√	√	√		FV#<1:0>
FI	PPMU Current Force **V-FI**				√	N/A
	Tracks DUT_GND (FV, MV)					
	Does NOT Track DUT_GND (FI, MI)					

Voltage Range Options vs. Function

Different functional blocks require different DC level voltage ranges. The allowed combinations are listed in Table 58.

DC Calibration

The part is designed and tested to meet its DC accuracy specifications after a two point, two iteration calibration. The actual calibration points are different for each voltage range, and may even be different for the same voltage range but for different functional blocks. In general, most calibration points will be at 20% and 80% of the full scale value for that range. (The actual calibration points are listed separately for each functional block in the DC specification section.)

The test points are broken into two categories:

1. inner test
2. outer test.

The inner test is one specific test point (typically) at 50% of the full scale value of the particular range. The outer test is usually taken at the end points of the voltage range, or 0% and 100% of the full scale value.

In general, the inner test will be performed against tighter, more accurate limits. But every part shipped will be calibrated and tested against the limits in the specification section, and is guaranteed to perform within those limits under the documented calibration technique.

Typical calibration and test point set-up:

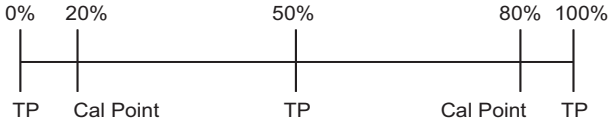


FIGURE 53.

System Level DC Accuracy

Other calibration schemes and techniques, using more or fewer calibration points or different test points, may also be employed. The resulting system level accuracy may be superior or inferior to the part's specified limits, and will be dependent on the details of the particular application.

CALIBRATION PROCEDURE

1. Calibrate the MONITOR
2. Calibrate the DAC using the DAC cal bits
3. Calibrate the Offset DAC
4. Calibrate the Gain DAC
5. Calibrate the DC Level

Level Calibration

INITIALIZE

- Select desired voltage range (VR0, VR1, VR2, VIR)
- Set Gain = 1.0; Offset = 0.0V

MEASURE

- Set Level 1 = Cal Point 1. Measure Output1'
- Set Level 2 = Cal Point 2. Measure Output2'

CALCULATE

- Gain' = (Output2' - Output1') / (Level 2 - Level1)
- Offset' = (Output2' - Vmid) - Gain' • (Level2 - Vmid)

FINISH

- Set Offset = - Offset' / Gain'
- Set Gain = 1.0 / Gain'

DAC Calibration

To facilitate superior DC accuracy, the DAC supports the ability to independently calibrate the top 5 MSBs. The default condition of these adjustment bits is the zero correction state.

The magnitude of the bit correction is an integer count of LSB voltage added or subtracted from the individual bit weighting, and is therefore a function of the particular voltage range selected for each level. The DAC MSB adjustment is applied to the DC level prior to the gain correction.

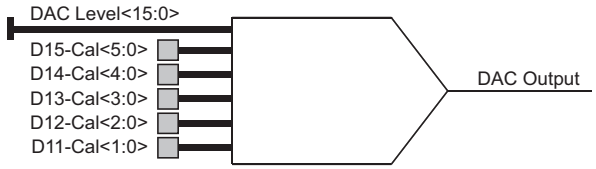


FIGURE 54.

TABLE 59. D15 Calibration

Cal 5	Cal 4	Cal 3	Cal 2	Cal 1	Cal 0	Adjustment
0	1	1	1	1	1	+93 LSB
			•			•
0	0	0	0	0	1	+3 LSB
0	0	0	0	0	0	No Adjustment
1	0	0	0	0	0	No Adjustment
1	0	0	0	0	1	–3 LSB
			•			•
1	1	1	1	1	1	–93 LSB

TABLE 60. D14 Calibration

Cal 4	Cal 3	Cal 2	Cal 1	Cal 0	Adjustment
0	1	1	1	1	+45 LSB
		•			•
0	0	0	0	1	+3 LSB
0	0	0	0	0	No Adjustment
1	0	0	0	0	No Adjustment
1	0	0	0	1	–3 LSB
		•			•
1	1	1	1	1	–45 LSB

TABLE 61. D13 Calibration

Cal 3	Cal 2	Cal 1	Cal 0	Adjustment
0	1	1	1	+21 LSB
	•			•
0	0	0	1	+3 LSB
0	0	0	0	No Adjustment
1	0	0	0	No Adjustment
1	0	0	1	–3 LSB
	•			•
1	1	1	1	–21 LSB

TABLE 62. D12 Calibration

Cal 2	Cal 1	Cal 0	Adjustment
0	1	1	+9LSB
0	1	0	+6 LSB
0	0	1	+3 LSB
0	0	0	No Adjustment
1	0	0	No Adjustment
1	0	1	–3 LSB
1	1	0	–6 LSB
1	1	1	–9 LSB

TABLE 63. D11 Calibration

Cal 1	Cal 0	Adjustment
0	1	+3 LSB
0	0	No Adjustment
1	0	No Adjustment
1	1	–3 LSB

TABLE 64. Cal Range vs. Voltage Range vs. DAC Bit

	D15	D14	D13	D12	D11
VR0	5.67mV	2.75mV	1.28mV	549µV	183µV
VR1	11.35mV	5.5mV	2.56mV	1.1mV	366µV
VR2	22.7mV	10.1mV	5.12mV	2.2mV	732µV
VIR	2.84mV	1.38mV	640.5µV	275µV	91.5µV

External References & Components

Many on chip functional blocks reference a precision external:

1. Voltage
2. Resistance
3. Frequency.

By locking on chip performance to an external reference, circuit performance will be more consistent over:

1. variations in ambient temperature
2. part to part distribution.

V_REF

V_REF is an analog input voltage that is used to program the on chip DAC levels. V_REF should be held at +3.0V. Any noise or jitter on V_REF will contribute to the noise floor of the chip and therefore the V_REF should be filtered and be as quiet and stable as possible. There is one V_REF shared by both channels.

R_EXT

R_EXT is an external resistor used to control the output impedance of the driver. An external precision resistor with a low temperature coefficient will result in the driver output impedance remaining stable over changes in the ambient temperature.

R_EXT also determines the range of the output impedance adjustment for DVH, DVL and VTT with a total adjustment range of ± R_EXT/2000. There is one R_EXT pin shared by both channels.

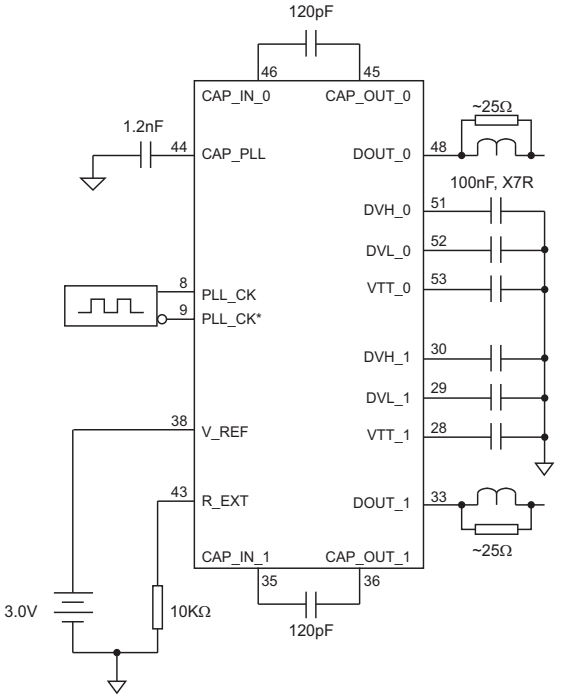


FIGURE 55.

Compensation Pins

CAP_IN_# and CAP_OUT_# are used for off chip capacitors used to compensate the PPMU op amp. An external capacitor must be connected between these two pins for each channel. The actual capacitor value may vary with the application as settling time and stability may be traded off.

PLL Frequency

PLL_CK is an external frequency that establishes the range and resolution of all on-chip delay elements, as well as the propagation delay of all logic gates in series with the high speed driver and comparator signal paths. **For any applications that do not use any delay elements, PLL_CK must be placed in a low state. Do NOT leave PLL_CK / PLL_CK* floating.**

PLL Filter Capacitor

A capacitor at pin CAP_PLL is used to compensate the op amp used in the PLL filter circuitry. The other end of the capacitor should be connected to ground.

Transmission line Inductors and Resistors

Depending on the particular application and specific details of the PC Board layout a series inductor with a parallel resistor may, or may not, be placed at the DOUT pin to compensate for the capacitance on that node. The actual inductor and resistor value is application specific.

Power Supply Restrictions

The following guidelines must be met to support proper operation:

1. VCC_SV ≥ VCC
2. VCC ≥ VDD; VEE ≤ GND
3. VDD ≥ GND.

Schottky diodes are recommended on a once per board basis to protect against a power supply restriction violation.

Power Supply Sequence

Ideally, all power supplies would become active simultaneously while also meeting the power supply restrictions. However, since it is difficult to guarantee simultaneous levels, the following sequence is recommended:

1. VEE
2. VCC_SV
3. VCC
4. VDD
5. V_REF

.

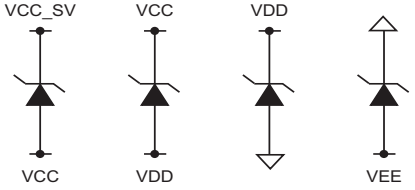


FIGURE 56.

ESD/EOS Protection

For the best Electrostatic Discharge (ESD) / Electrical Overstress (EOS) protection for the DOUT pins, please follow the guidelines below.

1. External Diodes on DOUT: Enhanced resistance to ESD can be improved by connecting 2 small signal diodes to the DOUT pin. One diode should be connected from VCC_SV to DOUT and the other from VEE to DOUT. These should be as close to the part and power planes as possible. Special attention should be paid to the leakage and AC performance specifications for these diodes. 1N914 silicon surface mount diodes are recommended.

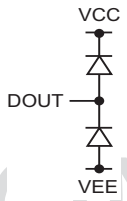


FIGURE 57.

2. Maximum Powered-On ESD Protection on pin DOUT_0 and DOUT_1
   a. Select Fast-HiZ. Set Fast-HiZ-En# in the Driver Configuration registers to 1.
   b. Program VTT_# to 2.5V or a voltage that meets the criteria listed in section 3 below.
   c. Select VTT Driver Mode. Set Dr-Mode# in the Driver Control registers to 1.
   d. Ensure SV# is low.
   e. Drive VTT. This can be accomplished two ways.
      1) Use the real time path through the part by driving pin pairs EN_#/EN_#* low.
      2) Use the CPU-En path. Set Sel-RT-En# in the Drive Control registers to 0.
      3) Set CPU-En0 and CPU-En1 in the CPU Force register to 0.
3. Driver Levels Programmed Values:
   a. Driver levels programming in driver mode:
      1) |DVH - DVL| <=8V
      2) |DVH - VTT| <=8V
      3) |DVL - VTT| <=8V
   b. When DOUT is in Hi-Z or PMU mode the driver levels should meet the following restrictions:
      1) |DOUT - DVH| <=8V
      2) |DOUT - DVL| <=8V
      3) |DOUT - VTT| <=8V

CPU Port

All on board DACs and registers are controlled through the CPU serial data port, which is capable of both writing to the chip as well as reading back from the chip (typically used for diagnostic purposes.)

Address

Address words for every CPU transaction are all 16 bits in length and contain the destination of the data word a write cycle, or the source to be read back for a read cycle. Address bits are shifted in LSB first, MSB last.

Data

Data words for every CPU transaction are all 16 bits in length and are loaded or read back LSB first, MSB last. The timing for data is different for a read cycle vs. a write cycle, as the drivers on the SDIO alternate between going into high impedance and driving the line.

Control Signals

There are 3 CPU interface signals - SDIO, CK, and STB. SDIO is a bidirectional data pin through which information is either loaded or written back. CK is the CPU port clock signal that transfers data back and forth. When data is going into the part, SDIO is latched on a rising edge of CK. When data is coming out of the part, SDIO is again updated on a rising edge of CK. STB is the control signal that identifies the beginning of a CPU transaction. STB remains high for the duration of the transaction, and must go low for at least 1 CK cycle before another CPU transaction may begin.

CK must be running at all times even if no CPU transactions are occurring. CK is used on chip for other functions and MUST run continuously for correct chip operation.

Write Enable

Various register bits in the memory map tables require a write enable (WE) to allow those bits to be updated during a CPU write cycle. WE control allows some bits within an address to be changed, while others are held constant. Each WE applies to all lower data bits, until another WE is reached.

If WE = 1, the registers in the WE group will be written to. If WE = 0, the registers will not be updated.

If WE = 0, the registers will not be updated but all data bits associated with that field must also be programmed to 0.

Read vs. Write Cycle

The first SDIO bit latched by CK in a transaction identifies the transaction type.

TABLE 65. Read vs. Write Cycle

1st SDIO Bit	CPU Transaction Type
0	Read – Data flows out of the chip
1	Write – Data flows into the chip

Parallel Write

The second SDIO bit of a transaction indicates whether a parallel write occurs.

TABLE 66. Parallel Write

2nd SDIO Bit	CPU Transaction Type
0	Data goes to the selected channel
1	Data goes to both channels

A parallel write ignores the particular channel address and writes the information into the same location on both channels.

Reset

RESET is an external hardware reset signal that places all internal registers and control lines into a low state. Reset must be executed independently after a power up sequence. **RESET does NOT place the DAC level memory into a known state, so this information must always be loaded after a power up sequence.**

RESET is active high.

FIGURE 58.

In addition, the CPU port can execute a reset (as a write only transaction.) If the CPU-Reset address is written to, regardless of the value of any of the SDIO bits, CPU-Reset will fire off a one shot pulse that performs the same function as an external RESET.

Chip ID

Chip ID (see memory map tables) is a read only function that identifies the product and the die revision.

TABLE 67. Chip ID

SDIO<15:4>	SDIO<3:0>
Prod-ID<11:0>	Die-Rev<3:0>

Product ID = 067 Hex = 103 Decimal.

DAC Sample and Hold (S/H) State Machine

The internal DACs used in the ISL55162 are S/H DACs. To update a single DAC level it takes 387 clock cycles. The clock used for this operation is the CPU interface clock. The first 256 clocks are used to select the desired level and let the DAC level settle. The next 128 clocks are needed to refresh the S/H. The 3 remaining clocks are used to control the state machine. To calculate the time to refresh one DAC level, multiply the CPU clock time by the number of clocks needed to update one level. If using a 25MHz clock, the time needed is: 40nS * 387cycles = 15.48µS. There are 28 total internal levels to the S/H DAC; therefore, to update all levels, the time would be: 28 * 40nS * 387cycles = 433.44µS.

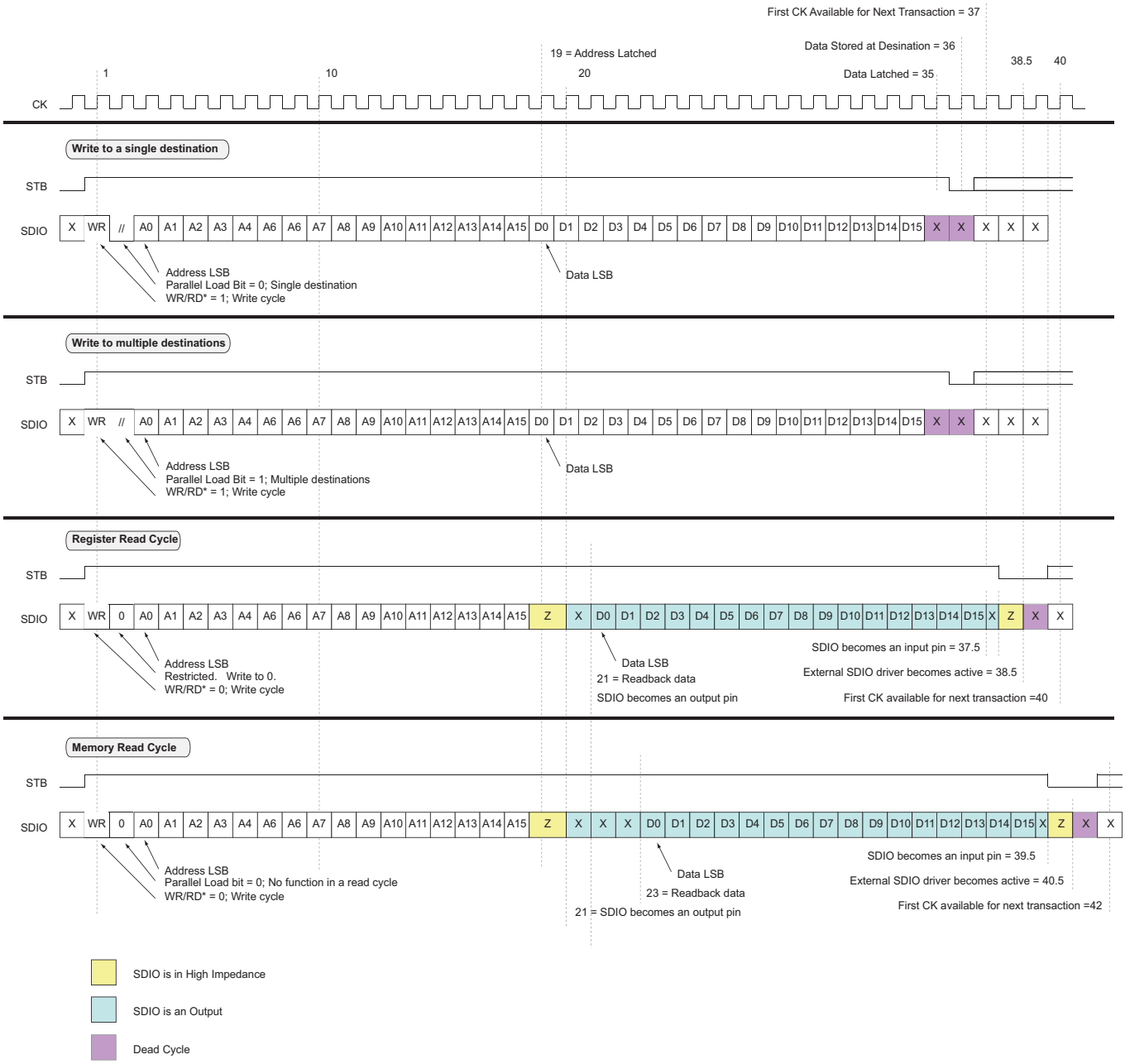
The sequence that the state machine uses to refresh the DAC matches the RAM address mapping: DVH-0, DVH-1, DVL-0, DVL-1, etc. This order allows both channels to update whenever a parallel write is performed for the same level on both channels.

When writing to a specific level, the state machine will complete the current level, then jump to the level which was just written. The state machine then proceeds in the normal order; it doesn't jump back. Therefore, you should assume, at worst case, it takes 774 clocks to update a single level after being written, 387 to complete the current level plus 387 to update the desired level. One caveat to this is with a parallel-channel write. There will still be, at worst case, 774 clocks to update channel 0 of the parallel-channel write. Channel 1 will be updated in sequence after channel 0. This means that if channel 0 and channel 1 are written as part of a parallel-channel write, channel 0 could take 774 clocks to update (worst case) and then channel 1 will update 387 clocks later.

There is another consideration when writing RAM location values. As stated above, there is a latency between when a new RAM value is written to a RAM location and when the actual voltage value will start to update due to the sample and hold. When a RAM value is written, its address is written to a "next address" stack so that it is the next address to be updated by the sample and hold DAC after the current location is finished. This "next address" stack is only 1 address deep; therefore, if you push another address on the stack before the current one is popped, you will lose the current "next address" to be written. This does not mean the RAM location will not be updated, it will just take a longer time to update. With this in mind, for the fastest update when writing several levels, the user should write the various levels in the reverse order that the S/H loop goes through them. This way, after completing the last write, all levels will update in order. For example, if you want to update DVH, DVL, and VTT, you would write VTT first, then DVL, then DVH.

The user also needs to be aware that when continuously writing to a particular level, other levels may be starved of being refreshed by the CPU clock. If this happens, levels can droop out of specification.

Protocol Timing Diagram



Memory Space

Information is stored on-chip in two ways:

- RAM
- Registers

Each storage mechanism is then broken into two categories:

- Per pin resources
- Central resources

TABLE 68. Memory Space

Address Range	Function
0 – 63	Channel 0 RAM (DC Levels)
64 – 111	Channel 0 Registers
112 – 127	Central Registers
128 – 191	Channel 1 RAM (DC Levels)
192 – 239	Channel 1 Registers
240 – 255	Central Registers
256+	Unused

TABLE 69. RAM Storage

Channel 0 Address	Channel 1 Address	Resource	D15 –D0
0	128	DVH-#	DAC Level
1	129	DVL-#	DAC Level
2	130	VTT-#	DAC Level
3	131	CVA-#	DAC Level
4	132	CVB-#	DAC Level
5	133	CVA-PPMU-#	DAC Level
6	134	CVB-PPMU-#	DAC Level
7	135	V-FV-#	DAC Level
8	136	V-FI-#	DAC Level
9	137	V-CI-Hi-#	DAC Level
10	138	V-CI-Lo-#	DAC Level
11–15	139–143	Not Used	

Channel 0 Address	Channel 1 Address	Resource	D15 –D0
16	144	DVH-#	DAC Level Offset
17	145	DVL-#	DAC Level Offset
18	146	VTT-#	DAC Level Offset
19	147	CVA-#	DAC Level Offset
20	148	CVB-#	DAC Level Offset
21	149	CVA-PPMU-#	DAC Level Offset
22	150	CVB-PPMU-#	DAC Level Offset
23	151	V-FV-#	DAC Level Offset
24	152	V-FI-#	DAC Level Offset
25	153	V-CI-Hi-#	DAC Level Offset
26	154	V-CI-Lo-#	DAC Level Offset
27–31	155-159	Not Used	

Channel 0 Address	Channel 1 Address	Resource	D15 –D0
32	160	DVH-#	DAC Level Gain
33	161	DVL-#	DAC Level Gain
34	162	VTT-#	DAC Level Gain
35	163	CVA-#	DAC Level Gain
36	164	CVB-#	DAC Level Gain
37	165	CVA-PPMU-#	DAC Level Gain
38	166	CVB-PPMU-#	DAC Level Gain
39	167	V-FV-#	DAC Level Gain
40	168	V-FI-#	DAC Level Gain
41	169	V-CI-Hi-#	DAC Level Gain
42	170	V-CI-Lo-#	DAC Level Gain
43–63	171–191	Not Used	

Per Channel Registers - Driver

Address	Resource	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
64 0040H 192 00C0H	Driver Terminations							WE	Sel-En#-BP	WE	Sel-D#-BP	WE	EZ#<1>	EZ#<0>	WE	DZ#<1>	DZ#<0>
65 0041H 193 00C1H	Driver Configuration	WE	CPU-XOR#	D#-XOR		WE	Sel-En#-OR	WE	HiZ-Override	WE	Fast-HiZ-En#	WE	Sel-SV#-En	WE	Sel-D#-OR	Sel-En#	Sel-D#
66 0042H 194 00C2H	Driver Control	WE	Hold-SV#	WE	Hold-En#	WE	Hold-D#			WE	Dr-Mode#	WE	Sel-RT-SV#	WE	Sel-RT-En#	WE	Sel-RT-D#
67 0043H 195 00C3H	Data Deskew	WE	Sel-D#-CD	WE	D#-CD<4>	D#-CD<3>	D#-CD<2>	D#-CD<1>	D#-CD<0>	WE	Sel-D#-FD		WE	D#-FD<3>	D#-FD<2>	D#-FD<1>	D#-FD<0>
68 0044H 196 00C4H	Data Falling Edge Adjust	WE	Sel-D#-CFEA		WE	D#-CFEA<3>	D#-CFEA<2>	D#-CFEA<1>	D#-CFEA<0>	WE	Sel-D#-FFEA		WE	D#-FFEA<3>	D#-FFEA<2>	D#-FFEA<1>	D#-FFEA<0>
69 0045H 197 00C5H	Enable Deskew	WE	Sel-En#-CD	WE	En#-CD4	En#-CD<3>	En#-CD<2>	En#-CD<1>	En#-CD<0>	WE	Sel-En#-FD		WE	En#-FD<3>	En#-FD<2>	En#-FD<1>	En#-FD<0>
70 0046H 198 00C6H	Enable Falling Edge Adjust	WE	Sel-En#-CFEA		WE	En#-CFEA<3>	En#-CFEA<2>	En#-CFEA<1>	En#-CFEA<0>	WE	Sel-En#-FFEA		WE	En#-FFEA<3>	En#-FFEA<2>	En#-FFEA<1>	En#-FFEA<0>
71 0047H 199 00C7H	Output Impedance		WE	RO-VTT#<3>	RO-VTT#<2>	RO-VTT#<1>	RO-VTT#<0>	WE	RO-DVH#<3>	RO-DVH#<2>	RO-DVH#<1>	RO-DVH#<0>	WE	RO-DVLV<3>	RO-DVL#<2>	RO-DVL#<1>	RO-DVL#<0>
72 – 79 200 – 207	Not Used																

NOTE: Channel 0 addresses are listed on the top, and Channel 1 addresses are listed on the bottom of each address entry.

Per Channel Registers - Comparator

Address	Resource	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
80 0050H 208 00D0H	Comparator Configuration				WE	Sel-C#-BP	WE	CPU-CB#	CPU-CA#	WE	Sel-CPU-C#	WE	Sel-Ch#-Mux		WE	Sel-MU-B#	Sel-MU-A#
81 0051H 209 00D1H	Comp A Deskew	WE	Sel-CA#-CD	WE	CA#-CD<4>	CA#-CD<3>	CA#-CD<2>	CA#-CD<1>	CA#-CD<0>	WE	Sel-CA#-FD		WE	CA#-FD<3>	CA#-FD<2>	CA#-FD<1>	CA#-FD<0>
82 0052H 210 00D2H	Comp A Falling Edge Adjust								WE	Sel-CA#-FFEA		WE	CA#-FFEA<4>	CA#-FFEA<3>	CA#-FFEA<2>	CA#-FFEA<1>	CA#-FFEA<0>
83 0053H 211 00D3H	Comp B Deskew	WE	Sel-CB#-CD	WE	CB#-CD<4>	CB#-CD<3>	CB#-CD<2>	CB#-CD<1>	CB#-CD<0>	WE	Sel-CB#-FD		WE	CB#-FD<3>	CB#-FD<2>	CB#-FD<1>	CB#-FD<0>
84 0054H 212 00D4H	Comp B Falling Edge Adjust								WE	Sel-CB#-FFEA		WE	CB#-FFEA<4>	CB#-FFEA<3>	CB#-FFEA<2>	CB#-FFEA<1>	CB#-FFEA<0>
85 0055H 213 00D5H	Comparator Diagnostics (Read Only in Yellow) (Write Only in Green)	PMU-CB#	PMU-CA#	RT-CB#	RT-CA#				WE	CPU-Pulse#	WE	D#-Diag	En#-Diag	Edge#-Par	En-SV#	Sel-C#-Diag	Ring#-En
86 – 95 216 – 223	Not Used																

NOTE: Channel 0 addresses are listed on the top, and Channel 1 addresses are listed on the bottom of each address entry.

Per Pin Channel Registers - PMU

Address	Resource	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
96 0060H 224 00E0H	PPMU Configuration			WE	PPMU-En#	WE	V-Cl-En#	WE	Sel-MV#	WE	Sel-MU#	WE	Loop#	WE	MI/MV*#	WE	FI/FV*#
97 0061H 225 00E1H	PPMU Current Ranges								WE	IR#<7>	IR#<6>	IR#<5>	IR#<4>	IR#<3>	IR#<2>	IR#<1>	IR#<0>
98 0062H 226 00E2H	Ext Force/Sense									WE	Sel-Ext-DAC#	WE	Sel-Ext-Sense#	WE	En-Ext-Sense#	WE	En-Ext-Force#
99 0063H 227 00E3H	PPMU Diagnostics									WE	Sel-MU#-Diag		WE	MU#-Diag<3>	MU#-Diag<2>	MU#-Diag<1>	MU#-Diag<0>
100 0064H 228 00E4H	DC Level Range Select					WE	PPMU#<1>	PPMU#<0>	WE	FV#<1>	FV#<0>	WE	Comp#<1>	Comp#<0>	WE	Drive#<1>	Drive#<0>
101 – 111 229 – 239	Not Used																

NOTE: Channel 0 addresses are listed on the top, and Channel 1 addresses are listed on the bottom of each address entry.

Central Registers

Address	Resource	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
112 0070H	Monitor													WE	Sel-Mon	WE	Mon-OE
113 0071H	CPU Force				WE	CPU-SV1	WE	CPU-En1	WE	CPU-D1		WE	CPU-SV0	WE	CPU-En0	WE	CPU-D0
114 0072H	PLL						WE	PLL-Dis	WE	Fclamp<1>	Fclamp<0>	WE	Vswing<1>	Vswing<0>	WE	PLL-Z<1>	PLL-Z<0>
115 0073H	CPU Reset (Write Only)	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X
116 – 126 0076H 007EH	Not Used																
127 007FH	Die ID (Read Only)	Prod-ID<11>	Prod-ID<10>	Prod-ID<9>	Prod-ID<8>	Prod-ID<7>	Prod-ID<6>	Prod-ID<5>	Prod-ID<4>	Prod-ID<3>	Prod-ID<2>	Prod-ID<1>	Prod-ID<0>	Die-Rev<3>	Die-Rev<2>	Die-Rev<1>	Die-Rev<0>
– 214 00D6H	Upper DAC Bit Calibration				WE	D14-Cal<4>	D14-Cal<3>	D14-Cal<2>	D14-Cal<1>	D14-Cal<0>	WE	D15-Cal<5>	D15-Cal<4>	D15-Cal<3>	D15-Cal<2>	D15-Cal<1>	D15-Cal<0>
– 215 00D7H	Mid DAC Bit Calibration					WE	D11-Cal<1>	D11-Cal<0>	WE	D12-Cal<2>	D12-Cal<1>	D12-Cal<0>	WE	D13-Cal<3>	D13-Cal<2>	D13-Cal<1>	D13-Cal<0>
240 – 254 00F0H - 00FEH	Not used																
255 00FFH	Null Command	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X

Manufacturing Information

Moisture Sensitivity

The part is a Level 3 (JEDEC Standard 033A) moisture sensitive part. All Pre Production and Production shipments will undergo the following process post final test:

- Baked @ +125°C ± 5°C for a duration ≥ 16 hours
- Vacuum sealed in a moisture barrier bag (MBB) within 30 minutes after being removed from the oven.

PCB Assembly

The floor life is the time from the opening of the MBB to when the unit is soldered onto a PCB.

Product Floor Life ≤ 168 Hours

Units that exceed this floor life must be baked before being soldered to a PCB.

Solder Profile

The recommended solder profile is dependent upon whether the PCB assembly process is lead-free or not.

TABLE 70. Solder Profile

Profile Feature	Pb-Free Assembly
Average ramp up rate (T_L to T_P)	3°C/sec (max)
Preheat • Min Temp (Ts min) • Max Temp (Ts max) • Time (min to max) (ts)	 150°C 200°C 60 – 180 sec
Ts max to T_L • Ramp Up Rate	 3°C/sec (max)
Time above • Temperature (T_L) • Time (t_L)	 217°C 60 – 150 sec
Peak Temperature (T_P)	260°C
Time within 5°C of actual peak temp (tp)	20 sec – 40 sec
Ramp down rate	6°C/sec (max)
Time 25°C to peak temperature	8 minutes (max)

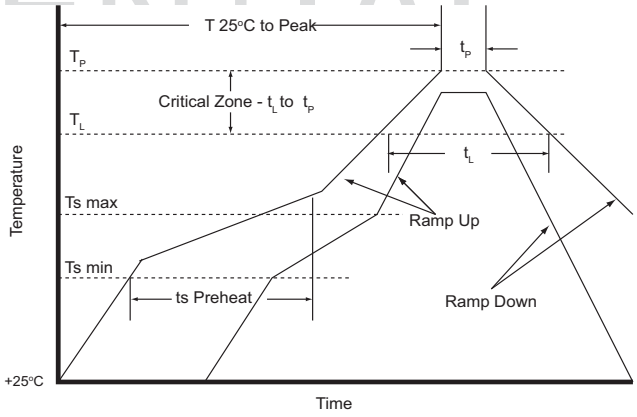


FIGURE 59.

Package Thermal Analysis

Junction Temperature

Maintaining a low and controlled junction temperature is a critical aspect of any system design. Lower junction temperatures translate directly into superior system reliability. A more stable junction temperature translates directly into superior AC and DC accuracy.

The junction temperature follows the equation:

$T_j = P_d \bullet \theta_{JA} + T_a$

T_j = Junction Temperature

P_d = Power Dissipation

θ_{JA} = Thermal Resistance (Junction to Ambient)

T_a = Ambient Temperature

Heat can flow out of the package through two mechanisms:

- conduction
- convection

Conduction

Conduction occurs when power dissipated inside the chip flows out through the leads of the package and into the printed circuit board. While this heat flow path exists in every application, most of the heat flow will NOT occur with thermal conduction into the PCB.

Conduction also occurs in applications using liquid cooling, in which case most of the heat will flow directly out of the top of the package through the exposed heat slug and into the liquid cooled heat sink. The heat sink represents a low thermal resistance path to a large thermal mass with a controlled temperature.

The total thermal resistance is the series combination of the resistance from the junction to case (exposed paddle) (θ_{JC}) plus the resistance from the case to ambient (θ_{CA})

Convection

The most common cooling scheme is to use airflow and (potentially) a heat sink on each part. In this configuration, most of the heat will exit the package via convection, as it flows through the die, into the paddle, and off the chip into the surrounding air flow.

Thermal Resistance

Each system will have its own unique cooling strategy and overall theta JA. However, the resistance between the junction and the case is a critical and common component to the thermal analysis in all designs.

$$\theta_{JA} = \theta_{JC} + \theta_{CA}$$

θ_{CA} is determined by the system environment of the part and is therefore application specific. θ_{JC} is determined by the construction of the part.

θ_{JC} CALCULATION

$$\theta_{JC} = \theta(\text{silicon}) + \theta(\text{die attach}) + \theta(\text{paddle})$$

The thermal resistance of any material is defined by the equation:

θ = (Intrinsic material resistance) • Thickness / Area

or

θ = Thickness / (Intrinsic material conductivity • Area).

INTRINSIC THERMAL CONDUCTIVITY

Die Attach Thermal Conductivity = 1.4 W / M °K

Silicon Thermal Conductivity = 141.2 W / M °K

Paddle Thermal Conductivity = 263 W / M °K

Plastic Thermal Conductivity = 0.88 W / M °K

(Although some heat will flow throw the plastic package, the molding compound conductivity is not specifically used in the calculation of Theta JC through the paddle.)

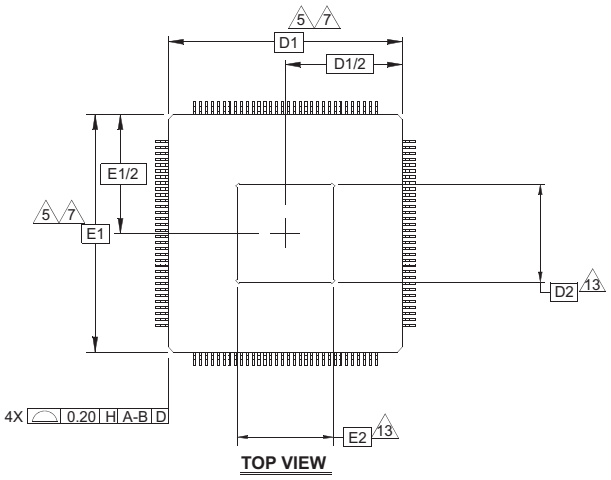
THERMAL RESISTANCE CALCULATION

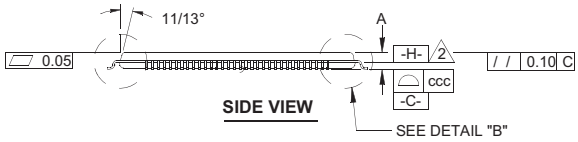
θ_{JC} = 0.12°C / W + 0.6°C/W + 0.01°C/W

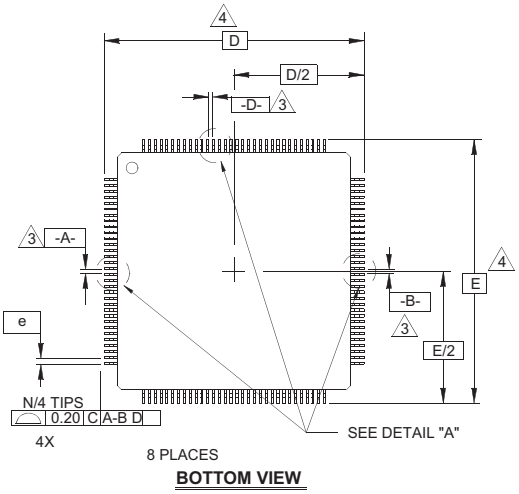
θ_{JC} = 0.73°C/W

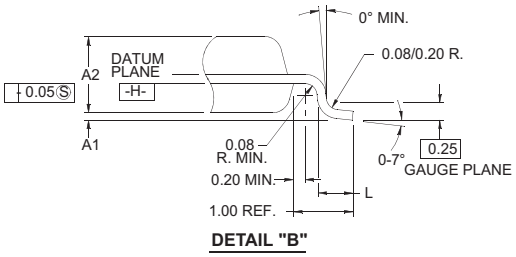
Package Information

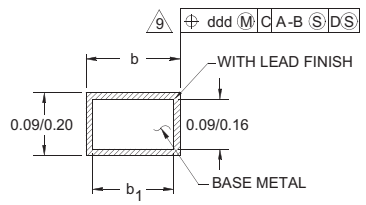
THIN PLASTIC QUAD FLATPACK PACKAGE WITH TOP EXPOSED PAD (TEP-LQFP)











Q64.10x10E

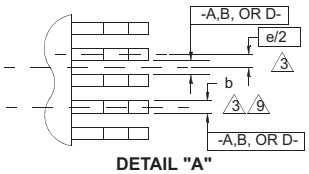
64 LEAD THIN PLASTIC QUAD FLATPACK PACKAGE WITH TOP EXPOSED PAD (TEP-LQFP)

SYMBOL	ACD MIN	ACD NOM.	ACD MAX	NOTES
A			1.20	
A1	0.05		0.15	12
A2	0.95	1.00	1.05	
D		12.00 BSC		4
D1		10.00 BSC		7, 8
D2		7.49 BSC		13
E		12.00 BSC		4
E1		10.00 BSC		7, 8
E2		7.49 BSC		13
L	0.45	0.60	0.75	
N		64		
e		0.50 BSC		
b	0.17	0.22	0.27	9
b1	0.17	0.20	0.23	
ccc			0.08	
ddd			0.08	

Rev. 0 6/09

NOTES:

1. All dimensions and tolerances per ANSI Y14.5-1982.
2. Datum plane -H- located at mold parting line and coincident with lead, where lead exits plastic body at bottom of parting line.
3. Datums A-B and -D- to be determined at center line between leads where leads exit plastic body at datum plane -H- .
4. To be determined at seating plane -C- .
5. Dimensions D1 and E1 do not include mold protrusion. Allowable mold protrusion is 0.254 mm on D1 and E1 dimensions.
6. "N" is the total number of terminals.
7. These dimensions to be determined at datum plane -H- .
8. The top of package is smaller than the bottom of package by 0.15 millimeters.
9. Dimension b does not include dambar protrusion. allowable dambar protrusion shall be 0.08mm total in excess of the b dimension at maximum material condition. Dambar cannot be located on the lower radius or the foot.
10. Controlling dimension: millimeter.
11. This outline conforms to jedec publication 95 registration MS-026, variations ACB, ACC, ACD & ACE.
12. A1 is defined as the distance from the seating plane to the lowest point of the package body.
13. Dimension D2 and E2 represent the size of the exposed pad.
14. Exposed pad shall be coplanar with bottom of package within 0.05.
15. JEDEC variation.



Revision History

DATE	CHANGE
January 8, 2016	• Page 63: Power Supply Sequence Section - change power supply sequence • Page 72: Table 70 - change Peak Temperature to 260 °C
April 1, 2015	• Change from Intersil to Elevate format
June 7, 2013	• Page 55: Temperature Sensing: Equation changed
December 3, 2012	• Page 60, add ESD/EOS Protection section • Page 61 - add DAC Sample and Hold Section

Ordering Information

PART NUMBER	PART MARKING	TEMP.RANGE (°C)	PACKAGE
ISL55162CNEZ (Note 1)	ISL55162CNEZ	+25°C to +100°C	64 Lead, 10mmx10mm TQFP w/top exposed heat slug

NOTES:

1. These Elevate Semiconductor Pb-free plastic packaged products employ special Pb-free material sets, molding compounds/die attach materials, and 100% matte tin plate plus anneal (e3 termination finish, which is RoHS compliant and compatible with both SnPb and Pb-free soldering operations). Elevate Semiconductor Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020.