SOC Pin Electronics Companion PMU/DAC/Resistive Load

ISL55187

The ISL55187 (Neptune Plus) is a highly integrated System-on-a-Chip pin electronics support solution incorporating two independent channels of:

- PMU
- DC Levels for the Pin Electronics
- Resistive Load

The interface, the control, and the I/O are digital. All analog circuitry is inside the chip. Two complete and independent channels are integrated into each chip.

For most tester applications, except for the pin electronics, no additional analog hardware is required on a per pin basis.

Features

- Per Pin PMU
  - FV, FI, MV, MI
  - 8 Current Ranges (32mA, 8mA, 2mA, 512µA, 128µA, 32µA, 8µA, 2µA)
  - FI Voltage Clamps
  - FV Current Clamps
  - On-Chip Current Ganging
  - Supports 64mA/Channel in FV Mode
- On-Chip DC Levels
  - All PMU Levels Generated On-Chip
  - 13 Levels/Channel Brought Off-Chip
  - 16 Bits per Level
  - 16 Bit per Level Offset Correction
  - 16 Bit per Level Gain Corrective
- Resistive Load
  - 8 Resistance Options
  - High Speed Real Time Control
- External Force/Sense Switches On-Chip
- 3-Bit Serial Port
- Package/Power Dissipation
  - 56 Ld 8mmx8mm QFN with Exposed Heat Slug
  - Pdq ≤ 343mW/channel; Pdq ≤ 685mW/Chip (No Output Current)
  - Pdmax ≤ 700mW/Channel/ Pdmax ≤1.4W/Chip (Maximum Output Current)

Applications

- Automated Test Equipment
- Instrumentation
- ASIC Verifiers

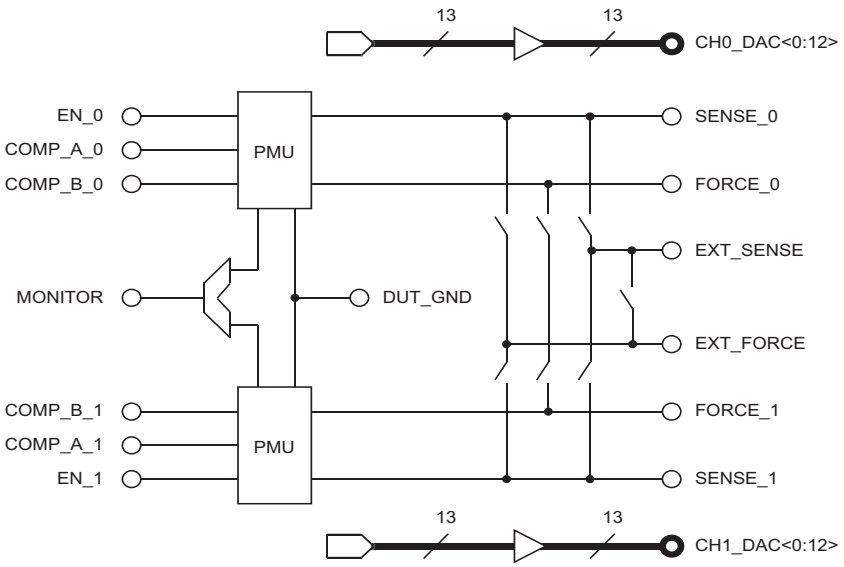


Table of Contents

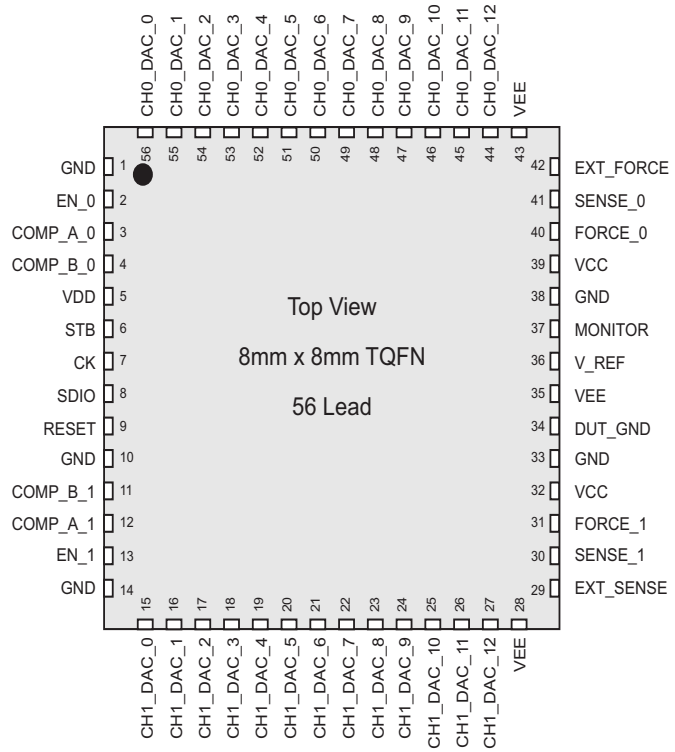
Pin Descriptions

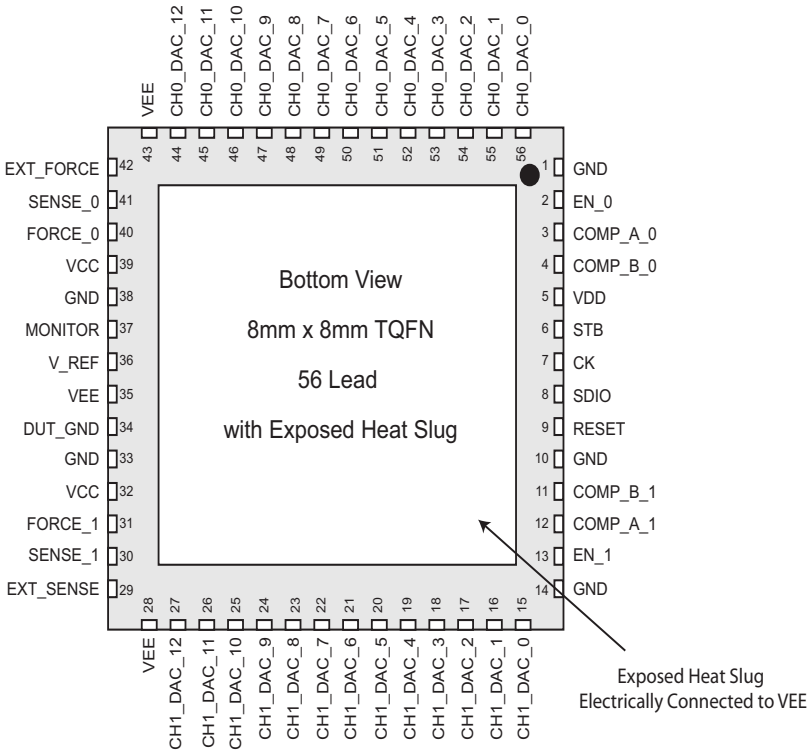
PIN #	PIN NAME	DESCRIPTION
Channel 0 Digital Pins		
2	EN_0	Channel 0 driver real time enable input.
3, 4	COMP_A_0, COMP_B_0	Channel 0 real time comparator outputs, real time monitor control inputs.
Channel 1 Digital Pins		
13	EN_1	Channel 1 driver real time enable input.
12, 11	COMP_A_1, COMP_B_1	Channel 1 real time comparator outputs, real time monitor control inputs.
Channel 0 Analog Pins		
40	FORCE_0	Channel 0 PMU output force pin.
41	SENSE_0	Channel 0 PMU output sense pin.
56	CH0_DAC_0	Channel 0 DAC 0 output.
55	CH0_DAC_1	Channel 0 DAC 1 output.
54	CH0_DAC_2	Channel 0 DAC 2 output.
53	CH0_DAC_3	Channel 0 DAC 3 output.
52	CH0_DAC_4	Channel 0 DAC 4 output.
51	CH0_DAC_5	Channel 0 DAC 5 output.
50	CH0_DAC_6	Channel 0 DAC 6 output.
49	CH0_DAC_7	Channel 0 DAC 7 output.
48	CH0_DAC_8	Channel 0 DAC 8 output.
47	CH0_DAC_9	Channel 0 DAC 9 output.
46	CH0_DAC_10	Channel 0 DAC 10 output.
45	CH0_DAC_11	Channel 0 DAC 11 output.
44	CH0_DAC_12	Channel 0 DAC 12 output.
Channel 1 Analog Pins		
31	FORCE_1	Channel 1 PMU output force pin.
30	SENSE_1	Channel 1 PMU output sense pin.
15	CH1_DAC_0	Channel 1 DAC 0 output.
16	CH1_DAC_1	Channel 1 DAC 1 output.
17	CH1_DAC_2	Channel 1 DAC 2 output.
18	CH1_DAC_3	Channel 1 DAC 3 output.
19	CH1_DAC_4	Channel 1 DAC 4 output.
20	CH1_DAC_5	Channel 1 DAC 5 output.
21	CH1_DAC_6	Channel 1 DAC 6 output.
22	CH1_DAC_7	Channel 1 DAC 7 output.
23	CH1_DAC_8	Channel 1 DAC 8 output.
24	CH1_DAC_9	Channel 1 DAC 9 output.
25	CH1_DAC_10	Channel 1 DAC 10 output.
26	CH1_DAC_11	Channel 1 DAC 11 output.
27	CH1_DAC_12	Channel 1 DAC 12 output.

Pin Descriptions (Continued)

PIN #	PIN NAME	DESCRIPTION
Analog Pins Per Chip		
34	DUT_GND	Analog voltage used to track GND at the DUT
36	V_REF	External precision voltage reference.
37	MONITOR	Analog voltage output of the PPMU.
42, 29	EXT-FORCE, EXT_SENSE	External PMU connections pins
CPU Interface		
7, 8, 6	CK, SDIO, STB	3-bit serial port (clock, data, strobe).
9	RESET	Chip reset.
Power Supplies		
32, 39	VCC	Analog positive power supply.
28, 35, 43	VEE	Analog negative voltage supply.
5	VDD	Digital power supply.
1, 10, 14, 33, 38	GND	Digital ground.

Pin Configuration





Absolute Maximum Ratings

Parameter	Min	Typ	Max	Units
Power Supplies				
VCC	VDD – 0.5		+32	V
VEE	–22		+0.5	V
VDD	+0.5		+5	V
VCC – VEE	0		+34	V
Analog Input/Output Voltages				
EXT_SENSE	VEE – 0.9		VCC + 0.9	V
EXT_FORCE	VEE – 0.9		VCC + 0.9	V
Digital Pins				
SDIO Output Current	–20		+20	mA
Digital Input Voltage Range	GND – 0.5		VDD + 0.5	V
External References				
V_REF	GND – 0.5		VDD + 0.5	V
Thermal Information				
Typical Thermal Resistance θJA (Note 1)		22.5		°C/W
Typical Thermal Resistance θJC (Note 2)		0.57		°C/W
Junction Temperature	55		150	°C

CAUTION: Do not operate at or near the maximum ratings listed for extended periods of time. Exposure to such conditions may adversely impact product reliability and result in failures not covered by warranty.

NOTES:

1. θJA is measured with the component mounted on a high effective thermal conductivity test board in free air.
2. For θJC, the “case temp” location is taken at the package top center.

Recommended Operating Conditions

Parameter	Min	Typ	Max	Units
Power Supplies				
VCC	+8		+13	V
VEE	–7		–3	V
VDD	+3.25		+3.5	V
GND		0		V
VCC – VEE		+16		V
Digital Inputs/Outputs				
CK, SDIO, STB, RESET	GND		VDD	V
Threshold Levels				
CVA_PPMU, CVB-PPMU	VEE + 2		VCC – 2	V
V-Cl-Lo	VEE + 1		VCC – 3	V
V-Cl-Hi	VEE + 3		VCC – 1	V
V-Cl-Hi – V-Cl-Lo		1		V
SENSE (w/voltage clamps active)	VCL + 0.1		VCH – 0.1	V
MI (w/current clamps active)	0.1 •ICL		0.9 • ICH	mA
PPMU Levels				
V-FV	VEE + 1		VCC – 1	V
V-FI	–1		+1	V
I-Cl-Hi, I-Cl-Lo	–1.5		+3	V
DAC Outputs				
Current Output Voltage Compliance	–2		+3.3	V
Voltage Output Operating Range	VEE + 1		VCC – 1	V
External References				
V_REF	+2.99		+3.01	V
EXT_SENSE	VEE		VCC	V
EXT_FORCE	VEE		VCC	V
Miscellaneous				
Junction Temperature	+25		85	°C
CPU Port CK Frequency	10		0	MHz
Capacitive Load at DOUT_#		1		nF
Capacitive Load				
IR7		400		nF
IR6		100		nF
IR5		40		nF
IR4		10		nF
IR3		4		nF
IR2		2		nF
IR1		1		nF
IR0		1		nF

DC Characteristics

For all of the following DC Electrical Specifications, compliance to datasheet limits is assured by one or more methods: production test, characterization and/or design.

DC Electrical Specifications – Power Supplies

VCC = +11.5V, VEE = –5.5V, VDD = +3.5V, V_REF = +3V, DUT_GND = 0V

SPEC #	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS	Pd (TYP)
Quiescent – No Load							**2.2W/Chip**
11100	VCC	Iout = 0mA, V_FV = 1.5V	20	33	45	mA	638mW
11200	VEE	Iout = 0mA, V_FV = 1.5V	20	35	50	mA	290mW
11300	VDD	Iout = 0mA, V_FV = 1.5V	20	33	45	mA	155mW
Quiescent – 32mA Load/Channel; 64mA/Chip							**1.1W/Chip**
11110	VCC	Iout = 64mA (gang mode); V_FV = 5.0V	70	96	110	mA	1,320mW
11210	VEE	Iout = 64mA (gang mode); V_FV = 5.0V	20	35	50	mA	290mW
11310	VDD	Iout = 64mA (gang mode); V_FV = 5.0V	20	33	50	mA	155mW

DC Electrical Specifications – CPU Port

VCC = +11V, VEE = –5V, VDD = +3.3V, V_REF = 3.0V, DUT_GND = 0V.

SPEC #	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
SDIO, CK, STB, RESET						
17100	VIH		2.0			V
17110	VIL				0.8	V
17120	Iin Input Leakage Current	Tested at 0V and VDD	–100	0	+100	nA
17200	VOH (SDIO Only)	Output Current = 8mA	2.4			V
17210	VOL (SDIO Only)	Input Current = 8mA			0.8	V

DC Electrical Specifications – Comparator Inputs/Outputs

VCC = +11V, VEE = –5V, VDD = +3.3V, V_REF = 3.0V, DUT_GND = 0V

SPEC #	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Comparator Outputs (COMP_A, COMP_B)						
13361	VOH Output Impedance		30	50	70	Ω
13360	VOL Output Impedance		30	50	70	Ω
Comparator Outputs when Used as Inputs (COMP_A_#, COMP_B_#)						
13250	VIH		2.0			V
13250	VIL				0.8	V
13252	Iin (Input Leakage Current) (HiZ)	Tested at 0V and VDD	–100	0	+100	nA
Enable Inputs (EN_0, EN_1)						
13260	VIH		2.0			V
13261	VIL				0.8	V
13262	Iin (Input Leakage Current) (HiZ)	Tested at 0V and VDD	–100	0	+100	nA

DC Electrical Specifications – Analog Pins

VCC = +11V, VEE = –5V, VDD = +3.3V, V_REF = 3.0V, DUT_GND = 0V

SPEC #	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
10999	V_REF Input Current	Tested at 0V and VDD	–1	0	+1	µA
10998	DUT_GND Input Current	Tested at 0V	–10	0	+10	nA
14090	FORCE, SENSE HiZ Leakage	Tested at 0V	–5	0	+5	nA
14091	FORCE, SENSE HiZ Leakage	Tested at VCC and VEE	–10	0	+10	nA
10997	EXT_FORCE, EXT_SENSE HiZ Leakage	Tested at 0V	–5	0	+5	nA
10996	EXT_FORCE, EXT_SENSE HiZ leakage	Tested at VCC and VEE	–10	0	+10	nA

DC Electrical Specifications – DAC

There are 3 on-chip internal DACs per channel used for: DC Level, DC Level Offset Correction, and DC Level Gain Correction. DAC testing is performed post-DAC calibration using a 4-segment calibration algorithm for the gain and offset DAC and only a 2-point calibration for the level DAC.

These on-chip DACs are not used off-chip explicitly as stand-alone outputs. Rather, they are internal resources that are used by every functional block. The DACs are tested many times over by the DC tests for driver, comparator and PMU. However, the DACs are specifically tested independently from all other functional blocks to verify basic functionality.

VCC = +10.75V, VEE = –4.75V, VDD = +3.15V, V_REF = 3.0V, DUT_GND = 0V.

SPEC #	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Level DAC Test						
16100	Span	Notes 1, 2 and 4	7.6	8.0	8.4	V
16110	Linearity	Notes 1, 2 and 3	–6	0	+6	mV
16120	Bit Test	Notes 1, 2 and 5	–6	0	+6	mV
16140	DAC Noise Test	FV = 0V, VR2, Measured at FORCE_0/1, RMS			1	mV
16190	Level Droop Test	Note 6			100	µV/ms
16191	Level Droop Test	Note 7			600	µV/ms
Offset DAC Test						
16200	+Adjustment Range	Notes 1, 8 and 9	+4.5	+5.2	+6.0	% of Span
16210	–Adjustment Range	Notes 1, 8 and 9	–6.0	–5.2	–4.5	% of Span
16220	Linearity	Notes 1, 3 and 8	–6	0	+6	mV
16230	Bit Test	Notes 1, 6 and 8	–6	0	+6	mV
Gain DAC Test						
16300	+Adjustment Range	Notes 1 and 10	1.07	1.10	1.15	V/V
16310	–Adjustment Range	Notes 1 and 10	0.850	0.886	0.922	V/V
16320	Linearity	Notes 1, 3 and 10	–6	0	+6	mV/V
16330	Bit Test	Notes 1, 5 and 10	–6	0	+6	mV/V

DC Electrical Specifications – DAC

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VCC = +10.75V, VEE = –4.75V, VDD = +3.15V, V_REF = 3.0V, DUT_GND = 0V.

SPEC #	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS

NOTES:

1. DAC tests performed using the PMU in FV mode and the MONITOR output VR1
2. Offset and Gain DACs both programmed to mid-scale (Code 7FFF)
3. Linearity Test: 17 equal spaced codes relative to a straight line determined by 3/17 and 15/17 measurement points: 0000, 0FFF, **1FFF**, 2FFF, 3FFF, 4FFFF, 5FFFF, 6FFFF, 7FFFF, 8FFFF, AFFFF, BFFFF. CFFF, **DFFF**, EFFF, FFFF
4. Span = DAC(FFFF) - DAC (0000)
5. Bit Test - Walking 1 and walking 0 to determine bit weight:
   1's: 8000, 4000, 2000, 100, 0800, 0400, 0200, 0100, 0080, 0040, 0020, 0010, 0008, 0004, 0002, 0001;
   0's: 7FFF, BFFF, DFFF, EFFF, F7FF, FBFF, FDFF, FEFF, FF7F, FFF, FFDF, FFEF, FFF7, FFFB, FFFD, FFFE
6. CPU CK turned off. 216ms delay between measurements. V-FV, V-FI, CVA-PPMU and CVB-PPMU tested one at a time.
7. CPU CK turned off. 216ms delay between measurements. V-CI-Lo, V-CI-Hi, I-CI-Lo, I-CI-Hi and CH#_DAC_<0-12> tested one at a time.
8. Level and gain DACs both programmed to mid-scale (Code 7FFF).
9. Code 0000, FFFF relative to mid-scale (7FFF).
10. Level at full scale (FFFF) and Offset DAC programmed to mid-scale (Code 7FFF).

DC Electrical Specifications– Force Voltage

The sequence of events performed for FV Testing is:

1. Program FV
2. Force current at FORCE
3. Measure the voltage at FORCE

FV Tests:

1. VR0 tested in IR5
2. VR1 tested in IR5
3. VR2 tested in all current ranges.
4. Vmid = 1011

VCC = +10.75V, VEE = –4.75V, VDD = +3.15V, V_REF = 3.0V, DUT_GND = 0V.

SPEC #	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
FV (Post Calibration)						
14200	Output Force Error	Note 11	–5		+5	mV
14201	Output Force Error	Note 12	–10		+10	mV
14202	Output Force Error	Note 13	–15		+15	mV

NOTES:

11. VR0, IR5: Cal Points = 0V/0µA and +3V/0µA; FV Test Points = –0.5V/0µA, +1.5V/0µA and +3.5V/µA.
12. VR1, IR5: Cal Points = 0V/0µA and +5V/0µA; FV Test Points = –1V/0µA, +4V/0µA and +7V/µA.
13. VR2, IR6 & IR7: Cal Points = 0V/0µA and +8V/0µA; FV Test Points = –2V/0µA, +6V/0µA and +9V/µA; VR2, IR0 - 7: 0V/0µA and +8V/0µA; FV Test Points = –1V/0µA, and +7V/µA.

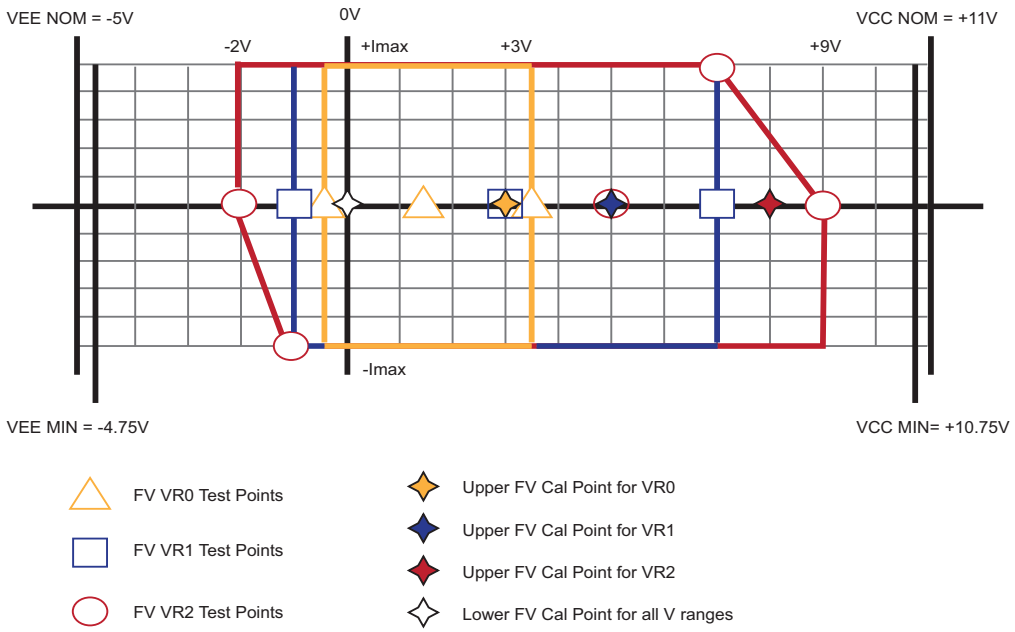


FIGURE 1.

DC Electrical Specifications – Force Current

VCC = +10.75V, VEE = –4.75V, VDD = +3.15V, V_REF = 3.0V, DUT_GND = 0V.

The sequence of events performed for FI Testing is:

1. Program FI to the desired current
2. Force voltage with external PMU at FORCE
3. Measure the current at FORCE

SPEC #	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
14800	Force Current Error	IR0, Note 14	–7.5		+7.5	nA
14810	Force Current Error	IR0, Note 15	–10		+10	nA
14801	Force Current Error	IR1, Note 14	–40		+40	nA
14811	Force Current Error	IR1, Note 15	–40		+40	nA
14802	Force Current Error	IR2, Note 14	–120		+120	nA
14812	Force Current Error	IR2, Note 15	–160		+160	nA
14803	Force Current Error	IR3, Note 14	–480		+480	nA
14813	Force Current Error	IR3, Note 15	–640		+640	nA
14804	Force Current Error	IR4, Note 14	–1.92		+1.92	µA
14814	Force Current Error	IR4, Note 15	–2.56		+2.56	µA
14805	Force Current Error	IR5, Note 14	–7.5		+7.5	µA
14815	Force Current Error	IR5, Note 15	–10		+10	µA
14806	Force Current Error	IR6, Note14	–30		+30	µA
14816	Force Current Error	IR6, Note 15	–40		+40	µA
14807	Force Current Error	IR7, Note 16	–120		+120	µA
14817	Force Current Error	IR7, Note 14	–160		+160	µA

NOTES:

14. FI Test Points: –2V/0µA, +8V/0µA, –1V/–Imax, +7V/+Imax, Cal Points +3V/+0.8 • Imax, +3V/–0.8 • Imax.
15. FI Test Points: +9V/0µA; Cal Points: +3V/+0.8 • Imax, +3V/–0.8 • Imax.
16. FI Test Points: –2V/0µA, +8V/0µA, 0V/–Imax, +7V/+Imax, Cal Points +3V/+0.8 • Imax, +3V/–0.8 • Imax.

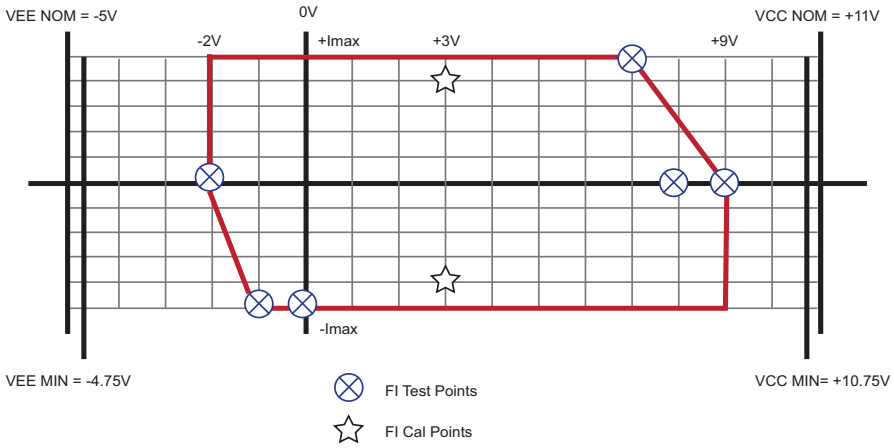


FIGURE 2.

DC Electrical Specifications – Measure Current

VCC = +10.75V, VEE = –4.75V, VDD = +3.15V, V_REF = 3.0V, DUT_GND = 0V. MI tested in VR2, IR0 –IR7. MI tested post 2-point software calibration.

SPEC #	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
MI (Post Calibration)						
14100	Measure Current Error	IR0, Note 17	–7.5		+7.5	nA
14110	Measure Current Error	IR0, Note 18	–10		+10	nA
14101	Measure Current Error	IR1, Note 17	–30		+30	nA
14111	Measure Current Error	IR1, Note 18	–40		+40	nA
14102	Measure Current Error	IR2, Note 17	–120		+120	nA
14112	Measure Current Error	IR2, Note 18	–160		+160	nA
14103	Measure Current Error	IR3, Note 17	–480		+480	nA
14113	Measure Current Error	IR3, Note 18	–640		+640	nA
14104	Measure Current Error	IR4, Note 17	–1.92		+1.92	µA
14114	Measure Current Error	IR4, Note 18	–2.56		+2.56	µA
14105	Measure Current Error	IR5, Note 17	–7.5		+7.5	µA
14115	Measure Current Error	IR5, Note 18	–10		+10	µA
14106	Measure Current Error	IR6, Note 17	–30		+30	µA
14116	Measure Current Error	IR6, Note 18	–40		+40	µA
14107	Measure Current Error	IR7, Note19	–120		+120	µA
14117	Measure Current Error	IR7, Note 18	–160		+160	µA
CMRR						
14140	Maximum CMRR Adj	FV Mode, VR1, Iout = 0 (PMU Switch Open), IR5, FORCE = -1V, +7V, Max Code	1.0005			%/V
14141	Minimum CMRR Adj	FV Mode, VR1, Iout = 0 (PMU Switch Open), IR5, FORCE = -1V, +7V, Min Code			0.9995	%/V

NOTES:

17. MI Test Points: –2V/0µA, +8V/0µA, –1V/–Imax, +7V/+Imax, Cal Points +3V/+0.8 • Imax, +3V/–0.8 • Imax
18. MI Test Points: +9V/0µA; Cal Points: +3V/+0.8 • Imax, +3V/–0.8 • Imax
19. MI Test Points: –2V/0µA, +8V/0µA, 0V/–Imax, +7V/+Imax, Cal Points +3V/+0.8 • Imax, +3V/–0.8 • Imax

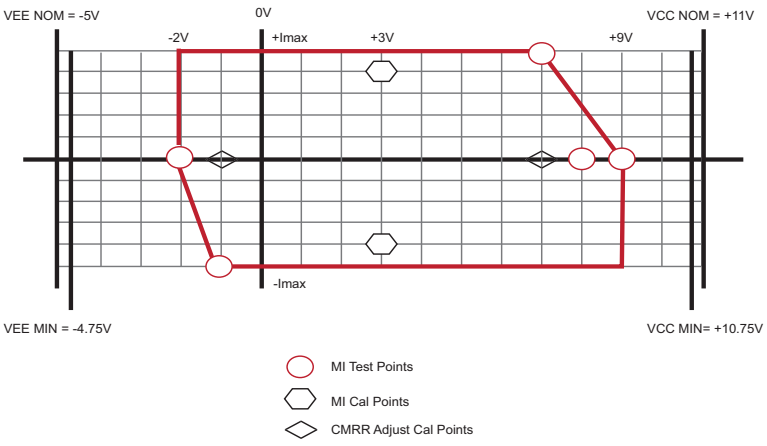


FIGURE 3.

DC Electrical Specifications – CMRR

VCC = +10.75V, VEE = –4.75V, VDD = +3.15V, V_REF = 3.0V, DUT_GND = 0V. FV Mode, VR2, Iout = 0 (open switch), tight loop, measure MI @ MONITOR, test @ +1V and +9V.

SPEC #	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
14203	Uncalibrated CMRR, IR0	IR0	–4		+4	nA/V
14213	Uncalibrated CMRR, IR1	IR1	–16		+16	nA/V
14223	Uncalibrated CMRR, IR2	IR2	–64		+64	nA/V
14233	Uncalibrated CMRR, IR3	IR3	–256		+256	nA/V
14243	Uncalibrated CMRR, IR4	IR4	–1024		+1024	nA/V
14253	Uncalibrated CMRR, IR5	IR5	–4		+4	µA/V
14263	Uncalibrated CMRR, IR6	IR6	–16		+16	µA/V
14273	Uncalibrated CMRR, IR7	IR7	–64		+64	µA/V

DC Electrical Specifications – Measure Voltage (Monitor)

The sequence of events performed for the MONITOR is:

1. Program FV to the desired voltage (in VR2, IR5, Iload = 0)
2. Measure the voltage at FORCE
3. Measure the voltage at MONITOR
4. Calculate the difference to determine the error

SPEC #	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
14710	HiZ Leakage Current	Note 21; Tested at MONITOR= 0V, VCC, VEE	–10	0	+10	nA
14700	Output Impedance	Note 21; Tested at +3V, Iout = 0µA, 500µA	.4	0.7	1.2	kΩ
14720	Voltage Error	Note 20	–5		+5	mV
14730	MONITOR GND Buffer Error	Note 20; DUT_GND = ±300mV, Mon-GND-OE = 1, measured @ EXT_SENSE relative to GND, Post Cal	–5		+5	mV
14740	MONITOR GND Buffer Output Impedance	Note 21; Tested at +3V, Iout = 0µA, 500µA	3	6	8	kΩ
14741	DUT_GND Error	Note 20; DUT_GND = ±300mV, FV Mode, V-FV = +3V, measured @ FORCE relative to GND	–5		+5	mV

NOTES:

20. VCC_SV = +10.5V, VEE = –4.75V, VDD = 3.15V, V_REF = 3.0V, DUT_GND = 0V.
21. VCC_SV = +11V, VEE = –5V, VDD = +3.3V, VREF = 3.00V, DUT_GND = 0V.

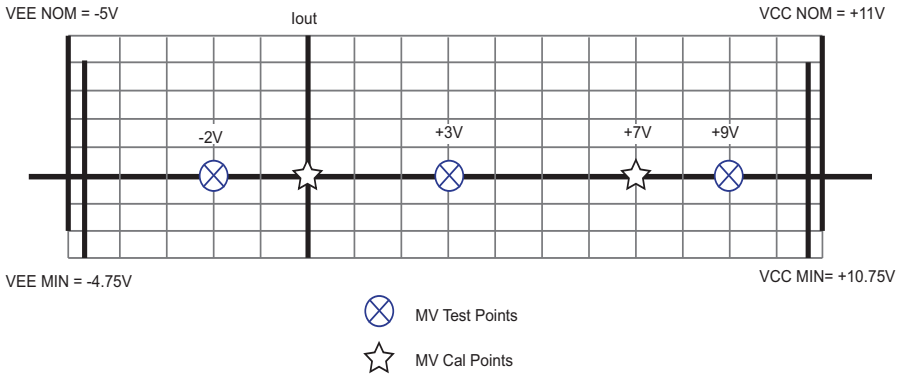


FIGURE 4.

DC Electrical Specifications – Measure Voltage (Comparator)

VCC = +10.75V, VEE = –4.75V, VDD = +3.15V, V_REF = 3.0V, DUT_GND = 0V.

SPEC #	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
14600	Threshold Error, VR0	Note 22; Cal Points 0V and +3V, Test Points –.5V, +1.5V and +3.5V	–5		+5	mV
14601	Threshold Error, VR1	Note 23; Cal Points 0V and +5V, Test Points –1V, +3V and +7V	–10		+10	mV
14602	Threshold Error, VR2	Note 24; Cal Points 0V and +7V, Test Points –1V, +6V and +9V	–25		+25	mV
14603	Threshold Error, VIR	Note 25; Cal Points –.8V and +.8V, Test Points -1V, 0V and +1V	–3.75		+3.75	mV

NOTES:

22. PMU comparator threshold test points, VR0, test the internal references via Test & Cal Mux.
23. PMU comparator threshold test points, VR1, test the internal references via Test & Cal Mux.
24. PMU comparator threshold test points, VR2, test the comparator outputs using a binary search.
25. PMU comparator threshold test points, VIR, test the internal references via Test & Cal Mux.

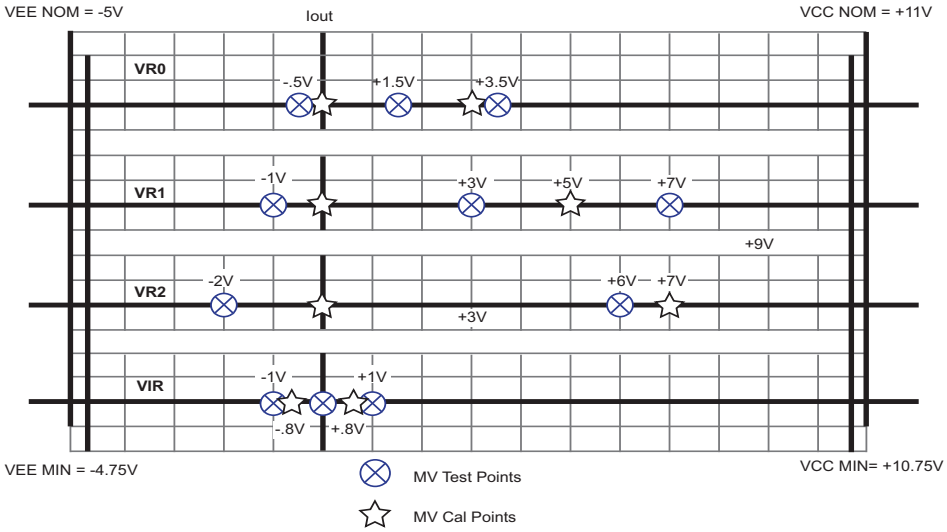


FIGURE 5.

DC Electrical Specifications – Voltage Clamp Low

VCC = +10.75V, VEE = –4.75V, VDD = +3.15V, V_REF = 3.0V, DUT_GND = 0V.

SPEC #	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
14400	Low Voltage Clamp Error, VR0	Note 26; Cal Points 0V and +2V, Test Points –0.5V, +1.5V, +2.5V	–50		+50	mV
14410	Low Voltage Clamp Error, VR1	Note 27; Cal points 0V and +5V, Test Points –1V, +3V and +5V	–50		+50	mV
14420	Low Voltage Clamp Error, VR2	Note 28; Cal points 0V and +5V, Test Points –2V, +3V and +5V	–50		+50	mV

NOTES:

26. Low voltage clamp test points, VR0.
27. Low voltage clamp test points; VR1.
28. Low voltage clamp test points; VR2.

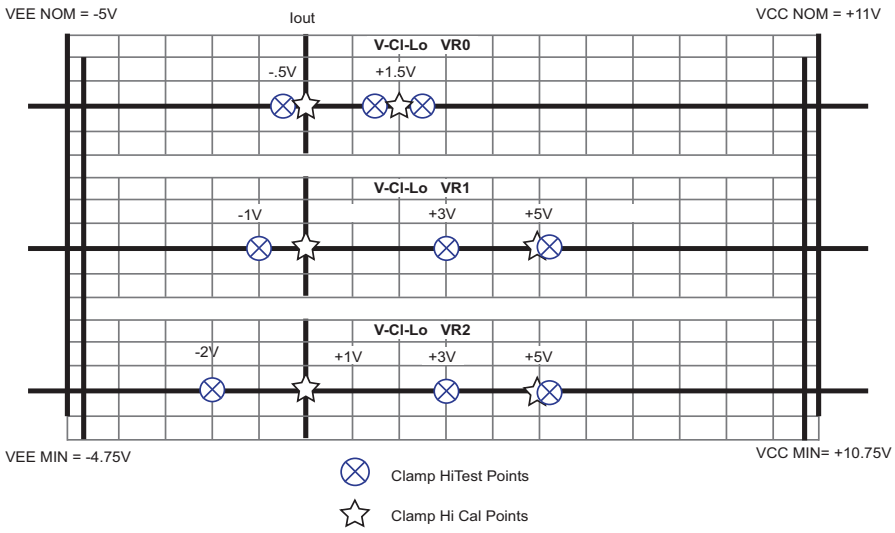


FIGURE 6.

DC Electrical Specifications – Voltage Clamp High

VCC = +10.75V, VEE = –4.75V, VDD = +3.15V, V_REF = 3.0V, DUT_GND = 0V.

SPEC #	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
14440	High Voltage Clamp Error, VR0	Note 29; Cal Points +1V and +3V; Test Points +1V, +1.5V and +3.5V	–50		+50	mV
14450	High Voltage Clamp Error, VR1	Note 30; Cal Points +1V and +5V; Test Points +1V, +3V and +7V	–50		+50	mV
14460	High Voltage Clamp Error, VR2	Note 31; Cal Points +1V and +7V; Test Points +1V, +5V and +9V	–50		+50	mV

NOTES:

29. High voltage clamp test points; VR0.
30. High voltage clamp test points; VR1.
31. High voltage clamp test points; VR2.

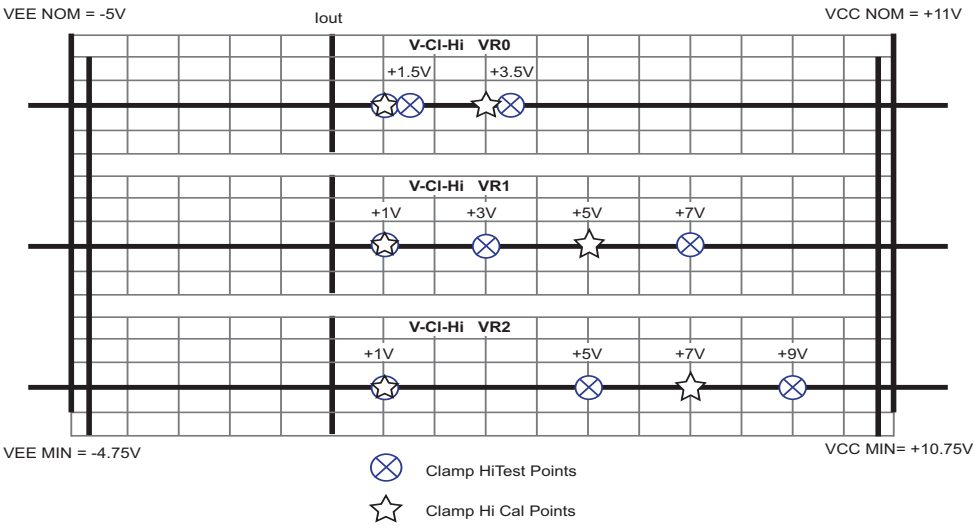


FIGURE 7.

DC Electrical Specifications – Current Clamps

Current clamps are tested in all 8 current ranges. In current ranges IR0-IR5, the clamps are tested in a non-calibrated state. IR6 and IR7 have been calibrated using the calibration points listed below. The sequence of events to test the high current clamps are:

1. Program I-Cl-Hi
2. Program FV = +3V
3. Program the tester PMU to +2V
4. Measure the current at FORCE

The sequence of events to test the low current clamps are:

1. Program I-Cl-Lo
2. Program FV = +3V
3. Program the tester PMU to +4V
4. Measure the current at FORCE.

VCC = +10.75V, VEE = –4.75V, VDD = +3.15V, V_REF = 3.0V, DUT_GND = 0V

SPEC #	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
13500	High Current Clamp	IR0-5; I-Cl-Hi = FFFF, Gain = FFFF, Offset = FFFF; not calibrated	2.5 • Imax	3 • Imax		mA
	High Current Clamp TempCo	Limits established by characterization and are not production tested.		0.1		%FS/°C
13520	Low Current Clamp	IR0-5; I-Cl-Lo = 0000, Gain = FFFF, Offset = 0000, not calibrated		–3 • Imax	–2.5 • Imax	mA
	Low current Clamp TempCo	Limits established by characterization and are not production tested.		0.1		%FS/°C
13506	High/Low Current Clamp Error	IR6 calibrated at 8mA and 16mA. Tested at 19.2mA.	–1.25		+1.25	mA
13507	High/Low Current Clamp Error	IR7 calibrated at 32mA and 64mA. Tested at 75mA.	–5		+5	mA

DC Electrical Specifications – Vmid DAC

VCC = +10.75V, VEE = –4.75V, VDD = +3.15V, V_REF = 3.0V, DUT_GND = 0V. The DAC is not recalibrated after changing the Vmid value. DAC tests performed using the PMU in FV mode and the MONITOR output.

SPEC #	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
16400	VR0 Error	Min Test Points –1.875V and +2.125V; Max Test Points 0V and +4V.	–50		+50	mV
16410	VR1 Error	Min Test Points –2V and +4.25V; Max Test Points 0V and +8V	–100		+100	mV
16420	Linearity	Note 32	–20		+20	mV

NOTE:

32. Linearity Test - 16 all codes relative to a straight line determined by 2/16 and 13/16 measurement points:

0000, 00001, 0010, 0011 ... 1100, 1101, 1110, 1111

DAC Code = 7FFF, FV Mode, VR1

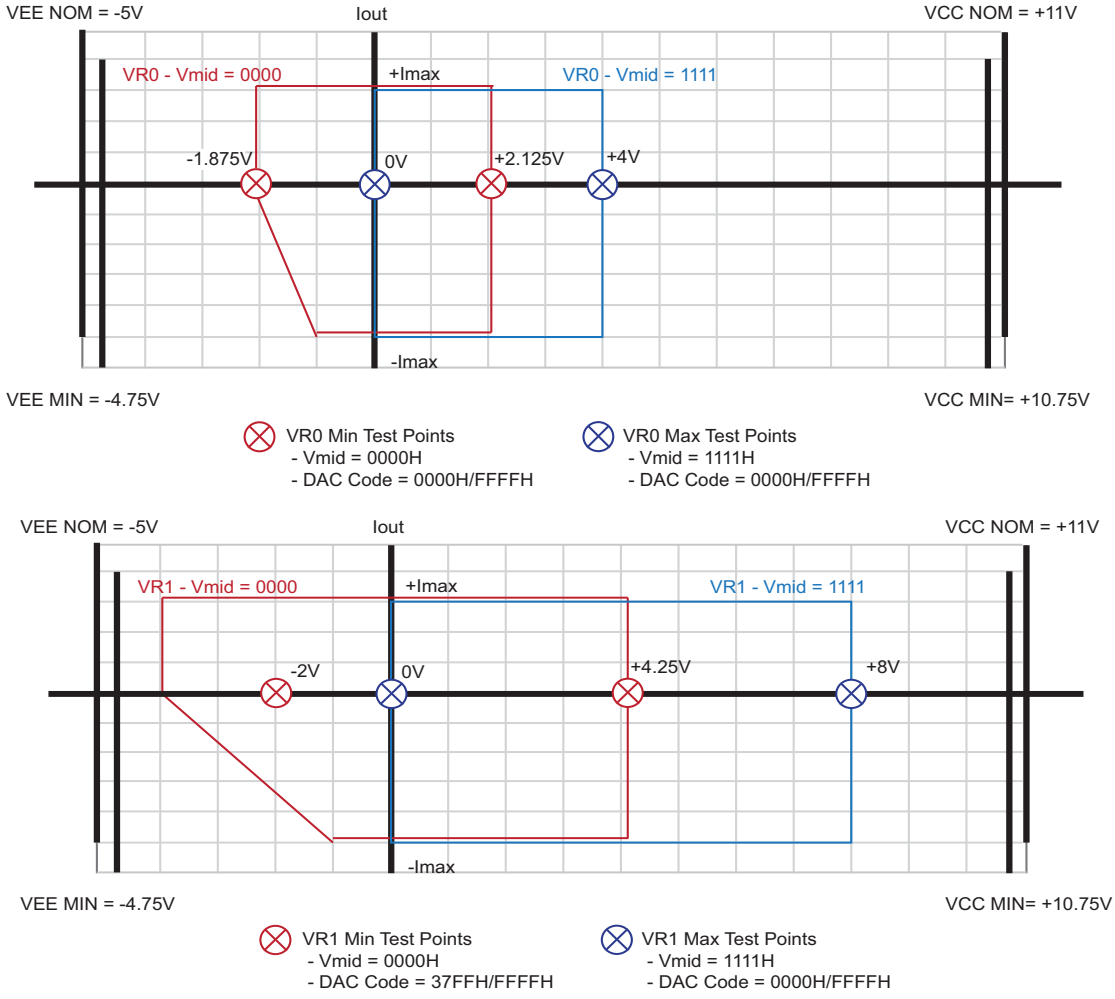


FIGURE 8.

DC Electrical Specifications – DAC Outputs

VCC = +10.75V, VEE = –4.75V, VDD = +3.15V, V_REF = 3.0V, DUT_GND = 0V.

SPEC #	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
CH#_DAC_0-12 in FV Mode						
16005	VR0	Cal Points 0V and +3V, Test Points –0.5V, +1.5V and +3.5V	–10		+10	mV
16006	VR1	Cal Points 0V and +5V, Test Points –1V, +3V and +7V	–15		+15	mV
16007	VR2	Cal Points 0V and +7V, Test Points –2V, +6V and +9V	–20		+20	mV
CH#_DAC_8-12 in FI Mode						
16008	250µA range	Cal Points 10% • Imax/+3V and 90% • Imax/+3V; Test Points 0µA/+3V, 0.5 • Imax/+3V, Imax/+3V	–2.5		+2.5	µA
16009	2.5mA range	Cal Points 10% • Imax/+3V and 90% • Imax/+3V; Test Points 0µA/+3V, 0.5 • Imax/+3V, Imax/+3V	–25		+25	µA

DC Electrical Specifications – Resistor Values

VCC = +11V, VEE = –5V, VDD = 3.15V, V_REF = 3.0V, DUT_GND = 0V.

SPEC #	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Sense Resistors						
19000	IR0			500		kΩ
19010	IR1			125		kΩ
19020	IR2			31.25		kΩ
19030	IR3			7.81		kΩ
19040	IR4			1.95		kΩ
19050	IR5			500		Ω
19060	IR6			125		Ω
19070	IR7			31.25		Ω
On-Chip FET Switches						
19130	PPMU Connect#		15	25	40	Ω
19131	Con-PPMU-F(1-#)		15	25	40	Ω
19132	Con-FS#		3	5	8	kΩ
19133	Con-ES-S#		3	5	8	kΩ
19134	Con-EF-F#		15	25	40	Ω
19135	Con-ES-F#		3	5	8	kΩ
19136	Con-EF-ES		3	5	8	kΩ
DAC Output Voltages						
16090	CH#_DAC_0 - CH#_DAC_7		150	250	400	Ω
16091	CH#_DAC_8 - CH#_DAC_10		350	550	750	Ω
16092	Ch#_DAC_11 - CH#_DAC_12		250	375	500	Ω

AC Characteristics

For all of the following AC Electrical Specifications, compliance to datasheet limits is assured by one or more methods: production test, characterization and/or design.

AC Electrical Specifications – CPU Port

SPEC #	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
	Set-Up Time					
27100	SDIO to Rising CK		10			ns
27110	STB to Rising CK		10			ns
	Hold Time					
27120	SDIO to rising CK		10			ns
27130	Rising CK to STB		10			ns
27140	CK Minimum Pulse Width High		24			ns
	CK Minimum Pulse Width Low		20			ns
27160	CK Period		50		100	ns
	Propagation Delay					
27180	Rising CK to SDIO Out				10	ns
27170	Reset Minimum Pulse Width		100			ns

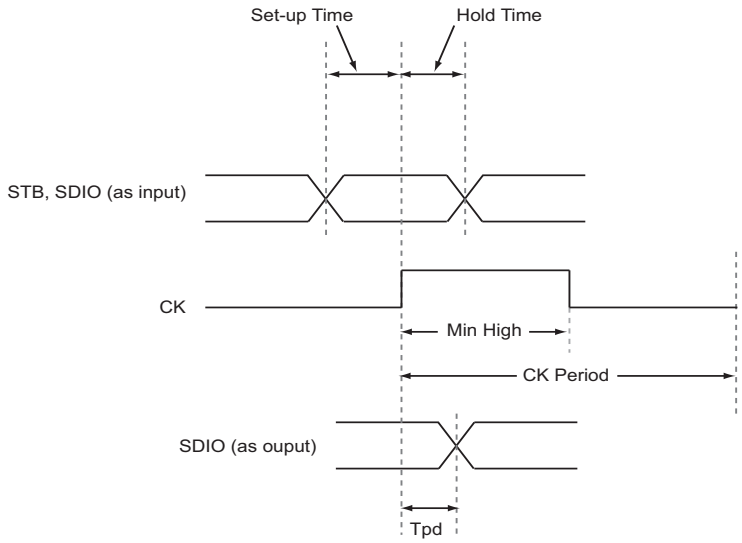


FIGURE 9.

AC Electrical Specifications – PMU

Limits established by characterization and are not production tested. VCC = +11V, VEE = –5V, VDD = 3.15V, V_REF = 3.0V, DUT_GND = 0V unless otherwise noted.

SPEC #	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
FV Settling Time						
	IR0	Note 1		400		µs
	IR1	Note 1		120		µs
	IR2	Note 1		60		µs
	IR3	Note 1		30		µs
	IR4	Note 1		20		µs
	IR5	Note 1		16		µs
	IR6	Note 1		16		µs
	IR7	Note 1		16		µs
FI Settling Time						
	IR0	Note 2		1.7		ms
	IR1	Note 2		450		µs
	IR2	Note 2		150		µs
	IR3	Note 2		120		µs
	IR4	Note 2		110		µs
	IR5	Note 2		100		µs
	IR6	Note 2		90		µs
	IR7	Note 2		80		µs
	MV Settling Time	PMU in HiZ; measured at MONITOR; IR0-IR7.		1		µs

NOTES:

1. Measured at FORCE; Iclamps enabled at 100%; VR1; 0V to +5V; Cload = 100pF within 1% of final value.
2. Measured at FORCE. Rload = Rsense; Cload = 100pF.

Chip Overview

Neptune Plus is a highly integrated System on a Chip pin electronics support solution incorporating 2 independent Channels of:

- PMU
- DC Levels for the Pin Electronics
- Resistive Load.

The interface, the control, and the I/O are digital; all analog circuitry is inside the chip. Two complete and independent channels are integrated into each chip.

For most tester applications, except for the pin electronics, no additional analog hardware is required on a per pin basis.

CPU Control

All configuration set up and the writing to and reading back of the internal registers is controlled through the 3 bit serial data CPU port. The CPU port is typically used to set up the operating conditions of each channel prior to executing a test, or to change modes during a test.

An internal register chart (Memory Map), listed later in the data sheet, lists all programmable control signals and their addresses. This chart shows how to program each internal signal.

Real Time Control

All real time control and observation is accomplished via the high speed input and output signals:

- EN_0; EN_1 (Single Ended Inputs)
- COMP_A_0; COMP_A_1 (Single Ended Outputs)
- COMP_B_1; COMP_B_1 (Single Ended Outputs).

These control lines can be used to make the PPMU function like a low speed pin electronics driver and comparator.

Analog Reference

All on-chip voltage and current levels are related to one off-chip precision reference - V_REF.

This external reference is used to provide accurate and stable analog circuit performance that does not vary over time, temperature, supply voltage, part to part, or process changes

External Signal Nomenclature

All input and output pins, when referred to in the data sheet or in any circuit diagram, use the following naming conventions:

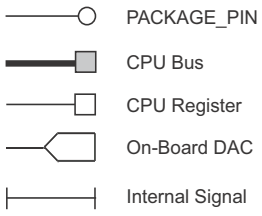
1. all capital letters (i.e., DATA_0, CK, SDIO)
2. underscores for clarity (i.e., DATA_0, COMP_B_1)
3. shown next to an I/O circle in any schematic.

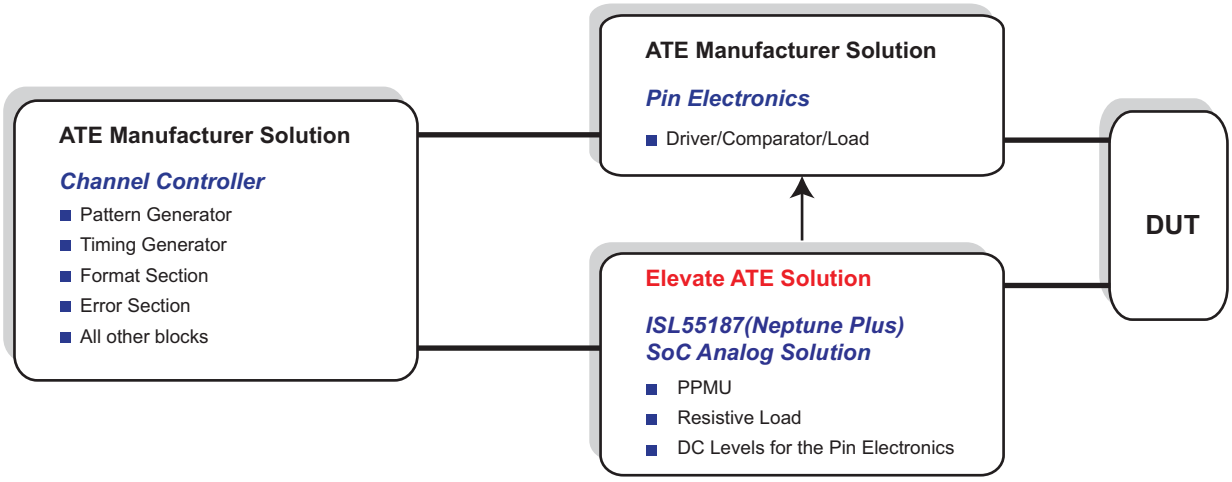
CPU Programmed Control Line Nomenclature

Any internal signal, DAC level, or control signal which is programmed via the CPU port uses a different nomenclature:

1. the first letter in a word is always a capital letter
2. subsequent letters within the same word are small
3. dashes (*but never an underscore*) for clarity
4. NOT shown with an I/O circle in any schematic.

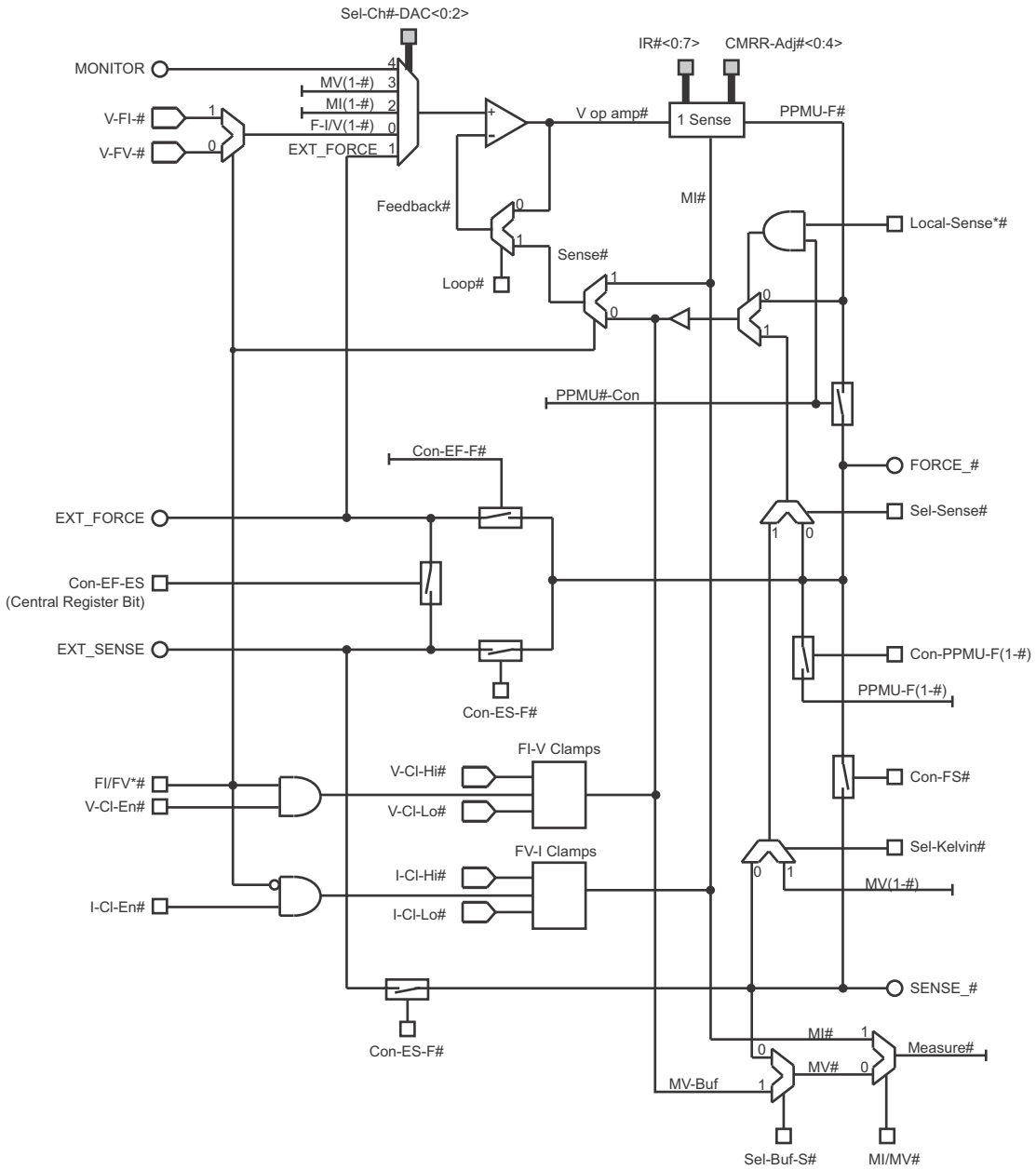
Control lines, internal registers, and other internal signals, which are programmable by the CPU port, are listed in the Memory Map table.





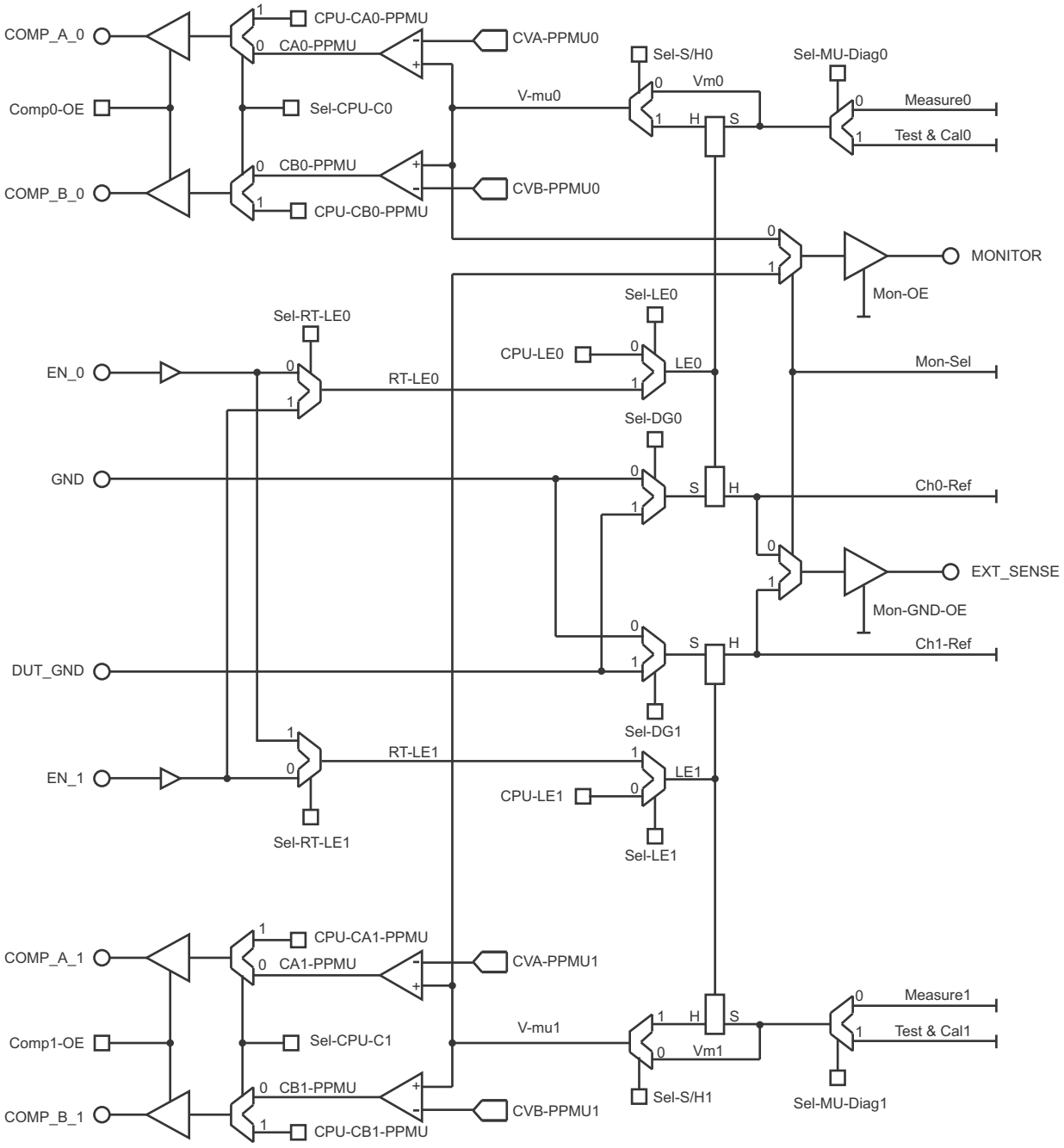
Block Diagrams

Per Channel PMU



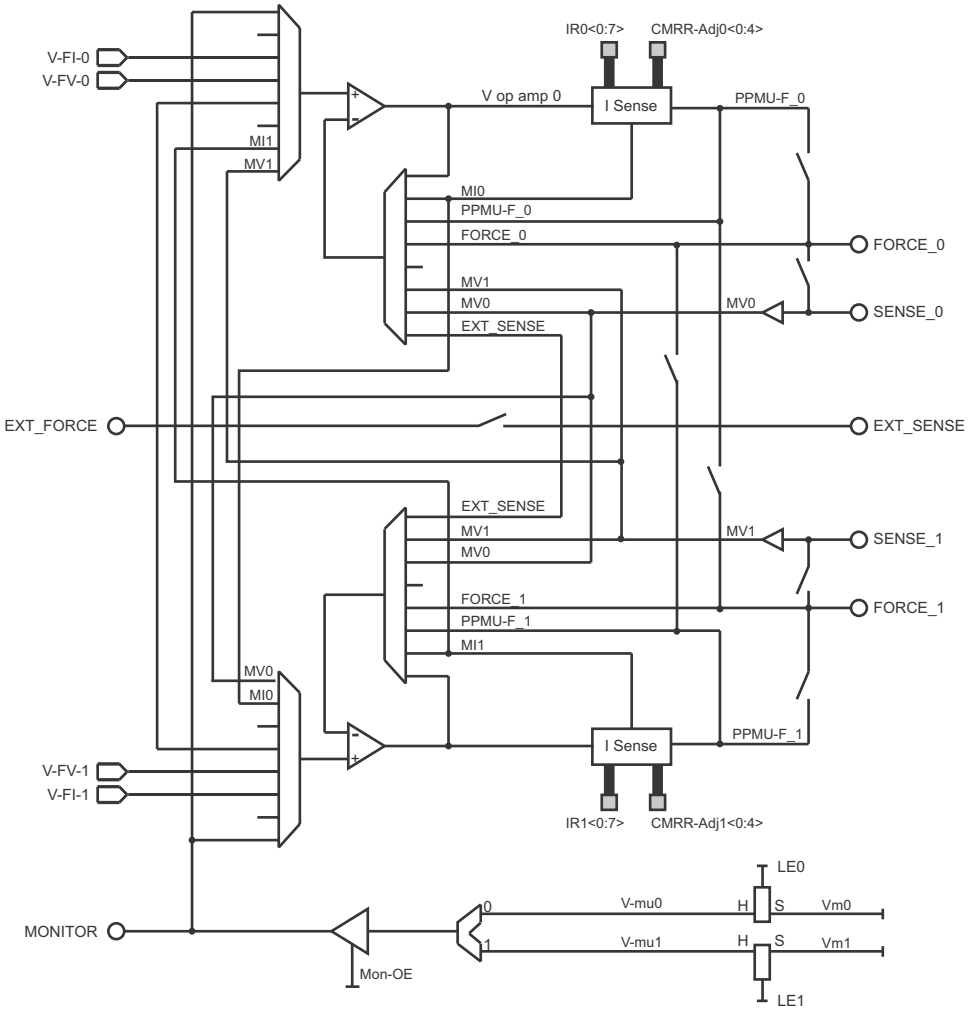
Block Diagrams (Continued)

Measurement Unit



Block Diagrams (Continued)

Force and Sense Options



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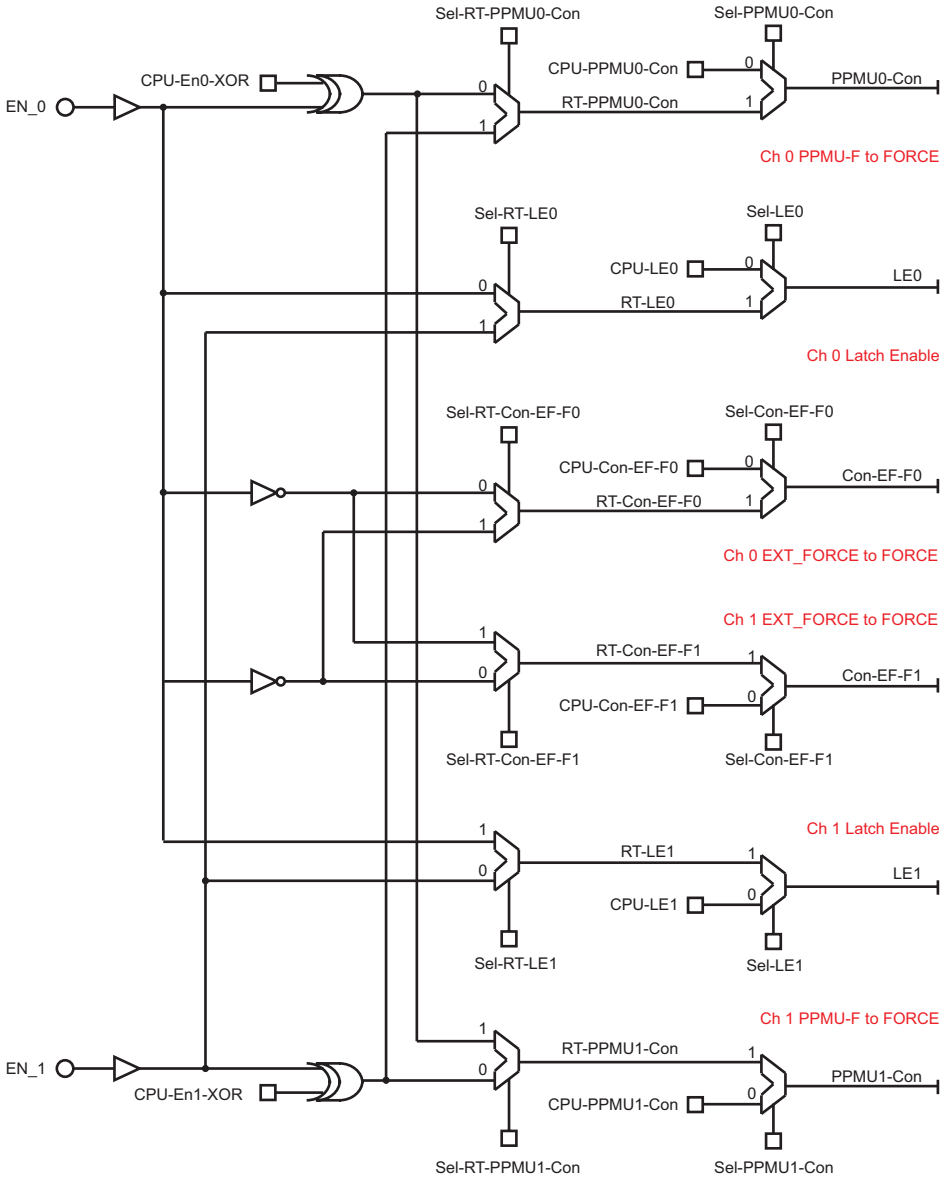
Real Time Enable Control



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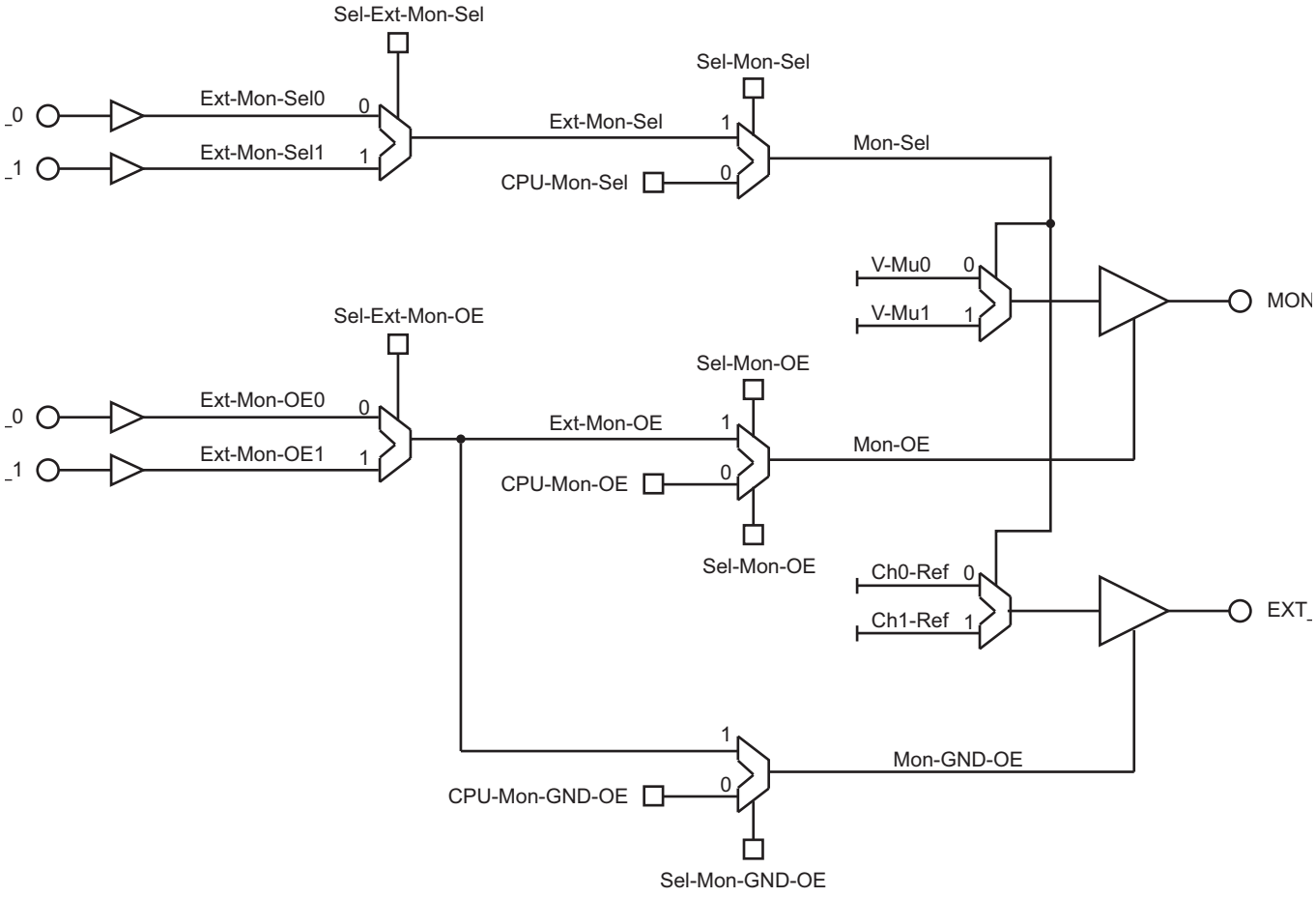
External Real Time MONITOR Control Options



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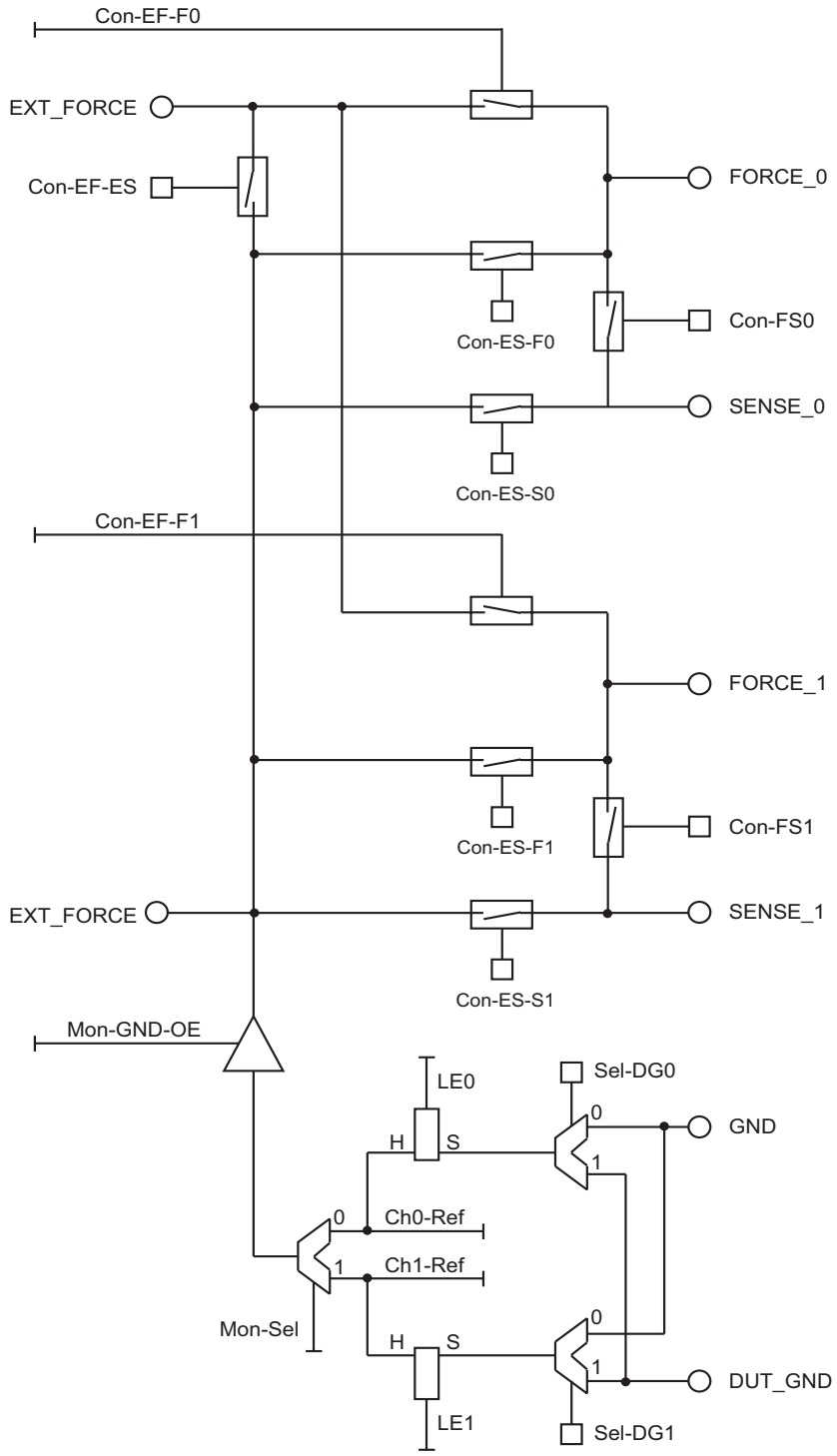
External Force/Sense Matrix



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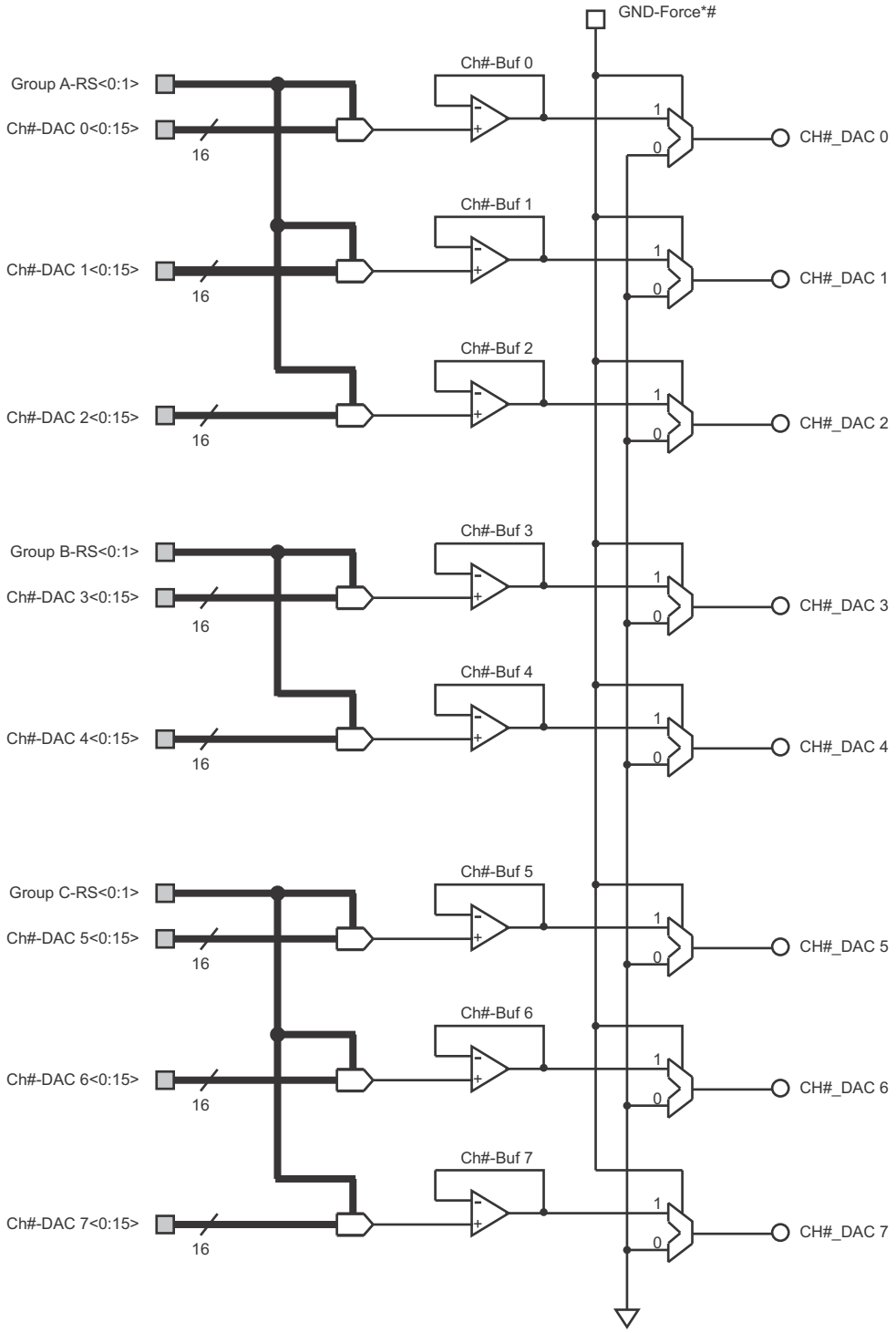
Voltage DAC Outputs



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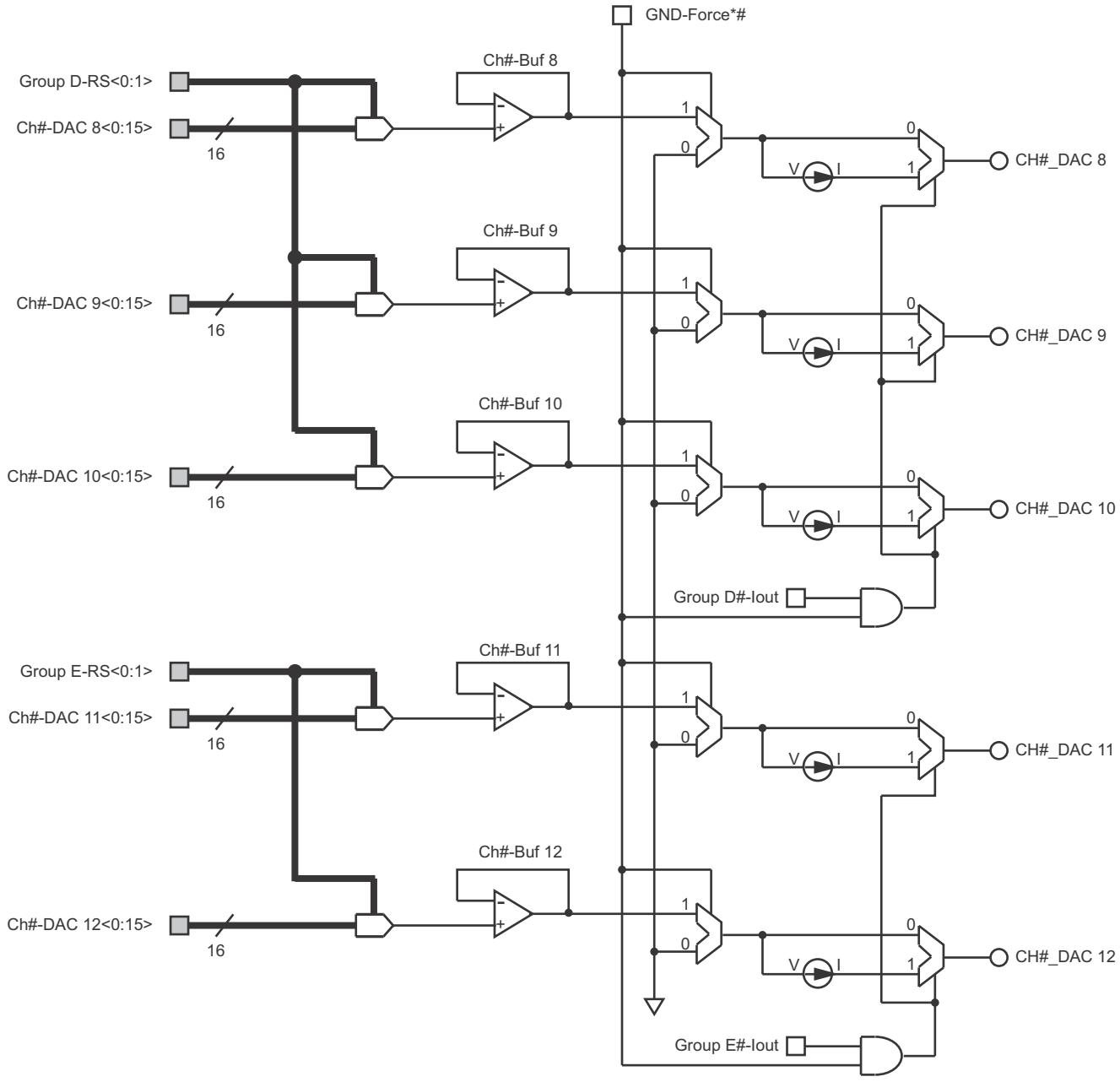
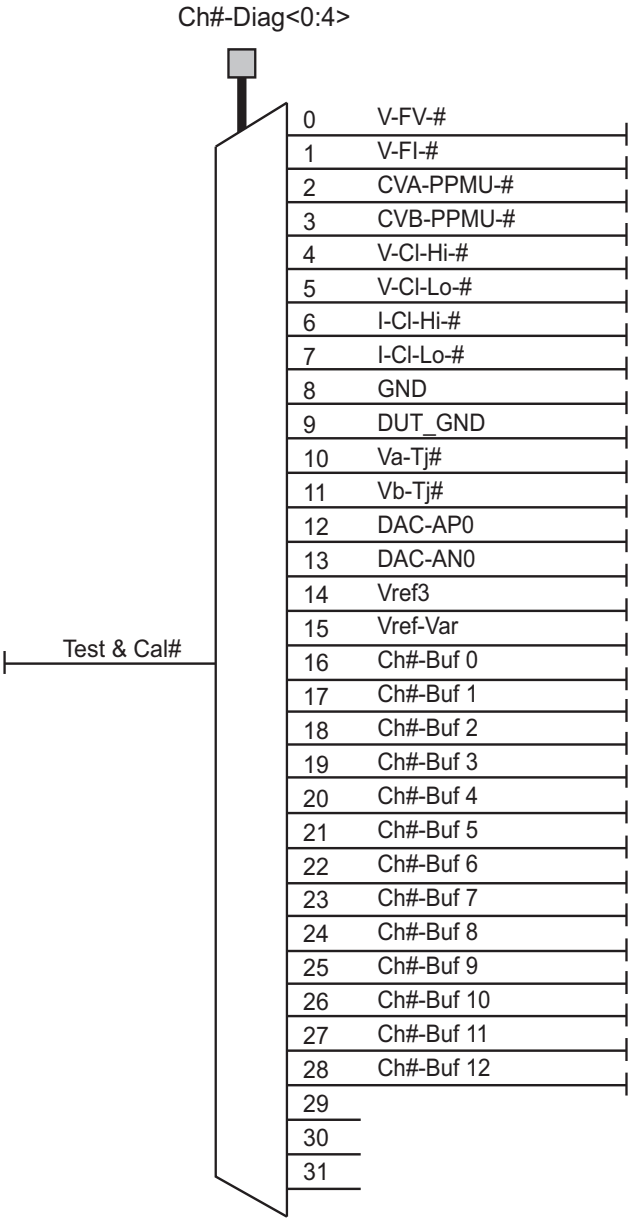
Voltage/Current DAC Outputs



Block Diagrams (Continued)

Diagnostics



PMU

Functional Block Overview

Each separate Parametric Measurement Unit (PMU) has the ability to:

- Force Voltage
- Measure Voltage
- Force Current
- Measure Current

The current or voltage measured may be tested via two paths:

- On-board PMU Dual Comparator (per channel)
- MONITOR Analog Voltage Output (per chip)

PMU High Impedance

The PMU may be placed into a high impedance state, where the FORCE output pin draws very low current between the supply levels VCC and VEE, by disconnecting the PPMU-F node from the FORCE output pin by opening the on-chip connection switch.

TABLE 1.

PPMU#-CON	CHANNEL# PPMU
0	HiZ
1	Active

Current Ranges

Each PMU can force current up to a maximum of ±32mA. In order to achieve the maximum accuracy while measuring a wide range of currents, 8 current ranges are supported.

TABLE 2.

CURRENT RANGE	IMAX	SENSE RESISTOR
IR0	±2µA	500kΩ
IR1	±8µA	125kΩ
IR2	±32µA	31.25kΩ
IR3	±128µA	7.81kΩ
IR4	±512µA	1.95kΩ
IR5	±2mA	500Ω
IR6	±8mA	125Ω
IR7	±32mA	31.25Ω

The current range is selected and controlled by the internal registers IR<0:7>, which are set through the CPU port.

Each range select bit has independent control, allowing a wide variety of make/break combinations when changing current ranges. This flexibility is useful in controlling the transient response of the PPMU over a wide variety of DUT environments.

Activating more than one range simultaneously will have the effect of placing the sense resistors in parallel, thus altering the transfer function. Activating more than one range at the same time is NOT recommended for taking measurements, but may be useful to control the transient response when changing ranges or modes.

Operating Modes

The decision whether to force current or voltage, or to measure current or voltage, is controlled by internal registers FI/FV* and MI/MV* and are programmed via the CPU port.

TABLE 3.

FI/FV*#	CH# PMU FORCE FUNCTION
0	Force Voltage
1	Force Current

MI/MV*#	CH# PMU MEASURE FUNCTION
0	Measure Voltage
1	Measure Current

There are no restrictions between what is forced and what is measured. Eight combinations are possible:

- FI/MI
- FI/MV
- FV/MI
- FV/MV
- FI Only
- FV Only
- MI Only
- MV Only

PMU Op Amp Forcing Voltage

There are several potential voltage sources that drive the PMU forcing op amp.

TABLE 4.

SEL-CH#-DAC<2:0>	CHANNEL # FORCING VOLTAGE
0	F-I/V#
1	EXT_FORCE
2	MI(1-#) (Other channel's MI)
3	MV(1-#) (Other channel's MV)
4	MONITOR
5-7	Not used

Voltage Force

In FV mode, there is a 1:1 correspondence between the voltage source and the forced voltage at FORCE.

V(FORCE_#) = V(Op Amp Forcing Voltage)

Current Force

In FI mode, the forcing voltage source has the following transfer function.

TABLE 5.

OP AMP FORCING VOLTAGE	CURRENT AT FORCE_#
–1V	–Imax
0V	0
+1V	+Imax

Measurement Unit

The measurement unit generates a voltage output (V-mu#) that corresponds to the parameter being measured. There are 4 sources of parameters for V-mu:

- Current at FORCE (MI)
- Buffered voltage at SENSE (MV)
- Unbuffered voltage at SENSE (MV)
- Internal diagnostic node (Test & Cal.)

TABLE 6.

Sel-MU-Diag#	MI/MV*#	Sel-Buf-S#	Vm#	MODE
1	X	X	Test & Cal#	Diagnostic
0	1	X	MI#	MI
0	0	0	Unbuffered V (SENSE_#)	MV
0	0	1	Buffered V (SENSE_#)	MV

Sample and Hold Capability

The selected parameter for the Vm# may be passed directly to V-mu# or it may be latched, allowing the measurement to be taken at a later time. The GND reference for Vm# is also sampled and held simultaneously. The source of the GND reference is either chip GND or DUT_GND, depending on the mode. The MONITOR ground reference is passed off the chip through the EXT_SENSE pin. In this mode, the EXT_SENSE pin must be disconnected.

TABLE 7.

Sel-S/H#	LE#	V-mu#
0	X	Vm# (Transparent)
1	0	Vm# (Transparent)
1	1	Value of Vm# on rising LE#

Sel-DG#	LE#	MONITOR REFERENCE
0	0	GND (Transparent)
0	1	Value of GND on rising LE#
1	0	DUT_GND (Transparent)
1	1	Value of DUT_GND on rising LE#

Latch Enable Sources

Each channel has an independent latch enable (LE#) signal used to control the sample and hold circuits, and may be driven by 3 sources:

1. EN_0
2. EN_1
3. CPU Port

A 2x2 cross point switch allows each channel's LE to be driven by either channel's real time EN input. In addition, the CPU port can override all real time input signals and take direct control over the LE signal.

TABLE 8.

Sel-LE#	Sel-RT-LE#	LE#
0	X	CPU-LE#
1	0	EN_#
1	1	EN(1-#)

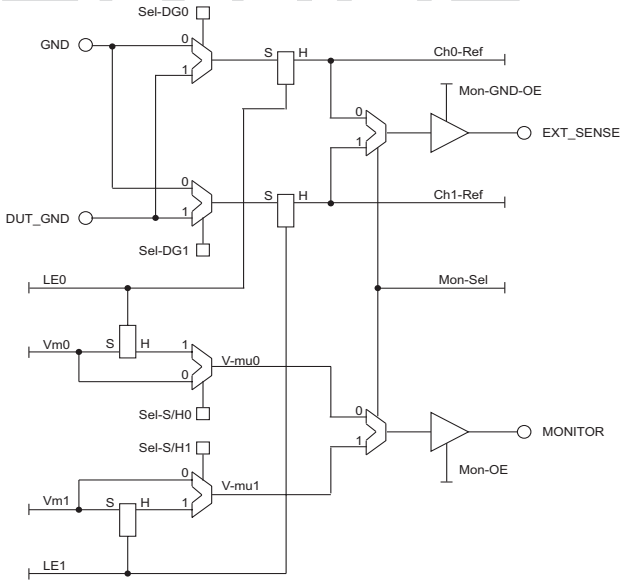


FIGURE 10.

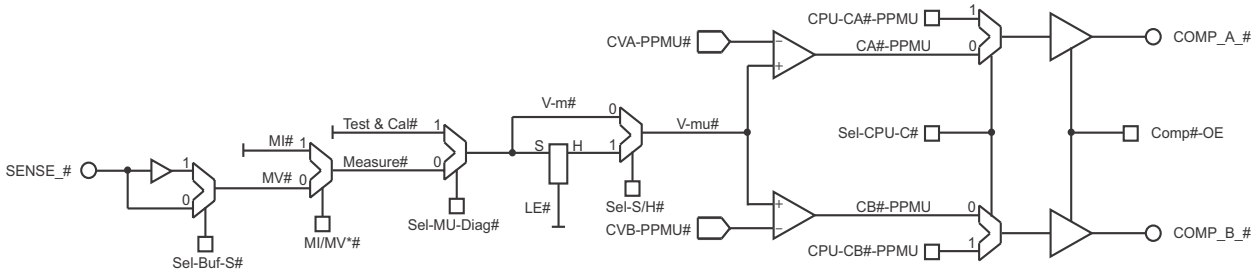


FIGURE 11.

Measurement Options

Once the V-mu source is selected, there are 2 methods to measure and test the parameter:

- Go/No-Go testing
- Analog measurement

Analog Measurement

MONITOR is an analog voltage output whose voltage source is the measurement unit output (V-mu0 or V-mu1) from either channel 0 or 1. There is 1 MONITOR per chip. The CPU port selects which channel is present at the MONITOR output.

Monitor Transfer Function

When measuring voltage, MONITOR has a 1:1 transfer function with SENSE. When measuring current, MONITOR varies between -1V and +1V for -Imax and +Imax at FORCE.

TABLE 9.

MODE	PARAMETER	MONITOR
MV	V at SENSE_#	V(SENSE_#)
MI	–Imax at FORCE_#	–1V
	0	0
	+Imax at FORCE_#	+1V

Go/No-Go Testing

An on-board window comparator allows 2 bit "Go/No-Go" testing. V-mu is the voltage output of the measurement unit, and it corresponds either to the voltage present at SENSE or to the current flowing through FORCE. V-mu is the input to the PPMU window comparator, whose references are set with on-board DC levels through the CPU port.

The comparator references are relative to DUT_GND when the PMU is in MV mode. The references are relative to chip GND when the PMU is in MI mode.

In MI mode, the comparator thresholds support 200% Imax for the limits.

TABLE 10.

CVA-PPMU-#<15:0> CVB-PPMU-#<15:0>	THRESHOLD	CURRENT LEVEL
0000 Hex	–2V	–2 * Imax
FFFF Hex	+2V	+2 * Imax

The results are routed off-chip through the output pins COMP_A and COMP_B and may be processed by the error section of the timing generator.

CPU Read Back of Internal States

The window comparator outputs CA#-PPMU and CB#-PPMU may be read back through the CPU port, granting direct access to the actual comparator states at any time.

CPU Comparator Override

The CPU may override the measurement unit and set the comparator outputs COMP_A and COMP_B directly, allowing the outputs to be placed in a known state. This feature is used typically for system diagnostic purposes.

TABLE 11.

Sel-CPU-C#	COMP_A(B)_#	CONFIGURATION
0	CA(B)#-PPMU	PPMU Control
1	CPU-CA(B)#-PPMU	CPU Control

Comparator Output Stage

Each channel supports two comparator outputs (COMP_A and COMP_B) with the following characteristics:

1. Single ended outputs
2. 50Ω series terminated outputs

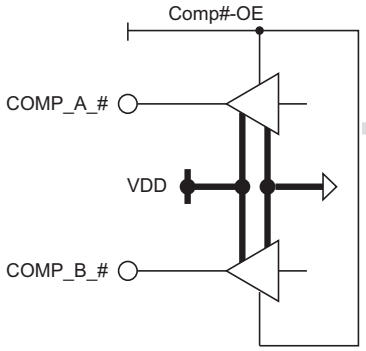


FIGURE 12.

Comparator Output Supply Levels

VDD and GND are voltage power supply inputs that set the high and low level of COMP_A and COMP_B. VDD and GND provide the current required to drive the off-chip transmission line, and any DC current associated with any termination used. Therefore, these inputs should be driven by a low impedance and low inductance source with ample current drive.

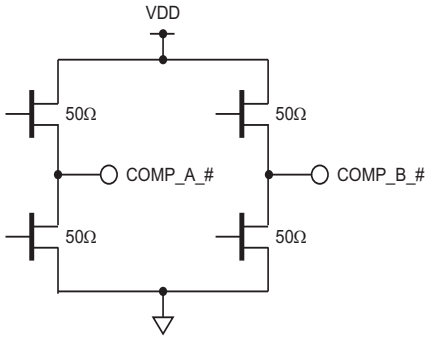


FIGURE 13.

Comparator Output HiZ

Each channel may place its COMP_A and COMP_B outputs into a HiZ state via the CPU port. This HiZ feature is useful when multiple channels are ganged together or when the comparator pins are configured as input pins. The default state upon power up and Reset is HiZ.

TABLE 12.

COMP#-OE	COMP_A_#, COMP_B_#
0	HiZ
1	Active

Comparator Source Termination

In this configuration no external components are required and a full amplitude signal is realized at the destination.

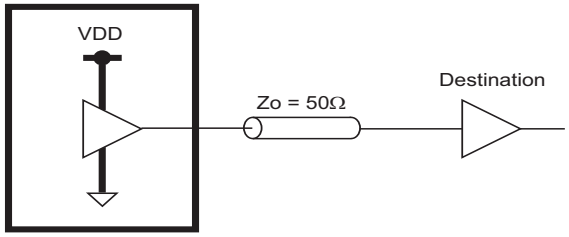


FIGURE 14.

Comparator Source and Destination Termination

In this configuration, one external component is required and a 505 amplitude signal is realized at the destination.

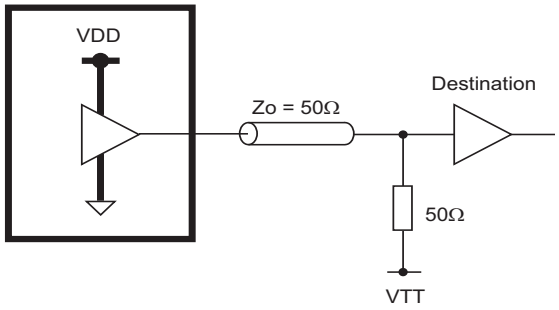


FIGURE 15.

Differential MONITOR Output

The MONITOR voltage is relative to DUT_GND when measuring voltage and relative to GND when measuring current. A differential MONITOR signal may be created by connecting MONITOR and EXT_SENSE to the two inputs of an off-chip analog to digital converter.

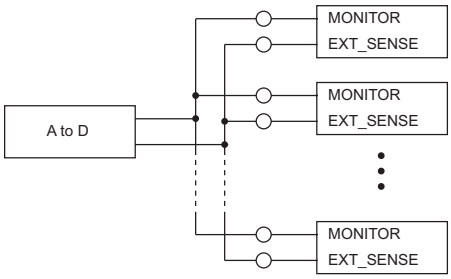


FIGURE 16.

MONITOR HiZ

MONITOR may be placed into a high impedance state by setting Mon-OE = 0. This HiZ feature is useful when connecting multiple MONITOR pins from multiple ICs to one A to D converter, without having to construct an off-chip analog multiplexer.

TABLE 13.

Mon-OE	Mon-Sel	MONITOR
0	X	HiZ
1	0	V-mu0
1	1	V-mu1

Mon-GND-En	Mon-Sel	EXT_SENSE
0	X	HiZ
1	0	Ch0-Ref
1	1	Ch1-Ref

CMRR Calibration

The current force (FI) and current measure (MI) transfer functions will have some small amount of common mode error, as the current will change slightly as the voltage at the FORCE output varies. Each channel has a correction register that can be set via the CPU port to adjust the CMRR.

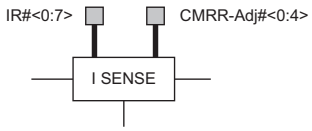


FIGURE 17.

TABLE 14.

CMRR-Adj<4> (Parity)	CMRR-Adj<3:0> (Code)	CMRR ADJUSTMENT
0	1111	1.0015
•	•	•
0	0001	1.0001
0	0000	1.0000
1	0000	1.0000
1	1111	0.9999
•	•	•
1	0001	0.9985

Resolution = 0.01%/V (of full scale current range)

The CMRR gain correction is superimposed on the nominal pre-calibration CMRR error in an effort to cancel each other out.

The default state is 00000, which results in no CMRR calibration. By setting CMRR-Adj<0:4> correctly, the actual transfer function can more closely track the ideal transfer function.

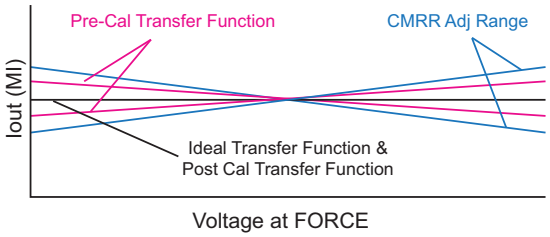


FIGURE 18.

Real Time External MONITOR Control Options

Rather than use the CPU port to select which channel drives the MONITOR output pin, external control over the MONITOR source and output enable may be realized. This external control may be useful for faster sequencing through multiple ganged MONITOR outputs.

Comparator Output HiZ

The comparator outputs COMP_A and COMP_B may be placed into a HiZ state, and those pins become input pins which drive the real time MONITOR control.

TABLE 15.

COMP#-OE	COMP_A_#	COMP_B_#
0	Input Pin (Ext-Mon-Sel#)	Input Pin (Ext-Mon-OE#)
1	Output Pin (COMP_A_#)	Output Pin (COMP_B_#)

Either channel may control the selection of the MONITOR source and output enable. The default condition upon power up and Reset are:

- CPU Control
- MONITOR and Monitor GND in HiZ
- Channel 0 selected.

TABLE 16.

MONITOR Source Control		
Sel-Mon-Sel	**Sel-Ext-Mon-Sel**	**Mon-Sel**
0	X	CPU-Mon-Sel
1	0	COMP_A_0
1	1	COMP_A_1
MONITOR Output Enable Control		
Sel-Mon-Sel	**Sel-Ext-Mon-Sel**	**Mon-OE**
0	X	CPU-Mon-OE
1	0	COMP_B_0
1	1	COMP_ B_1
MONITOR GND Output Enable Control		
Sel-Mon-GND-Sel	**Sel-Ext-Mon-OE**	**Mon-GND-OE**
0	X	CPU-Mon-GND-OE
1	0	COMP_B_0
1	1	COMP_ B_1

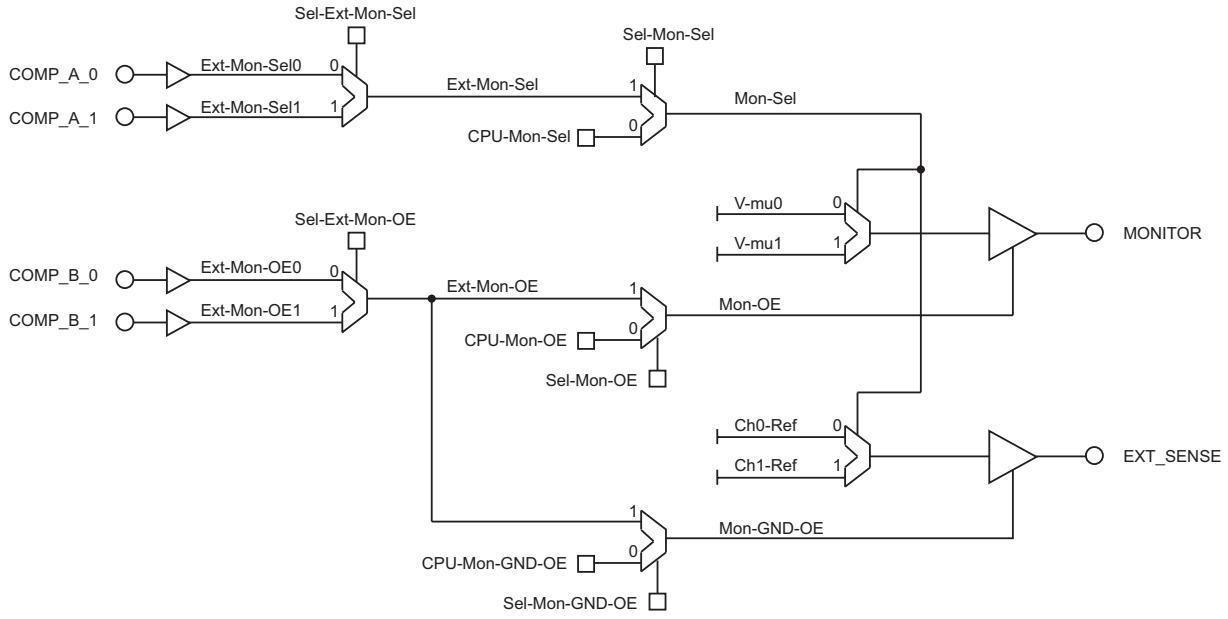


FIGURE 19.

Sense Options

The sense path is used to precisely control either the voltage at SENSE (or FORCE) or the current present at FORCE, and can lock on multiple parameters:

- Current at FORCE (FI)
- Voltage at FORCE (FV)
- Voltage at SENSE (FV)
- Op Amp output (V op amp (Tight Loop))
- Voltage at PPMU-F (Local Sense)

TABLE 17.

LOOP#	FI/MV*#	LOCAL SENSE*#	SEL-SENSE#	SEL-KELVIN#	CH# SENSED PARAMETER FEEDBACK#	CONFIGURATION
0	X	X	X	X	V op amp	Tight Lop
1	1	X	X	X	MI#	FI
1	0	0	X	X	PPMU-F#	Local Sense
1	0	1	0	X	FORCE_#	FV
1	0	1	1	0	SENSE_#	FV (Remote)
1	0	1	1	1	MV(1-#)	FV (Kelvin)

The local sense configuration is forced whenever Local Sense* = 0 or the switch between the PPMU-F and FORCE is open (RT-Con-PMU# = 0.) In this manner, the forcing op amp will never be left in an open loop state.

TABLE 18.

LOCAL SENSE#*	PPMU#-CON	CONFIGURATION
0	X	Local Sense
X	0	Local Sense
1	1	PMU (FV or FI)

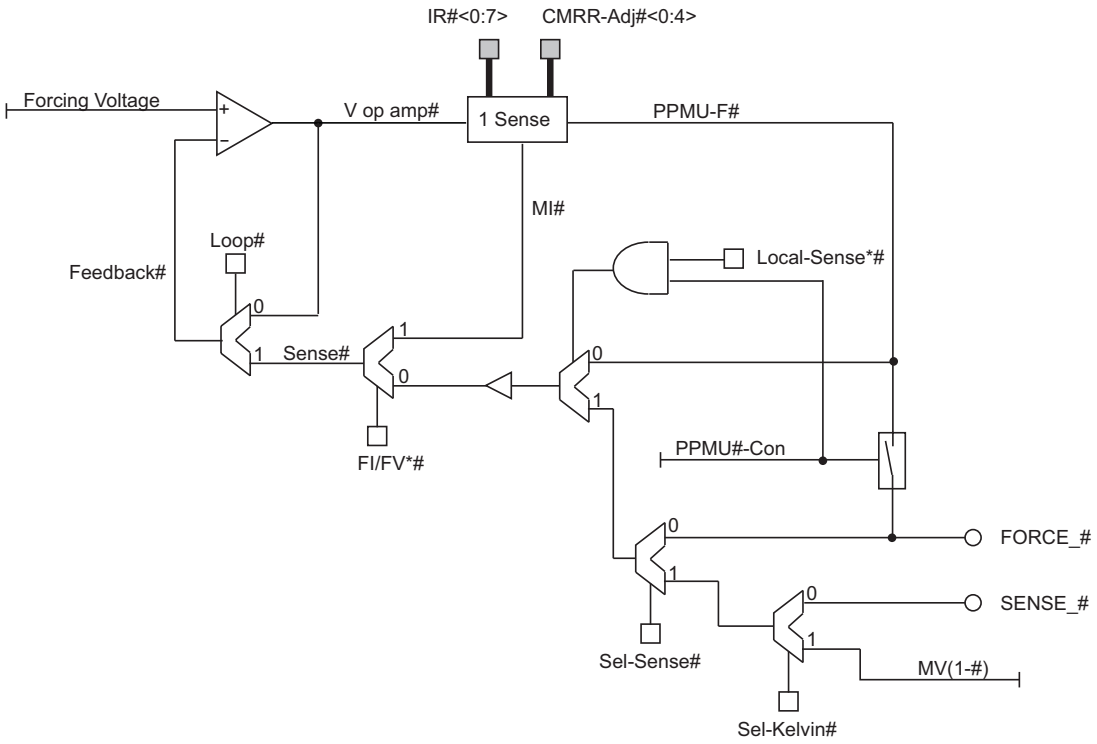


FIGURE 20.

Real Time PPMU Connection

There is a switch between PPMU-F and FORCE that connects and disconnects these two nodes. The high speed EN input is used to allow pattern control over when to connect and disconnect the PPMU.

An XOR gate in series with RT-En# allows either parity of EN to control the switch, as some applications (resistive load, for example) require the PPMU to be connected during a driver disable, while other applications (PPMU as a pin electronics driver) require the PPMU to be connected during a driver enable.

TABLE 19.

PPMU#-Con	PPMU-F# to FORCE#
0	Disconnected
1	Connected

TABLE 20.

Sel-PPMU#-Con	Sel-RT-PPMU#-Con	CPU-En0-XOR	CPU-En1-XOR	PPMU#-Con SOURCE
0	X	X	X	CPU-PPMU#-Con
1	0	0	X	EN_0
1	0	1	X	EN_0*
1	1	X	0	EN_!
1	1	X	1	EN_1*

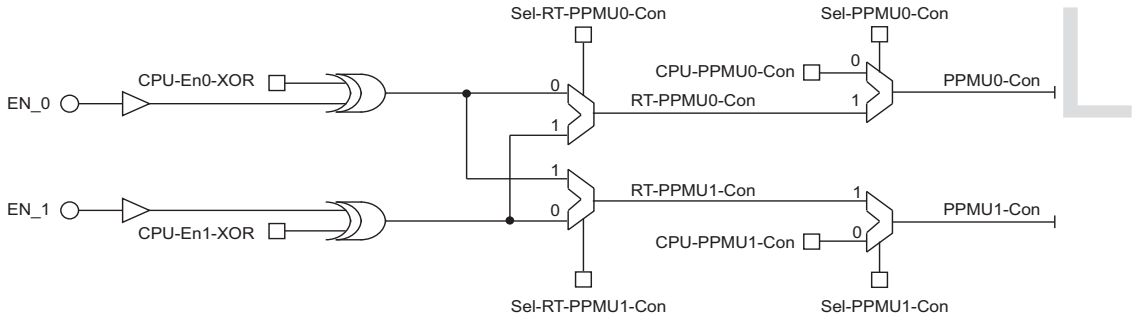


FIGURE 21.

External Force and Sense

An external force path exists to the FORCE pin of each channel. In addition, external sense paths exist to both the SENSE pin and the FORCE pin of each channel. These paths are useful to bypass the PPMU completely and provide direct access to the DUT, which is useful for:

1. Connecting an external PMU to the DUT
2. Direct measurement of the DUT voltage
3. DC calibration

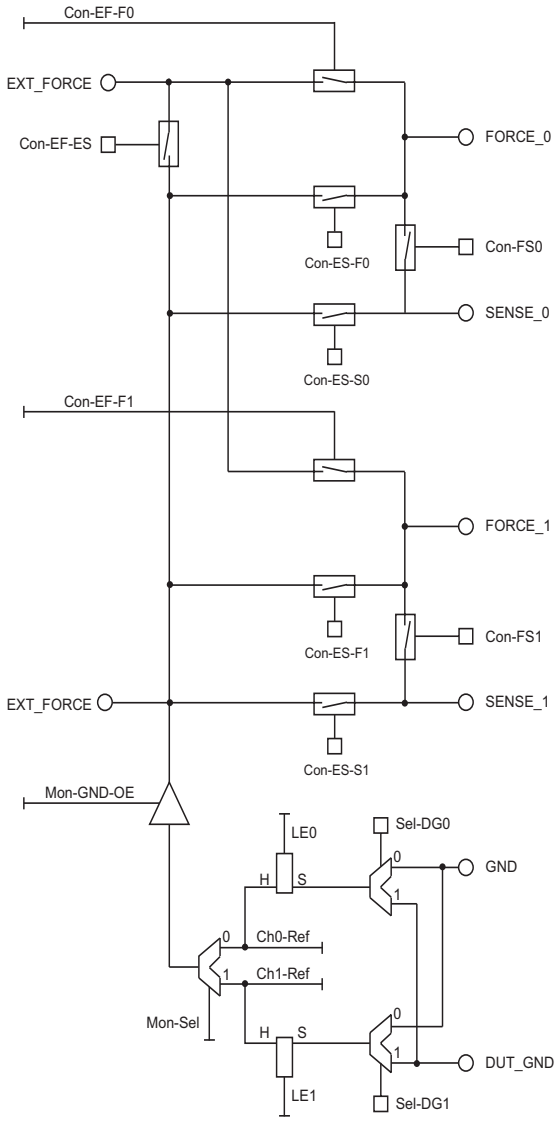


FIGURE 22.

Real Time External Force to FORCE_# Connection

Each channel has the ability to connect and disconnect the EXT_FORCE pin to its FORCE output in real time with 3 sources of control:

1. EN_0
2. EN_1
3. CPU port

A 2x2 cross point switch allows either channel's real time force to be driven by either channel's EN input. The EN input is inverted, such that the switch will be connected when EN is low.

TABLE 21.

Con-EF-F#	FORCE_# to EXT_FORCE
0	Disconnected
1	Connected

TABLE 22.

Sel-Con-EF-F#	Sel-RT-Con-EF-F#	Con-EF-F#
0	X	CPU-Con-EF-F#
1	0	EN_#*
1	1	EN_1(1-#)*

TABLE 23. EXTERNAL SENSE TO FORCE_#

Con-ES-F#	FORCE_# to EXT_SENSE
0	Disconnected
1	Connected

TABLE 24. EXTERNAL FORCE TO SENSE_#

Con-ES-S#	SENSE_# to EXT_SENSE
0	Disconnected
1	Connected

External Force to External Sense Connection

The CPU port can connect the EXT_FORCE and EXT_SENSE pins together directly, independent of the status of any other switch connected to the EXT_FORCE and EXT_SENSE pins.

TABLE 25.

Con-EF-ES	EXT_FORCE to EXT_SENSE
0	Disconnected
1	Connected

FORCE/SENSE Connection

Each channel has the ability to connect its FORCE and SENSE pins directly on-chip. This feature is useful in applications where remote sensing is not feasible.

TABLE 26.

Con-FS#	FORCE_# to SENSE_#
0	Disconnected
1	Connected

FI Voltage Clamps

Each PMU has programmable voltage clamps that limit the voltage swing at SENSE when the PPMU is forcing current. These clamps can be used to protect the DUT when current is being forced into a high impedance node at the DUT.

The clamps may be turned off by setting V-Cl-En = 0, in which case the clamps will remain high impedance between the supply voltages VCC and VEE.

TABLE 27.

FI/FV*#	V-Cl-En#	Ch# CLAMPS
0	X	HiZ
1	0	HiZ
1	1	Active

When active, the clamps sense the voltage at SENSE. If SENSE is within the limits of the high and low clamps, no action is taken. If SENSE exceeds the high or low voltage clamp, the PMU reduces the output current in order for the output voltage to not exceed the clamp voltage. If the voltage at SENSE subsequently drops back to within the clamp levels, the PPMU resumes sourcing or sinking its programmed current.

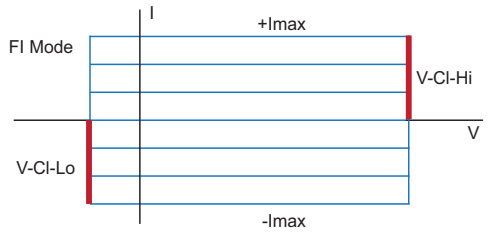


FIGURE 23.

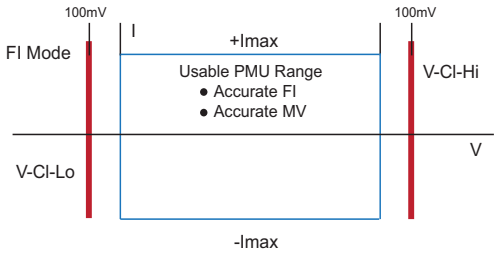


FIGURE 24.

FV Current Clamps

Each PMU has programmable current clamps that limit the current flow at FORCE when the PPMU is forcing a voltage. These clamps are useful in protecting the DUT from an over current situation.

The clamps may be disabled by setting I-Cl-En = 0.

TABLE 28.

FI/FV*#	I-Cl-En#	Ch# I-CLAMPS
1	X	Disabled
0	0	Disabled
0	1	Active

When Active, the I-Clamps sense the current at FORCE. If the current is within the boundaries set by I-Cl-Hi and I-Cl-Lo, no action is taken. If the measured current exceeds the upper or lower current clamp, the PMU reduces the output voltage in order for the output current to not exceed the clamp current. If the current at FORCE drops back to within the clamp levels, the PPMU resumes forcing its programmed voltage.

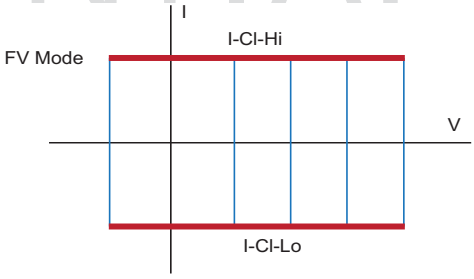


FIGURE 25.

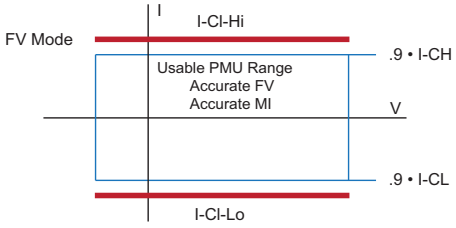


FIGURE 26.

The current clamps are programmable to 300% Imax.

TABLE 29.

I-Cl-Lo-#<15:0> I-Cl-Hi-#<15:0>	THRESHOLD	CURRENT LEVEL
0000 Hex	–3V	–3 * Imax
FFFF Hex	+3V	+3 * Imax

High Current Applications

Each individual channel supports a maximum current up to 32mA. However, multiple channels may be ganged together in order to create one PMU but with a higher maximum current.

On-Chip Ganging

The two channels on-chip may be combined into 1 PMU with 2X output current capability of an individual channel. This 2X Imax PMU may be configured internally to the IC, without the requirement of connecting the pins externally.

To create a high current FV/MI source, the following steps are taken:

- Determine which channel is the master PMU and which channel is the slave PMU.
- Place the master PMU into FV mode and the slave PMU into FI mode.
- Select the MI output signal of the master PMU as the forcing input to the slave PMU (Sel-Ch#-DAC<1:0> = 10B.) This routing is accomplished internally on-chip with the forcing voltage analog mux.
- Connect the master and slave FORCE output pins together (Con-PPMU-F(1-#) = 1).

The maximum output current is the sum of the individual output currents of the master and the slave PPMUs.

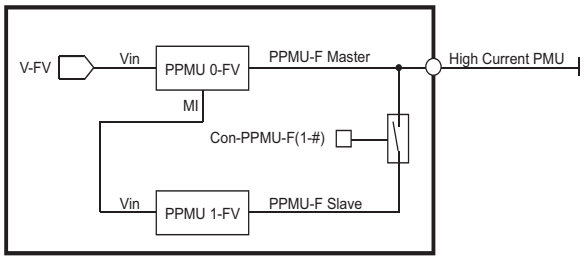


FIGURE 27.

TABLE 30.

Con-PPMU-F(1-#)	PPMU-F(1-#) to FORCE_#
0	Disconnected
1	Connected (ganged on-chip)

Multi-Chip Ganging

Multiple ICs may also be ganged together, allowing the creation of a very high current PMU. The control information to link all the devices together is passed from the master PMU to the slave PMUs through the MONITOR pins.

Any high current PMU requiring 3 or more PMUs to be ganged must be connected off-chip. There is no limit to the number of PMUs that may be ganged together.

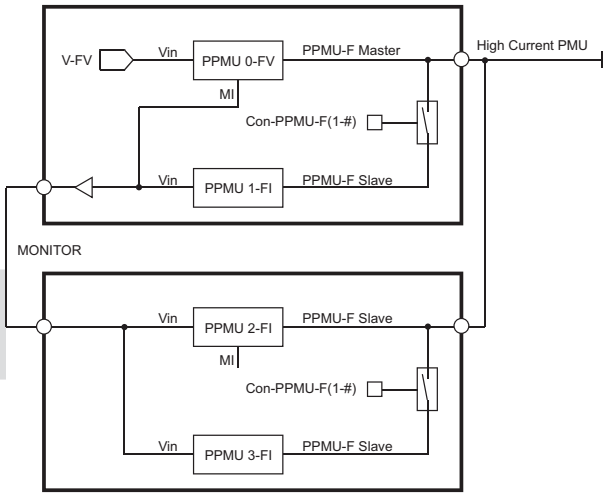


FIGURE 28.

Diagnostics

Each PPMU has access to key internal nodes so that the voltage on these nodes may be monitored. This access is typically used for testing and diagnostic purposes.

PER CHANNEL DIAGNOSTIC OPTIONS

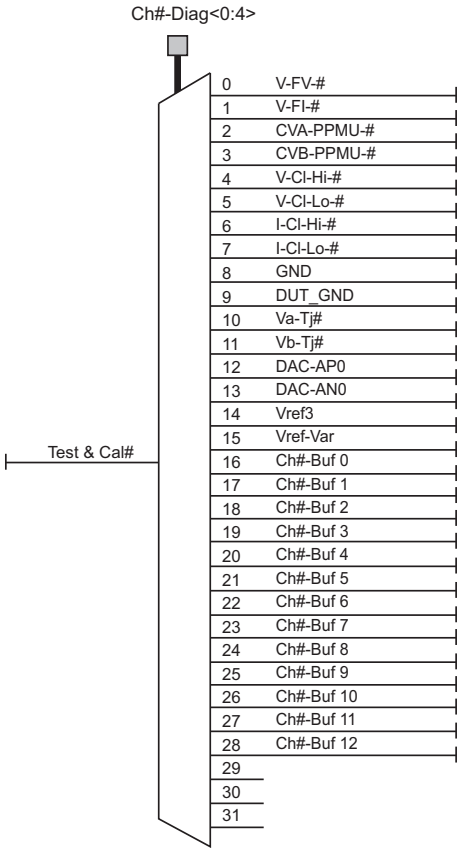


FIGURE 29.

When selected by the diagnostic multiplexer, the output DAC levels CH#_DAC_0 - CH#_DAC_12 are selected directly at the package pin output. When the output DAC is programmed to be a current output and that pin is selected for Test & Cal, the measurement unit will see the voltage going to the V to I converter on that pin and will not see actual current flowing through the output pin.

In normal operation the diagnostic mux should select location 8 such that no internal node is connected and GND is on the test node.

Temperature Sensing

It is possible to measure and monitor the junction temperature on a per channel basis. Test voltages Va-T_J and Vb-T_J are generated on-chip and allow the calculation of the junction temperature. The equation is:

$$T_J = \{(Va\text{-}T_J - Vb\text{-}T_J) \bullet 1,637\} - 221°C \quad \text{(EQ. 1)}$$

Va-T_J and Vb-T_J must be read back separately through the PPMU and off the chip via the MONITOR pin for the calculation to be performed.

Required Off-Chip Components

There are no external components required, but there is a V_REF level required per chip. However, there may be a need for decoupling capacitors on two types of pins:

1. Power Supplies
2. DAC outputs

The need for decoupling capacitors is dependent upon the particular application, and is therefore system dependent. But there is nothing inherent in the chip design that mandates or requires these capacitors.

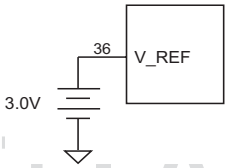


FIGURE 30.

Power Supply Restrictions

The following guidelines must be met to support proper operation:

1. VCC ≥ VDD
2. VEE ≤ GND
3. VDD ≥ GND

Schottky diodes are recommended on a once per board basis to protect against a power supply restriction violation.

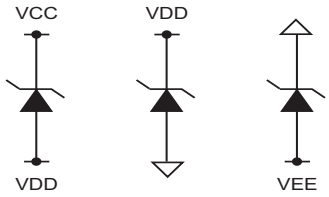


FIGURE 31.

Power Supply Sequence

Ideally, all power supplies would become active simultaneously while also meeting the power supply restrictions. However, since it is difficult to guarantee simultaneous levels, the following sequence is recommended:

1. VEE
2. VCC
3. VDD
4. V_REF

Internal DC Levels

Each channel's PMU requires 8 independent DC levels for proper operation. Each DC level may be programmed over 3 or 4 voltage ranges, depending on the particular level.

TABLE 31.

GROUP-RS<1:0>		VOLTAGE RANGE
0	0	VR0 (4V)
0	1	VR1 (8V)
1	0	VR2 (16V)
1	1	VIR

DC Level Groups

The DC levels are partitioned into 3 separate groups. Within each group, all DACs share a common voltage range.

TABLE 32.

GROUP	OUTPUTS	RANGE SELECT BITS
CV	CVA-PPMU-# CVB-PPMU-#	CV#-RS<0:1)
FV	V-FV-# V-CI-Hi-# V-CI-Lo-#	FV#-RS<0:1>
FI	V-FI-# I-CI-Hi-# I-CI-Lo-#	N/A

Voltage Level Outputs

Each channel supports 8 voltage DAC output pins that are capable of setting the required DC levels for the channel's pin electronics functions. Each voltage DAC may be programmed over 3 voltage ranges, as different ranges are useful when trying to achieve maximum resolution and accuracy for different output values.

TABLE 33.

GROUP-RS<1:0>		VOLTAGE RANGE
0	0	VR0 (4V)
0	1	VR1 (8V)
1	0	VR2 (16V)
1	1	VIR

DAC Groups

The DAC levels are partitioned into 5 separate groups, each optimized for a typical pin electronics application. Within each group, all DACs share a common voltage range and a common output impedance.

TABLE 34.

GROUP	#DACS	OUTPUTS	TYPE	RANGE SELECT BITS
A	3	CH#_DAC0-2	V	Group A#-RS<0:1>
B	2	CH#_DAC3-4	V	Group B#-RS<0:1>
C	3	CH#_DAC5-7		Group C#-RS<0:1>
D	3	CH#_DAC8-10		Group D#-RS<0:1>
E	2	CH#_DAC11-12		Group E#-RS<0:1>

Voltage DAC Impedance

Each voltage DAC has a nominal output impedance of ~250Ω.

Ground Force

All voltage DAC outputs may be set to ground by setting GND-Force*# = 0. This setting is the default condition, and is a useful way to quickly place all DAC levels into a known and safe state.

TABLE 35.

GND-FORCE*#	DAC OUTPUT
0	GND
1	Programmed Value

Voltage/Current Level Outputs

Each channel supports 5 DAC output pins that can provide either a voltage or a current. The 5 voltage/current DACs are partitioned into 2 separate groups. Within each group, all DACs share:

- Voltage/current selection
- Range selection
- Output impedance (if voltage output)

TABLE 36.

DAC GROUP	RANGE SELECT BITS
Group D	Group D#-RS<0:1>
Group E	Group E#-RS<0:1>

If a particular group is programmed to be voltage output DACs, these outputs have the same options and features as the voltage only DAC outputs.

Current DAC Outputs

The CPU port may configure these 5 DACs as current output DACs.

TABLE 37.

GROUP D#-IOUT GROUP E#-IOUT	GND-FORCE*#	DAC CONFIGURATION
0	1	Voltage Output
1	1	Current Output
X	0	Voltage Output

If in Iout mode and GND-FORCE* = 0, the output mode converts to Vout at 0V.

The current outputs are source only and support 2 current ranges:

- 25µA
- 2.5mA

Within each group, all DACs share a common current range. Once a current is selected for the DAC output, the LSB of the corresponding range selection is used to determine Imax for that group.

TABLE 38.

GROUP#-IOUT	GROUP#-RS<0>	IMAX	RESOLUTION (LSB)
1	0	250mA	3.81nA
1	1	2.5µA	38.1nA

Iout = (DAC Code) * LSB

TABLE 39.

DAC CODE (HEX)	IOUT
0000H	0
FFFFH	+Imax

Default State

DAC outputs that can be either a voltage or a current default (upon power up or reset) to:

- Voltage outputs
- Vout = GND
- Rout = 250Ω

DC Levels

Every functional block requires a variety of DC voltage levels in order to function properly. These levels are all generated on-chip with a 16 bit DAC that is programmed through the CPU port.

There are 4 voltage range options. Various DC levels are grouped together, and the selected voltage range is common for all levels within each group. (See table below)

The realizable voltage range is restricted by the power supply levels and headroom limitations, especially in VR2. If a level is programmed beyond the recommended operating conditions, saturation will occur and the actual DC level will not match the desired programmed level.

Voltage Range Options vs Function

Within each DAC group, the voltage range selection is common and is programmed via the CPU port.

CVA-PPMU and CVB-PPMU should use the IR range when measuring current (MI), and use VR0, VR1 or VR2 when measuring a voltage (MV).

TABLE 40.

RANGE SELECT<1:0>	VOLTAGE RANGE	OUTPUT VOLTAGE SWING (V)	RESOLUTION (LSB) (µV)	VMID (V)
0	VR0	8	61	0.125 to +2
1	VR1	8	122	0.250 to +4
2	VR2	16	244	0.5 to +8
3	VIR (FI)	2	30.5	0
3	VIR (MI)	4	61	0
3	VIR (ICL)	6	92.5	0

The voltage range associated with VIR depends upon the particular function. VIR (FI) refers to the on-chip DC level used to drive the forcing op amp when the PMU is in FI mode. VIR (MI) refers to the threshold levels of the comparators. VIR (ICL) refers to the current clamp function.

Offset and Gain

Each individual DC level has an independent offset and gain correction. These correction values allow the desired output level to be programmed at their true post calibrated value and to be loaded simultaneously across multiple pins without having to correct for per pin errors. The range of possible offset voltage correction is a % of the full scale voltage range of each particular voltage group.

TABLE 41.

OFFSET CODE	OFFSET VALUE	GAIN CODE	GAIN VALUE
0000H	–5.4% of FS	0000H	0.875
7FFFH	0	7FFFH	1.0
FFFFH	+5.4% of FS	FFFFH	1.125

Device Under Test Ground

The actual ground reference level at the DUT may be different than that used by the DAC reference. DUT_GND is a high impedance analog voltage input that provides a means of tracking the destination ground and making an additional offset to the programmed level so the programmed level is correct with respect to the DUT. DUT_GND is common for all channels within a package and is super imposed upon all voltage levels generated on the chip.

The input at DUT_GND should be:

1. Filtered for noise
2. Stable
3. Reflect the actual ground level at the DUT

V_REF

V_REF is an analog input voltage that is used to program the on-chip DC levels. V_REF should be held at +3.0V with respect to GND. Any noise or jitter on V_REF will contribute to the noise floor of the chip, and therefore V_REF should be as quiet and stable as possible.

There is one V_REF pin shared by all channels on the same chip.

V_REF Sensitivity

The above equations that predict the DAC output assume that V_REF = 3.000V. Any variation in V_REF at the input pin will affect the Level by a 1:1 ratio before being multiplied by the gain.

Level = Programmed Level * (1 - (V_REF - 3.0))

Offset adjust has ample range to correct for deviations in V_REF, in addition to any offset requirements. As long as V_REF is held stable after calibration, deviation in V_REF from 3.0V will not affect DC accuracy.

Adjustable Vmid

To support applications that require a wide variety of voltage range options, the value for Vmid in the output level calculation is programmable. This adjustment allows the same total voltage swing in each of the different voltage ranges, only now that voltage span may be adjusted more positive or more negative.

Vmid is not adjustable in the current measure range (IR).

TABLE 42.

VOLTAGE RANGE	Vmid LSB	Vmid-Adj<3:0>	Vmid
VR0	125mV	0000 1111	+125mV +2.0V
VR1	250mV	0000 1111	+250mV +4.0V
VR2	500mV	0000 1111	+500mV +8.0V

Voltage Range Table

Several examples of different voltage ranges are shown in the table below. For simplicity in each example:

Gain Correction = 1.0

Offset Correction = 0.0V

DUT_GND = 0.0V

Level Programming

Voltage Ranges VR0, VR1, and VR2 use Equation 2:

$$V_{OUT} = (Value - V_{MID}) \bullet Gain + Offset + V_{MID} + DUT\_GND \quad \text{(EQ. 2)}$$

Current force mode (VIR) uses Equation 3 :

$$V_{OUT} = (Value - V_{MID}) \bullet Gain + Offset + V_{MID} \quad \text{(EQ. 3)}$$

Value is described by Equation 4:

$$Value = \{(DAC\ Code)/(2^{**}N - 1)\} \bullet FS + V_{MIN}, \text{ where} \quad \text{(EQ. 4)}$$

$N = 16; 2^{**}N - 1 = 65,535$ and

$V_{MIN} = V_{MID} - (FS/2)$.

Level Reference

All DC voltage levels are referenced to GND.

TABLE 43.

RANGE	FS	VMID CODE	VMID	DAC CODE	OUTPUT VOLTAGE	COMMENTS
VR0	4	0000	+0.125V	0000 Hex FFFF Hex	–1.875V +2.125V	VR0 shifted –1.375V
VR0	4	1011	+1.5V	0000 Hex FFFF Hex	–0.5V +3.5V	Nominal VR0
VR0	4	1111	+2V	0000 Hex FFFF Hex	0V 4V	VR0 shifted +0.5V
VR1	8	1011	+3V	0000 Hex FFFF Hex	–1V +7V	Nominal VR1
VR1	8	0011	+1V	0000 Hex FFFF Hex	–3V +5V	VR1 shifted –2V
VR1	8	1111	+4V	0000 Hex FFFF Hex	0V +8V	VR1 shifted +1V
VR2	16	1011	+6V	0000 Hex FFFF Hex	–2.0V +14V	Nominal VR2
VR2	16	1001	+5V	0000 Hex FFFF Hex	–3V +13V	VR2 shifted –1V
VR2	16	1111	+8V	0000 Hex FFFF Hex	0V +16V	VR2 shifted up

Voltage Range Options

Different functional blocks require different DC level voltage ranges. The allowed combinations are listed in Table 44.

TABLE 44.

		VR0	VR1	VR2	IR	RANGE SELECT BITS <1:0>
Internal DC Levels						
CV	CVA-PPMU-CVB-PPMU	√	√	√	√	CV#-RS<0:1>
FV	C-FV, V-CI-Hi, V-CI-Lo	√	√	√		FV#-RS<0:1>
FI	V-FI, I-CI-Hi, I-CI-Lo				√	N/A
External DC Levels						
Group A	(CH#_DAC_0 – CH#_DAC_2)	√	√	√		Group A#-RS<0:1>
Group B	(CH#_DAC_3 – CH#_DAC_4)	√	√	√		Group B#-RS<0:1>
Group C	(CH#_DAC_5 – CH#_DAC_7)	√	√	√		Group C#-RS<0:1>
Group D	(CH#_DAC_8 – CH#_DAC_10)	√	√	√	√	Group D#-RS<0:1>
Group E	(CH#_DAC_11 – CH#_DAC_12)	√	√	√	√	Group E#-RS<0:1>
	Tracks DUT_GND (FV, MV)					
	Does NOT Track DUT_GND (FI, MI)					

DC Calibration Procedure

The part is designed and tested to meet its DC accuracy specifications after a two-point calibration. The actual calibration points are different for each voltage range, and may even be different for the same voltage range but for different functional blocks. However, most calibration points will be at 20% and 80% of the full-scale value for that range. (The actual calibration points are listed separately for each functional block in the DC specification section.)

The test points are broken into two categories:

1. Inner test
2. Outer test

The inner test is one specific test point (typically) at 50% of the full-scale value of the particular range. The outer test is usually taken at the end points of the voltage range, or 0% and 100% of the full-scale value.

In general, the inner test will be performed against tighter, more accurate limits. But every part shipped will be calibrated and tested against the limits in the specification section, and is guaranteed to perform within those limits under the documented calibration technique.

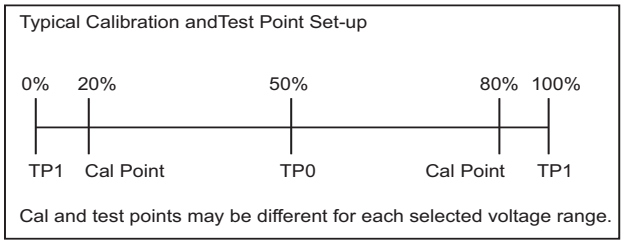


FIGURE 32.

System Level DC Accuracy Limits

Other calibration schemes and techniques, using different, more or fewer calibration points or different test points, may also be employed. The resulting system level accuracy may be superior or inferior to the part's specified limits, and will be dependent on the details of the particular application.

Calibration Procedure

1. Calibrate the MONITOR
2. Calibrate the DAC using the DAC cal bits
3. Calibrate the offset DAC
4. Calibrate the Gain DAC
5. Calibrate the DC Level

Level Calibration

- Initialize
  - Select desired voltage range (VR0, VR1, VR2, VIR)
  - Set Gain = 1.0; Offset = 0.0V
- Measure
  - Set Level 1 = Cal Point 1. Measure Output1' (low)
  - Set Level 2 = Cal Point 2. Measure Output2' (high)
- Calculate
  - Gain' = (Output2' - Output1')/(Level 2 - Level1)
  - Offset' = (Output2' - Vmid) - Gain' o (Level2 - Vmid)
- Finish
  - Set Offset = - Offset'/Gain'
  - Set Gain = 1.0/Gain'

DAC Calibration Options

Each channel has 1 dedicated 16 bit DAC used to generate the DC levels required for that channel. To facilitate superior DC accuracy, each DAC supports the ability to independently calibrate the top 5 MSBs. The default condition of these adjustment bits is the zero correction state.

The magnitude of the bit correction is an integer count of LSB voltage added or subtracted from the individual bit weighting, and is therefore a function of the particular voltage range selected for each level. The DAC MSB adjustment is applied to the DC level prior to the gain correction.

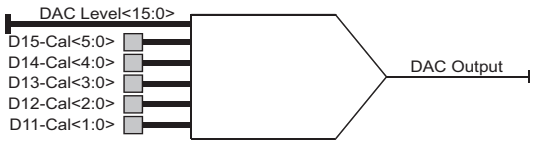


FIGURE 33.

TABLE 45. D15 CALIBRATION

CH#-D15-Cal 5	CH#-D15-Cal 4	CH#-D15-Cal 3	CH#-D15-Cal 2	CH#-D15-Cal 1	CH#-D15-Cal 0	CHANNEL # D15 ADJUSTMENT
0	1	1	1	1	1	+93 LSB
			•			•
0	0	0	0	0	1	+3 LSB
0	0	0	0	0	0	No Adjustment
1	0	0	0	0	0	No Adjustment
1	0	0	0	0	1	–3 LSB
			•			•
1	1	1	1	1	1	–93 LSB

TABLE 46. D14 CALIBRATION

Ch#-D14-Cal 4	Ch#-D14-Cal 3	Ch#-D14-Cal 2	Ch#-D14-Cal 1	Ch#-D14-Cal 0	CHANNEL # D14 ADJUSTMENT
0	1	1	1	1	+45 LSB
		•			•
0	0	0	0	1	+3 LSB
0	0	0	0	0	No Adjustment
1	0	0	0	0	No Adjustment
1	0	0	0	1	–3 LSB
		•			•
1	1	1	1	1	–45 LSB

TABLE 47. D13 CALIBRATION

Ch#-D13-Cal 3	Ch#-D13-Cal 2	Ch#-D13-Cal 1	Ch#-D13-Cal 0	CHANNEL # D13 ADJUSTMENT
0	1	1	1	+21 LSB
	•			•
0	0	0	1	+3 LSB
0	0	0	0	No Adjustment
1	0	0	0	No Adjustment
1	0	0	1	–3 LSB
	•			•
1	1	1	1	–21 LSB

TABLE 48. D12 CALIBRATION

CH#-D12-Cal 2	CH#-D12-Cal 1	CH#-D12-Cal 0	CHANNEL # D12 ADJUSTMENT
0	1	1	+9LSB
0	1	0	+6 LSB
0	0	1	+3 LSB
0	0	0	No Adjustment
1	0	0	No Adjustment
1	0	1	–3 LSB
1	1	0	–6 LSB
1	1	1	–9 LSB

TABLE 49. D11 CALIBRATION

Ch#-D11-Cal 1	Ch#-D11-Cal 0	CHANNEL # D11 ADJUSTMENT
0	1	+3 LSB
0	0	No Adjustment
1	0	No Adjustment
1	1	–3 LSB

CPU - Overview

All on-board DACs and registers are controlled through the CPU serial data port, which is capable of both writing to the chip as well as reading back from the chip (typically used for diagnostic purposes.)

Address

Address words for every CPU transaction are all 16 bits in length and contain the destination of the data word a write cycle, or the source to be read back for a read cycle. Address bits are shifted in LSB first, MSB last.

Data

Data words for every CPU transaction are all 16 bits in length and are loaded or read back LSB first, MSB last. The timing for data is different for a read cycle vs a write cycle, as the drivers on the SDIO alternate between going into high impedance and driving the line.

Control Signals

There are 3 CPU interface signals - SDIO, CK, and STB. SDIO is a bidirectional data pin through which information is either loaded or written back. CK is the CPU port clock signal that transfers data back and forth.

When data is going into the part, SDIO is latched on a rising edge of CK. When data is coming out of the part, SDIO is again updated on a rising edge of CK. SDIO is a 50Ω output impedance output pin in this mode.

STB is the control signal that identifies the beginning of a CPU transaction. STB remains high for the duration of the transaction, and must go low before another transaction may begin.

Clock Requirements

CK must be running at all times.

Even if no CPU transactions are occurring, CK is used on-chip for other functions and MUST therefore toggle continuously for correct chip operation.

Write Enable

Various register bits in the memory map tables require a write enable (WE) to allow those bits to be updated during a CPU write cycle. WE control allows some bits within an address to be changed, while others are held constant. Each WE applies to all lower data bits, until another WE is reached. Each group of registers with a common WE is shown in the memory map tables with a common background color.

If WE = 1, the registers in the WE group will be written to. If WE = 0, the registers will not be updated but all data bits associated with that field must also be programmed to 0.

If WE = 0, the registers will not be updated but all data bits associated with that field must also be programmed to 0.

Read vs Write Cycle

The first SDIO bit latched by CK in a transaction identifies the transaction type.

TABLE 50.

1st SDIO BIT	CPU TRANSACTION TYPE
0	Read - Data flows out of the chip
1	Write - Data flows into the chip

Parallel Write

The second SDIO bit of a transaction indicates whether a parallel write occurs. The parallel write is a convenient way to save time when identical information needs to go to multiple channels.

TABLE 51.

2nd SDIO BIT	CPU TRANSACTION TYPE
0	Data goes to the selected channel
1	Data goes to all channels

A parallel write ignores the particular channel address, and writes the information into the same location on all channels. During a parallel write, all channels on the chip will write the data to the selected destinations in parallel, regardless of which channel's address is input into the chip.

Reset

RESET is an external hardware reset signal that places all internal registers and control lines into a low state. Reset must be executed after a power up sequence. **RESET does NOT place the DAC level memory into a known state, so this information must always be loaded after a power up sequence.**

RESET is active high.

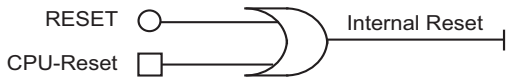


FIGURE 34.

In addition, the CPU port can execute a reset (as a write only transaction.) If the Reset address is written to, regardless of the value of any of the SDIO bits, CPU-Reset will fire off a one shot pulse that performs the same function as an external RESET.

Chip ID

Chip ID (see memory map tables) is a read only function that identifies the product and the die revision.

TABLE 52.

D15 ... D4	D3 ... D0
04BH	Die Revision

CPU - Address Description

Information is stored on-chip in two ways:

1. RAM
2. Registers.

Each storage mechanism is then broken into two categories:

1. Per Pin resources
2. Central resources.

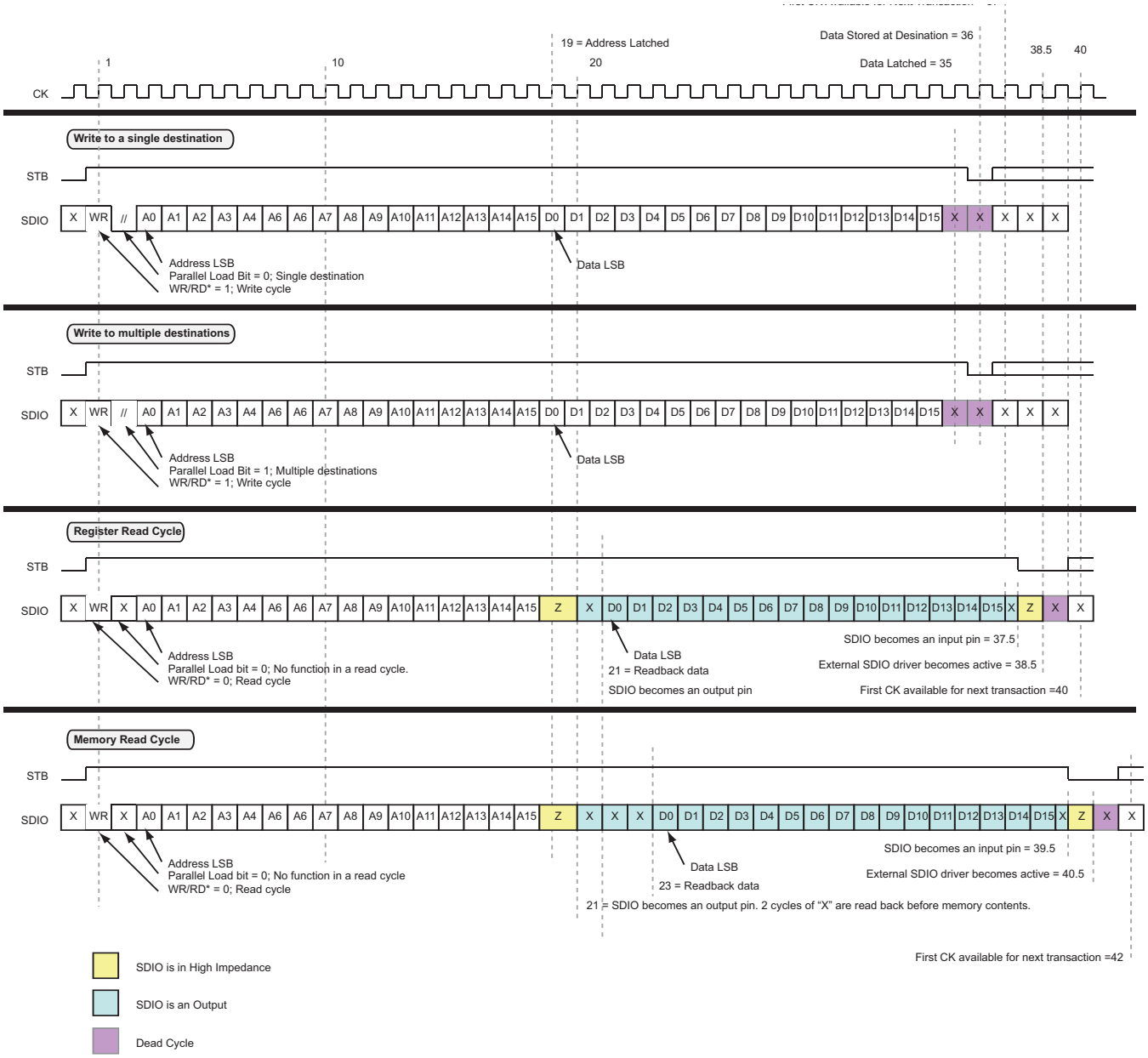
The address space is partitioned into several different segments to clearly mark the resource type and function.

Unused register bits should be written as a logical "0" and read back as don't care "X" conditions.

TABLE 53.

Per Pin Resource RAM Storage																
REGISTER BIT	CENTRAL BIT	CHANNEL ADDRESS							DAC FUNCTION		RESOURCE ADDRESS					DESCRIPTION
A15	A14	A13	A12	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0	
0	0	0	0	0	0	0	0	0	0	0	A4	A3	A2	A1	A0	Channel 0 DC Levels
0	0	0	0	0	0	0	0	0	0	1	A4	A3	A2	A1	A0	Channel 0 DC Level Offset Values
0	0	0	0	0	0	0	0	0	1	0	A4	A3	A2	A1	A0	Channel 0 DC level Gain Values
0	0	0	0	0	0	0	0	0	1	1	A4	A3	A2	A1	A0	Not Used
0	0	0	0	0	0	0	0	1	0	0	A4	A3	A2	A1	A0	Channel 1 DC Levels
0	0	0	0	0	0	0	0	1	0	1	A4	A3	A2	A1	A0	Channel 1 DC Level Offset Values
0	0	0	0	0	0	0	0	1	1	0	A4	A3	A2	A1	A0	Channel 1 DC level Gain Values
0	0	0	0	0	0	0	0	1	1	1	A4	A3	A2	A1	A0	Not Used
Per Pin Resource Register Storage																
REGISTER BIT	CENTRAL BIT	CHANNEL ADDRESS							RESOURCE ADDRESS							DESCRIPTION
1	0	0	0	0	0	0	0	0	A6	A5	A4	A3	A2	A1	A0	Channel 0 Registers
1	0	0	0	0	0	0	0	1	A6	A5	A4	A3	A2	A1	A0	Channel 1 Registers
Central Resource Register Storage																
REGISTER BIT	CENTRAL BIT	CHANNEL ADDRESS							RESOURCE ADDRESS							DESCRIPTION
1	1	0	0	0	0	0	0	0	A6	A5	A4	A3	A2	A1	A0	Central Resource Registers

CPU - Protocol Timing Diagram



Address Space - Per Pin DC Levels

Channels 0 and 1 RAM Storage																
REGISTER BIT	CENTRAL BIT	CHANNEL ADDRESS							DAC FUNCTION		RESOURCE ADDRESS					DESCRIPTION
A15	A14	A13	A12	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0	CHANNEL 0
0	0	0	0	0	0	0	0	0	0 ... 2		0	0	0	0	0	V-FV-0
0	0	0	0	0	0	0	0	0	0 ... 2		0	0	0	0	1	V-FI-0
0	0	0	0	0	0	0	0	0	0 ... 2		0	0	0	1	0	CVA-PPMU-0
0	0	0	0	0	0	0	0	0	0 ... 2		0	0	0	1	1	CVB-PPMU-0
0	0	0	0	0	0	0	0	0	0 ... 2		0	0	1	0	0	V-CI-Hi-0
0	0	0	0	0	0	0	0	0	0 ... 2		0	0	1	0	1	V-CI-Lo-0
0	0	0	0	0	0	0	0	0	0 ... 2		0	0	1	1	0	I-CI-Hi-0
0	0	0	0	0	0	0	0	0	0 ... 2		0	0	1	1	1	I-CI-Lo-0
0	0	0	0	0	0	0	0	0	0 ... 2		0	1	0	0	0	Not used
0	0	0	0	0	0	0	0	0	0 ... 2		0	1	0	0	1	Not used
0	0	0	0	0	0	0	0	0	0 ... 2		10 - 15					Not used
0	0	0	0	0	0	0	0	0	0 ... 2		1	0	0	0	0	Ch0-DAC-0
0	0	0	0	0	0	0	0	0	0 ... 2		1	0	0	0	1	Ch0-DAC-1
0	0	0	0	0	0	0	0	0	0 ... 2		1	0	0	1	0	Ch0-DAC-2
0	0	0	0	0	0	0	0	0	0 ... 2		1	0	0	1	1	Ch0-DAC-3
0	0	0	0	0	0	0	0	0	0 ... 2		1	0	1	0	0	Ch0-DAC-4
0	0	0	0	0	0	0	0	0	0 ... 2		1	0	1	0	1	Ch0-DAC-5
0	0	0	0	0	0	0	0	0	0 ... 2		1	0	1	1	0	Ch0-DAC-6
0	0	0	0	0	0	0	0	0	0 ... 2		1	0	1	1	1	Ch0-DAC-7
0	0	0	0	0	0	0	0	0	0 ... 2		1	1	0	0	0	Ch0-DAC-8
0	0	0	0	0	0	0	0	0	0 ... 2		1	1	0	0	1	Ch0-DAC-9
0	0	0	0	0	0	0	0	0	0 ... 2		1	1	0	1	0	Ch0-DAC-10
0	0	0	0	0	0	0	0	0	0 ... 2		1	1	0	1	1	Ch0-DAC-11
0	0	0	0	0	0	0	0	0	0 ... 2		1	1	1	0	0	Ch0-DAC-12
0	0	0	0	0	0	0	0	0	0 ... 2		29 - 31					Not used
A15	A14	A13	A12	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0	CHANNEL 1
0	0	0	0	0	0	0	0		0 ... 2		0	0	0	0	0	V-FV-1
0	0	0	0	0	0	0	0		0 ... 2		0	0	0	0	1	V-FI-1
0	0	0	0	0	0	0	0		0 ... 2		0	0	0	1	0	CVA-PPMU-1
0	0	0	0	0	0	0	0		0 ... 2		0	0	0	1	1	CVB-PPMU-1
0	0	0	0	0	0	0	0		0 ... 2		0	0	1	0	0	V-CI-Hi-1
0	0	0	0	0	0	0	0		0 ... 2		0	0	1	0	1	V-CI-Lo-1
0	0	0	0	0	0	0	0		0 ... 2		0	0	1	1	0	I-CI-Hi-1
0	0	0	0	0	0	0	0		0 ... 2		0	0	1	1	1	I-CI-Lo-1
0	0	0	0	0	0	0	0		0 ... 2		0	1	0	0	0	Not used
0	0	0	0	0	0	0	0		0 ... 2		0	1	0	0	1	Not used
0	0	0	0	0	0	0	0		0 ... 2		10 - 15					Not used
0	0	0	0	0	0	0	0		0 ... 2		1	0	0	0	0	Ch1-DAC-0
0	0	0	0	0	0	0	0		0 ... 2		1	0	0	0	1	Ch1-DAC-1
0	0	0	0	0	0	0	0		0 ... 2		1	0	0	1	0	Ch1-DAC-2
0	0	0	0	0	0	0	0		0 ... 2		1	0	0	1	1	Ch1-DAC-3
0	0	0	0	0	0	0	0		0 ... 2		1	0	1	0	0	Ch1-DAC-4
0	0	0	0	0	0	0	0		0 ... 2		1	0	1	0	1	Ch1-DAC-5
0	0	0	0	0	0	0	0		0 ... 2		1	0	1	1	0	Ch1-DAC-6
0	0	0	0	0	0	0	0		0 ... 2		1	0	1	1	1	Ch1-DAC-7
0	0	0	0	0	0	0	0		0 ... 2		1	1	0	0	0	Ch1-DAC-8
0	0	0	0	0	0	0	0		0 ... 2		1	1	0	0	1	Ch1-DAC-9
0	0	0	0	0	0	0	0		0 ... 2		1	1	0	1	0	Ch1-DAC-10
0	0	0	0	0	0	0	0		0 ... 2		1	1	0	1	1	Ch1-DAC-11
0	0	0	0	0	0	0	0		0 ... 2		1	1	1	0	0	Ch1-DAC-12
0	0	0	0	0	0	0	0		0 ... 2		29 - 31					Not used

Per Pin Registers

Channel 0 - 1 Control Register (0 ≤ # ≤ 1)																				
REGISTER BIT	CENTRAL BIT	CHANNEL ADDRESS	RESOURCE ADDRESS	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	DESCRIPTION
1	0	#	0	WE	Sel-Kelvin#	WE	Sel-PPMU#-Con	CPU-PPMU#-Con	CPU-En#-XOR	Sel-RT-PPMU#-Con	WE	Sel-S/H#	Sel-LE#	Sel-RT-LE#	CPU-LE#	WE	Comp#-OE	WE	Sel-DG#	Configuration Control Bits
1	0	#	1	WE	CMRR-Adj#-4	CMRR-Adj#-3	CMRR-Adj#-2	CMRR-Adj#-1	CMRR-Adj#-0	WE	Reserved	IR#7	IR#6	IR#5	IR#4	IR#3	IR#2	IR#1	IR#0	Current Range/ CMRR Adjust
1	0	#	2	WE	I-Cl-En#	WE	Sel-Sense#	WE	V-Cl-En#	WE	Sel-Buf-S#	WE	Local-Sense*#	WE	Loop#	WE	Mi/MV*#	WE	Fi/FV*#	PPMU Configuration
1	0	#	3		CB#-PPMU	CA#-PPMU	WE	0	WE	Sel-CPU-C#	CPU-CB#-PPMU	CPU-CA#-PPMU	WE	Sel-MU-Diag#	Ch#-Diag4	Ch#-Diag3	Ch#-Diag2	Ch#-Diag1	Ch#-Diag0	Diagnostics (Yellow = Read Only)
1	0	#	4					WE	Group E#-Iout	WE	GroupD#-Iout	WE	GND-Force*#	WE	FV#-RS1	FV#-RS0	WE	CV#-RS1	CV#-RS0	Internal Level Range Selection
1	0	#	5	WE	Con-FS#	WE	Con-PPMU-F(1-#)	WE	Sel-Ch#-DAC2	Sel-Ch#-DAC1	Sel-Ch#-DAC0	WE	Con-ES-S#	WE	Con-ES-F#	WE	Sel-Con-EF-F#	Sel-RT-Con-EF-F#	CPU-Con-EF-F#	Force/Sense Options
1	0	#	6		WE	Group E#-RS1	Group E#-RS0	WE	Group D#-RS1	Group D#-RS0	WE	Group C#-RS1	Group C#-RS0	WE	Group B#-RS1	Group B#-RS0	WE	Group A#-RS1	Group A#-RS0	External Level Range Selection
1	0	#	7-63																	Not used
1	0	#	64				WE	Ch#-D14-Cal4	Ch#-D14-Cal3	Ch#-D14-Cal2	Ch#-D14-Cal1	Ch#-D14-Cal0	WE	Ch#-D15-Cal5	Ch#-D15-Cal4	Ch#-D15-Cal3	Ch#-D15-Cal2	Ch#-D15-Cal1	Ch#-D15-Cal0	Upper DAC Bit Calibration
1	0	#	65			WE	0	WE	Ch#-D11-Cal1	Ch#-D11-Cal0	WE	Ch#-D12-Cal2	Ch#-D12-Cal1	Ch#-D12-Cal0	WE	Ch#-D13-Cal3	Ch#-D13-Cal2#	Ch#-D13-Cal1	Ch#-D13-Cal0	Mid DAC Bit Calibration
1	0	#	66-127																	Not used

Central Resource Registers

Central Resource Control Registers																			
REGISTER BIT	CENTRAL BIT	CHANNEL ADDRESS	RESOURCE	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	DESCRIPTION
1	1	0	0					WE	CPU-Mon-Sel	Sel-Mon-Sel	Sel-Ext-Mon-Sel	WE	Con-EF-ES	WE	Sel-Mon-GND-OE	CPU-Mon-GND-OE	CPU-Mon-OE	Sel-Mon-OE	Sel-Ext-Mon-OE	Central Control Bits
1	1	0	1	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	Chip Reset (Blue = Write Only)
1	1	0	2												WE	Vmid3	Vmid2	Vmid1	Vmid0	Vmid
1	1	0	3-127																	Not used
1	1		127	Product-ID11	Product-ID10	Product-ID9	Product-ID8	Product-ID7	Product-ID6	Product-ID5	Product-ID4	Product-ID3	Product-ID2	Product-ID1	Product-ID0	Die-Rev3	Die-Rev2	Die-Rev1	Die-Rev0	Die ID (Yellow = Read Only)

Manufacturing Information

Moisture Sensitivity

The part is a Level 3 (JEDEC Standard 033A) moisture sensitive part. All Pre Production and Production shipments will undergo the following process post final test:

- Baked @ +125°C ± 5°C for a duration ≥ 16 hours
- Vacuum sealed in a moisture barrier bag (MBB) within 30 minutes after being removed from the oven.

PCB Assembly

The floor life is the time from the opening of the MBB to when the unit is soldered onto a PCB.

Product Floor Life ≤168 Hours

Units that exceed this floor life must be baked before being soldered to a PCB.

Solder Profile

The recommended solder profile is dependent upon whether the PCB assembly process is lead-free or not.

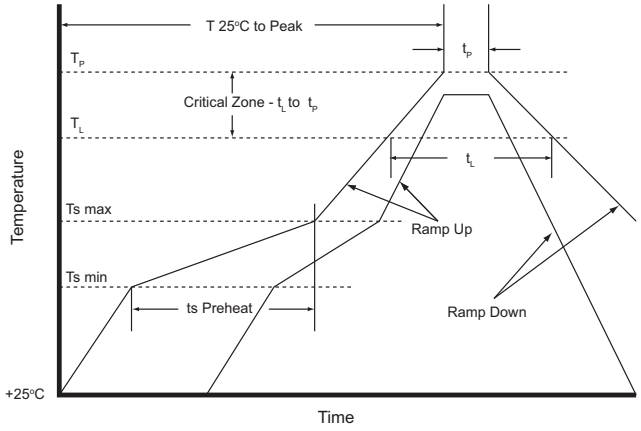


FIGURE 35.

TABLE 54. SOLDER PROFILE

PROFILE FEATURE	Sn-Pb EUTECTIC ASSEMBLY	Pb-FREE ASSEMBLY
Average ramp up rate (T_L to T_P)	3°C/sec (max)	3°C/sec (max)
Preheat • Min Temp (Ts min) • Max Temp (Ts max) • Time (min to max) (ts)	 +150°C +200°C 60 – 180 sec	 +150°C +200°C 60 – 180 sec
Ts max to T_L • Ramp-Up Rate	 	 3°C/sec (max)
Time above • Temperature (T_L) • Time (t_L)	 +183°C 60 – 150 sec	 +217°C 60 – 150 sec
Peak Temperature (T_P)	+240°C +0/–5°C	+250°C +0/–5°C
Time within 5°C of actual peak temp (tp)	10 sec – 30 sec	20 sec – 40 sec
Ramp down rate	6°C/sec (max)	6°C/sec (max)
Time +25°C to peak temperature	6 minutes (max)	8 minutes (max)

Package Thermal Analysis

Junction Temperature

Maintaining a low and controlled junction temperature is a critical aspect of any system design. Lower junction temperatures translate directly into superior system reliability. A more stable junction temperature translates directly into superior AC and DC accuracy.

The junction temperature follows the equation:

$T_J = Pd \bullet \theta_{JA} + T_A$

T_J = Junction Temperature

Pd = Power Dissipation

θ_{JA} = Thermal Resistance (Junction to Ambient)

T_A = Ambient Temperature

Heat can flow out of the package through two mechanisms:

- Conduction
- Convection

Conduction

Conduction occurs when power dissipated inside the chip flows out through the leads of the package and into the printed circuit board. As the part has an exposed metal slug on the bottom of the package there will be a low thermal resistance path from the silicon through the slug to the internal VEE plane inside the PC board.

Convection

The most common cooling scheme is to use airflow and (potentially) a heat sink on each part. In this configuration, most of the heat will exit the package via convection, as it flows from the top of the die through the plastic package and off the chip into the surrounding air flow.

Thermal Resistance

Each system will have its own unique cooling strategy and overall θ_{JA}. However, the resistance between the junction and the case is a critical and common component to the thermal analysis in all designs.

$\theta_{JA} = \theta_{JC} + \theta_{CA}$

θ_{CA} is determined by the system environment of the part and is therefore application specific. θ_{JC} is determined by the construction of the part.

CONVECTION θ_{JC} CALCULATION

$\theta_{JC} = \theta$ (moulding compound)

CONDUCTION θ_{JC} CALCULATION

θ_{JC} = θ(silicon)
+ θ(die attach)
+ θ(paddle)

The thermal resistance of any material is defined by the equation:

θ = (Intrinsic material resistance) • Thickness/Area

or

θ = Thickness/(Intrinsic material conductivity • Area).

INTRINSIC THERMAL CONDUCTIVITY

Die Attach Thermal Conductivity = 1.4W/M °K

Silicon Thermal Conductivity = 141.2W/M °K

Paddle Thermal Conductivity = 263W/M °K

Plastic Thermal Conductivity = 0.88W/M °K

Theta JC Convection = +11.7°C/W

θ_{JC} Conduction = 0.05 °C/W + 0.5°C/W + 0.02°C/W

θ_{JC} Conduction = 0.57°C/W

However, these calculations are based upon many assumptions and it should be treated as typical values.

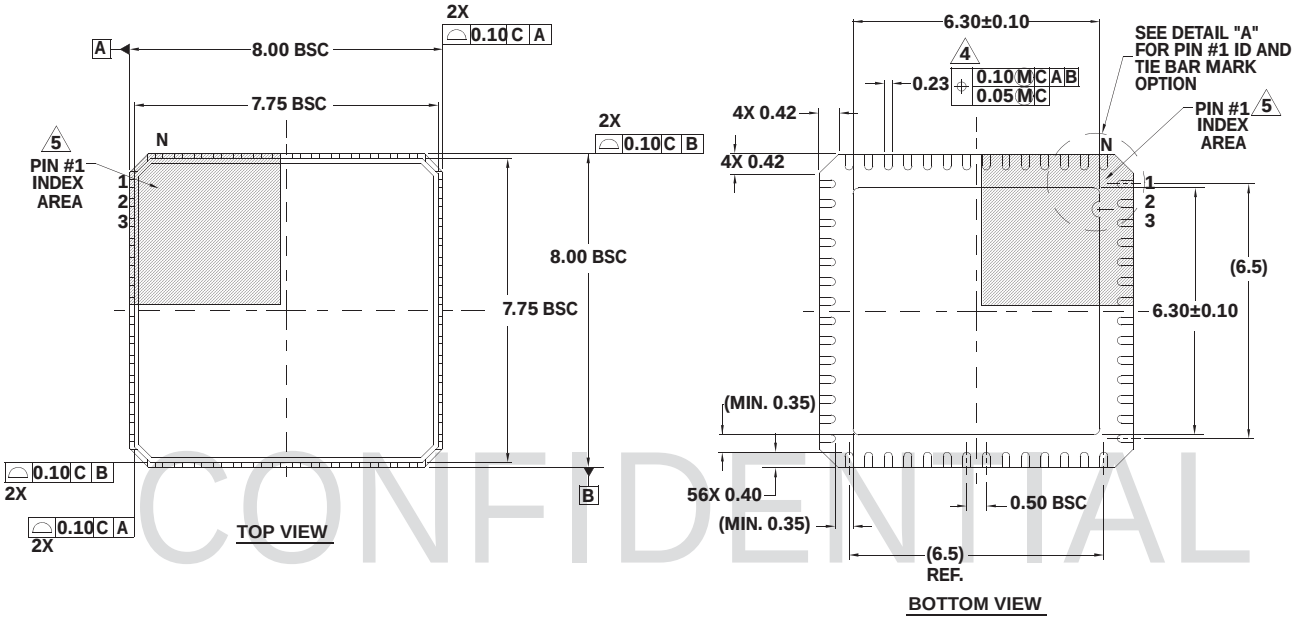
θ_{JC} Conduction is significantly lower than θ_C Convection and therefore most of the heat will try to leave the package through the exposed paddle and go into the PC board VEE plane. However, the conduction path is affected by the ability of the system to remove heat from the PC board while the convection path may be enhanced by adding heat sinks and air flow.

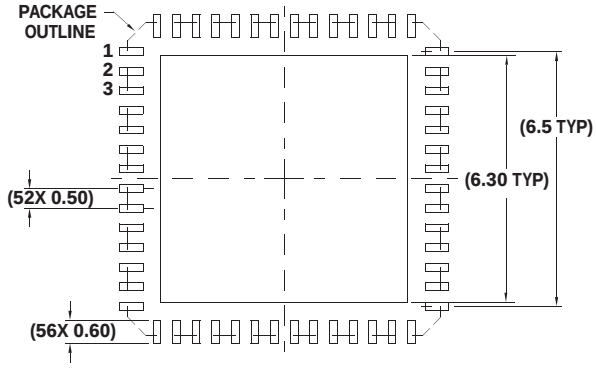
The final θ_{JA} will be the parallel combination of θ Conduction and θ Convection while included the system level details that cover the thermal resistance from case to ambient.

Package Outline Drawing

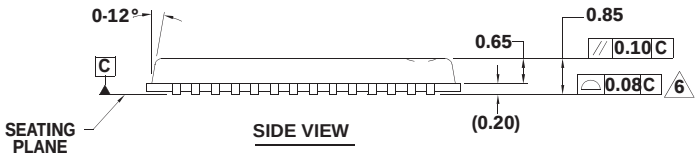
L56.8x8F

56 LEAD QUAD FLAT NO-LEAD PLASTIC PACKAGE
Rev 0, 4/10

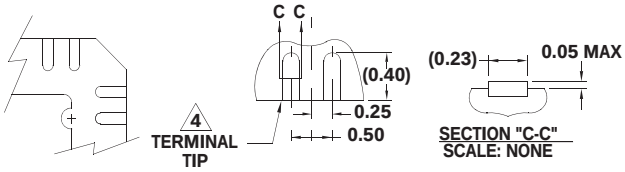




TYPICAL RECOMMENDED LAND PATTERN



SIDE VIEW



DETAIL "A" - PIN #1 ID AND LEAD FIGURES

NOTES:

1. Dimensions are in millimeters.
   Dimensions in ( ) for Reference Only.
2. Dimensioning and tolerancing conform to ASME Y14.5M-1994.
3. Unless otherwise specified, tolerance : Decimal ± 0.05
4. Lead width dimension applies to the metallized terminal and is measured between 0.15mm and 0.30mm from the terminal tip.
5. The configuration of the pin #1 identifier is optional, but must be located within the zone indicated. The pin #1 identifier may be either a mold or mark feature.
6. Bilateral coplanarity zone applies to the exposed pad as well as the terminals.
7. JEDEC reference drawing: MO-220WLLD.

Revision History

DATE	CHANGE
January 8, 2016	• Page 45: Power Supply Sequence Section - update power supply sequence
April 1, 2015	• Update to Elevate Semicondutor format
November 1, 2013	• Pages 39 - 57: Replace gray squares with diagrams.
June 7, 2013	• Page 9: DAC Calibration Table - Spec #'s updated • Page 12: Spec #14817, Test Conditions: change Note 19 to Note 18 • Page 13: Change Spec # 148076 to 14140. • Page 18: Updated first paragraph - Spec 13506: Change S/W calibration to read IR6 Calibrated - spec 13507: change S/W calibration to read IR7 Calibrated

Ordering Information

PART NUMBER (Note 1)	PART MARKING	TEMP. RANGE (°C)	PACKAGE	PKG. DWG. #
ISL55187CRZ	ISL55187CRZ	+25°C to +85°C	56 Lead 8 x 8 QFN	L56.8x8F

NOTE:

1. These Elevate Semiconductor Pb-free plastic packaged products employ special Pb-free material sets, molding compounds/die attach materials, and 100% matte tin plate plus anneal (e3 termination finish, which is RoHS compliant and compatible with both SnPb and Pb-free soldering operations). Elevate Semiconductor Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020.