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ISL5571A

Access High Voltage Switch

FN4920
Rev 5.00
Jul 2004

The ISL5571A is a solid state device designed to replace the electromechanical relay used on Subscriber Line Cards. The device contains two Line Break MOSFET switches, one Ring Return MOSFET switch and one Ring Access SCR switch.

The ISL5571A is pin-for-pin compatible with the Lucent L7581AAE LCAS and Clare CPCL7581A Products. Improvements include: line break switches r_{ON} match (0.5Ω Max) higher dV/dt sensitivity (5000V/µs), protection SCR hold current set to 110mA.

The line break MOSFETs have very low on resistance (<16.0Ω Typ) and Ron match (<0.05Ω Typ, 0.5Ω Max) and a blocking voltage >330V. The Ring Return MOSFET has a typical Ron of 50Ω and a blocking voltage >330V. The Ringing Access switch is implemented with a SCR device with a blocking voltage >480V. The SCR switch inherently offers low EMI connect and disconnect circuitry. All control I/Os use TTL thresholds making the device compatible with 3V logic.

The ISL5571A also includes on-chip protection in the form of an over-voltage clamping circuit, current-limited MOSFET switches, and thermal shutdown circuitry. The over-voltage clamping circuit consists of a diode bridge and SCR.

Ordering Information

PART NUMBER	PROT SCR	TEMP RANGE (°C)	PACKAGE TYPE	PKG. DWG. #
ISL5571AIB	Yes	-40 to 85	16 Ld SOIC	M16.3
ISL5571AIBZ (Note)	Yes	-40 to 85	16 Ld SOIC (Pb-free)	M16.3

NOTE: Intersil Pb-free products employ special Pb-free material sets; molding compounds/die attach materials and 100% matte tin plate termination finish, which is compatible with both SnPb and Pb-free soldering operations. Intersil Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J Std-020B.

Add “-T” for tape and reel.

Features

- Small Size/Surface-Mount Packaging
- Low Impulse Noise, Low EMI
- Clean, Bounce-Free Switching
- Line Break Switches
  - 0.5Ω Max r_{ON} Match
  - 28Ω Max r_{ON}
- Built-In Current Limiting, Thermal Shutdown and Secondary Protection for the SLIC
- Optimized for Short Loop High REN Applications
- 3V/5V Logic-Capable I/O
- Pb-free Available

Applications

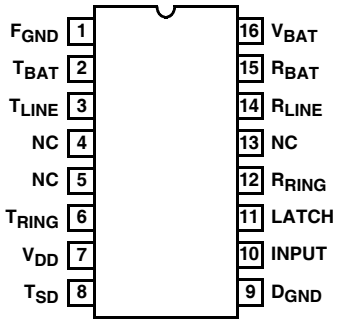
- Central Office
- PBX
- DLC
- HFC
- FITL
- DAML

Related Literature

- Technical Brief TB363 “Guidelines for Handling and Processing Moisture Sensitive Surface Mount Devices (SMDs)”
- Technical Brief TB379 “Thermal Characterization of Packages for ICs”
- Texas Instruments TISPL758LF3D Data Sheet
- Teccor Electronics Document DO-214AA

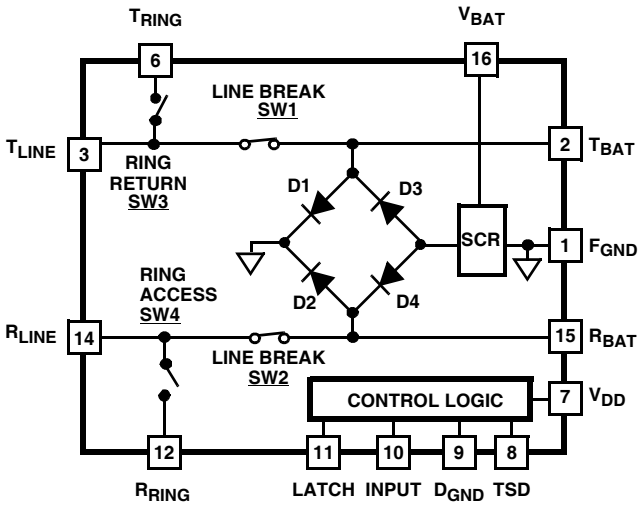
Pinout

ISL5571A
TOP VIEW



Block Diagram

ISL5571A - 16 LEAD SOIC



Absolute Maximum Ratings $T_A = 25°C$

Maximum Supply Voltages
(V_{DD}) . . . . . -0.5V to +7V
(V_{BAT}) . . . . . -19V to -100V
ESD Rating (Human Body Model) 500V

Die Characteristics

Substrate Potential. . . . . V_{BAT}
Process . . . . . .6-inch BIMOS Bonded Wafer

Thermal Information

Thermal Resistance (Typical, Note 1)	θ_{JA} (°C/W)
SOIC	100

Maximum Junction Temperature Plastic . . . . . .150°C
Maximum Storage Temperature Range . . . . . -65°C to 150°C
Maximum Lead Temperature (Soldering 10s) . . . . . .300°C
(SOIC - Lead Tips Only)

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTE:

1. θ_{JA} is measured with the component mounted on a low effective thermal conductivity test board in free air. See Tech Brief TB379 for details.

Electrical Specifications T_A = -40°C to 85°C, Unless Otherwise Specified

TABLE 1. BREAK SWITCHES - ISL5571A - SW1, SW2

PARAMETER	TEST CONDITION	MEASURE	MIN	TYP	MAX	UNITS
OFF-State Leakage Current:						
-40°C	$V_{SWITCH\ (DIFFERENTIAL)}$ = -310V to GND $V_{SWITCH\ (DIFFERENTIAL)}$ = -60V to +250V	I_{SWITCH}	-	-	1	µA
25°C	$V_{SWITCH\ (DIFFERENTIAL)}$ = -320V to GND $V_{SWITCH\ (DIFFERENTIAL)}$ = -60V to +260V	I_{SWITCH}	-	-	1	µA
85°C	$V_{SWITCH\ (DIFFERENTIAL)}$ = -330V to GND $V_{SWITCH\ (DIFFERENTIAL)}$ = -60V to +270V	I_{SWITCH}	-	-	1	µA
ON-Resistance:						
-40°C	T_{LINE} = ±10mA, ±40mA, T_{BAT} = -2V	ΔV_{ON}	-	12	-	Ω
25°C	T_{LINE} = ±10mA, ±40mA, T_{BAT} = -2V	ΔV_{ON}	-	16	-	Ω
85°C	T_{LINE} = ±10mA, ±40mA, T_{BAT} = -2V	ΔV_{ON}	-	-	28	Ω
ON-Resistance Match	Per ON-resistance Test Condition of SW1, SW2	Magnitude r_{ON} SW1 - r_{ON} SW2		0.05	0.5	Ω
ON-State Voltage (Note 2)	Break Switches in ON-State; $I_{switch} = I_{LIMIT}$ at 50/60Hz	V_{ON}	-	-	220	V_{Peak}
DC Current Limit:						
-40°C	$V_{SWITCH\ (ON)}$ = ±10V	I_{SWITCH}	-	-	250	mA
25°C	$V_{SWITCH\ (ON)}$ = ±10V	I_{SWITCH}	-	125	-	mA
85°C	$V_{SWITCH\ (ON)}$ = ±10V	I_{SWITCH}	80	-		mA
Dynamic Current Limit (t = <0.5µs)	Break Switches in ON-state; Ringing Access Switches OFF; Apply ±1000V at 10/1000µs Pulse; Appropriate External Secondary Protection in Place	I_{SWITCH}	-	1.5	2.0	A
Isolation:						
-40°C	V_{SWITCH} (Both Poles) = ±310V Logic Inputs = GND	I_{SWITCH}	-	-	1	µA
25°C	V_{SWITCH} (Both Poles) = ±320V Logic Inputs = GND	I_{SWITCH}	-	-	1	µA
85°C	V_{SWITCH} (Both Poles) = ±330V Logic Inputs = GND	I_{SWITCH}	-	-	1	µA
dV/dt Sensitivity (Note 3)			-	5000	-	V/µs

NOTES:

2. Choice of secondary protection should ensure this rating is not exceeded.
3. Applied voltage is $100V_{P-P}$ square wave at 100Hz.

TABLE 2. RING RETURN SWITCH - ISL5571A - SW3

PARAMETER	TEST CONDITION	MEASURE	MIN	TYP	MAX	UNITS
OFF-State Leakage Current:						
-40°C	$V_{SWITCH\ (DIFFERENTIAL)}$ = -310V to GND $V_{SWITCH\ (DIFFERENTIAL)}$ = -60V to +250V	I_{SWITCH}	-	-	1	µA
25°C	$V_{SWITCH\ (DIFFERENTIAL)}$ = -320V to GND $V_{SWITCH\ (DIFFERENTIAL)}$ = -60V to +260V	I_{SWITCH}	-	-	1	µA
85°C	$V_{SWITCH\ (DIFFERENTIAL)}$ = -330V to GND $V_{SWITCH\ (DIFFERENTIAL)}$ = -60V to +270V	I_{SWITCH}	-	-	1	µA
DC Current Limit						
-40°C	$V_{SWITCH\ (ON)}$	I_{SWITCH}	-	-	350	mA
25°C	$V_{SWITCH\ (ON)}$	I_{SWITCH}	-	200	-	mA
85°C	$V_{SWITCH\ (ON)}$	I_{SWITCH}	120	-	-	mA
Dynamic Current Limit (t = <0.5µs)	Break Switches in OFF-State; Ringing Access Switches ON; Apply ±1000V at 10/1000µs Pulse; Appropriate External Secondary Protection in Place	I_{SWITCH}	-	1.5	2.0	A
ON-Resistance	T_{LINE} = 0, ±10mA	ΔV_{ON}	-	-	100	Ω
ON-State Voltage (Note 4)	Ring Return Switch in ON-State; I_{switch} = I_{LIMIT} at 50/60Hz	V_{ON}	-	-	130	V_{Peak}
Isolation:						
-40°C	V_{SWITCH} (Both Poles) = ±310V Logic Inputs = GND	I_{SWITCH}	-	-	1	µA
25°C	V_{SWITCH} (Both Poles) = ±320V Logic Inputs = GND	I_{SWITCH}	-	-	1	µA
85°C	V_{SWITCH} (Both Poles) = ±330V Logic Inputs = GND	I_{SWITCH}	-	-	1	µA
dV/dt Sensitivity (Note 5)			-	5000	-	V/µs

NOTES:

4. Choice of secondary protection should ensure this rating is not exceeded.
5. Applied voltage is $100V_{P-P}$ square wave at 100Hz.

TABLE 3. RING ACCESS SWITCH - ISL5571A - SW4

PARAMETER	TEST CONDITION	MEASURE	MIN	TYP	MAX	UNITS
OFF-State Leakage Current:						
-40°C	$V_{SWITCH\ (DIFFERENTIAL)}$ = -245V to +210V $V_{SWITCH\ (DIFFERENTIAL)}$ = +245V to -210V	I_{SWITCH}	-	-	1	µA
25°C	$V_{SWITCH\ (DIFFERENTIAL)}$ = -255V to +210V $V_{SWITCH\ (DIFFERENTIAL)}$ = +255V to -210V	I_{SWITCH}	-	-	1	µA
85°C	$V_{SWITCH\ (DIFFERENTIAL)}$ = -270V to +210V $V_{SWITCH\ (DIFFERENTIAL)}$ = +270V to -210V	I_{SWITCH}	-	-	1	µA
ON-Resistance	$I_{SWITCH\ (ON)}$ = ±70mA, ±80mA	ΔV_{ON}	-	-	12	Ω
ON Voltage	I_{SWITCH} (ON) = ±1mA	V_{ON}	-	-	3	V
Ring Access Switch Quiescent Current During Ringing	V_{CC} = 5V, Ring Access Switches On, All Other Switches Off	$I_{RING\ QUIESCENT}$ (Note 6)	-	2.0	-	mA
Steady State Current (Note 7)			-	-	150	mA
Surge Current (Note 7)	Ring Access Switch On, Time Duration = 100µs		-	-	2	A
Release Current			200	-	1000	µA
Isolation:						
-40°C	V_{SWITCH} (Both Poles) = ±310V Logic Inputs = GND	I_{SWITCH}	-	-	1	µA
25°C	V_{SWITCH} (Both Poles) = ±320V Logic Inputs = GND	I_{SWITCH}	-	-	1	µA
85°C	V_{SWITCH} (Both Poles) = ±330V Logic Inputs = GND	I_{SWITCH}	-	-	1	µA
dV/dt Sensitivity (Note 8)			-	5000	-	V/µs

NOTES:

6. Magnitude of the ring generator current not supplied to the ring load. $I_{RING\ QUIESCENT}$= $I_{RING\ GEN}$ - $I_{RING\ LOAD}$.
7. Choice of secondary protector and series current-limit resistor should ensure these ratings are not exceeded.
8. Applied voltage is $100V_{P-P}$ square wave at 100Hz.

TABLE 4. LOGIC I/O ELECTRICAL CHARACTERISTICS - ISL5571A

PARAMETER	TEST CONDITION	MEASURE	MIN	TYP	MAX	UNITS
Digital Input Characteristics:						
Input Low Voltage	-	-	-	-	0.8	V
Input High Voltage	-	-	2.4	-	-	V
Input Leakage Current (High)	V_{DD} = 5.5V, V_{BAT} = -75V, $V_{LOGIC-IN}$ = 5V	$I_{LOGIC-IN}$	-	-	1	µA
Input Leakage Current (Low)	V_{DD} = 5.5V, V_{BAT} = -75V, $V_{LOGIC-IN}$ = 0V	$I_{LOGIC-IN}$	-	-	1	µA

TABLE 5. LOGIC I/O POWER REQUIREMENTS - ISL5571A

PARAMETER	TEST CONDITION	MEASURE	MIN	TYP	MAX	UNITS
Power Requirements:						
Power Dissipation	V_{DD} = 5.5V, V_{BAT} = -48V,					
	Idle/Talk State	I_{DD}, I_{BAT}	-	6.6	8.5	mW
	All OFF-State	I_{DD}, I_{BAT}	-	8.8	11.5	mW
	Ringing State	I_{DD}	-	11.0	18.2	mW
V_{DD} Current	V_{DD} = 5.5V,					
	Idle/Talk State	I_{DD}	-	1.2	2.0	mA
	All OFF-State	I_{DD}	-	1.6	2.1	mA
	Ringing State	I_{DD}	-	2.0	3.3	mA
V_{BAT} Current	V_{BAT} = -48V,					
	Idle/Talk State	I_{BAT}	-	1.0	10	µA
	All OFF-State	I_{BAT}	-	1.0	10	µA
	Ringing State	I_{BAT}	-	1.0	10	µA
Temp. Shutdown Requirements (Note 9)						
Shutdown Activation Temperature		T_J	115	125	135	°C
Shutdown Circuit Hysteresis			7	14	21	°C

NOTE:

9. The Temperature Shutdown logic pin (TSD) will be high during normal operation and low during temperature shutdown state.

TABLE 6. ELECTRICAL SPECIFICATION - PROTECTION CIRCUITRY - ISL5571A

PARAMETER	TEST CONDITION	MEASURE	MIN	TYP	MAX	UNITS
PARAMETERS RELATED TO DIODES						
Voltage Drop at Continuous Current (50Hz/60Hz)	Apply ±DC Current Limit of Break Switches	Forward Voltage	-	-	3	V
Voltage Drop at Surge Current	Apply ±Dynamic Current Limit of Break Switches	Forward Voltage	-	5	-	V
PARAMETERS RELATED TO PROTECTION SCR						
Surge Current	Twice ±Dynamic Current Limit of Break Switches		-	-	4	A
Gate Trigger Current		$-V_{BAT}$ Current	-	50	-	mA
Hold Current			110	-		mA
Gate Trigger Voltage	Trigger Current		V_{BAT} - 4V	-	V_{BAT} - 2V	V
Reverse Leakage Current	V_{BAT}		-	-	1.0	µA
ON-state Voltage (Note 10)	0.5A, t = 0.5µs		-	-3	-	V
	2.0A, t = 0.5µs		-	-5	-	V

NOTES:

10. In some instances, the typical ON-state voltage can range as low as -25V.

TABLE 7. POWER SUPPLY SPECIFICATIONS

SUPPLY	MIN	TYP	MAX	UNITS
V_{DD}	4.5	-	5.5	V
V_{BAT}	-19	-	-72	V

TABLE 8. PIN DESCRIPTIONS - ISL5571A

PIN NO.	PIN NAME	DESCRIPTION	PIN NO.	PIN NAME	DESCRIPTION
1	F_{GND}	Fault Ground. Internally, this pin is electrically isolated from D_{GND}.	16	V_{BAT}	Battery Voltage. Used as a reference for protection circuit. Provides Trigger current for the protection SCR.
2	T_{BAT}	Connect to TIP on SLIC side.	15	R_{BAT}	Connect to RING on SLIC side.
3	T_{LINE}	Connect to TIP on line or phone side.	14	R_{LINE}	Connect to RING on line or phone side.
4	NC	No Connection.	13	NC	No Connection.
5	NC	No Connection.	12	R_{RING}	Connect to ringing generator.
6	T_{RING}	Connect to Return Ground for Ringing Generator.	11	LATCH	Logic State Latch Control, active-high, transparent low.
7	V_{DD}	+5V supply.	10	INPUT	Logic Level Input Switch Control.
8	T_{SD}	Temperature Shutdown Pin. Can be used as a logic level input or output. See Truth Table. As an output, will read +5V when device is in its operational mode and 0V in the thermal shutdown mode. In the ISL5571A, the thermal shutdown mechanism cannot be disabled.	9	D_{GND}	Digital Ground. Internally, this pin is electrically isolated from F_{GND}.

Pinout

ISL5571A
TOP VIEW

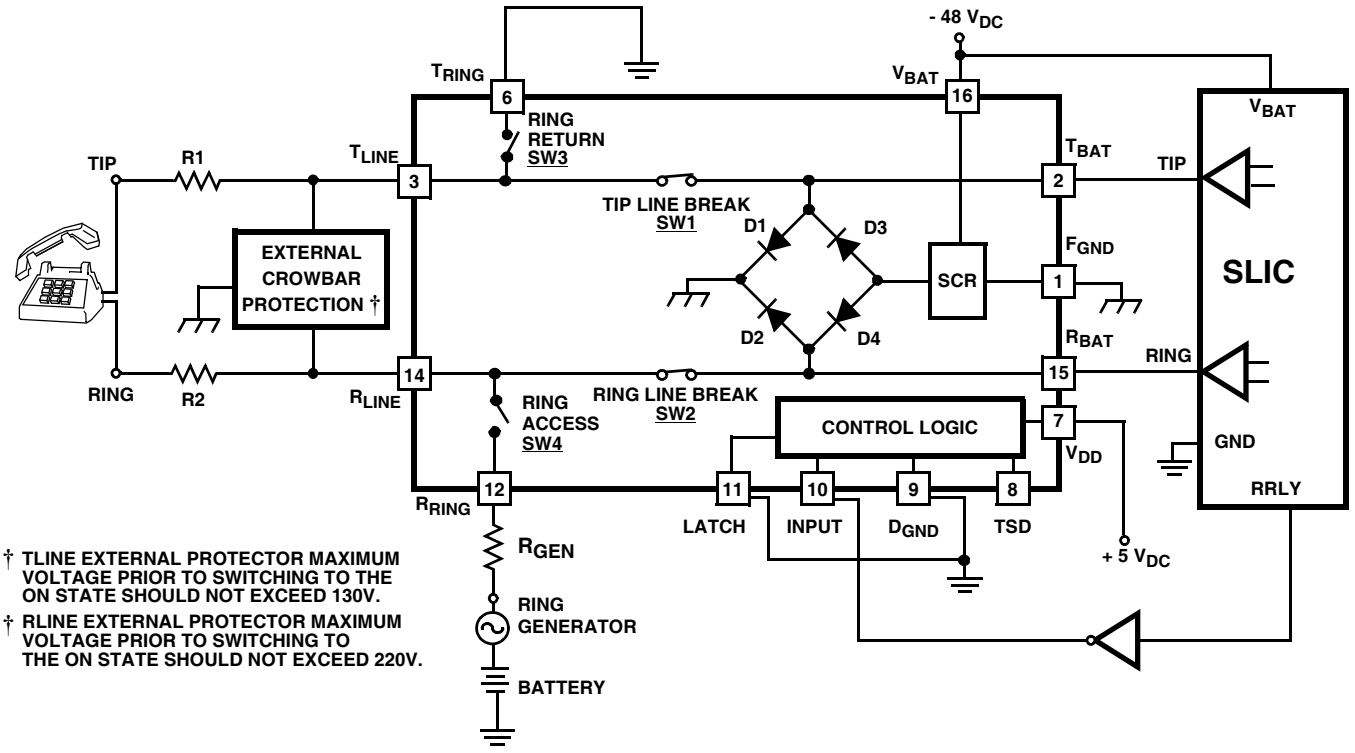


FIGURE 1. APPLICATION CIRCUIT

TABLE 9. TRUTH TABLE - ISL5571A

	LOGIC INPUTS			SWITCH CONDITION			
LOGIC STATE	LATCH	INPUT	T_{SD}	TIP LINE BREAK SWITCH	RING LINE BREAK SWITCH	RINGING RETURN SWITCH	RING ACCESS SWITCH
IDLE / TALK	0	0	1 or Floating (Note 11)	ON	ON	OFF	OFF
POWER RINGING	0	1	1 or Floating (Note 11)	OFF	OFF	ON	ON
IDLE / TALK LATCHED (Note 12)	1	0	1 or Floating (Note 11)	ON	ON	OFF	OFF
POWER RINGING LATCHED (Note 12)	1	1	1 or Floating (Note 11)	OFF	OFF	ON	ON
All OFF	X	X	0 (Note 13)	OFF	OFF	OFF	OFF

NOTES:

11. Thermal shutdown mechanism is active with TSD floating or equal to 5V.
12. If the LATCH pin is low, the logic state of the device is controlled by the INPUT pin. When the LATCH pin goes high, the current logic state is latched. As long as the LATCH pin is held high, the device will no longer respond to any changes applied to the INPUT control pin. The state of the device will be permanently latched until the LATCH pin is taken low.
13. Setting TSD to a logic low overrides the LATCH and INPUT logic pins and forces all switches to turn OFF.

Circuit Operation and Design Information

Introduction

The ISL5571A was designed to be used in subscriber line card applications. A typical application circuit is shown in Figure 1. Its main purpose is to momentarily disconnect the voice circuit (SLIC and CODEC) and connect an external ring generator to ring the phone. This function has been traditionally done by electromechanical relays. The ISL5571A offers the system designer a solid-state switching solution with distinct advantages over the electromechanical relay. These advantages are as follows:

- Lower power consumption (20mW vs. 150mW for the relay)
- Smaller size, surface mounted package
- Bounce-Free switching
- Lower impulse noise, Low EMI
- Longer life
- Provides current limiting, thermal shutdown, and over-voltage protection for the SLIC and CODEC

Their bounce-free operation, long lifetime, small size, and low power consumption make the solid-state access switch the preferred choice over electromechanical relays whenever board area, high reliability, and heat reduction are primary concerns.

The ISL5571A was designed to be a drop in replacement for the Lucent ATTL7581AAE LCAS device. The Intersil ISL5571A offers superior r_{ON} matching between the line break switches for optimal longitudinal balance, higher temperature operation (enabling continuous operation in short loop, high Ringer Equivalency Number applications) and with 3V TTL logic controlled inputs.

Basic Functional Description

This section describes the basic operation of the ISL5571A. From the application circuit shown in Figure 1, the ISL5571A consists of four switches, the Line Break switches (SW1, SW2), the Ring Return switch (SW3), and the Ring Access switch (SW4). The Line Break switches (SW1 and SW2) open and close in unison to connect and disconnect the voice / data signal from the phone. The Ring Access switch and the Ring Return switch (SW3 and SW4) open and close in unison, to connect and disconnect the external ring generator to the phone.

The ISL5571A has three possible operating states: the Idle / Talk state, the Power Ringing state, and the All OFF state. It also has a built in Logic State Latch. The Logic State Latch enables the user to latch the logic state of the ISL5571A in either the Idle / Talk state or the Power Ringing state.

The three control logic pins for the ISL5571A are the INPUT pin, the TSD pin and the LATCH pin. These logic pins are controlled by TTL logic levels (0V - 0.8V for logic low and 2.4V - 5.0V for logic high). The combination of the logic levels applied at these pins determine which of the three logic states the device will be in and whether the Logic State Latch is active. The truth table for the ISL5571A is shown in Table 9. A description of each operating state and the control logic pins follows:

Idle / Talk State (LATCH = 0, INPUT = 0, TSD = 1 or Floating)

In this state the Line Break switches (SW1 and SW2) are closed (on) and the Ring Return and Ring Access switches

(SW3 and SW4) are open (off). The subscriber line circuit is either on-hook or off-hook:

1. In the on-hook condition, the SLIC is monitoring the Tip and Ring lines through the Line Break switches for an off-hook condition. This is called the Idle state.
2. In the off-hook condition, a telephone conversation between two or more parties is in progress or data is being transferred between modems. This is called the Talk state. The SLIC is providing DC power through the Line Break switches to the telephone handset for modulation. Modulated AC voice signals or data are traveling through the Line Break switches SW1 and SW2.

Power Ringing State (LATCH = 0, INPUT = 1, TSD = 1 or Floating)

In this state the Line Break switches (SW1 and SW2) are open (off) and the Ring Return and Ring Access switches (SW3 and SW4) are closed (on). For ring injected ringing as shown in Figure 1, a ring generator is connected to the phone through the Ring Access switch (SW4) and returned to ground through the Ring Return switch (SW3).

All OFF State (LATCH = X, INPUT = X, TSD = 0)

In this state both the Line Access switches (SW1 and SW2) and the Ring Return and Ring Access switches (SW3 and SW4) are open (off). The ISL5571A will enter the All Off state when the following conditions occur:

1. The TSD pin is used as a control input and is programmed to logic low.
2. The device has enter thermal shutdown due to a fault condition. (Thermal Shutdown is described in the Auxiliary Functions and Features section below.)
3. If V_{BAT} rises above -10V or disappears.

While in the All OFF state, communication and power ringing are inoperable because all the ISL5571A switches are open (off).

Logic State Latch (LATCH = 1, TSD = 1 or floating, INPUT = 0 or 1)

A Logic State Latch is Integrated into the ISL5571A, see Figure 2. If the LATCH control pin is high and the TSD pin is high or floating, the device will no longer respond to logic level changes at the INPUT pin. The state of the switches will be determined by the logic level of the INPUT pin at the time the LATCH pin transitions from logic low to logic high. The state of the switches at the time of this transition will be permanently held as long as the LATCH pin is high. When the LATCH pin is taken low the device will again be under the control of the INPUT pin and the switches will immediately go to the state specified by the logic level at the INPUT pin. (Note: The TSD pin overrides the LATCH pin and the INPUT pin. When the TSD pin is low the ISL5571A goes to the ALL OFF state regardless of the logic levels applied at the LATCH pin and the INPUT pin.)

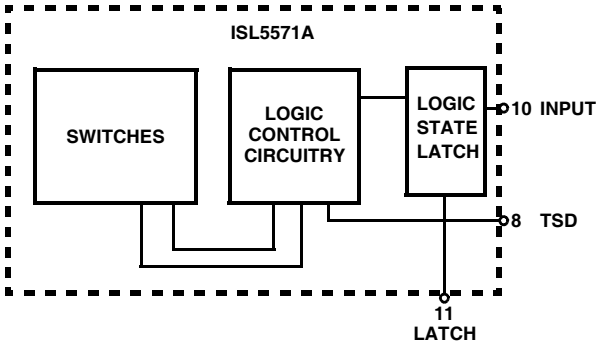


FIGURE 2. BLOCK DIAGRAM OF LOGIC CONTROL

INPUT Pin

The INPUT pin (pin 10) is the main logic input control pin. Reference Table 9 for logic state table. When the LATCH pin is low and the TSD pin is high or floating, you can toggle back and forth between the Idle / Talk state and the Power Ringing state by changing the logic level at the INPUT pin. This is the normal operating mode of the device.

NOTE: If the LATCH pin is high, the INPUT pin is no longer active and the device will no longer respond to logic changes at the INPUT pin.

The TSD pin overrides all other logic pins. If the TSD pin is low, the device will enter an All OFF state and will no longer respond to logic changes at the INPUT pin.

Latch Pin

The LATCH pin (pin 11) is the control for the Logic State Latch. Reference Table 9 for logic state table. When the LATCH pin is low, the latch is disabled and the state of the ISL5571A will be determined by the logic level applied at the other logic inputs.

When the LATCH pin is high, the latch is active and the logic state of the switches at the time the LATCH pin went high will be latched. As long as the LATCH pin is held high the switches will not respond to logic changes at the INPUT control pin.

TSD Pin

The TSD pin (pin 8) can be used as a logic level input or output. Reference Table 9 for logic state table. The TSD pin overrides all other logic pins.

As an input, if this pin is driven low, either by external logic applied to it or by the internal thermal shutdown circuitry, the ISL5571A device will enter the All OFF state. In the All OFF state all switches of the ISL5571A are open (off).

As an output, it is capable of driving a TTL input (2.8V at 200µA). The TSD pin will read +5V when the device is in normal operating mode and 0V when the device is in thermal shutdown. This pin can be monitored on an oscilloscope to determine if the ISL5571A device has enter thermal shutdown. (Thermal Shutdown is described in the Auxiliary Functions and Features section below.)

Connecting the TSD pin to 5V will have no effect on the performance of the ISL5571A device and will not disable the thermal shutdown circuitry.

Auxiliary Functions and Features

In addition to the ISL5571A main function of momentarily connecting and disconnecting an external ring generator to ring the phone, the ISL5571A device also provides surge and power-cross protection to the SLIC and CODEC. This fault protection is provided by a combination of current-limiting circuitry, a thermal shutdown mechanism and an over-voltage clamping circuit. Another feature the device offers is a V_{BAT} fault detection circuit. The following describes each in detail.

Current Limiting

The Line Break switches (SW1 and SW2) and the Ring Return switch (SW3) are all current-limited. These switches have a DC current limiting response and a dynamic current limiting response which were built into the device to provide protection during lightning and power-cross faults. Each of these current limiting responses are explained below.

DC CURRENT LIMITING RESPONSE

The ON state V-I Graph for SW1, SW2, and SW3 is shown in Figure 3. It represents the DC current limiting response of the switches. The graph shows that over a certain range of positive and negative voltages, the current and voltage relationship is linear and behaves according to Ohms law (V = IR). Note: At around ±1.5V an inflection point occurs decreasing the on resistance by 2/3. The on resistance specified in the data sheet is measured in the region prior to the inflection point (between ±1.5V).

When current through the switch reaches the current limit of the switch, the current is clamped and held at a constant value. The switch then operates as a constant current source. Increasing the voltage beyond this point will not change the value of the current.

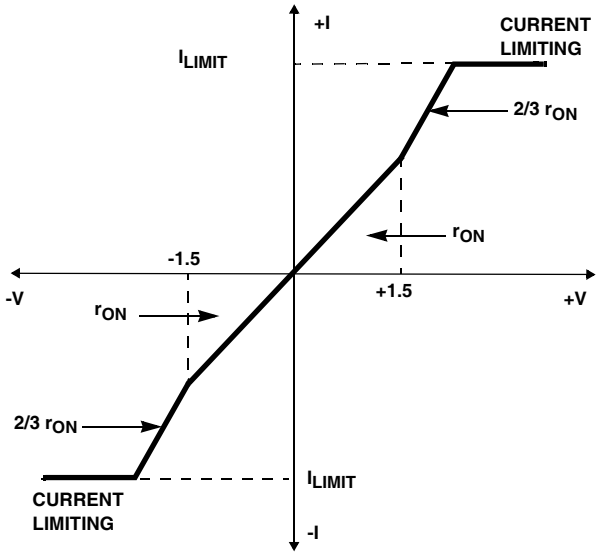


FIGURE 3. ON STATE V-I GRAPH OF SW1, SW2 AND SW3

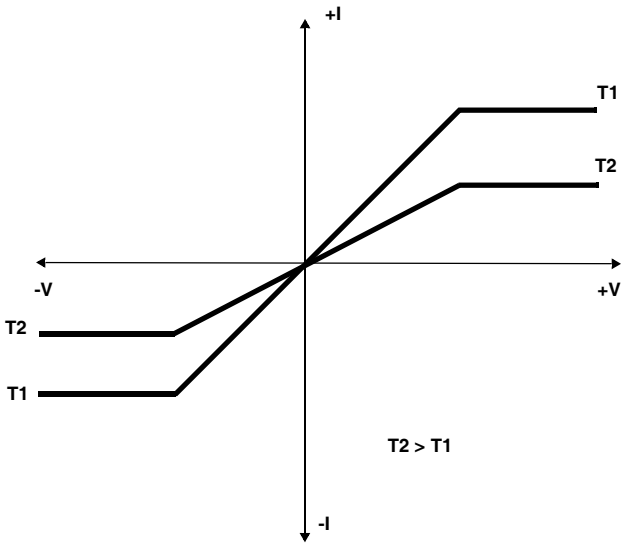


FIGURE 4. EFFECT OF TEMPERATURE ON DC CURRENT LIMIT

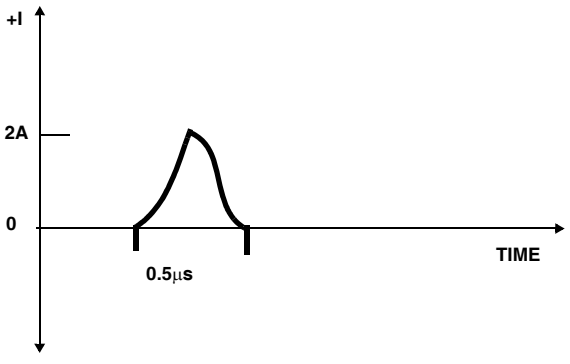


FIGURE 5. DYNAMIC CURRENT LIMIT RESPONSE

The DC current limiting response has a negative temperature coefficient. As the temperature of the device increases the DC current limit of the switch will decrease. This is illustrated in Figure 4.

Figure 4 shows the V-I curves of a switch at two different die temperatures, T1 and T2. In this illustration T2 is greater in temperature than T1. This shows that when a switch is driven into current limit and held there, the current limit will decrease over time as the switch temperature increases. If the power through the switch is great enough, the temperature of the switch will continue to increase until the switch goes into thermal shutdown (Thermal Shutdown is described below).

Dynamic Current Limiting Response

The DC current limit response described above pertains to DC and AC voltage sources applied across the switches. The dynamic response is the response of the current limit circuit to a fast or high dv/dt pulse. The dynamic response would be seen, for example, during a lightning surge

Figure 5 shows the dynamic response that is observed when SW1, SW2 or SW3 is surged with a 1000V at 10/1000µs telecom surge pulse. (Note: This surge test is done with the switch in the on state and with the appropriate external secondary protection in place.) The dynamic current limit of SW1, SW2 or SW3 will limit the current through the switch to less than 2.0A for 0.5µs as shown in Figure 5. Once the switch has turned off, the voltage at the T_{Line} and R_{Line} terminals will increase to a point where the external secondary protection device will trigger and crowbar the voltage at T_{Line} and R_{Line} to a low voltage, protecting the ISL5571A against damage.

Since the Line Break switches (SW1, SW2) have this dynamic current limit feature, the internal over-voltage protection clamping circuit of the ISL5571A device will need to only protect the SLIC against a 2.0A ≤0.5µs pulse during a lightning surge.

Thermal Shutdown (TSD)

The ISL5571A has a built in thermal shutdown protection circuit. The thermal shutdown protection mechanism is invoked if a fault condition causes the junction temperature of the die to exceed about 150°C. Once the thermal limit is exceeded the thermal shutdown circuitry will force the switches into an All OFF state, regardless of the logic inputs. While in thermal shutdown the TSD logic pin (pin 11) will be driven low by the thermal shutdown circuit. (Note: During normal operation the TSD pin is high.) The thermal shutdown mechanism was designed to have a thermal hysteresis of about 12°C. Once in thermal shutdown the device will begin to cool down, because all the switches are off and no current flows. When the temperature of the die cools to about 138°C the ISL5571A will cycle out of thermal shutdown and the switches will close again. If the fault condition is still present, the temperature of the die will again increase and this cycle will be repeated.

Over Voltage Protection Clamping Circuit

The ISL5571A contains an over-voltage clamping circuit on the SLIC side of the Line Break switches, see Figure 1. This clamping circuit consists of a diode bridge and SCR. During lightning surges and power-cross fault conditions this circuit will clamp the voltage at the T_{BAT} and R_{BAT} terminals of the SLIC to a safe level and will shunt harmful currents to ground away from the SLIC.

The clamping circuit is externally connected to ground through the F_{GND} pin (pin 1) of the device. The battery voltage of the SLIC is connected to the clamping circuit through the V_{BAT} pin (pin 16) of the device. The operation of diode bridge and the SCR circuit is described below.

DIODE BRIDGE WITH SCR (ISL5571A)

During a positive lightning surge or during the positive cycle of a power-cross / induction fault, the voltage at the T_{BAT} and R_{BAT} terminals of the SLIC will be clamped to a diode drop above ground. The fault current will flow harmlessly through diodes D1 and D2 of the diode bridge to ground (see Figure 1).

During a negative lightning surge or during the negative cycle of a power-cross / induction fault when the voltage at the T_{BAT} and R_{BAT} terminals reach 2V to 4V more negative than the V_{BAT} voltage, the protection SCR will trigger and turn on. When the SCR turns on and latches, it will crowbar the voltage at the T_{BAT} and R_{BAT} lines to a low-voltage state, approximately 3 diode drops below ground. This low-voltage on state will cause the current resulting from the over voltage to be safely direct to ground through diodes D3 and D4 of the diode bridge and the SCR (see Figure 1). Once the fault current decrease below the protection SCR holding current (110mA) the SCR will turn off and the SLIC will be able to return to normal operation.

V_{BAT} Fault Circuit Protection - Loss of Battery Voltage

The ISL5571A device contains a V_{BAT} fault circuit which monitors the SLIC battery voltage (V_{BAT}). When this circuit detects that the V_{BAT} voltage has risen above -10V, it will cause the ISL5571A to enter the All OFF state. All the switches will remain off (open) until the circuit detects that the SLIC battery voltage has dropped below -15V.

Design Considerations

External Protection

Subscriber line card circuits using the ISL5571A require the use of an external protection circuit on the loop side or phone side of the device, see Figure 1. This protection is required to minimize the power stress on the ISL5571A during overvoltage and overcurrent conditions. When the proper external protection circuitry is used in conjunction with the integrated secondary protection, features offered by the ISL5571A, the

application circuit will pass the AC power-cross and lightning immunity tests of the following regulatory requirements:

- GR 1089-CORE
- ITU-T K.20

This section will discuss the issues that must be considered when designing an external protection circuit for use with the ISL5571A.

The external protection circuitry should be designed to limit the peak voltages on the T_{Line} and R_{Line} terminals of the ISL5571A. The most potentially stressful condition concerning the ISL5571A is low level power-cross when the ISL5571A switches are closed. Under this condition, the external protection circuitry limits the voltage and corresponding power dissipation until the ISL5571A thermal shutdown circuitry opens the switches.

The external protector chosen for the T_{Line} terminal must limit at a maximum of 130V thereby limiting the power stress on the Ring Return switch (SW3).

The protector chosen for the R_{Line} terminal must limit at a maximum of 220V thereby limiting the power stress on the Line Break switch (SW2). The 220V break-over voltage of the protector on RLine is large enough to not interfere with the AC ring signal during ringing.

Texas Instruments and Teccor Electronics have designed specific parts to protect solid state line card access switches. The following protectors are recommended:

Texas Instruments Part Number TISPL758LF3D(T_{Line} and R_{Line})

Teccor Electronics Part Number P1200SC (T_{Line}) and P2000SC (R_{Line})

Refer to the above company's data sheets for information on their parts and reference designs for protection of solid state line card access switches, see Related Literature section on Page One.

Break-Before-Make Operation

The ISL5571A device inherently has a Break-before-Make condition between the following switches:

a. Between the Line Break switch SW1 and the Ring Return switch SW3 during the transition from the Idle state to the Power Ringing state.

b. Between the Line Break switch SW2 and the Ring Access switch SW4 during the transition from the Idle state to the Power Ringing state.

Make-Before-Break Operation

The ISL5571A device could exhibit a Make-before-Break condition between the Line Break switch SW2 and the Ring Access switch SW4 during the transition from the Power Ringing state to the Idle / Talk state. There is a period of time that can be as much as 25ms (1/2 cycle of the 20Hz ring signal) when both SW2 and SW4 will both be on (closed). This occurs because SW4 is an SCR and requires a zero current crossing to turn off.

Protection SRC Latch-Up

In the Make-before-Break condition, when transiting from the Power Ringing state to the Idle/ Talk state, during the negative cycle of the ring generator it is possible for enough current to flow that the protection SCR will turn on. This will result in shorting the ring generator and the Ring terminal of the SLIC to ground. When either SW2 or SW4 turns off, the Ring terminal of the SLIC will remain shorted to ground unless the output current limit of the SLIC is less than the holding current (110mA) of the protection SCR. The current limit of most SLICs are set well below the 110mA minimum holding current of the ISL5571A protection SCR and therefore should not be a concern. Another method to prevent latch-up of the protection SCR would be to strobe the TSD pin of the ISL5571A. as discussed in Break-Before-Make section.

Ring Access Switch Quiescent Current During Ringing

The Ring Access switch (SW4) is a silicon control rectifier type switch (SCR). During power ringing, the Ring Access switch will draw a nominal 2mA of current from the ring generator. This current is called $I_{RING\ QUIESCENT}$ and is equal to:

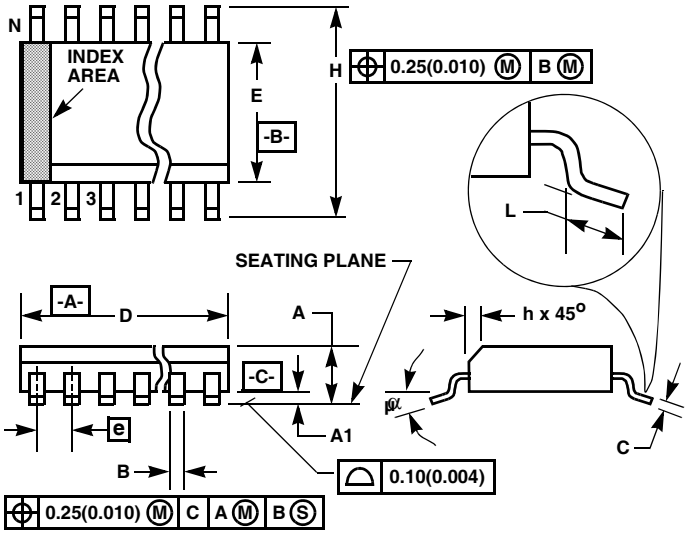
$$I_{RING\ QUIESCENT} = I_{RING\ GEN} - I_{RING\ LOAD}.$$

System designers need to ensure that this additional current can be provided by the ring generator.

Glossary of Acronyms

AC = Alternating Current
BIMOS = Bipolar Metal-Oxide Semiconductor
CO = Central Office
CODEC = CODer-DECoder
DC = Direct Current
DLC = Digital Loop Carrier
DAML = Digitally Added Main Line
EMI = Electromagnetic Interference
ESD = Electrostatic Discharge
FITL = Fiber in the Loop
HFC = Hybrid Fiber Coax
ICs = Integrated Circuits
LCAS = Line Card Access Switch
PBX = Private Branch Exchange
REN = Ring Equivalency Number
MOSFET = Metal-Oxide Semiconductor Field-Effect Transistor
SCR = Silicon Control Rectifier
SLIC = Subscriber Line Interface Circuit
SMDs = Surface Mount Devices
SOIC = Small Outline Integrated Circuit
TSD = Thermal ShutDown
TTL = Transistor-Transistor Logic

Small Outline Plastic Packages (SOIC)



M16.3 (JEDEC MS-013-AA ISSUE C)
16 LEAD WIDE BODY SMALL OUTLINE PLASTIC PACKAGE

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	0.0926	0.1043	2.35	2.65	-
A1	0.0040	0.0118	0.10	0.30	-
B	0.013	0.0200	0.33	0.51	9
C	0.0091	0.0125	0.23	0.32	-
D	0.3977	0.4133	10.10	10.50	3
E	0.2914	0.2992	7.40	7.60	4
e	0.050 BSC		1.27 BSC		-
H	0.394	0.419	10.00	10.65	-
h	0.010	0.029	0.25	0.75	5
L	0.016	0.050	0.40	1.27	6
N	16		16		7
α	0^o	8^o	0^o	8^o	-

Rev. 0 12/93

NOTES:

1. Symbols are defined in the “MO Series Symbol List” in Section 2.2 of Publication Number 95.
2. Dimensioning and tolerancing per ANSI Y14.5M-1982.
3. Dimension “D” does not include mold flash, protrusions or gate burrs. Mold flash, protrusion and gate burrs shall not exceed 0.15mm (0.006 inch) per side.
4. Dimension “E” does not include interlead flash or protrusions. Interlead flash and protrusions shall not exceed 0.25mm (0.010 inch) per side.
5. The chamfer on the body is optional. If it is not present, a visual index feature must be located within the crosshatched area.
6. “L” is the length of terminal for soldering to a substrate.
7. “N” is the number of terminal positions.
8. Terminal numbers are shown for reference only.
9. The lead width “B”, as measured 0.36mm (0.014 inch) or greater above the seating plane, shall not exceed a maximum value of 0.61mm (0.024 inch)
10. Controlling dimension: MILLIMETER. Converted inch dimensions are not necessarily exact.