ISL58792

Laser Diode Driver with Serial Control and Write Current DAC

FN7580
Rev 3.00
December 14, 2015

The ISL58792 is a highly integrated, single supply laser diode driver designed to support multi-standard writable optical drives in CD, DVD, and Blu-Ray formats at various speeds. It is a 'hybrid' part having an interface compatible with a conventional LDD, but an internal architecture similar to a write strategy LDD. This combination adds versatility to the conventional interface.

The rise time, fall time and overshoot of all outputs are adjustable to compensate for high and low resistance lasers.

The ISL58792 architecture includes dual write current banks, which can be selected using the bank select line, BSEL. This eliminates the need to synchronize the serial port to the media.

The oscillator is internally activated through program assignment to attach to any WEN state.

The WEN lines have internal 100Ω terminators. There is a skew detector on the WEN receiver outputs.

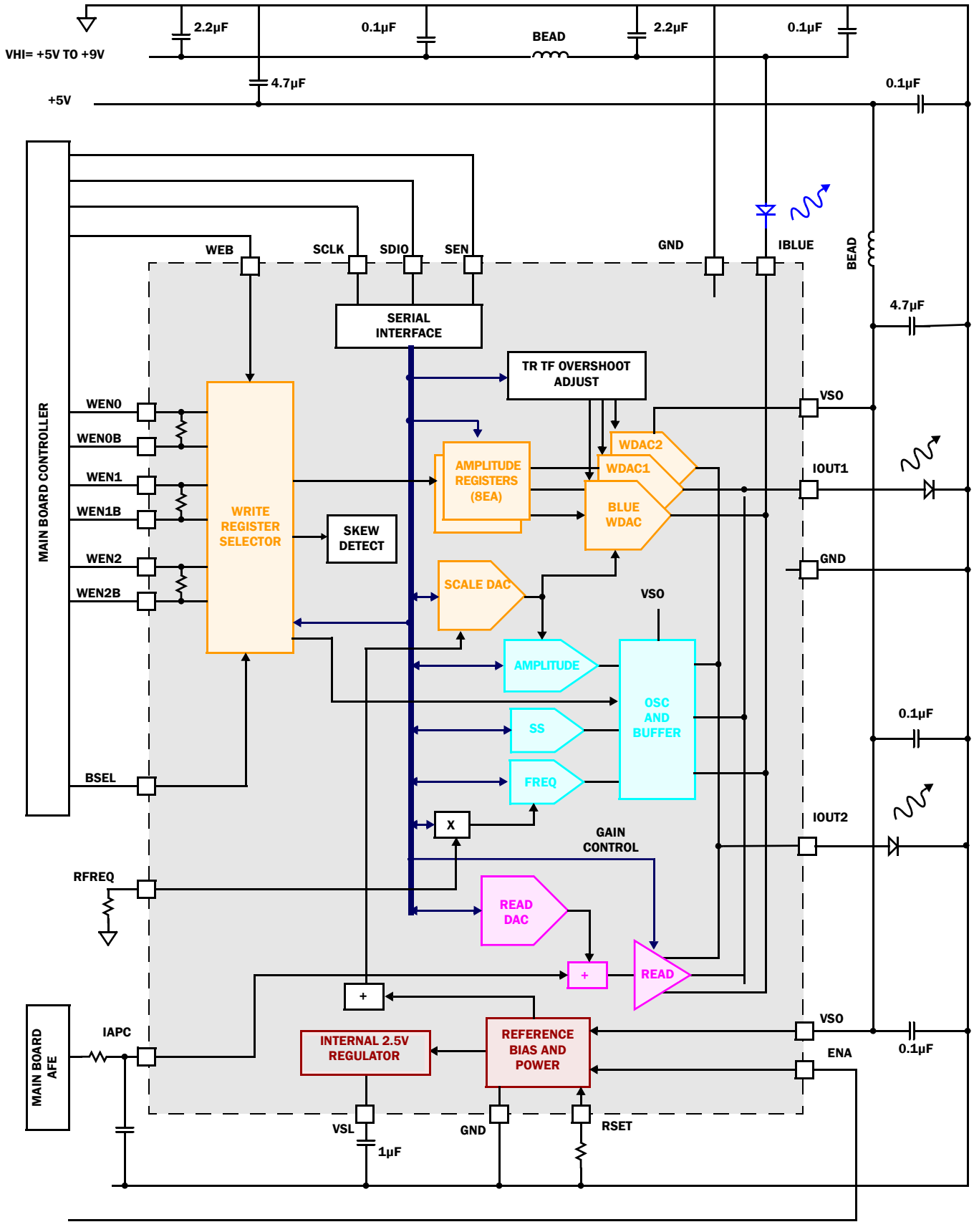
Applications

- Combination DVD, CD, and Blue Writable Drives
- BD Camcorders
- BD Video Recorders

Features

- Compatible with all Conventional Controllers Having a Serial Port, with Some Programming
- Programmable Snubber on all Outputs
- Compatible with Future Controllers Having Gray Coded WEN Lines for Glitchless High-Speed Operation
- WEN Line Skew Detection
- 1000mA Maximum Total Write Output Current.
- 10-bit x 10-bit Multiplying DAC Output Provides 10-bit Full Scale Adjustment and 10-bit Resolution at any Full Scale Output
- Three Laser Outputs Allow Read/Write DVD, CD, and Blue Combinations
- Single +5V Supply
- Analog Inputs Supports Read APC
- HFM Oscillator Programmable to $100mA_{P-P}$ and Range from 100MHz to >1GHz
- Programmable HFM On, Off and Cooling Levels
- Programmable Spread Spectrum for Low EMI
- Built-in ADC to Sample Laser Voltage Allows Power Reduction by Optimizing Headroom
- Built-in Thermal Sensor Aids in Thermal Design
- Serial Input Works up to 50MHz
- Pb-Free (RoHS Compliant)

Application Block Diagram



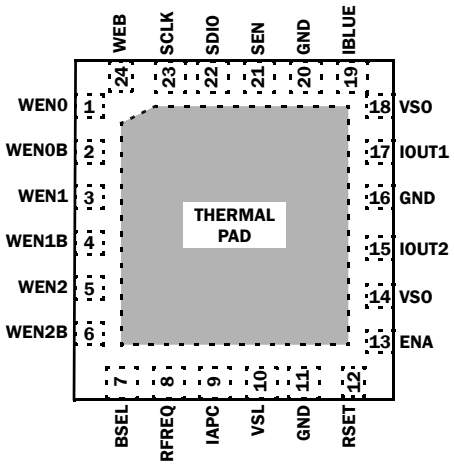
Ordering Information

PART NUMBER (Note 2)	PART MARKING	TEMP RANGE (°C)	PACKAGE Tape & Reel (Pb-free)	PKG. DWG.#
ISL58792CRTZ	587 92CRTZ	-10 to +85	24 Ld TQFN	L24.4x4E
ISL58792CRTZ-T13 (Note 1)	587 92CRTZ	-10 to +85	24 Ld TQFN	L24.4x4E
ISL58792CRTZ-T7A (Note 1)	587 92CRTZ	-10 to +85	24 Ld TQFN	L24.4x4E

1. Please refer to TB347 for details on reel specifications.
2. These Intersil Pb-free plastic packaged products employ special Pb-free material sets, molding compounds/die attach materials, and 100% matte tin plate plus anneal (e3 termination finish, which is RoHS compliant and compatible with both SnPb and Pb-free soldering operations). Intersil Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020.

Pin Configuration

ISL58792
(24 LD TQFN)
TOP VIEW



Pin Descriptions

PIN NAME	PIN NUMBER	I/O	PIN TYPE	PIN DESCRIPTION
WEN0, WEN0B	1, 2	I	LVDS	Write Enable 0. When WEN0 > WEN0B, the result is a logic 1 in the write current selection. Otherwise it is logic 0.
WEN1, WEN1B	3, 4	I	LVDS	Write Enable 1. When WEN1 > WEN1B, the result is a logic 1 in the write current selection. Otherwise it is logic 0.
WEN2, WEN2B	5, 6	I	LVDS	Write Enable 2. When WEN2 > WEN2B, the result is a logic 1 in the write current selection. Otherwise it is logic 0.
BSEL	7	I	Digital	Bank Select input selects the write current register banks.
RFREQ	8	I/O	Analog	A resistor from RFREQ to GND sets the range of the HFM frequency.
IAPC	9	I	Analog	A 1kΩ impedance current input; 100*IAPC flows to the output. This controls the read current, which may also include a current from an internal DAC.
VSL	10	O	Power	The internal 2.5V regulator; a 1µF capacitor from VSL to GND is recommended. Do not use VSL for other loads.
GND	11, 16, 20		Ground	Ground
RSET	12	I/O	Analog	A resistor from RSET to analog ground sets the DAC full-scale current.

Pin Descriptions (Continued)

PIN NAME	PIN NUMBER	I/O	PIN TYPE	PIN DESCRIPTION
ENA	13	I	Digital	Chip enable input (H = enable, L = disable)
VSO	14, 18		Power	Supply voltage. (connect all pins)
IOUT2	15	O	Analog	Laser diode output #2
IOUT1	17	O	Analog	Laser diode output #1
IBLUE	19	O	Analog	Blue laser diode output
SEN	21	I	Digital	Serial control enable (H = enable, L = disable)
SDIO	22	I/O	Digital	Serial data for parameters and control; in/out
SCLK	23	I	Digital	Serial control clock
WEB	24	I	Digital	Write enable Bar. When low, write current is enabled.
PD			Thermal	The Thermal pad should be grounded and connected to a heat sink.

NOTE: Pins with the same name are internally connected together; however, LDD pins must not be used for connecting together external components or features.

Absolute Maximum Ratings (T_A = +25°C)

V_{SO}, Supply Voltage 6V
I_{BLUE}, Voltage at I_{BLUE} 7V
$I_{OUT1,2}$, Output Current 1000mApk
I_{BLUE}, Output Current 600mApk
V_{IN}, Logic Input Voltages . . . . . -0.5V to V_{SO} + 0.5V
I_{IN}, Current into R_{SET}, R_{FREQ}, I_{APC} 5mA
ESD Rating
Human Body Model (Tested per JESD22-A114F) 1500V
Machine Model (Tested per JESDD22 A115B). 100V
Charge Device Model (Tested per JESDD22-C101D). 1500V
Latch-up. . . . . 100mA @+125°C

Thermal Information

Thermal Resistance (Typical)	θ_{JA} (°C/W)	θ_{JC} (°C/W)
24 Lead TQFN (Notes 3, 4)	42	5.4

P_D, Maximum Power Dissipation . . . . . see Figure 12 on page 13
T_S, Storage Temperature Range. . . . . -60°C to +150°C
Pb-Free Reflow Profile . . . . . see link below
http://www.intersil.com/pbfree/Pb-FreeReflow.asp

Operating Conditions

T_A, Ambient Temperature Range . . . . . -10°C to +85°C
T_J, Junction Temperature Range. . . . . -10°C to +150°C

CAUTION: Do not operate at or near the maximum ratings listed for extended periods of time. Exposure to such conditions may adversely impact product reliability and result in failures not covered by warranty.

NOTES:

3. θ_{JA} is measured in free air with the component mounted on a high effective thermal conductivity test board with "direct attach" features. See Tech Brief TB379.
4. For θ_{JC}, the "case temp" location is the center of the exposed metal pad on the package underside.

IMPORTANT NOTE: All parameters having Min/Max specifications are guaranteed. Typical values are for information purposes only. Unless otherwise noted, all tests are at the specified temperature and are pulsed tests, therefore: $T_J = T_C = T_A$

Standard Conditions Unless otherwise indicated, all of the following tables are: $V_{SO} = V_{HI}$ = 5V, R_{SET} = 620Ω, R_{FREQ} = 4.7kΩ, $R_{LOAD-IOUT1/2}$ = 8Ω to GND, $R_{LOAD-BLUE}$ = 10Ω to V_{HI}, PMAX = 0x3FF, Reg 1-21 = 88h, Reg x-00 bit6 = 0, T_A = +25°C.

Electrical Specifications Standard conditions apply unless otherwise noted.

PARAMETER	DESCRIPTION	MIN (Note 13)	TYP	MAX (Note 13)	UNIT
DC ELECTRICAL SPECIFICATIONS					
V_{SO}	(Notes 5, 6)	4.5		5.7	V
V_{IBLUE}	IBLUE pin; R_{LOAD} = 10Ω			7.0	V
I_{VSO}	Supply Current (No Current Output)		19	30	mA
I_S, $dis_{(nom)}$	Supply Current, Disable Mode		17	100	µA
I_S, $dis_{(high)}$	Supply Current; VSO = 5.5V, Disable Mode		25	100	µA
$I_{BLUE-LEAK1}$	V_{IBLUE} = 7.0V; I_{BLUE} is Selected; CE = OE = 1; Reg1-21 = 00h		150	300	µA
$I_{BLUE-LEAK2}$	V_{IBLUE} = 7.0V; I_{BLUE} is Selected; CE = OE = 1; I_{APC} pin voltage = 0V			80	µA
$I_{BLUE-LEAK3}$	V_{IBLUE} = 7.0V; I_{BLUE} is not Selected; CE = OE = 1		1.1	1.6	mA
V_{IH}	Input Logic High Level	2.0			V
V_{IL}	Input Logic Low Level			0.8	V
V_{OH}	SDIO High Level, I_L = -5mA	2.4			V
V_{OL}	SDIO Low Level, I_L = 5mA			0.4	V
I_{INH}	Logic Input Current High Level	-15		+15	µA
I_{INL}	Logic Input Current Low Level	-15		+10	µA

NOTES:

5. Required voltage at the device pins. Allowance must be made for any voltage drop between the power supply and the device.
6. Required voltage also depends on laser diode manufacturer and pickup optical efficiency. Also, see R_{OUT} spec of WDAC.

PMAX DAC (10-bit) DC Specifications Standard conditions apply unless otherwise noted.

PARAMETER	DESCRIPTION	CONDITIONS	MIN (Note 13)	TYP	MAX (Note 13)	UNIT
DNL-PMAX	Differential Non-Linearity	(Note 7)	-3.5		+3.5	LSB
INL-PMAX	Integral Non-Linearity	At 200h Resistive Load ~0V to ~3V		+40		LSB
ZS-PMAX	Zero-Scale Error	(Note 8)	-2	0	+2	LSB
V_{RSET}	RSET Pin Voltage		1.03	1.06	1.11	V

NOTES:

7. Differential non-linearity (DNL) is the differential between the measured and ideal 1 LSB change of any two adjacent codes.
8. Zero-scale error (ZS) is the deviation from zero current output when the digital input code is zero.

IOUT1/2 Write Power DAC (10-bit) DC Specifications Standard conditions apply unless otherwise noted.

PARAMETER	DESCRIPTION	CONDITIONS	MIN (Note 13)	TYP	MAX (Note 13)	UNIT
DNL-W	Differential Non-Linearity		-1.7		+1.0	LSB
INL-W	Integral Non-Linearity	At 200h Resistive Load ~0V to ~3V		+21		LSB
FS_{OUT}-W620	Write DAC Full-Scale Output Current R_{SET} = 620Ω	WriteDAC = 0x3FF. Headroom depends on I_{OUT}	475	525		mA
FS_{OUT}-H1.1	Write DAC Full-Scale Output Current	WriteDAC = 0x3FF, Fixed Headroom = 1.1V	700	800	875	mA
$PSRR_{-FS}$	Power Supply Rejection - Full-Scale Current	vs V_{SO} (Note 9)		-30		dB
$TC_{-FS-IOUT}$	Temperature Coefficient - Full-Scale Current	(Note 10) 0°C to +85°C		-32		ppm/°C
ZS-W	Zero-scale Error	(Note 11)	-2	0	+2	LSB
R_{OUT}-WDAC	Write DAC Output Series Resistance	WriteDAC = PMAX = 0x3FF PMAX bias overdriven (Note 12)		1.1	1.4	Ω

NOTES:

9. Full scale output current power supply sensitivity (SFS) is measured by varying the V_{SO} from 4.5V to 5.5V DC and measuring the effect of this signal on the full-scale output current.
10. Full scale output current temperature coefficient (TFS) is given by delta (full scale output current)/Δ(T).
11. Zero-scale error (ZS) is the deviation from zero current output when the digital input code is zero.
12. PMAX bias overdriven via R_{SET}.
13. Compliance to datasheet limits is assured by one or more methods: production test, characterization and/or design.

IBLUE Write Power DAC (10-bit) DC Specifications Standard conditions apply unless otherwise noted.

PARAMETER	DESCRIPTION	CONDITIONS	MIN (Note 13)	TYP	MAX (Note 13)	UNIT
DNL-W	Differential Non-Linearity		-4.9		+2.0	LSB
INL-W	Integral Non-Linearity	At fixed 2.5V headroom		+60		LSB
FS_{OUT}-H2.0	Write DAC Full-Scale Output Current R_{SET} = 620Ω	WriteDAC = 0x3FF; Fixed Headroom = 2.0V; Reg 1-21 = 8F	380	450	575	mA
TR_{RANGE}	Tr Tf Adjustment Range	Reg 1-0A from X0h to X7h		1		ns
$PSRR_{-FS}$	Power Supply Rejection - Full-Scale Current	vs V_{SO} (Note 14)		-40		dB
$TC_{FS-IBLUE}$	Temperature Coefficient - Full-Scale Current	(Note 15)		600		ppm/°C
ZS-W	Zero-Scale Error	V_{IOUT} = 2V (Note 16)	-8	0	+8	LSB
R_{OUT}-WDAC	Write DAC Output Series Resistance	WriteDAC = PMAX = 0x3FF PMAX bias overdriven (Note 17)		3.4	4.5	Ω

NOTES:

14. Full scale output current power supply sensitivity (SFS) is measured by varying the V_{SO} from 4.5V to 5.5V DC and measuring the effect of this signal on the full-scale output current.
15. Full scale output current temperature coefficient (TFS) is given by delta (full scale output current)/Δ(T).
16. Zero-scale error (ZS) is the deviation from zero current output when the digital input code is zero.
17. PMAX bias overdriven via R_{SET}.

IBLUE Read APC Amplifier DC Specifications Standard conditions apply unless otherwise noted.

PARAMETER	DESCRIPTION	CONDITIONS	MIN (Note 13)	TYP	MAX (Note 13)	UNIT
$IAPC_{MIN-GAIN}$	Current Gain @ Min Gain	Reg1-21h = 1X, I_{APC} = 0µA, 500µA	8	15	25	mA/mA
$IAPC_{MAX-GAIN}$	Current Gain @ Max Gain	Reg1-21h = FX, I_{APC} = 0µA, 500µA	195	250	295	mA/mA
$IAPC_{GAIN}$	Current Gain	I_{APC} = 0µA, 500µA	95	135	175	mA/mA
$IAPC_{OS}$	Current Offset	I_{APC} = 0µA	-2	1	3	mA
LIN_{APC}	Output Current Linearity; Best Fit	I_{APC} = 0µA, 500µA, 1.0mA	-12		1	%
I_{OUT}-R-APC	Blue Read Output Current, Using I_{APC} Input	I_{APC} = 1.5mA	150			mA
R_{IN}	I_{APC} Input Impedance to GND		700	950	1200	Ω
$PSRR_{APC}$	I_{APC} Current Power Supply Rejection	$I_{OUT-average}$ = 100mA, varying V_{SO}		-46		dB

OUT1/2 Read APC Amplifier DC Specifications Standard conditions apply unless otherwise noted.

PARAMETER	DESCRIPTION	CONDITIONS	MIN (Note 13)	TYP	MAX (Note 13)	UNIT
$IAPC_{MIN-GAIN}$	Current Gain @ Min Gain	Reg1-21h = 1X, I_{APC} = 0µA, 500µA	11	14.5	19	mA/mA
$IAPC_{MAX-GAIN}$	Current Gain @ Max Gain	Reg1-21h = FX, I_{APC} = 0µA, 500µA	155	173	200	mA/mA
$IAPC_{GAIN}$	Current Gain	I_{APC} = 0µA, 500µA	85	100	115	mA/mA
$IAPC_{OS}$	Current Offset	I_{APC} = 0µA	-2	1	3	mA
LIN_{APC}	Output Current Linearity; Best Fit	I_{APC} = 0µA, 500µA, 1.0mA	-1		6	%
I_{OUT}-R-APC	Read Output Current, Using I_{APC} Input	I_{APC} = 1.5mA	120			mA
R_{IN}	I_{APC} Input Impedance to GND		700	950	1200	Ω
$PSRR_{APC}$	I_{APC} Current Power Supply Rejection	I_{APC-IN} = 0.45mA, varying V_{SO}		-48		dB

Read DAC (12-bit) DC Specifications Standard conditions apply unless otherwise noted.

PARAMETER	DESCRIPTION	CONDITIONS	MIN (Note 13)	TYP	MAX (Note 13)	UNIT
DNL-R	Read DAC Differential Non-Linearity	PREAD: Reg 0-19 + Reg 1-09	-2		+2	LSB
INL-R	Read DAC Integral Non-Linearity	@ 900h on Resistive Load. 0V to ~3V		+90		LSB
I_{OUT}-R-DAC-RED	Read Output Current, Read DAC at Full-Scale, I_{OUT1} or I_{OUT2}	PREAD = 0xFFF, I_{APC} = 0mA, Reg 1-21 = 8F	120	150	180	mA
$PSRR_{-FS}$	Power Supply Rejection - Full-Scale Current	Varying the V_{SO} (Note 18)		-42		dB
$TC_{-FS-IOUT}$	Temperature Coefficient - Full-Scale Current	Not including the R_{SET} tempco (Note 19) 0°C to +85°C		-48		ppm/°C
ZS-R	Zero-Scale Error	V_{IOUT} = 2V (Note 20)	-80	0	80	LSB

NOTES:

18. Full scale output current power supply sensitivity (SFS) is measured by varying the V_{SO} from 4.5V to 5.5V DC and measuring the effect of this signal on the full-scale output current.
19. Full scale output current temperature coefficient (TFS) is given by delta (full scale output current)/Δ(T).
20. Zero-scale error (ZS) is the deviation from zero current output when the digital input code is zero.

HFM (High Frequency Modulator) Standard conditions unless otherwise noted.

PARAMETER	DESCRIPTION	CONDITIONS	MIN (Note 13)	TYP	MAX (Note 13)	UNIT
$I_{MAX-RED-OFF-LINK}$	Max HFM Off DC Output, I_{OUT1} or I_{OUT2} in Link Mode	HFMOFF = 0xFFF	110	145	180	mA
$I_{MAX-RED-OFF-UNLINK}$	Max HFM Off DC Output, I_{OUT1} or I_{OUT2} in Unlink Mode	HFMOFF = 0xFFF	100	135	170	mA
$I_{MAX-BLUE-OFF}$	Max HFM Off DC Output, IBLUE	HFMOFF = 0xFFF	45	62	75	mA
$I_{MIN-RED-OFF}$	Min HFM Off DC Output, I_{OUT1} or I_{OUT2}	HFMOFF = 0x000	-3	0	3	mA
$I_{MIN-BLUE-OFF}$	Min HFM Off DC Output, I_{BLUE}	HFMOFF = 0x000	-3	0	3	mA
$I_{MAX-RED-ON-LINK}$	Max HFM Oscillator Output, I_{OUT1} or I_{OUT2} in Link Mode	HFMON = Reg 0-17h = 0xFF		118		mA_{P-P}
$I_{MAX-RED-ON-UNLINK}$	Max HFM Oscillator Output, I_{OUT1} or I_{OUT2} in Unlink Mode	HFMON = Reg 0-17h = 0xFF		114		mA_{P-P}
$I_{MAX-BLUE-ON}$	Max HFM Oscillator Output, I_{BLUE}	HFMON = 0xFF		60		mA_{P-P}
$F_{OSC-HI-MAX}$	Max HFM Frequency, High Range	Reg 0-16 = FFh, Reg X-00 bit 6 = 0	900	1086	1300	MHz
$F_{OSC-HI-MIN}$	Min HFM Frequency, High Range	Reg 0-16 = 01h, Reg X-00 bit 6 = 0	135	190	255	MHz
$F_{OSC-LO-MAX}$	Max HFM Frequency, Low Range	Reg 0-16 = FFh, Reg X-00 bit 6 =1	470	565	670	MHz
$F_{OSC-LO-MIN}$	Min HFM Frequency, Low Range	Reg 0-16 = 01h, Reg X-00 bit 6 = 1	55	80	110	MHz
$PSRR_{OSC-FREQ}$	PSRR - HFM Frequency	VSO from 4.5V to 5.0V		0.5		%/V
$PSRR_{OSC-AMP-IOUT}$	PSRR - HFM Amplitude	350MHz; HFMON = FFh; Link		3		%/V
$PSRR_{OSC-AMP-IBLUE}$	PSRR - HFM Amplitude	700MHz; HFMON = FFh; Link		1.2		%/V
$TF_{OSC400MAX}$	HFM Frequency Temperature Coefficient	Range from 200MHz to 400MHz		0 - 900		ppm/°C
$TF_{OSC900MAX}$	HFM Frequency Temperature Coefficient	Range from 400MHz to 900MHz		±250		ppm/°C
VR_{FREQ}	R_{FREQ} Pin Voltage	R_{FREQ} = 4.7kΩ	0.9	1.03	1.2	V
$SS_{-WIDTH-10h}$	Spread Spectrum Spreading Width	R_{FREQ} = 4.7kΩ, Reg 1-18 = 10h, Reg 0-16 = 26h; Reg X-00 bit 6 = 0	0.15	0.35	0.75	%
$SS_{-WIDTH-70h}$	Spread Spectrum Spreading Width	R_{FREQ} = 4.7kΩ, Reg 1-18 = 70h, Reg 0-16 = 26h; Reg X-00 bit 6 = 0	0.65	1.4	2.1	%

HFM (High Frequency Modulator) Standard conditions unless otherwise noted. **(Continued)**

PARAMETER	DESCRIPTION	CONDITIONS	MIN (Note 13)	TYP	MAX (Note 13)	UNIT
$SS_{-WIDTH-78h}$	Spread Spectrum Spreading Width	R_{FREQ} = 4.7kΩ, Reg 1-18 = 78h, Reg 0-16 = 26h; Reg X-00 bit 6 = 0	1.7	2.8	4	%
SS_Shift	Shift of Center Frequency when SS is Enabled vs when it's Disabled	R_{FREQ} = 4.7kΩ, Reg 1-18 = 00h to 40h, Reg 0-16 = 26h; Reg X-00 bit 6 = 0		1.4		%
SS_Mod	Spread Spectrum Modulation Frequency	REG 1-18h Bit 7 = 0; Reg X-00 bit 6 = 0	50	76	105	kHz
SS_Mod	Spread Spectrum Modulation Frequency	REG 1-18h Bit 7 = 1; Reg X-00 bit 6 = 0	25	44	65	kHz

Serial Interface AC Performance Standard conditions unless otherwise noted.

PARAMETER	DESCRIPTION	CONDITIONS	MIN (Note 13)	TYP	MAX (Note 13)	UNIT
F_{SER}	SCLK Operating Range	Static logic not limited at low frequency			50	MHz
t_{EH}	SEN "H" Time	@ 50MHz	320			ns
t_{EL}	SEN "L" Time	@ 50MHz	160			ns
t_{ERSR}	SEN Rising Edge to the First SCLK Rising Edge	@ 50MHz	10			ns
t_{CDS}	SDIO Set Up Time	@ 50MHz		10		ns
t_{CDH}	SDIO Hold Time	@ 50MHz		10		ns
t_{SREF}	Last SCLK Rising Edge to SEN Falling Edge	@ 50MHz	10			ns
t_{CC}	SCLK Cycle Time1	@ 50MHz	20			ns
Duty	SCLK "H" Duty Cycle	@ 50MHz	40	50	60	%
t_{CDD}	SDIO Output Delay	@ 50MHz			4	ns
t_{EDH}	SDIO Output Hold Time	@ 50MHz	2			ns

LVDS Specifications Standard conditions unless otherwise noted.

PARAMETER	DESCRIPTION	CONDITIONS	MIN (Note 13)	TYP	MAX (Note 13)	UNIT
$V_{IN-HIGH}$	Maximum Single Line Voltage			2.4		V
V_{IN-LOW}	Minimum Single Line Voltage			0		V
R_{IN}	Input Resistance		85	100	115	Ω
V_{MIN}	Minimum Differential Voltage	Signal tested with ±240mV differential input	240			mV_{PK}

Laser Driver AC Performance Demo board test, 10% duty cycle pulse, load = equivalent circuitry to [laser + flex cable] and/or as noted. V_{SO} = 5V. T_A = +25°C

PARAMETER	DESCRIPTION	CONDITIONS	MIN	TYP	MAX	UNIT
$t_{R\text{-}IOUTx}$	$I_{OUT1/2}$ Write Rise Time (10% to 90%)	300mW Optical ML229U7		1.3		ns
$t_{F\text{-}IOUTx}$	$I_{OUT1/2}$ Write Fall Time (10% to 90%)	300mW Optical ML229U7		800		ps
$O/S_{\text{-}IOUTx}$	$I_{OUT1/2}$ Write Pulse Overshoot	300mW Optical ML229U7		11		%
$t_{D\text{-}IOUTx}$	$I_{OUT1/2}$ Write Pulse Delay From LVDS = Zero crossing to I_{OUT} rise 10%			5.3		ns
$t_{R\text{-}BLUE}$	I_{BLUE} Write Rise Time (10% to 90%)	300mW Optical		650		ps
$t_{F\text{-}BLUE}$	I_{BLUE} Write Fall Time (10% to 90%)	300mW Optical		450		ps
$O/S_{\text{-}BLUE}$	I_{BLUE} Write Pulse Overshoot	300mW Rising Optical		12		%
$t_{D\text{-}BLUE}$	I_{BLUE} Write Pulse Delay From LVDS = Zero crossing to I_{OUT} rise 10%			5.2		ns
$I_{NOISE}\text{-}I_{OUTx}$	$I_{OUT1/2}$ Read Output Current Noise	I_{OUT} = 50mA, measured @ 10MHz		0.55		nA/√Hz
$I_{NOISE}\text{-}I_{OUTx}$	$I_{OUT1/2}$ Read and HFM Output Current Noise	I_{OUT} = 50mA+30$mA_{P\text{-}P}$; measured @ 10MHz		0.96		nA/√Hz
$I_{NOISE\text{-}BLUE}$	I_{BLUE} Read Output Current Noise	I_{OUT} = 50mA, measured @ 10MHz		0.37		nA/√Hz
$I_{NOISE\text{-}BLUE}$	I_{BLUE} Read and HFM Output Current Noise	I_{OUT} = 50mA+10$mA_{P\text{-}P}$; measured @ 10MHz		0.47		nA/√Hz
BW_{APC}	Read Amplifier 3dB Bandwidth	I_{OUT} = 50mA		0.5		MHz

TABLE 1. AMPLITUDE SELECTION REGISTER ACTIVATION

NAME	ENA	WEB	CR0 Bit 2	WEN2	WEN1	WEN0	MSB BSEL = 0	LSB BSEL = 0	MSB BSEL = 1	LSB BSEL = 1
OFF	0	X	x	X	X	X	X	X	X	X
READ	1	1	0	X	X	X	0-19	1-09	0-19	1-09
W0	1	0	1	0	0	0	0-10	2-10	0-11	2-11
W1	1	0	1	0	0	1	0-04	2-04	0-05	2-05
W2	1	0	1	0	1	0	0-06	2-06	0-07	2-07
W3	1	0	1	0	1	1	0-08	2-08	0-09	2-09
W4	1	0	1	1	0	0	0-0A	2-0A	0-0B	2-0B
W5	1	0	1	1	0	1	0-0C	2-0C	0-0D	2-0D
W6	1	0	1	1	1	0	0-0E	2-0E	0-0F	2-0F
W7	1	0	1	1	1	1	0-12	2-12	0-13	2-13

NOTES:

21. There are two sets of write current registers. When BSEL = 1, bank 1 is selected. When BSEL = 0, bank 0 is selected.
22. Read and write are independent. Read is enabled with a control bit.
23. Register terminology is page Number-Register number (hex). Thus 1-09 is page 1, register 09h.

Applications Information

I_{OUT}

The data sheet values for oscillator current, and write current are based on an R_{SET} of 620Ω when PMAX and WriteDAC are both set to full scale. The user may choose R_{SET} to match the output current needs of the application.

The PMAX DAC is biased by I_{RSET} (= V_{RSET}/R_{SET}). See the "Typical Performance Curves" on page 11.

The write channel output capability for a typical part is shown in Figures 1, 2, and 3. The amount of I_{OUT} will be limited by the available headroom voltage at the I_{OUTx} pins.

A four input DAC (Reg 1-0A bits 3, 2, 1, 0) can be used to control the amount of RC snubbing applied to the outputs. For IBLUE, there is an extra bit (Reg 1-0A bit 4) weighted as MSB.

Read current may be controlled by either the Read DAC or the IAPC input. When set by the PREAD DAC, I_{READ} is limited to the data sheet value, whereas the I_{APC} input will allow a significantly higher value to be obtained. The ReadDAC and I_{APC} currents sum together.

Glitches could occur if two or three WEN lines are changed simultaneously, and the propagation delay is different for the two lines between the inner circuits of the controller and the inner circuits of the LDD. Because the WEN lines are encoded, the selected write current will be correct before the change in code, and again after the code changes. But some other output could result momentarily if the propagation delays are not matched. The skew detector detects the first rising edge at the LVDS outputs.

F_{OSC}

Both F_{OSC} and R_{FREQ} may be chosen to accommodate the desired range or operating point of the HFMFREQ DAC. Although F_{OSC} is relatively linear with DAC code, monotonicity is not guaranteed (see Figures 5 and 6).

The oscillator may be turned on by the WEN code selected. The particular code that selects the oscillator is under program control. The P_{COOL} function is also available through the program control and WEN selection.

The WEB enables write current. WEN code 000 through 111 will select a write current as described in Table 1.

Power

The main power consumption is caused by the headroom voltage across the output stage (V_{SO} - V_{IOUT}) x I_{OUT}. For I_{OUT1} and I_{OUT2}, the V_{SO} can be reduced below 5.0V, as long as sufficient headroom voltage is available to obtain the desired output current. For the blue outputs, the built in ADC can be used to obtain the output voltage, which is also the headroom voltage. The HFM oscillator power consumption will increase with increasing frequency and amplitude (see Figure 7).

Note that in the TQFN package, the die is mounted directly on the thermal pad. This provides a very low thermal resistance Junction to thermal pad of just a few °C/W. The problem is in moving the heat from the thermal pad to some other heat sink.

Figure 12 shows that when mounted well on a 4-layer PCB with 3 ground plane layers, and an area of 10cmx10cm, the θ_{JA} is +42°C/W. The typical application will not afford this good of a heat sink.

Typical Performance Curves

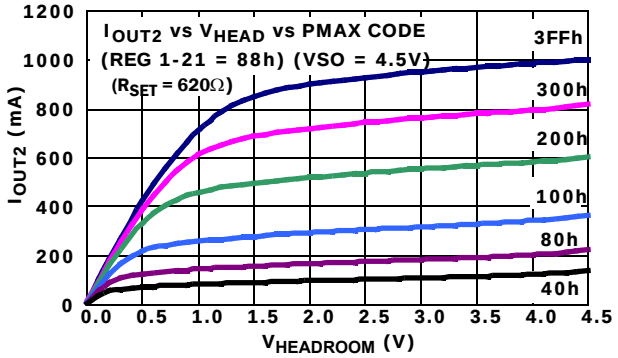


FIGURE 1. I_{OUT} WRITE CURRENT vs $V_{HEADROOM}$ vs PMAX

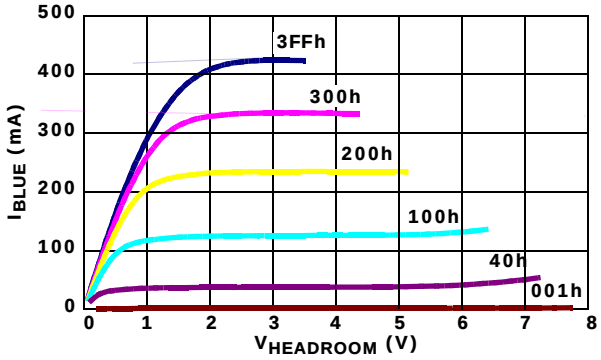


FIGURE 2. I_{BLUE} vs P_{MAX} vs $V_{HEADROOM}$ (V_{SO} = 5.0V) (R_{SET} = 620Ω) (1-21 = FFh), (R_{LOAD} = 10Ω)

Typical Performance Curves (Continued)

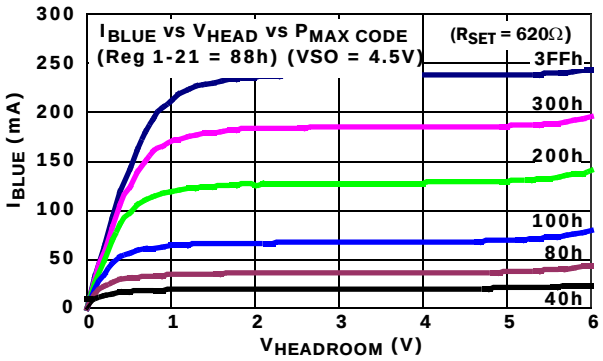


FIGURE 3. I_{BLUE} WRITE CURRENT vs $V_{HEADROOM}$ vs PMAX

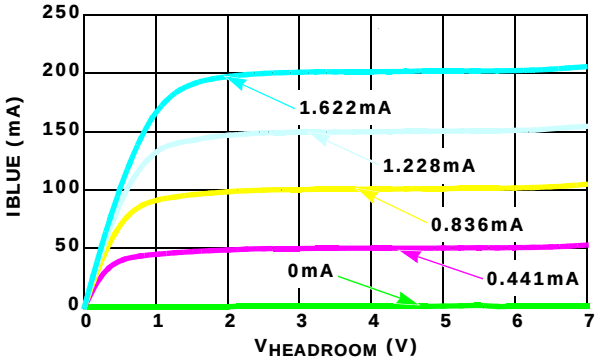


FIGURE 4. I_{BLUE} READ vs $V_{HEADROOM}$ vs I_{APC}, (REG 1-21 = 88h) (V_{SO} = 5.0V), (R_{SET} = 620Ω)

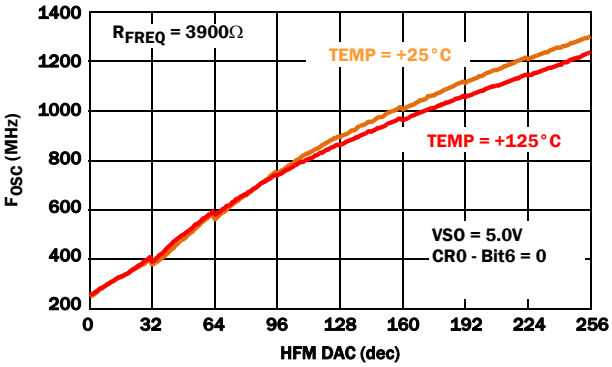


FIGURE 5. HFM CONTROL vs TEMPERATURES

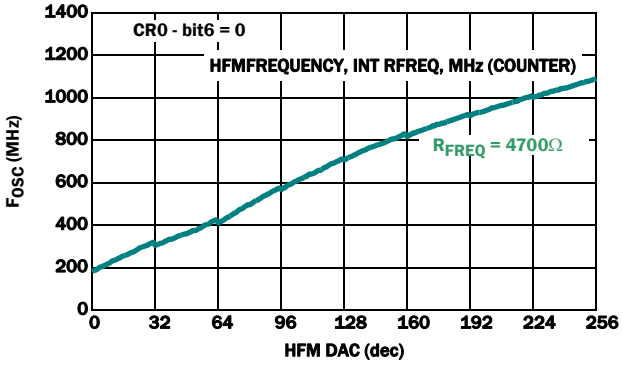


FIGURE 6. HFM CONTROL; VSO = 5.0V

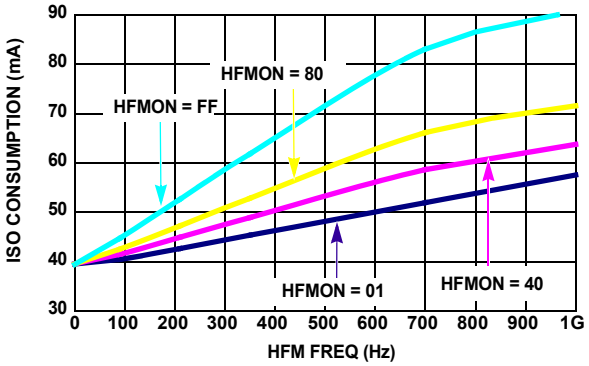


FIGURE 7. HFM OSCILLATOR CURRENT CONSUMPTION

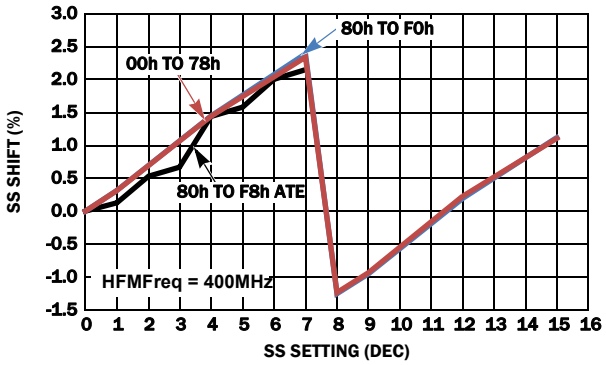


FIGURE 8. I_{BLUE} SS SHIFT vs SS SETTING @ 400MHz

Typical Performance Curves (Continued)

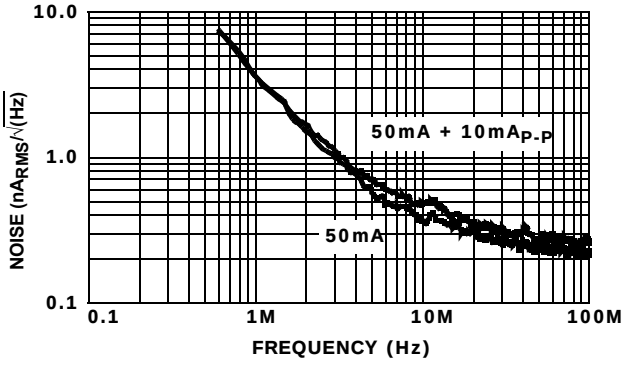


FIGURE 9. I_{BLUE} NOISE vs FREQUENCY

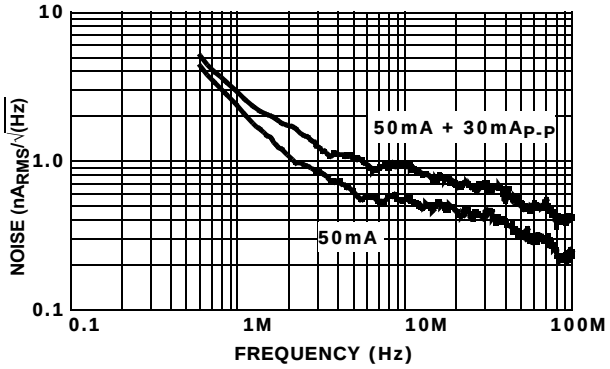


FIGURE 10. I_{OUTx} NOISE vs FREQUENCY

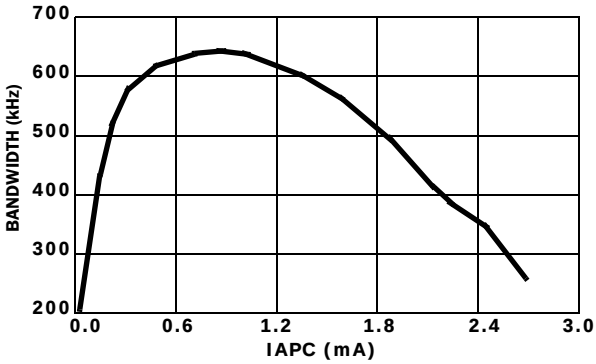


FIGURE 11. I_{OUT}/I_{APC} BANDWIDTH vs I_{APC}

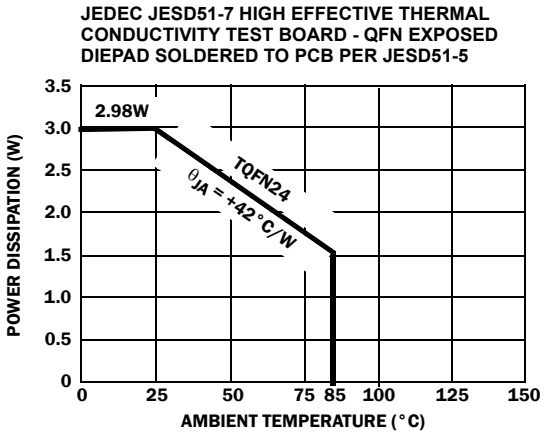


FIGURE 12. PACKAGE POWER DISSIPATION vs AMBIENT TEMPERATURE

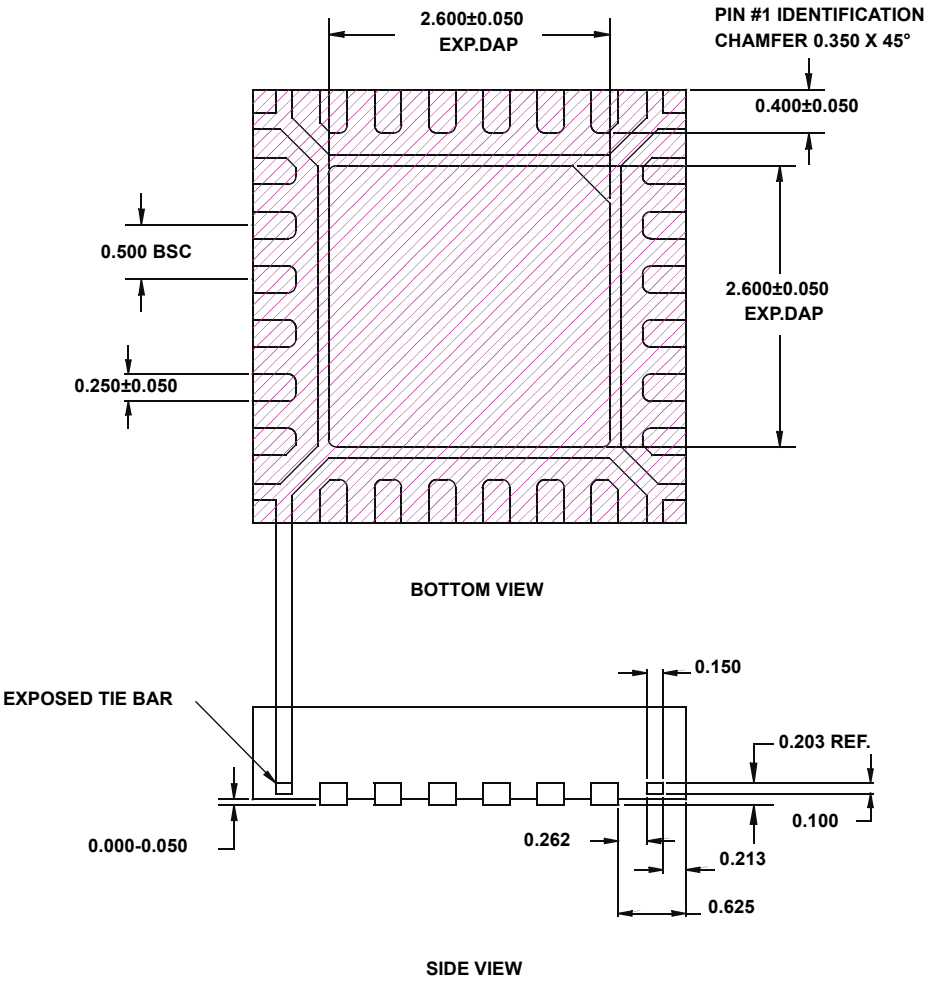


FIGURE 13. TIE BAR LOCATION FOR 4X4 TQFN

Revision History

The revision history provided is for informational purposes only and is believed to be accurate, but not warranted. Please go to web to make sure you have the latest Rev.

DATE	REVISION	CHANGE
December 14, 2015	FN7580.3	Removed ISL58792CRTZ-EVAL from Ordering Information table. Updated POD L24.4x4E from rev 0 to rev 2. Changes since rev 2: - Bottom View - Changed Exposed paddle dimension from 2.50 to 2.60 - Made correction in Typical land pattern - added 0 to .250 - Added tolerance to Exposed DAP in Bottom view: From: 2.60 sq. To: 2.60 ±0.10 with added square graphic in front of the 2.60
July 29, 2013	FN7580.2	Updated Products information verbiage to About Intersil verbiage.
January 6, 2012	FN7580.1	Added ISL58792CRTZ and ISL58792CRTZ-T7A to “Ordering Information” on page 3.
November 29, 2010	FN7580.0	Initial release.

About Intersil

Intersil Corporation is a leading provider of innovative power management and precision analog solutions. The company's products address some of the largest markets within the industrial and infrastructure, mobile computing and high-end consumer markets.

For the most updated datasheet, application notes, related documentation and related parts, please see the respective product information page found at www.intersil.com.

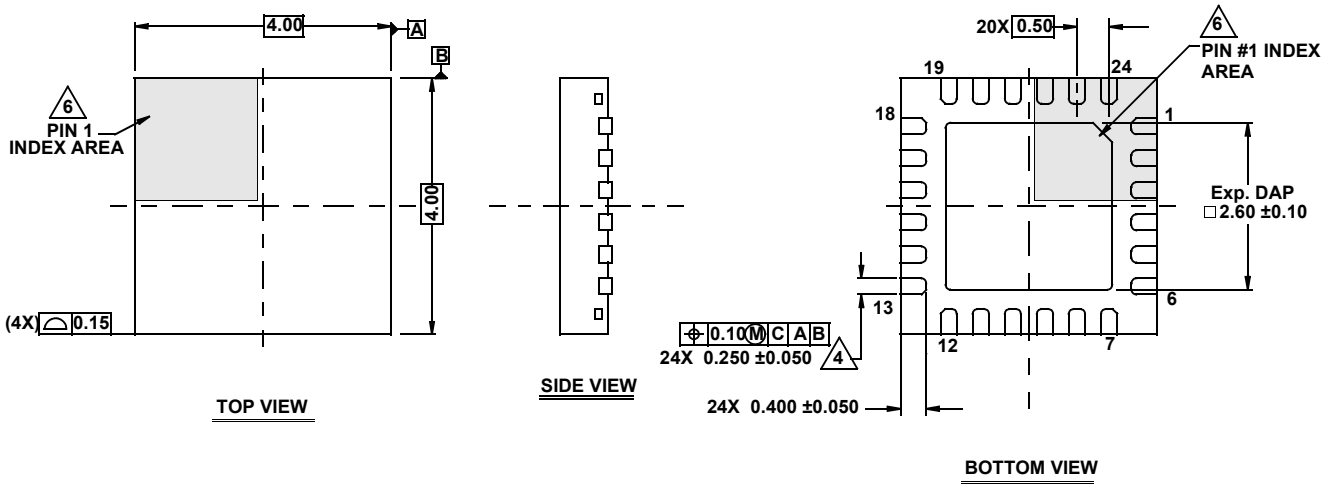
You may report errors or suggestions for improving this datasheet by visiting www.intersil.com/ask.

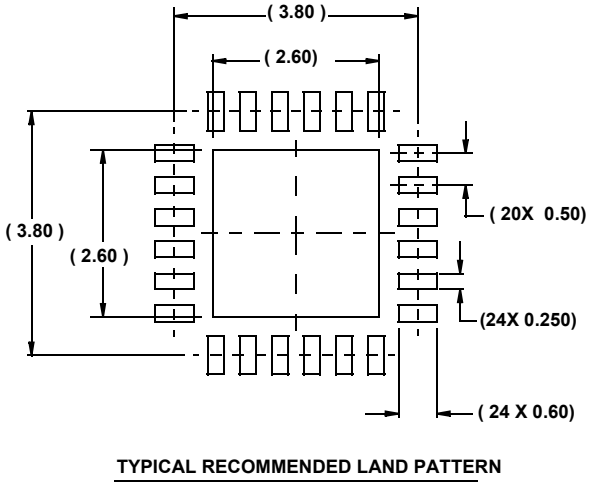
Reliability reports are also available from our website at www.intersil.com/support.

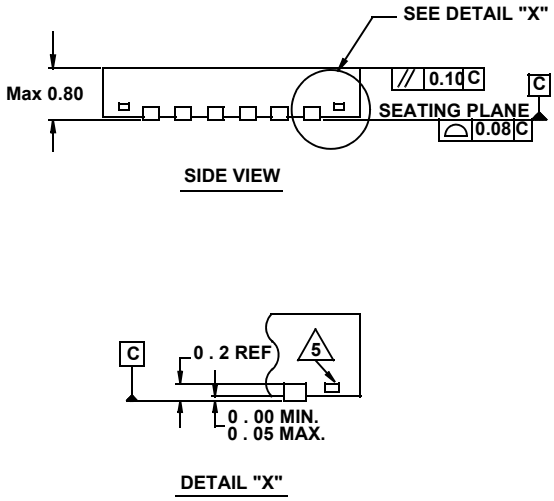
Package Outline Drawing

L24.4x4E

24 LEAD THIN QUAD FLAT NO-LEAD PLASTIC PACKAGE
Rev 2, 2/14







NOTES:

1. Dimensions are in millimeters.
   Dimensions in ( ) for Reference Only.
2. Dimensioning and tolerancing conform to AMSE Y14.5m-1994.
3. Unless otherwise specified, tolerance : Decimal ± 0.05
4. Dimension b applies to the metallized terminal and is measured between 0.15mm and 0.30mm from the terminal tip.
5. Tiebar shown (if present) is a non-functional feature.
6. The configuration of the pin #1 identifier is optional, but must be located within the zone indicated. The pin #1 identifier may be either a mold or mark feature.