

ISL58831

Dual Laser Driver with APC Amplifier and Spread Spectrum Oscillator

FN7440
Rev 1.00
Jan 28, 2016

The [ISL58831](#) is a combination read + 3 write level laser driver and I/V amplifier, with an extra read + oscillator ROM channel for use in dual-laser 'Combo' drivers. A separate (amplitude and frequency) oscillator modulates the selected output for laser noise reduction during read or write. All these functions are provided in a 24 Ld QFN package.

The SEL1 pin, when high, selects the DVD (write) laser. Positive current supplied to the I_N lines, through a user-selected resistor, allow the full-scale range of each amplifier to be matched to the full-scale range of the users control DACs. When the write laser is selected, and the WEN pins are switched low, the respective current is summed to the output with 1ns rise and fall times. Write channel 2 has 240mA output capability with an 250X gain amplifier.

The 100mA_{P,P} (maximum) oscillator is switched on and off by the OSCEN line. The SEL1 line allows the oscillator to operate at different amplitudes and frequencies for each laser.

The entire chip is powered down when ENABLE is low. The user can define the gain of the I/V amplifier. With a slew rate of 200V/μs, the I/V amplifier can normally settle to 1% within 30ns.

An internal spread spectrum circuit modulates the oscillator frequency to help reduce peak EMI.

Features

- "Shrink-small" outline package
- Voltage-controlled output current source requiring one external set resistor per channel
- Current-controlled output current source
- CH2 to 235mA maximum
- CH3 to 170mA maximum
- CH4 to 100mA maximum
- Rise time = 0.8ns
- Fall time = 0.8ns
- On-chip oscillator with frequency and amplitude control by use of external resistors to ground
- Oscillator to 600MHz
- Oscillator to 100mA_{P,P}
- Single +5V supply (±10%)
- Disable feature for power-up protection and power savings
- 200V/μs I/V amplifier
- Internal spread spectrum modulation to reduce peak EMI
- Pb-free (RoHS compliant)

Applications

- Combo CD-R + DVD-R
- DVD±RW to 8X
- Writable optical disk drives

Typical Application

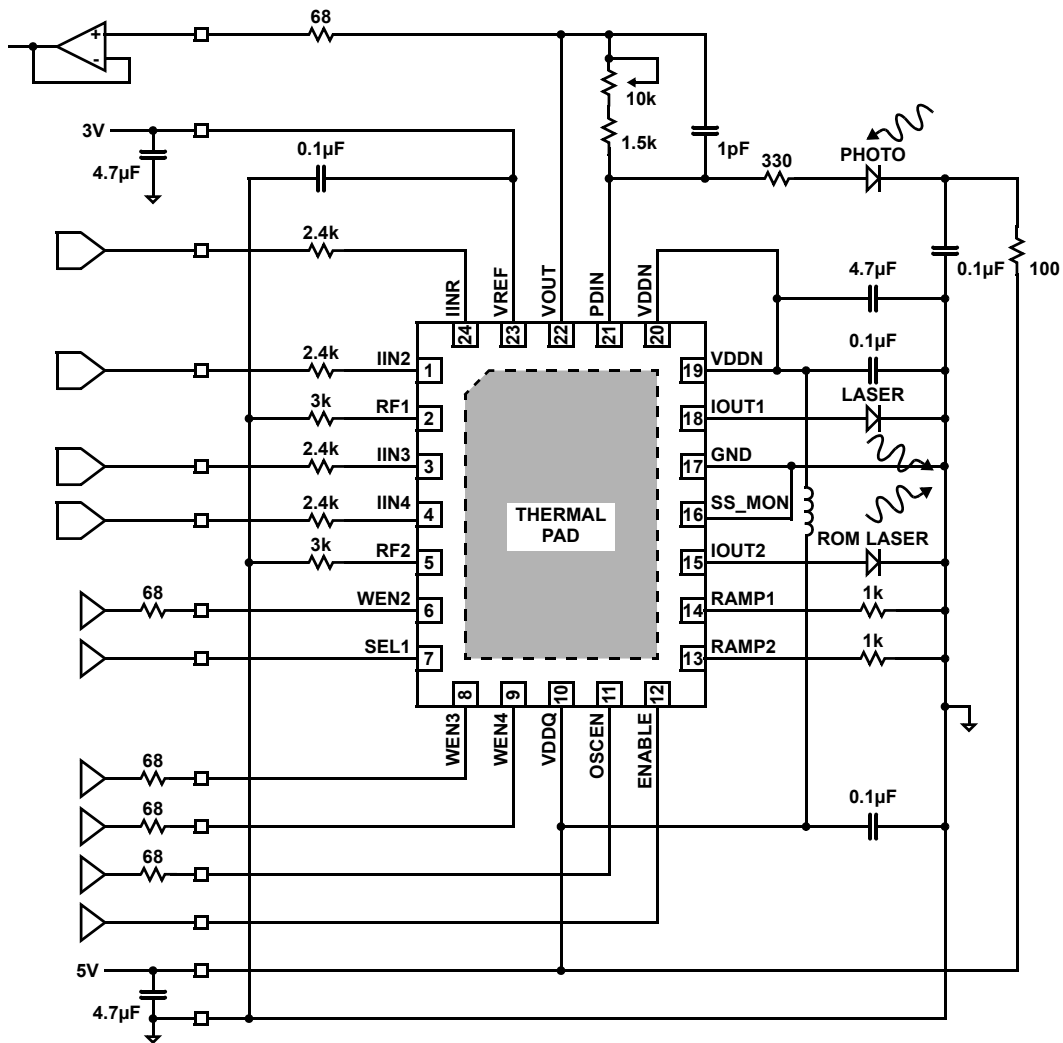


FIGURE 1. TYPICAL APPLICATION

Ordering Information

| PART NUMBER (Notes 2, 3) | PART MARKING | PACKAGE (RoHS Compliant) | TAPE AND REEL QUANTITY (UNITS) | PKG. DWG. # |
|-----------------------------|--------------|-----------------------------|-----------------------------------|-------------|
| ISL58831CRZ | 58831 CRZ | 24 Ld QFN | - | MDP0046 |
| ISL58831CRZ-T13 (Note 1) | 58831 CRZ | 24 Ld QFN | 2.5k | MDP0046 |

NOTES:

1. Please refer to [TB347](#) for details on reel specifications.
2. Intersil Pb-free plus anneal products employ special Pb-free material sets; molding compounds/die attach materials and 100% matte tin plate termination finish, which are RoHS compliant and compatible with both SnPb and Pb-free soldering operations. Intersil Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020.
3. For Moisture Sensitivity Level (MSL), please see product information page for [ISL58831](#). For more information on MSL, please see tech brief [TB363](#).

Block Diagram

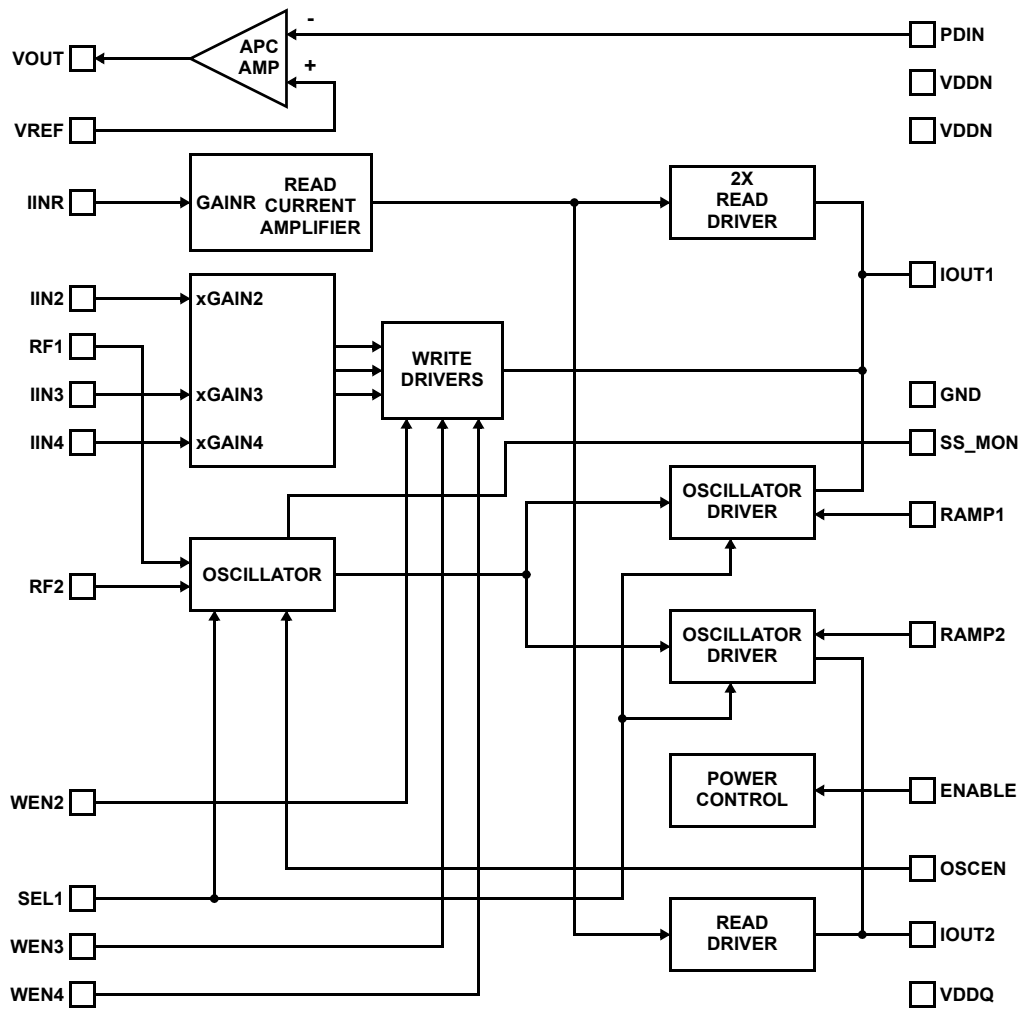
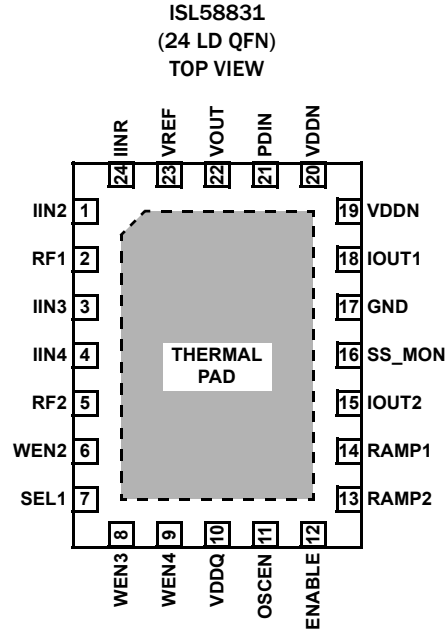


FIGURE 2. BLOCK DIAGRAM

Pin Configuration



Pin Descriptions

| PIN NUMBER | PIN NAME | PIN FUNCTION | PIN DESCRIPTION |
|------------|----------|--------------|--|
| 1 | IIN2 | Analog | Input pin for IIN2, which current is amplified and output to IOUT1 (add external series resistor when voltage driven). |
| 2 | RF1 | Analog | External resistor to ground sets the oscillator frequency when SEL1 = 1. |
| 3 | IIN3 | Analog | Input pin for IIN3, which current is amplified and output to IOUT1 (add external series resistor when voltage driven). |
| 4 | IIN4 | Analog | Input pin for IIN4, which current is amplified and output to IOUT1 (add external series resistor when voltage driven). |
| 5 | RF2 | Analog | External resistor to ground sets the oscillator frequency when SEL1 = 0. |
| 6 | WEN2 | Digital | WEN2 = 0 applies the current from the IIN2 amplifier to the IOUT pin. |
| 7 | SEL1 | Digital | If SEL1 = 1, IOUT1 and RFREQ1 and RAMP1 are selected, otherwise IOUT2 and RFREQ2 and RAMP2 are selected. |
| 8 | WEN3 | Digital | WEN3 = 0 applies the current from the IIN3 amplifier to the IOUT pin. |
| 9 | WEN4 | Digital | WEN4 = 0 applies the current from the IIN4 amplifier to the IOUT pin. |
| 10 | VDDQ | Power Supply | +5V supply for bias and amplifiers (connect all supplies). |
| 11 | OSCEN | Digital | OSCEN = 1 powers up the oscillator and oscillator driver and passes specified oscillator current to I _O UT. |
| 12 | ENABLE | Digital | ENABLE = 1 powers up the chip, ENABLE = 0 puts the chip in power-down mode. |
| 13 | RAMP2 | Analog | External resistor to ground sets the oscillator amplitude when SEL1 = 0. |
| 14 | RAMP1 | Analog | External resistor to ground sets the oscillator amplitude when SEL1 = 1. |
| 15 | IOUT2 | Analog | Output current source for ROM laser diode at $[82 * I_{INR} + I_{OSC} (ac)]$. |
| 16 | SS_MON | Analog | Modulation rate monitor. |
| 17 | GND | Power Supply | Ground (connect all grounds). |
| 18 | IOUT1 | Analog | Output current source for RW laser diode $[100 * (1.65 * I_{INR} + 2.5 * I_{IN2} + 2.0 * I_{IN3} + I_{IN4}) + I_{OSC} (ac)]$. |
| 19 | VDDN | Power Supply | +5V supply for output drivers (connect all supplies). |
| 20 | VDDN | Power Supply | +5V supply for output drivers (connect all supplies). |
| 21 | PDIN | Analog | Connect the photo diode to this pin for the I-V amplifier input; connect the gain resistor and compensation capacitor between PDIN and VOUT. |
| 22 | VOUT | Analog | Output voltage from I-V amplifier. |
| 23 | VREF | Analog | Reference voltage for the I-V amplifier. |
| 24 | IINR | Analog | Input pin for IINR (IINR2), which current is amplified and output to IOUT1 (IOUT2) (add external series resistor when voltage driven). |
| | PD | Thermal Pad | Should be connected to GND. |

Absolute Maximum Ratings ($T_A = +25^\circ\text{C}$)

Voltages Applied to:

| | |
|-----------------------------|-------------------------------------|
| V_{DD} | -0.5V to +6.0V |
| WEN | -0.5V to $V_{DD} + 0.5V$ |
| I_{INX} | -0.5V to +5.0V |
| I_{OUT} | -0.5V to $V_{DD} + 0.5V$ |
| Power Dissipation (maximum) | See page 9 |
| I_{OUT} Current | 300mA average, 500mA _{p-p} |

Thermal Information

Thermal Resistance (Typical)

 θ_{JA} ($^\circ\text{C}/\text{W}$)

| | |
|--|---|
| 24 Ld QFN Package (Note 4) | 42 |
| Maximum Junction Temperature | +150 $^\circ\text{C}$ |
| Storage Temperature Range | -65 $^\circ\text{C}$ to +150 $^\circ\text{C}$ |
| Pb-Free Reflow Profile | see TB493 |

Recommended Operating Conditions

| | |
|-------------------------------------|---|
| Operating Ambient Temperature Range | 0 $^\circ\text{C}$ to +80 $^\circ\text{C}$ |
| V_{DD} | .5V \pm 10% |
| R_{FREQ} | 1500 Ω (minimum) |
| R_{AMP} | 500 Ω (minimum) |
| F_{OSC} | 100MHz to 600MHz |
| A_{OSC} | 20mA _{p-p} to 100mA _{p-p} |

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTE:

- θ_{JA} is measured with the component mounted on a high effective thermal conductivity test board in free air. See Tech Brief [TB379](#) for details.

NOTE: Compliance to datasheet limits is assured by one or more methods: production test, characterization and/or design.

Electrical Specifications $V_{DD} = 5V$, $T_A = +25^\circ\text{C}$, ENABLE = HI, WEN = HI, OSCEN = LO, SEL1 = HI, unless otherwise specified.

| PARAMETER | DESCRIPTION | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|--------------------|---------------------------|--|------|-----|-----|---------------|
| V_{DD} | Supply Voltage | | 4.5 | 5.0 | 5.5 | V |
| IS1 | Supply Current (Disabled) | ENABLE = <0.5V | | 0.1 | 100 | μA |
| IS2 | Supply Current | $I_{INR} = 0\mu\text{A}$, $I_{IN2/3/4} = 20\mu\text{A}$ | 34 | 40 | 46 | mA |
| IS3 | Supply Current | OSCEN = HI, $I_{INR} = 0\mu\text{A}$, $I_{IN2/3/4} = 20\mu\text{A}$ | 50 | 60 | 70 | mA |
| IS4 | Supply Current | $I_{INR} = 0\mu\text{A}$, $I_{IN2/3/4} = 500\mu\text{A}$ | 61 | 73 | 85 | mA |
| IS5 | Supply Current | $I_{INR} = 200\mu\text{A}$, $I_{IN2/3/4} = 500\mu\text{A}$ | 94 | 112 | 130 | mA |
| DV _{LO} | Digital Low Voltage | WEN2/3/4, OSCEN inputs | | | 1.3 | V |
| EV _{LO} | Enable Low Voltage | ENABLE pin (to guarantee IS1) | | | 0.5 | V |
| DV _{HI} | Digital High Voltage | WEN2/3/4, OSCEN inputs | 2.2 | | | V |
| EV _{HI} | Enable High Voltage | ENABLE pin only | 2.2 | | | V |
| DV _{HICD} | Digital High Voltage | SEL1 only | 2.2 | | | V |
| DV _{LOCD} | Digital Low Voltage | SEL1 only | | | 1.3 | V |
| DI _{LO} | Digital Low Current | SEL1, OSCEN, ENABLE, WEN = 0.0V | -100 | | | μA |
| DI _{HI} | Digital High Current | SEL1, OSCEN, ENABLE, WEN = 5.0V | | | 100 | μA |
| V _{SHUT} | V_{DD} Shutdown Voltage | | 3.5 | | 3.9 | V |

Laser Amplifier $V_{DD} = 5V$, $T_A = +25^\circ\text{C}$, ENABLE = HI unless otherwise specified.

| PARAMETER | DESCRIPTION | CONDITIONS | MIN | TYP | MAX | UNIT |
|------------|-----------------------|--|-----|-----|-----|-------|
| GAINR | Best Fit Current Gain | Channel R - I_{OUT1} (Note 5) | 140 | 165 | 190 | mA/mA |
| GAINR2 | Best Fit Current Gain | Channel R2 - I_{OUT2} (Note 5) | 70 | 82 | 95 | mA/mA |
| GAIN2 | Best Fit Current Gain | Channel 2 - I_{OUT1} (Note 5) | 210 | 250 | 290 | mA/mA |
| GAIN3 | Best Fit Current Gain | Channel 3 - I_{OUT1} (Note 5) | 170 | 200 | 230 | mA/mA |
| GAIN4 | Best Fit Current Gain | Channel 4 - I_{OUT1} (Note 5) | 80 | 100 | 120 | mA/mA |
| I_{OUTR} | Output Current | $V_{DD} = 4.5V$, $V_{OUT} = 3.4V$, output is sourcing, channel R - I_{OUT1} (Note 5), $I_{INR} = 2\text{mA}$ | 150 | | | mA |

Laser Amplifier $V_{DD} = 5V$, $T_A = +25^\circ C$, ENABLE = HI unless otherwise specified. (Continued)

| PARAMETER | DESCRIPTION | CONDITIONS | MIN | TYP | MAX | UNIT |
|------------------------|--|---|-----|------|-----|-----------------|
| I _{OUTR2} | Output Current | $V_{DD} = 4.5V$, $V_{OUT} = 2.1V$, output is sourcing, channel R2 - I _{OUT2} (Note 5), I _{INR2} = 2mA | 120 | | | mA |
| I _{OUT2} | Output Current | $V_{DD} = 4.5V$, $V_{OUT} = 3.4V$, output is sourcing, channel 2 - I _{OUT1} (Note 5), I _{IN2} = 2mA | 235 | | | mA |
| I _{OUT3} | Output Current | $V_{DD} = 4.5V$, $V_{OUT} = 3.4V$, output is sourcing, channel 3 - I _{OUT1} (Note 5), I _{IN3} = 2mA | 170 | | | mA |
| I _{OUT4} | Output Current | $V_{DD} = 4.5V$, $V_{OUT} = 3.4V$, output is sourcing, channel 4 - I _{OUT1} (Note 5), I _{IN4} = 2mA | 100 | | | mA |
| IOSR | Best Fit Current Offset | Channel R (Note 5) | -6 | | +6 | mA |
| IOS2, 3, 4 | Best Fit Current Offset | Channels 2, 3, 4 (Note 5) | -6 | | +6 | mA |
| ILIN | Output Current Linearity | Any channel (Note 5) | -3 | | +4 | % |
| IDAC | Input Current Range | Input is sinking | 0 | | 2 | mA |
| R _{INR} | I _{INR} Input Impedance | R _{IN} is to GND | 562 | 750 | 937 | Ω |
| R _{IN2, 3, 4} | I _{IN2, 3, 4} Input Impedance | R _{IN} is to GND | 375 | 500 | 625 | Ω |
| VTH | WEN2/3/4 Threshold for Write Pulses | Temperature stabilized | | 1.68 | | V |
| I _{OFF1} | Output Off Current 1 | ENABLE = LO | | | 0.5 | mA |
| I _{OFF2} | Output Off Current 2 | WEN = HI, total for all channels | | | 1.5 | mA |
| I _{OFF3} | Output Off Current 3 | WEN = LO, I _{IN} = 0 μ A, total for all channels | | | 5 | mA |
| VC1 | I _{OUT} Supply Sensitivity | I _{OUT} = 40mA, $V_{DD} = 5V \pm 10\%$, read only | -3 | | 3 | %/V |
| VC2 | I _{OUT} Supply Sensitivity | I _{OUT} = 80mA, 40mA read + 40mA write | -3 | | 3 | %/V |
| IN _{OUT} | I _{OUT} Current Output Noise | I _{OUT} = 40mA, OSCEN = LO | | 3.5 | | nA/ \sqrt{Hz} |
| TC1 | I _{OUT} Temperature Sensitivity | I _{OUT} = 40mA, read only | | +100 | | ppm/ $^\circ C$ |
| TC2 | I _{OUT} Temperature Sensitivity | I _{OUT} = 80mA, 40mA read + 40mA write | | -100 | | ppm/ $^\circ C$ |

NOTE:

5. The amplifier linearity is calculated using a best fit method at three operating points. The output currents chosen are 20mA, 40mA, and 60mA. The transfer function for I_{OUT} is defined as follows: $I_{OUT} = (I_{IN} * GAIN) + I_{OS}$.

Laser Current Amplifier Outputs AC Performance $V_{DD} = 5V$, I_{OUT} = 40mA DC with 40mA pulse, $T_A = +25^\circ C$ unless otherwise specified.

| PARAMETER | DESCRIPTION | CONDITIONS | MIN | TYP | MAX | UNIT |
|-------------------|--|---|-----|-----|-----|-----------------|
| tr2 | Write Rise Time | I _{OUT} = 40mA (read) + 40mA (10%-90%) | | 0.8 | 2.0 | ns |
| tf2 | Write Fall Time | I _{OUT} = 40mA (read) + 40mA (10%-90%) | | 0.8 | 2.0 | ns |
| OS | Output Current Overshoot | Measured on 6.8 Ω resistor load | | 5 | | % |
| t _{ON} | I _{OUT} ON Propagation Delay | Input timing to I _{OUT} at 50% of final value (Note 6) | | 2.0 | | ns |
| t _{OFF} | I _{OUT} OFF Propagation Delay | Input timing to I _{OUT} at 50% of final value (Note 6) | | 2.0 | | ns |
| T _{DIS} | Disable Time | Input timing to I _{OUT} at 50% of final value (Note 6) | | 20 | | ns |
| T _{EN} | Enable Time | Input timing to I _{OUT} at 50% of final value (Note 6) | | 150 | | ns |
| BW | Amplifier Bandwidth | I _{OUT} = 50mA, all channels, -3dB value | | 8 | | MHz |
| F _{OSC} | Oscillator Frequency | R _{FREQ} = 5600 Ω | 290 | 328 | 360 | MHz |
| TC _{OSC} | Oscillator Temperature Coefficient | R _{FREQ} = 4500 Ω | | 200 | | ppm/ $^\circ C$ |

NOTE:

6. Input timing is defined as WENx or ENABLE input pulse crosses 1.68V. Input pulse is standard 3.3V CMOS-level TTL input.

APC Amplifier $V_{DD} = 5V$, $T_A = +25^\circ C$, $R_{LOAD} = 2k\Omega$ to V_{REF} unless otherwise specified.

| PARAMETER | DESCRIPTION | CONDITIONS | MIN | TYP | MAX | UNIT |
|--------------|--|--|------|-----|--------------|------------------|
| BW | Bandwidth | $G = 1$ | | 100 | | MHz |
| SR | Slew Rate | $G = 1$, $V_O = 0.5V$ to $3V$ | | 200 | | V/ μs |
| t_S | Settling Time | To 0.1%, $V_{OUT} = 0.5V$ to $3V$ | | 30 | | ns |
| A_{VOL} | Open Loop Voltage Gain | $V_{OUT} = 0.5V$ to $3V$ | | 80 | | dB |
| V_{OS} | Offset Voltage | $V_{REF} = 3V$ | -5 | | +5 | mV |
| $T_C V_{OS}$ | Input Offset Voltage Temperature Coefficient | | | +4 | | $\mu V/^\circ C$ |
| I_B | Input Bias Current | $V_{REF} = 3V$ | -0.5 | | +0.5 | μA |
| CMIR | Common-Mode Input Range | $CMRR \geq 54dB$ | 1 | | $V_{DD}-1$ | V |
| CMRR | Common-Mode Rejection Ratio | $V_{CM} = 1.0V$ to $4.0V$ | 55 | 75 | | dB |
| R_{IN} | Input Impedance | | | 1 | | M Ω |
| C_{IN} | Input Capacitance | Pin 21 (P_{DIN}) | | 2 | | pF |
| V_{OUT} | Output Voltage Swing | $R_L = 2k\Omega$ to V_{REF} (Note 7) | 0.5 | | $V_{DD}-0.5$ | V |

NOTE:

7. R_L is total load resistance due to feedback resistor and load resistor. Recommended feedback resistor is 5k Ω . **I_{OUT} Control**

| ENABLE | SEL1 | WEN2 | WEN3 | WEN4 | I_{OUT1} | I_{OUT2} |
|--------|------|------|------|------|-------------------------------------|----------------|
| 0 | X | X | X | X | OFF | OFF |
| 1 | 1 | 1 | 1 | 1 | $165 * I_{INR}$ | OFF |
| 1 | 1 | 0 | 1 | 1 | $(165 * I_{INR}) + (250 * I_{IN2})$ | OFF |
| 1 | 1 | 1 | 0 | 1 | $(165 * I_{INR}) + (200 * I_{IN3})$ | OFF |
| 1 | 1 | 1 | 1 | 0 | $(165 * I_{INR}) + (100 * I_{IN4})$ | OFF |
| 1 | 0 | X | X | X | OFF | $82 * I_{INR}$ |

Oscillator Control

| ENABLE | OSCN | SEL1 | $I_{OSCILLATOR}$ |
|--------|------|------|-----------------------------|
| 0 | X | X | OFF |
| 1 | 0 | X | OFF |
| 1 | 1 | 1 | Oscillator On to I_{OUT1} |
| 1 | 1 | 0 | Oscillator On to I_{OUT2} |

Timing Diagram

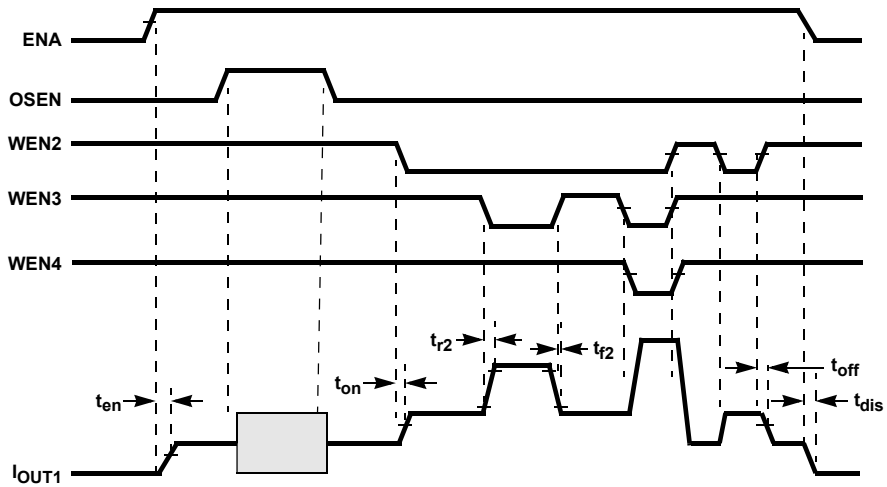


FIGURE 3. TIMING DIAGRAM

Typical Performance Curves

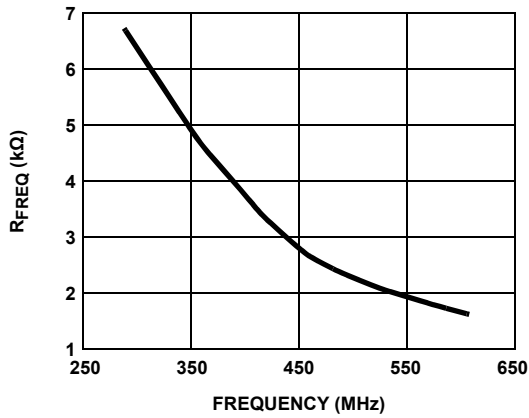


FIGURE 4. FREQUENCY CONTROL

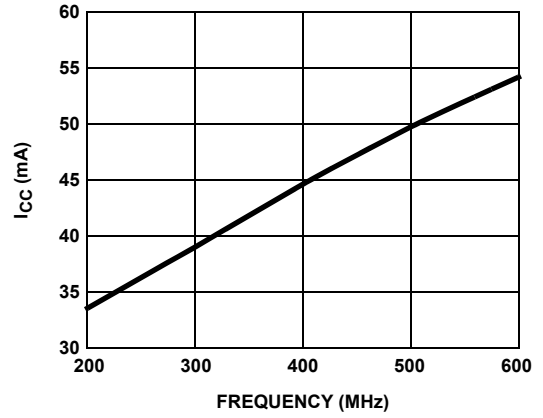


FIGURE 5. I_{CC} vs FREQUENCY (EXCLUDING I_{OUT})

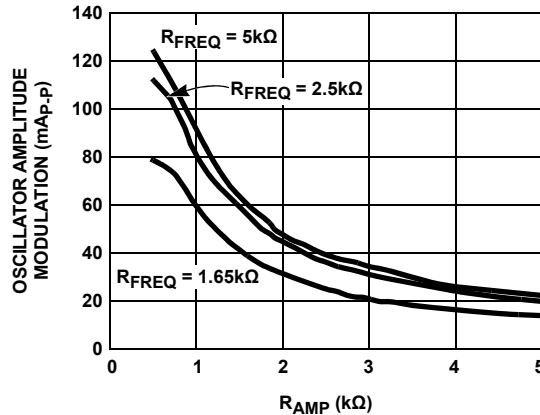


FIGURE 6. AMPLITUDE CONTROL

The ISL58831 oscillator frequency is controlled by the current being sourced at the R_{FREQ} pin. For a typical part, [Equation 1](#) (accurate to better than 5MHz at any frequency) should be used to determine the frequency of operation:

$$FREQ_{(MHz)} = -5.9672 \times 10^{-10} \times R_{FREQ}^3 + 1.5839 \times 10^{-5} \times R_{FREQ}^2 - 0.1596 \times R_{FREQ} + 841.34 \quad (EQ. 1)$$

Applications Information

Enable and Read Operation

The ENABLE line powers up the chip and supplies bias to all the circuits. After being enabled, read current can be obtained by applying a current to the I_{INR} input. The read power is usually operated in an automatic power control loop, by varying the current in the I_{INR} pin in response to the monitored laser light power. [Equation 2](#) is the defining equation for each amplifier:

$$I_{OUT} = \frac{V_{DAC}}{R_{SET} + R_{INx}} \times GAIN \quad (EQ. 2)$$

Oscillator Operation

Usually a laser will be noisy due to mode-hopping often caused by variable optical feedback into the laser. R_F current can be applied to reduce this noise effect by bringing the OSCEN pin high. The amplitude of the R_F is set by the R_{AMP} resistor and the frequency is set by the R_{FREQ} resistor. See the "[Typical Performance Curves](#)" on [page 8](#) for resistor set values.

R_F current is applied in a on/off fashion. Thus, if the R_F amplitude is 50mA_{P-P}, 50mA will be added to the read current for half the R_F cycle, and then 0mA will be added to the read current for half the R_F cycle. In this case, if the threshold current is only 40mA, the average laser power could exceed the intended read laser power by about 2mW, due to the 50% duty cycle current of 10mA above threshold. Therefore, in order to regulate the read power, it is necessary to make sure that the R_F amplitude is not much more than the required DC read current.

The circuit has a feature to increase the ability to turn off the laser for low threshold currents. At low read currents, the amplitude of the R_F will be reduced as the amplitude of the read current is reduced.

Write Levels

Typical applications will have at least two write powers. The recommended method to control the write power level is to assign Channel 2 to the lowest power level above read and add in Channel 3 to obtain the highest write power level. This spreads the gain over the most amplifiers, allows the largest current level to the laser, reduces the sensitivity of each input and provides the most protection to the laser in case of erroneous input commands.

Write Switching Waveforms

The WEN lines are applied to a fast comparator set to 1.67V. This makes it possible to have predictable rise and fall propagation delays from the WEN write pulse inputs to the laser.

Power Supply Decoupling

Due to the high values of current being switched rapidly on and off, it is important to ensure that the power supply is well decoupled to ground. During switching, the V_{DD} undergoes severe current transients, thus every effort should be made to decouple the V_{DD} as close to the package as possible, and to route the laser cathode to the decoupling capacitor with a short wide trace. Symptoms that could arise include poor rise/fall times, current overshoot and poor settling response. Since even a

well placed bypass capacitor will have a response limitation due to the lead inductance, it might be necessary to also place a lossy bead and a second decoupling capacitor on the supply side of the bead to prevent switching currents on the supply line from generating EMI.

Laser Diode Routing

It is very important to minimize the inductance of the trace between the IOUT pin and the laser diode. This trace acts as an antenna for EMI, inhibits the flow of R_F and pulse current to the laser and absorbs R_F current into ground. The ground return from the laser cathode to the chip and decoupling capacitors is best as a wide plane on both sides of the trace leading to the laser anode.

Ringing of the waveform might be observed on the IOUT pin. The best way is to check the optical output of the laser with an optical probe. If ringing is confirmed that cannot be reduced by an improved layout, the addition of an RC snubber network right at the output of the laser driver may be helpful. Be aware however, that the rise time might be affected and that the pulse power might be affected by pattern dependent voltage build-up on the snubber capacitor. Users should expect to lose 0.5ns of tr/ta for every 1cm of distance from IOUT to the laser diode and back to the V_{DD} decoupling capacitor.

Power Consumption Issues

The ISL58831 has been designed for low power consumption. When disabled, the part takes negligible power consumption, regardless of the state of the other pins. In addition, for V_{DD} < 3.5V, the ISL58831 will shut down to less than 1mA of supply current.

When in normal operation, the ISL58831 total power consumption depends strongly on the laser diode current and voltage. Since the total power consumption under worst case conditions could approach one watt, the burden is on the user to dissipate the heat into the board ground plane or chassis. An in-depth discussion of the effects of ground plane layout and size can be found in application note [AN1091](#).

An approximate equation for the device power consumption is shown in [Equation 3](#) (users must adjust accordingly for any duty cycle issues):

$$P_{DISS} = [(I_S + (14 \times \Sigma I_{IN})) \times V_{CC}] + [I_{DIODE} \times (V_{CC} - V_{DIODE})] \quad (EQ. 3)$$

Where:

I_S = I_{S2} when oscillator off, or I_{S3} when oscillator on (see [page 5](#))

ΣI_{IN} = Sum of all the I_{IN} currents

V_{DD} = Device power supply voltage

I_{DIODE} = Laser diode current

V_{DIODE} = Forward voltage of laser diode at current of I_{DIODE}

When using the ISL58831, the user must take extreme care not to exceed the maximum junction temperature of +150 °C. Since the case-to-ambient thermal coefficient will dominate, and since this is very much defined by the user's thermal engineering, it is not practical to define a strict limit on power consumption.

Furthermore, the case-to-ambient thermal coefficient may not be known precisely.

To assist in worst case conditions, it is possible to monitor the silicon temperature of the ISL58831 by forcing current into the ENABLE pin, which will then be at a voltage of $V_{DD} + V_{PN}$, where V_{PN} is the forward biased voltage of the ESD protection diode. Since ENABLE = HI is necessary for normal operation, the device can be operated as it would be in the real-life applications, while the temperature is monitored. The ISL58831 has been calibrated with a $1M\Omega$ resistor to +10V connected in series with the ENABLE pin, which results in an input current of approximately $4.5\mu A$.

Figure 7 allows the silicon temperature to be determined directly. The graph shows the measured ENABLE pin to VDD pin differential voltage, which shows a linear voltage sensitivity of $-2.26mV/^{\circ}C$. Users may wish to measure their specific part at $+20^{\circ}C$ (no warm-up) to allow for any statistical/process distribution, but the method is reliable and accurate.

By applying this method to the ISL58831 in an actual application, users can measure the silicon temperature under all operating conditions to determine whether their thermal engineering is sufficient. The thermal resistance of the QFN24 is $+140^{\circ}C/W$ when tested on a standard JEDEC JESD51-3 (single layer) test board. When using a standard JEDEC JESD51-7 (four layer) test board, the thermal resistance is $+112^{\circ}C/W$. Actual thermal resistance is highly dependent on circuit board layout considerations.

Temperature Measurement Set-Up and Results

Example: Measure ENABLE - V_{DD} under coolest condition of $V_{DD} = 0V$ and $V_{ENABLE} = 5V$ through $1M\Omega$. Suppose the result was $580mV$ at $T_{AMBIENT} = +20^{\circ}C$.

Now measure ENABLE - V_{DD} under the actual operating conditions. Suppose result (must be after thermal equilibrium has been reached) is $450mV$, and the new I_{CC} value is $100mA$.

Now one can calculate the temperature rise of $(450 \text{ to } 580) / -2.26 = +57^{\circ}C$. Using the power dissipation of $PW = (V_{DD} * I_{CC}) - (I_{CC} * V_{DD})$, the θ_{JA} of the application can be calculated.

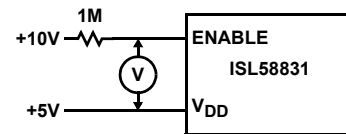
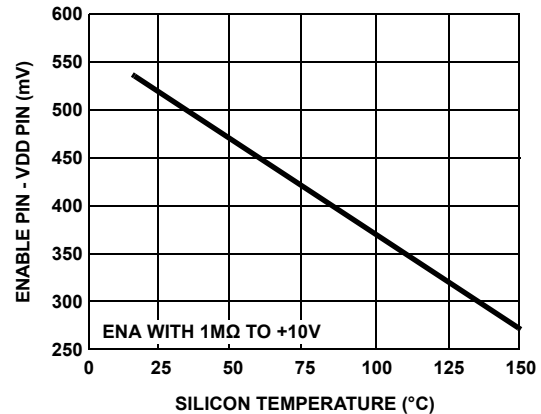


FIGURE 7. ISL58831 ON-CHIP THERMOMETER

Revision History

The revision history provided is for informational purposes only and is believed to be accurate, but not warranted. Please go to the web to make sure that you have the latest revision.

| DATE | REVISION | CHANGE |
|------------------|----------|--|
| January 28, 2016 | FN7440.1 | <p>Updated to newest template and order of content .</p> <p>Updated Ordering Information table - added quantity for Tape and Reel, added Tape and Reel and MSL notes.</p> <p>Page 5, above Electrical Spec table - changed "IMPORTANT NOTE: All parameters having Min/Max specifications are guaranteed. Typical values are for information purposes only. Unless otherwise noted, all tests are at the specified temperature and are pulsed tests, therefore: TJ = TC = TA." to: "NOTE: Compliance to datasheet limits is assured by one or more methods: production test, characterization and/or design."</p> <p>Page 6, Laser Current Amplifier Outputs AC Performance table, Output Current Overshoot - Changed Conditions from: See Application Notes to: Measured on 6.80 resistor load</p> <p>Page 8, Timing Diagram - corrected the polarity of the WEN2, WEN3 and WEN4 signals. Correct polarity is Active Low.</p> <p>Page 5, Added Thermal Information section, θ_{JA} (°C/W) of 42.</p> <p>Page 12, POD MDP0046 updated from rev 10 to rev 11. No changes to POD, only internal record.</p> |

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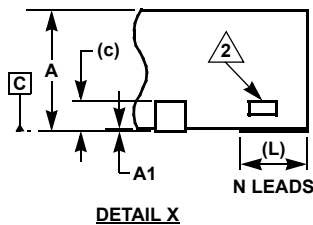
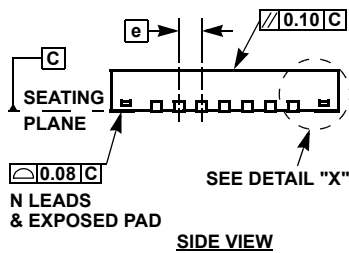
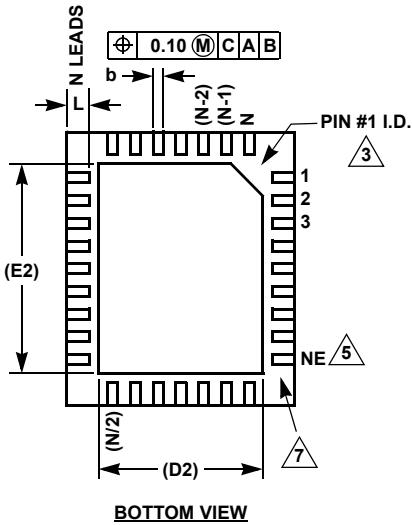
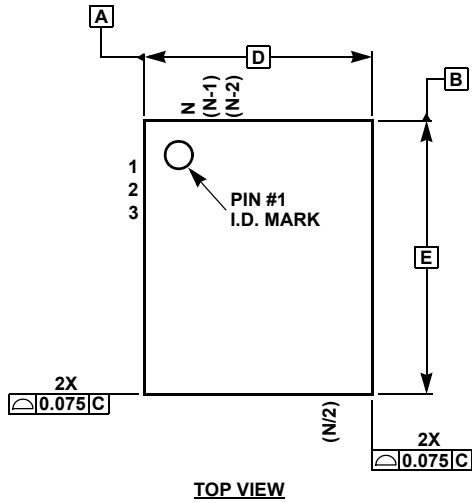
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QFN (Quad Flat No-Lead) Package Family



MDP0046

QFN (QUAD FLAT NO-LEAD) PACKAGE FAMILY
(COMPLIANT TO JEDEC MO-220)

| SYMBOL | MILLIMETERS | | | | TOLERANCE | NOTES |
|--------|-------------|-------|-------|-----------|-------------|-------|
| | QFN44 | QFN38 | QFN32 | | | |
| A | 0.90 | 0.90 | 0.90 | 0.90 | ±0.10 | - |
| A1 | 0.02 | 0.02 | 0.02 | 0.02 | +0.03/-0.02 | - |
| b | 0.25 | 0.25 | 0.23 | 0.22 | ±0.02 | - |
| c | 0.20 | 0.20 | 0.20 | 0.20 | Reference | - |
| D | 7.00 | 5.00 | 8.00 | 5.00 | Basic | - |
| D2 | 5.10 | 3.80 | 5.80 | 3.60/2.48 | Reference | 8 |
| E | 7.00 | 7.00 | 8.00 | 6.00 | Basic | - |
| E2 | 5.10 | 5.80 | 5.80 | 4.60/3.40 | Reference | 8 |
| e | 0.50 | 0.50 | 0.80 | 0.50 | Basic | - |
| L | 0.55 | 0.40 | 0.53 | 0.50 | ±0.05 | - |
| N | 44 | 38 | 32 | 32 | Reference | 4 |
| ND | 11 | 7 | 8 | 7 | Reference | 6 |
| NE | 11 | 12 | 8 | 9 | Reference | 5 |

| SYMBOL | MILLIMETERS | | | | TOLERANCE | NOTES | |
|--------|-------------|-------|-------|------|-----------|-------------|-------|
| | QFN28 | QFN24 | QFN20 | | | | QFN16 |
| A | 0.90 | 0.90 | 0.90 | 0.90 | 0.90 | ±0.10 | - |
| A1 | 0.02 | 0.02 | 0.02 | 0.02 | 0.02 | +0.03/-0.02 | - |
| b | 0.25 | 0.25 | 0.30 | 0.25 | 0.33 | ±0.02 | - |
| c | 0.20 | 0.20 | 0.20 | 0.20 | 0.20 | Reference | - |
| D | 4.00 | 4.00 | 5.00 | 4.00 | 4.00 | Basic | - |
| D2 | 2.65 | 2.80 | 3.70 | 2.70 | 2.40 | Reference | - |
| E | 5.00 | 5.00 | 5.00 | 4.00 | 4.00 | Basic | - |
| E2 | 3.65 | 3.80 | 3.70 | 2.70 | 2.40 | Reference | - |
| e | 0.50 | 0.50 | 0.65 | 0.50 | 0.65 | Basic | - |
| L | 0.40 | 0.40 | 0.40 | 0.40 | 0.60 | ±0.05 | - |
| N | 28 | 24 | 20 | 20 | 16 | Reference | 4 |
| ND | 6 | 5 | 5 | 5 | 4 | Reference | 6 |
| NE | 8 | 7 | 5 | 5 | 4 | Reference | 5 |

Rev 11 2/07

NOTES:

1. Dimensioning and tolerancing per ASME Y14.5M-1994.
2. Tiebar view shown is a non-functional feature.
3. Bottom-side pin #1 I.D. is a diepad chamfer as shown.
4. N is the total number of terminals on the device.
5. NE is the number of terminals on the "E" side of the package (or Y-direction).
6. ND is the number of terminals on the "D" side of the package (or X-direction). ND = (N/2)-NE.
7. Inward end of terminal may be square or circular in shape with radius (b/2) as shown.
8. If two values are listed, multiple exposed pad options are available. Refer to device-specific datasheet.