ISL59832

Dual Channel, Single Supply Video Reconstruction Filter with Charge Pump

FN6267
Rev 1.00
June 11, 2008

The ISL59832 is a dual channel, single supply video driver with reconstruction filter and charge pump. It is designed to drive SDTV displays with S-Video (Y/C) signals. It operates on a single supply (3.0V to 3.6V) and generates its own negative supply (-1.5V) using a regulated charge pump. Input signals can be AC- or DC-coupled. When AC-coupled, the sync tip clamp sets the blank level to ground at the output of Channel 1 thus ensuring that the sync-tip voltage level is set to approximately -300mV at the back-termination resistor of a standard video load. Channel 1 also has a sync detector whose output is available at SYNC_OUT pin. In a typical application where the luma is connected to Channel 1, and chrominance is connected to Channel 2, SYNC_IN is connected to SYNC_OUT thus providing timing to Channel 2. Channel 2 has a keyed clamp which sets the output to ground when SYNC_IN is driven to the logic high state. The ISL59832 is capable of driving two DC- or AC-coupled standard video loads. The ISL59832 features a 4th order Butterworth reconstruction filter that provides a 9MHz nominal -3dB frequency and 40dB of attenuation at 27MHz. Nominal operational current is 31mA. When powered down, the device draws 1µA maximum supply current. The ISL59832 is available in 16 Ld TQFN package.

Ordering Information

PART NUMBER	PART MARKING	TEMP. RANGE (°C)	PACKAGE (Pb-Free)	PKG. DWG. #
ISL59832IRZ	59 832IRZ	-40 to +85	16 Ld TQFN	MDP0046

NOTE: These Intersil Pb-free plastic packaged products employ special Pb-free material sets, molding compounds/die attach materials, and 100% matte tin plate plus anneal (e3 termination finish, which is RoHS compliant and compatible with both SnPb and Pb-free soldering operations). Intersil Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020.

Applications

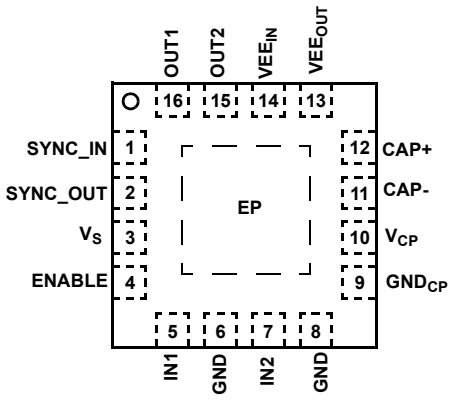
- Set Top Box Receiver
- Television
- DVD Player

Features

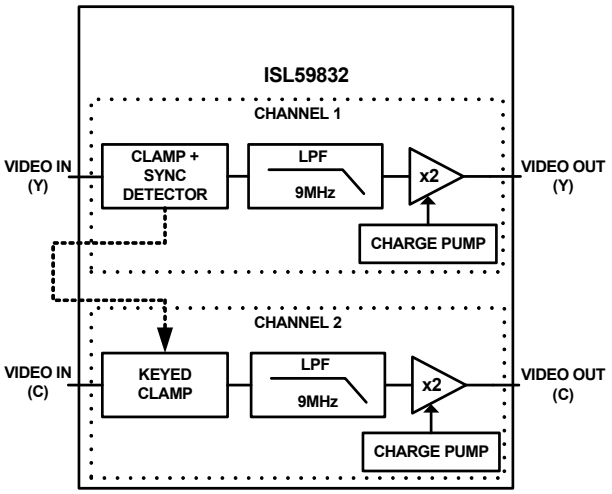
- 3.3V Nominal Supply, Operates Down to 3.0V
- DC-Coupled Outputs
- Inputs can be AC- or DC-Coupled
- Eliminates the Need for Large Output Coupling Capacitors
- Integrated Sync Tip Clamp sets Backporch to Ground at the Output For Channel 1 for $1V_{P-P}$ Standard Video Signal
- Integrated Keyed Clamp Puts Channel 2 Output to Ground During Sync
- Each Output Drives 2 Standard Video Loads
- Response Flat to 5MHz, with 40dB Attenuation at 27MHz
- Pb-Free (RoHS compliant)

Pinout

ISL59832
(16 LD TQFN)
TOP VIEW



Block Diagram



Absolute Maximum Ratings (T_A = +25°C)

V_S to GND 4V
V_{IN} to GND. . . . . GND - 0.3V to V_S + 0.3V
Maximum Continuous Output Current . . . . . ±50mA
Maximum Current into Any Pin . . . . . ±50mA
ESD Rating
Human Body Model (Per MIL-STD-883 Method 3015.7) . . .3500V
Machine Model (Per EIAJ ED-4701 Method C-111). 350V

Thermal Information

or Thermal Resistance (Typical, Note 1)	θ_{JA} (°C/W)
16 Lead TQFN Package	46

Maximum Junction Temperature (Plastic Package) . . . . . .+150°C
Maximum Storage Temperature Range. . . . . .-65°C to +150°C
Pb-free reflow profile . . . . . .see link below
http://www.intersil.com/pbfree/Pb-FreeReflow.asp

Operating Conditions

Temperature Range . . . . . .-40°C to +85°C

CAUTION: Do not operate at or near the maximum ratings listed for extended periods of time. Exposure to such conditions may adversely impact product reliability and result in failures not covered by warranty.

IMPORTANT NOTE: All parameters having Min/Max specifications are guaranteed. Typical values are for information purposes only. Unless otherwise noted, all tests are at the specified temperature and are pulsed tests, therefore: $T_J = T_C = T_A$

NOTES:

1. θ_{JA} is measured in free air with the component mounted on a high effective thermal conductivity test board with “direct attach” features. See Tech Brief TB379.
2. Parameters with MIN and/or MAX limits are 100% tested at +27°C, unless otherwise specified. Temperature limits established by characterization and are not production tested.

Electrical Specifications

$V_S = V_{CP}$ = 3.3V, C_F = 0.1µF, C_S = 0.22µF, C_{FIL} = 0.4µF, $C_{IN1} = C_{IN2}$ = 0.1µF, $R_{L1} = R_{L2}$ = 150Ω, Typical T_A = +27°C.

SYMBOL	PARAMETER	CONDITIONS	MIN (Note 2)	TYP	MAX (Note 2)	UNIT
DC CHARACTERISTICS						
V_S, V_{CP}	Supply Range	guaranteed by PSRR	3.0	3.3	3.6	V
VEE_{OUT}	Charge Pump Output		-1.75	-1.5	-1.25	V
I_S	Supply Current	No load		14	16	mA
I_{CP}	Charge Pump Supply Current	No load		17	20	mA
I_{PD}	Power-Down Current	ENABLE = 0.4V		0.3	2.5	µA
I_{IN}	Input Pull-down Current	Channel 1, V_{IN} = 0.5V	0.4	4	10	µA
I_B	Input Bias Current	Channel 2, V_{IN} = 0.5V, SYNC_IN = 0V	-10	-3	10	µA
A_V	DC Gain		1.94	2	2.05	V/V
V_{IN_MAX}	Max DC Input Range	DC-Coupled Input, guaranteed by DC gain test	1.4			V
$V_{CLAMPOUT1}$	Output Sync Tip Clamp Level (Channel 1)	$V_{IN} \leq 0$, AC-coupled input	-650	-590	-525	mV
$V_{CLAMPOUT2}$	Keyed Clamp Level (Channel 2)	Output level when SYNC_IN = 2.0V	-60	-25	0	mV
$V_{CLAMPIN}$	Input Clamp Level	Input floating	0	30	70	mV
$V_{CLAMPIN2}$	Input Keyed Clamp Level (Channel 2)	Input floating, input level when SYNC_IN ≥ 2.0V	275	300	375	mV
V_{OS}	Output Level Shift (Channel 1)	$V_{IN} > 0$, output shifted relative to input, DC-coupled input	-685	-620	-550	mV
	Output Level Shift (Channel 2)	$V_{IN} > 0$, output shifted relative to input, DC-coupled input	-380	-330	-280	mV

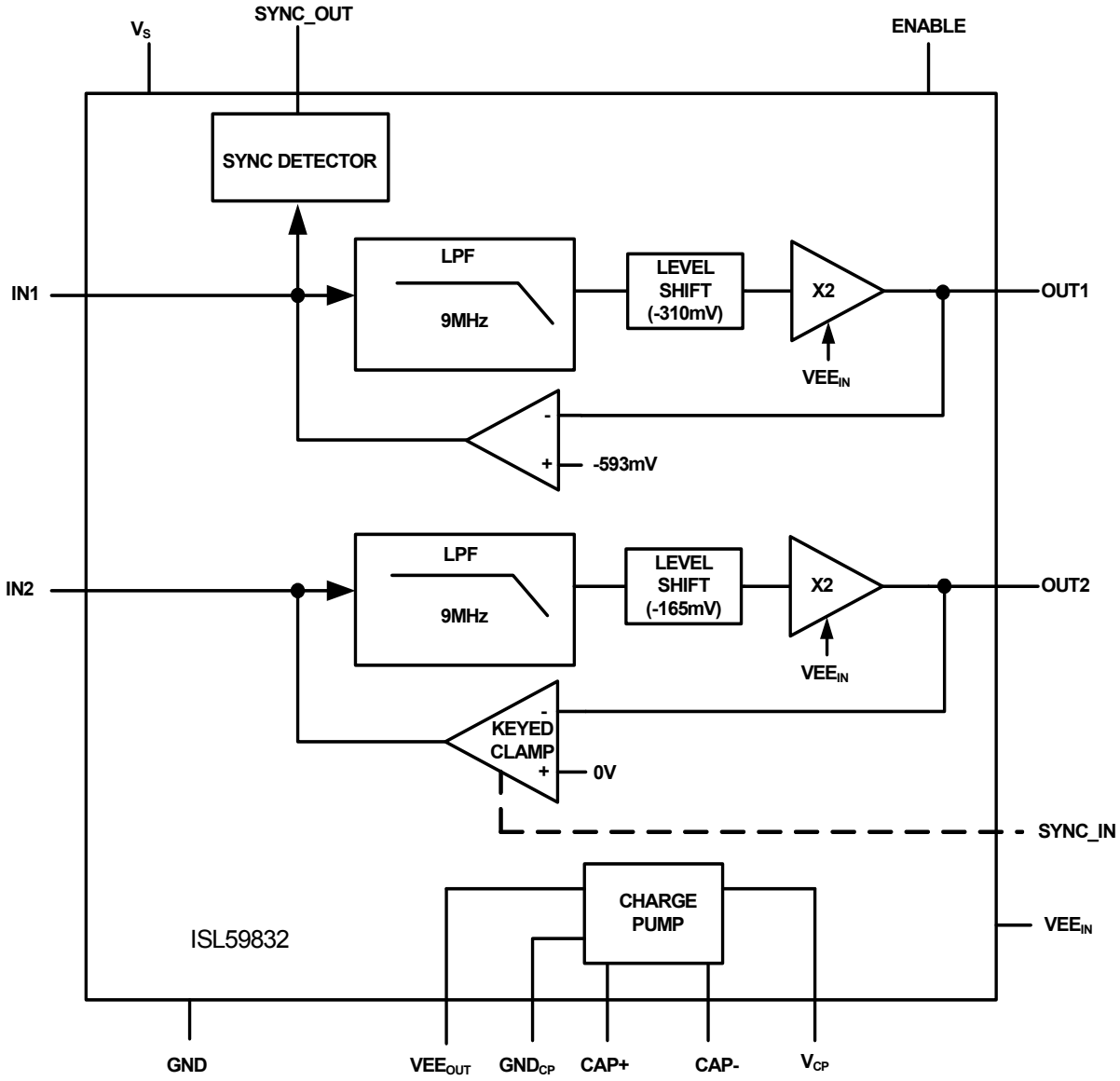
Electrical Specifications $V_S = V_{CP} = 3.3V$, $C_F = 0.1\mu F$, $C_S = 0.22\mu F$, $C_{FIL} = 0.4\mu F$, $C_{IN1} = C_{IN2} = 0.1\mu F$, $R_{L1} = R_{L2} = 150\Omega$, Typical $T_A = +27°C$. **(Continued)**

SYMBOL	PARAMETER	CONDITIONS	MIN (Note 2)	TYP	MAX (Note 2)	UNIT
I_{CLAMP}	Clamp Restore Current	Force V_{IN} = -0.3V, Channel 1		-5	-2.5	mA
		Force V_{IN} = 1V, Channel 2	135	180		µA
		Force V_{IN} = -0.3V, Channel 2		-200	-160	µA
V_{SLICE}	Sync Detect Threshold	Channel 1	100		200	mV
$PSRR_{DC}$	Power Supply Rejection	VS = +3.0 to +3.6	50	77		dB
AC CHARACTERISTICS						
A_{PB}	Passband Flatness	f = 5MHz, relative to 100kHz	0	0.8	1.25	dB
A_{SB}	Stopband Attenuation	f ≥ 27MHz relative to 100kHz		-50	-35	dB
dG	Differential Gain	11-step modulated staircase		0.45		%
dP	Differential Phase	11-step modulated staircase		-0.15		°
SNR	Signal To Noise Ratio	Peak signal ($1.4V_{P-P}$) to RMS noise, f = 10kHz to 10MHz		66		dB
GD_{MATCH}	DC Group Delay Match	Channel-to-channel group delay matching at 100kHz		0.1		ns
∆GD	Group Delay Deviation	Deviation from 100kHz to 3.58MHz		8		ns
PSRR	Power Supply Rejection	V_{IN} = $100mV_{P-P}$ sine wave, f = 100kHz to 5MHz		35		dB
X_{TALK}	Channel-to-Channel Crosstalk	f = 100kHz to 5MHz		-60		dB
V_{NOISE}	Input Voltage Noise			0.66		mV_{RMS}
LOGIC (ENABLE, SYNC_IN)						
V_{IL}	Logic Low Input Voltage				0.8	V
V_{IH}	Logic High Input Voltage		2.0			V
I_I	Logic Input Current		-1		1	µA
CHARGE PUMP						
f_{CP}	Charge Pump Clock Frequency			12.5		MHz

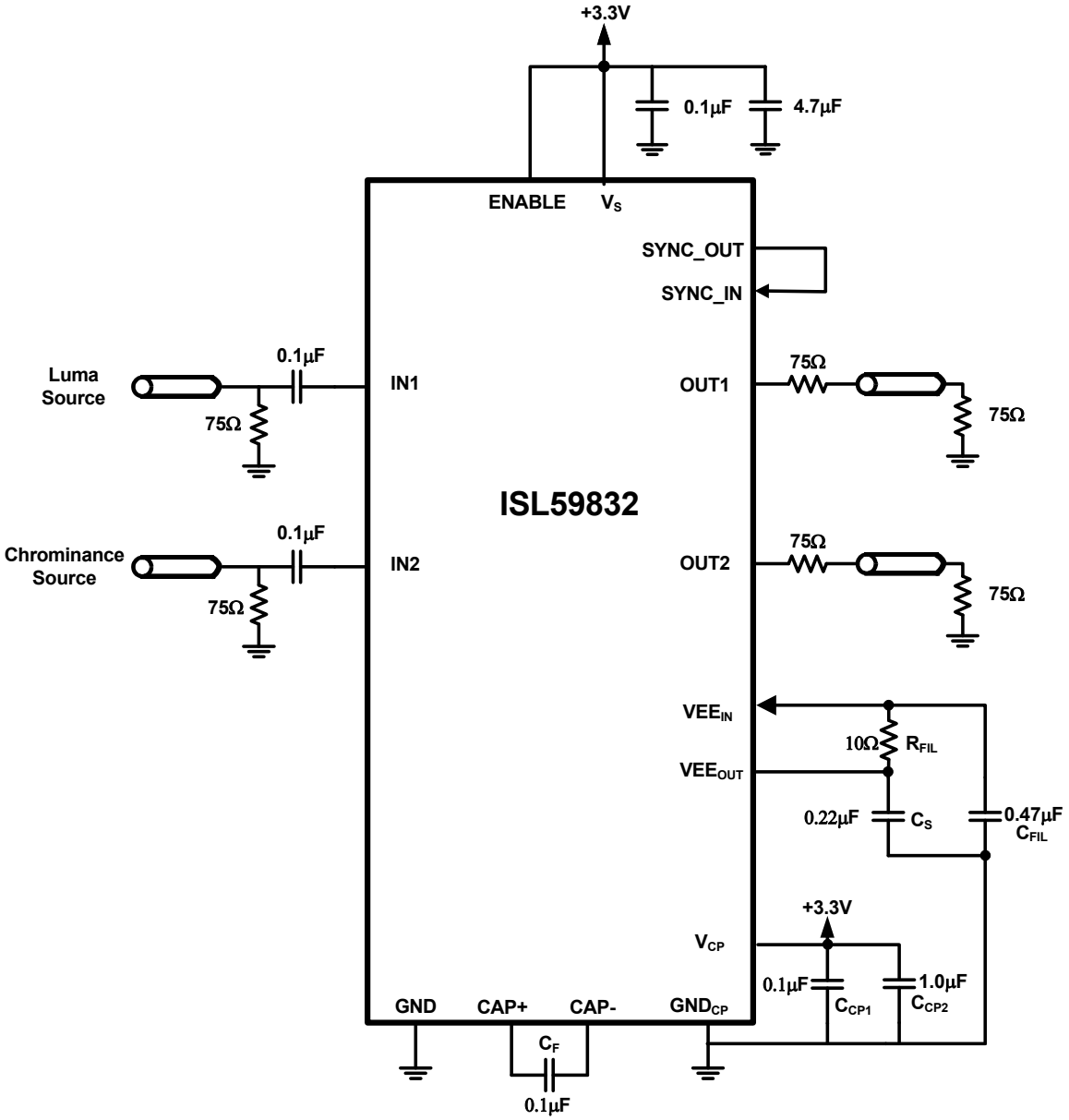
Pin Descriptions

NUMBER	NAME	FUNCTION
1	SYNC_IN	Sync Input. Sync timing logic input for Channel 2.
2	SYNC_OUT	Sync Output. Sync-detection logic output from Channel 1.
3	V_S	Positive Power Supply. Bypass to GND with a 0.1µF capacitor.
4	ENABLE	Enable. Connect to V_S to enable device.
5	IN1	Video Input 1. Luma Channel.
6, 8	GND	Ground
7	IN2	Video Input 2. Chroma Channel.
9	GND_{CP}	Charge Pump Ground.
10	V_{CP}	Charge Pump Power Supply. Bypass with a 0.1µF capacitor to GND_{CP}.
11	CAP-	Charge-Pump Flying Capacitor Negative Terminal. Connect a 0.1µF capacitor from CAP+ to CAP-
12	CAP+	Charge-Pump Flying Capacitor Positive Terminal. Connect a 0.1µF capacitor from CAP+ to CAP-
13	VEE_{OUT}	Charge Pump Negative Output. Bypass with a 0.22µF capacitor to GND.
14	VEE_{IN}	Negative Supply. Connect an RC filter between VEE_{IN} and VEE_{OUT}. See “S-Video Typical Application Circuit” on page 6.
15	OUT2	Video Output 2
16	OUT1	Video Output 1
-	EP	Exposed Pad. Connect to VEE_{IN}

Block Diagram



S-Video Typical Application Circuit



Typical Performance Curves $V_{CP} = V_S = 3.3V$, $C_F = 0.1\mu F$, $C_S = 0.22\mu F$, $C_{FIL} = 0.4\mu F$, $C_{IN1} = C_{IN2} = 0.1\mu F$, $R_{L1} = R_{L2} = 150\Omega$.

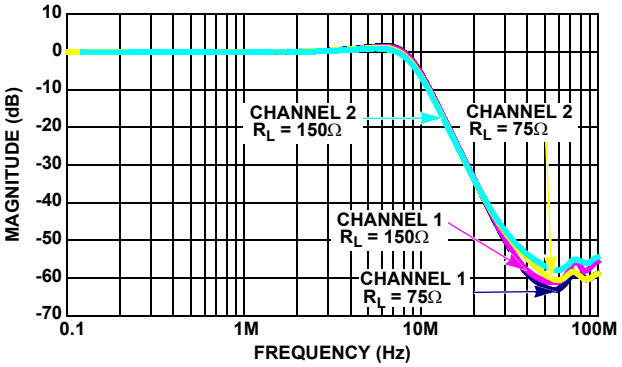


FIGURE 1. BANDWIDTH vs FREQUENCY

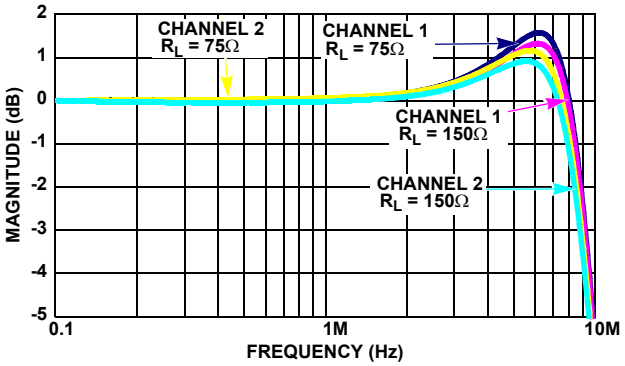


FIGURE 2. GAIN FLATNESS vs FREQUENCY

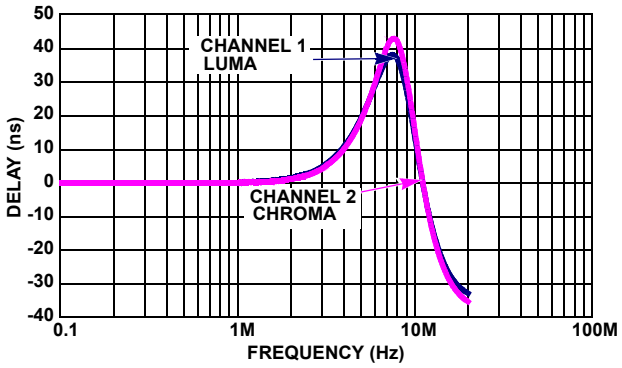


FIGURE 3. GROUP DELAY vs FREQUENCY

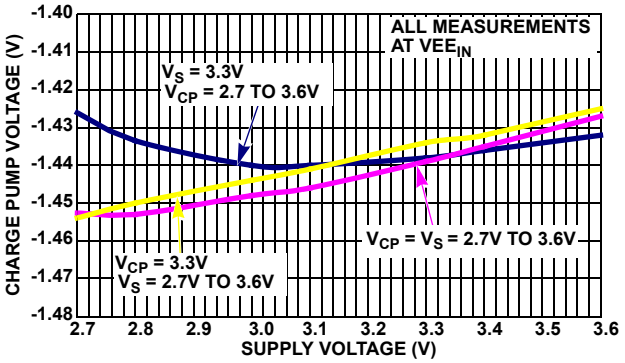


FIGURE 4. CHARGE PUMP VOLTAGE vs SUPPLY VOLTAGE

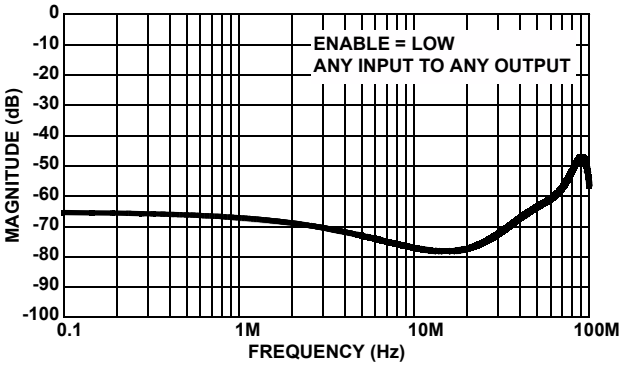


FIGURE 5. INPUT-TO-OUTPUT ISOLATION vs FREQUENCY

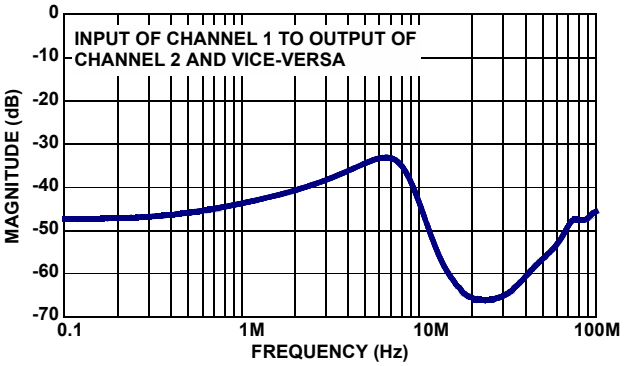


FIGURE 6. LUMA-TO-CHROMA CROSSTALK

Typical Performance Curves $V_{CP} = V_S = 3.3V$, $C_F = 0.1\mu F$, $C_S = 0.22\mu F$, $C_{FIL} = 0.4\mu F$, $C_{IN1} = C_{IN2} = 0.1\mu F$, $R_{L1} = R_{L2} = 150\Omega$.

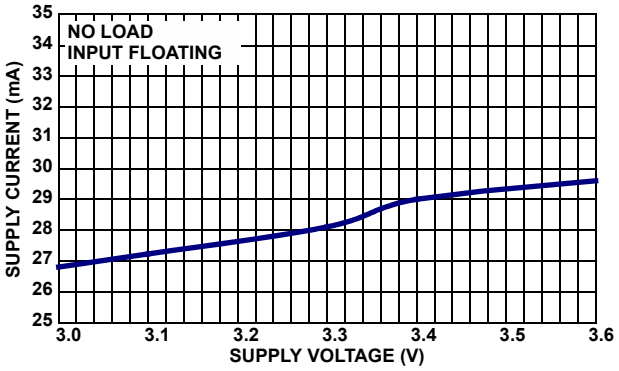


FIGURE 7. SUPPLY CURRENT vs SUPPLY VOLTAGE

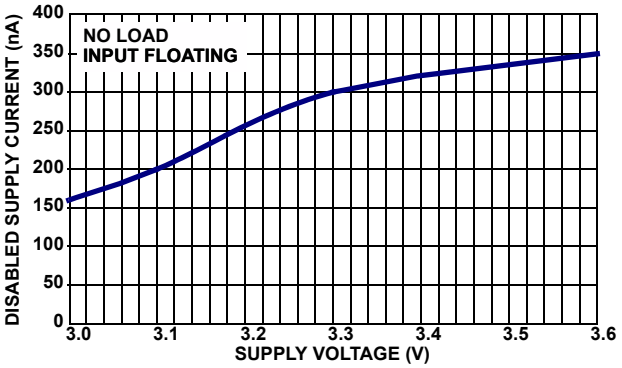


FIGURE 8. DISABLED SUPPLY CURRENT vs SUPPLY VOLTAGE

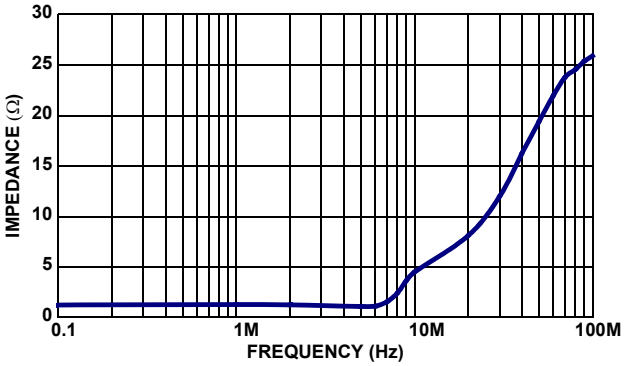


FIGURE 9. OUTPUT IMPEDANCE vs FREQUENCY

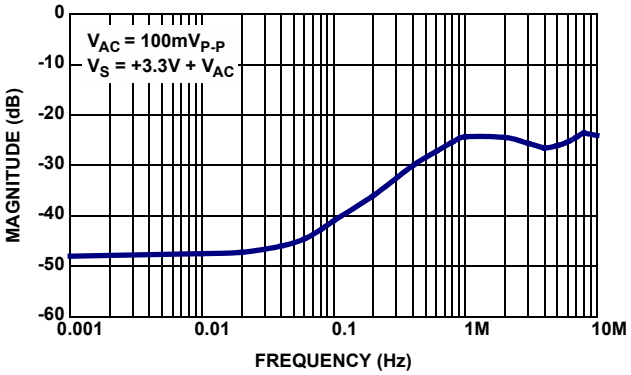


FIGURE 10. POWER SUPPLY REJECTION RATIO vs FREQUENCY

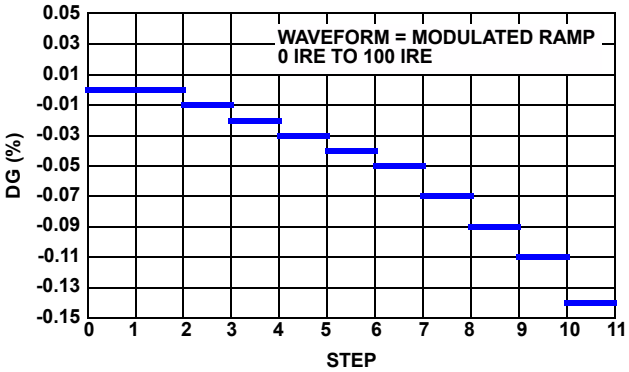


FIGURE 11. DIFFERENTIAL GAIN

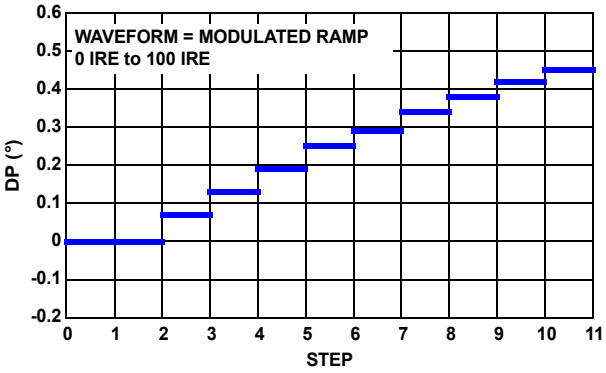


FIGURE 12. DIFFERENTIAL PHASE

Typical Performance Curves $V_{CP} = V_S = 3.3V$, $C_F = 0.1\mu F$, $C_S = 0.22\mu F$, $C_{FIL} = 0.4\mu F$, $C_{IN1} = C_{IN2} = 0.1\mu F$, $R_{L1} = R_{L2} = 150\Omega$.

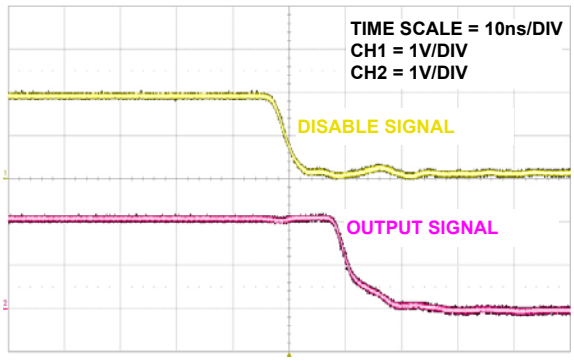


FIGURE 13. DISABLE TIME

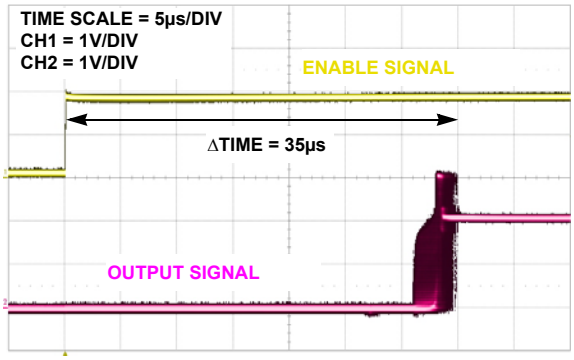


FIGURE 14. ENABLE TIME

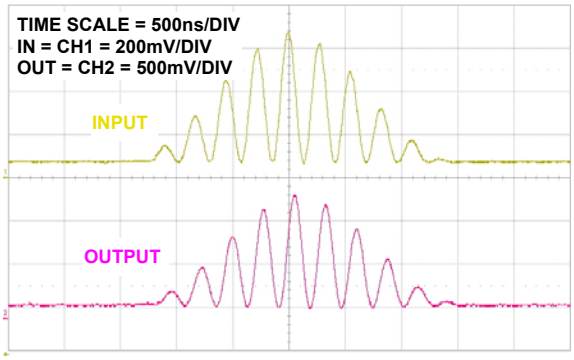


FIGURE 15. 12.5T RESPONSE

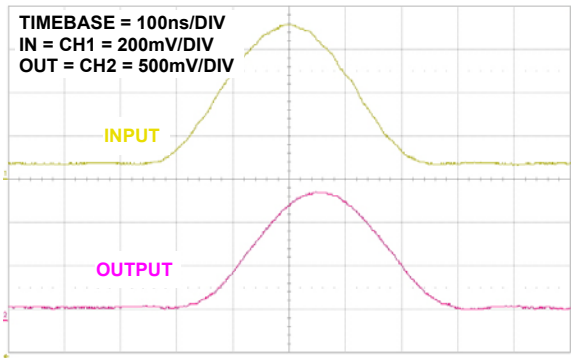


FIGURE 16. 2T RESPONSE

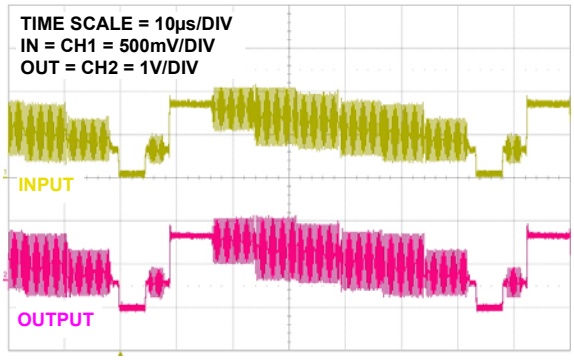


FIGURE 17. NTSC COLORBAR

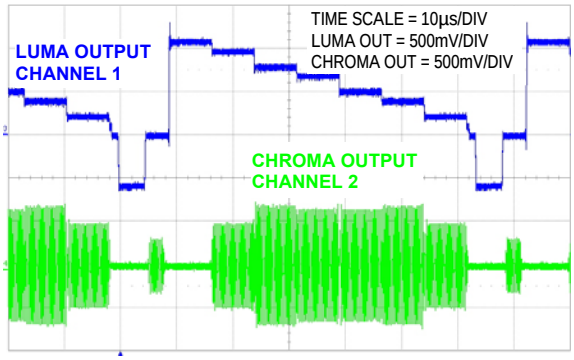


FIGURE 18. S-VIDEO SCOPE SHOT

Typical Performance Curves $V_{CP} = V_S = 3.3V$, $C_F = 0.1\mu F$, $C_S = 0.22\mu F$, $C_{FIL} = 0.4\mu F$, $C_{IN1} = C_{IN2} = 0.1\mu F$, $R_{L1} = R_{L2} = 150\Omega$.

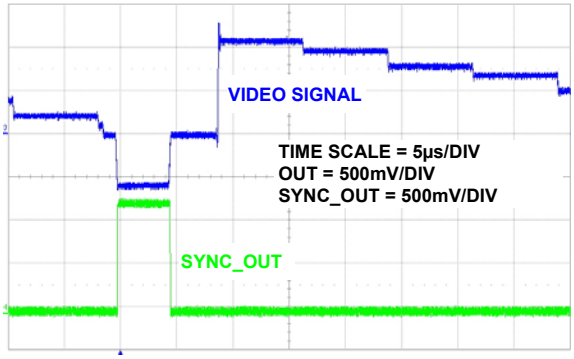


FIGURE 19. SYNC_OUT SIGNAL

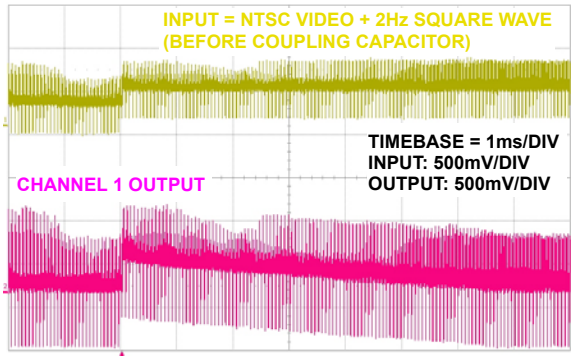


FIGURE 20. LUMA CLAMP RESPONSE TO POSITIVE TRANSIENT (CHANNEL 1)

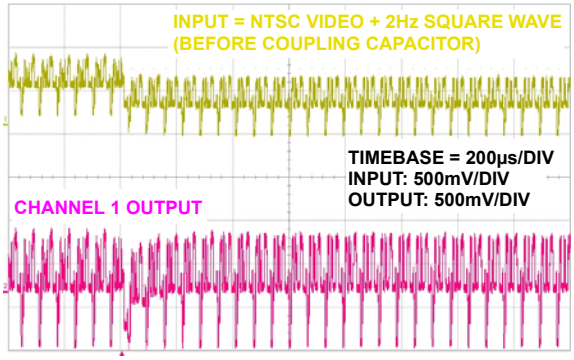


FIGURE 21. LUMA CLAMP RESPONSE TO NEGATIVE TRANSIENT (CHANNEL 1)

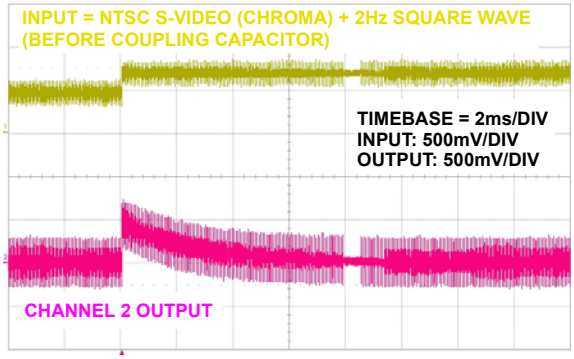


FIGURE 22. CHROMA CLAMP RESPONSE TO POSITIVE TRANSIENT (CHANNEL 2)

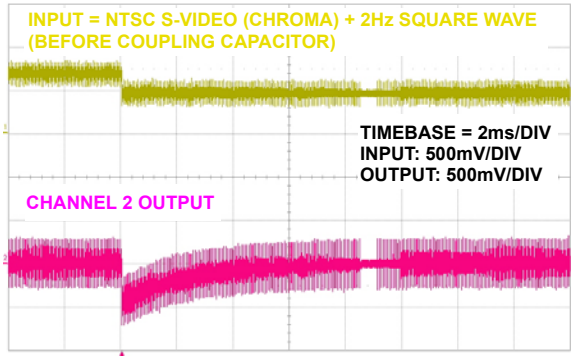


FIGURE 23. CHROMA CLAMP RESPONSE TO NEGATIVE TRANSIENT (CHANNEL 2)

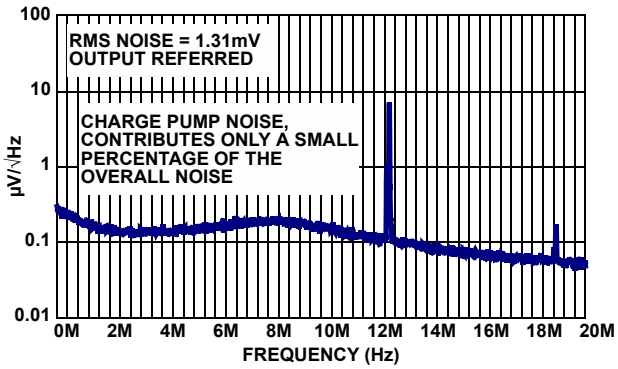


FIGURE 24. NOISE SPECTRUM

Typical Performance Curves $V_{CP} = V_S = 3.3V$, $C_F = 0.1\mu F$, $C_S = 0.22\mu F$, $C_{FIL} = 0.4\mu F$, $C_{IN1} = C_{IN2} = 0.1\mu F$, $R_{L1} = R_{L2} = 150\Omega$.

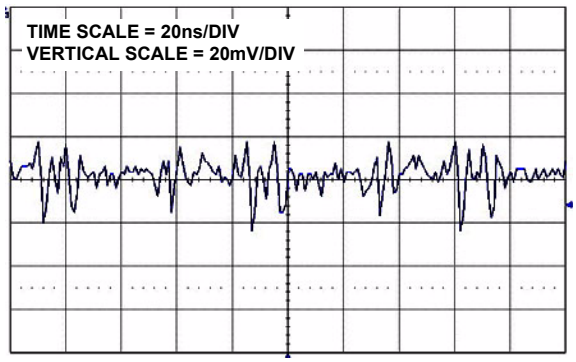


FIGURE 25. CHARGE PUMP FEEDTHROUGH AT AMPLIFIER OUTPUT

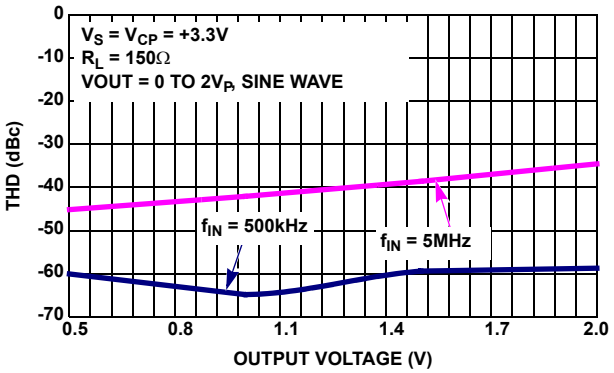


FIGURE 26. THD (dBc) vs OUTPUT VOLTAGE (V_{P-P})

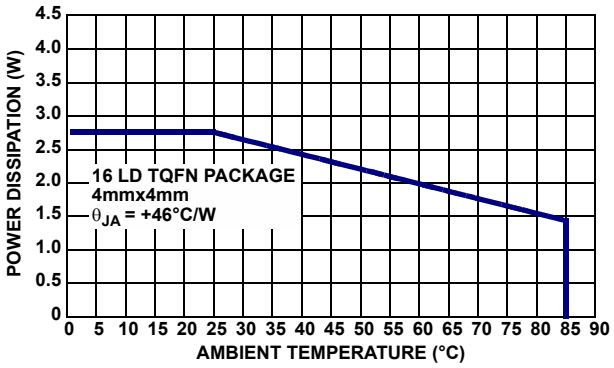


FIGURE 27. PACKAGE POWER DISSIPATION vs AMBIENT TEMPERATURE

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Description of Operation and Application Information

Theory of Operation

The ISL59832 is a single supply video driver with a reconstruction filter and an on-board charge pump. It is designed to drive SDTV displays with S-video (Y-C) or composite video (CV) signals. The input signals can be AC or DC-coupled. When AC-coupled, a sync tip clamp forces the blank level to ground at the output of Channel 1 and a keyed clamp forces the average level of Channel 2 to ground. The ISL59832 is capable of driving two AC- or DC-coupled standard video loads and has a 4th order Butterworth reconstruction filter with nominal -3dB frequency set to 10MHz, providing 40dB of attenuation at 27MHz. The ISL59832 is designed to operate with a single supply voltage range ranging from 3.0V to 3.6V. This eliminates the need for a split supply with the incorporation of a charge pump capable of generating a bottom rail as much as 1.5V below ground; providing a 4.8V range on a single 3.3V supply. This performance is ideal for NTSC video with negative-going sync pulses.

Output Amplifier

The ISL59832 output amplifiers provide a gain of +6dB. The Channel 1 output amplifier is able to drive a $2.8V_{P-P}$ video signal into a 150Ω load to ground, while the Channel 2 amplifier is able to drive a $2.8V_{P-P}$ into a 150Ω or 75Ω load to ground.

The outputs are highly-stable, low distortion, low power, high frequency amplifiers capable of driving moderate (10pF) capacitive loads.

Input/Output Range

The ISL59832 inputs have a dynamic range of 0 to $1.4V_{P-P}$. This allows the device to handle the maximum possible video signal inputs. As the input signal moves outside the specified range, the output signal will exhibit increasingly higher levels of harmonic distortion.

The Charge Pump

The ISL59832 charge pump provides a bottom rail up to 1.5V below ground while operating on a 3.0V to 3.6V power supply. The charge pump is driven by an internal 13MHz clock.

To reduce the noise on the power supply generated by the charge pump connect a lowpass RC-network between VEE_{OUT} and VEE_{IN}. See the Typical Application Circuit for further information.

VEE_{OUT} Pin

VEE_{OUT} is the output pin for the charge pump. Keep in mind that the output of this pin is a fully regulated supply that must be properly bypassed. Bypass this pin with a 0.47µF ceramic capacitor placed as close to the pin and connected to the ground plane of the board.

VEE_{IN} Pin

VEE_{IN} is the subtrate connection for the ISL59832. To reduce the noise on the power supply generated by the charge pump, connect a lowpass RC-network between VEE_{OUT} and VEE_{IN}. See the “S-Video Typical Application Circuit” on page 6 for further information.

Video Performance

DIFFERENTIAL GAIN/PHASE

For good video performance, an amplifier is required to maintain the same output impedance and the same frequency and phase response as DC levels are changed at the output. Special circuitry has been incorporated into the ISL59832 to reduce the output impedance variation with the current output. This results in outstanding differential gain and differential phase specifications of 0.45% and 0.15°, while driving 150Ω at a gain of +2V/V.

NTSC

The ISL59832, generating a negative rail internally, is ideally suited for NTSC video with its accompanying negative-going sync signals.

S-VIDEO

For a typical S-video application, connect the luma signal to Channel 1, and connect the chrominance signal to Channel 2. For clamp timing connect SYNC_OUT to SYNC_IN. See the “S-Video Typical Application Circuit” on page 6.

AC-Coupled Inputs

SYNC TIP CLAMP (CHANNEL 1)

The ISL59832 features a sync tip clamp that sets the black level of the output video signal to ground. This ensures that the sync-tip voltage level will be approximately -300mV at the back-termination resistor of a standard video load. The clamp is activated whenever the input voltage falls below 0V. The correction voltage required to do this is stored across the input AC-coupling capacitor. Refer to “S-Video Typical Application Circuit” on page 6 for a detailed diagram.

KEYED CLAMP (CHANNEL 2)

Channel 2 has a keyed clamp which sets the output to ground when SYNC_IN is driven to the logic high state. SYNC_IN may be connected to SYNC_OUT which ensures that Channel 2 clamps during the sync interval for Y-C applications.

SYNC DETECTOR AND CLAMP TIMING

Channel 1 and Channel 3 also have sync detectors whose outputs are available at SYNC_OUT.

The slice level for the sync detector is between 100 to 200mV. This means that if the signal level is below 100mV at Channel 1, then SYNC_OUT is high. If the signal level is above 200mV then SYNC_OUT is low. Figure 28 shows the operation of the sync detector.

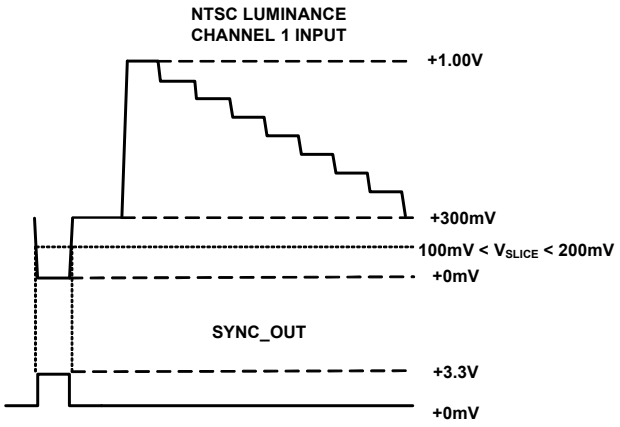


FIGURE 28. SYNC DETECTOR SLICE LEVEL

DC-Coupled Inputs (Channel 1)

When DC-coupling the inputs ensure that the lowest signal level is greater than +50mV to prevent the clamp from turning on and distorting the output. When DC-coupled the ISL59832 shifts the signal by -620mV.

Amplifier Disable

The ISL59832 can be disabled and its outputs placed in high impedance states. The turn-off time is around 10ns and the turn-on time is around 35µs. The turn-on time is longer because extra time is needed for the charge pump to settle before the amplifiers are enabled. When disabled, the device supply current is reduced to 2µA typically, reducing power consumption. The device's power-down can be controlled by standard TTL or CMOS signal levels at the ENABLE pin. The applied logic signal is relative to the GND pin. Applying a signal that is less than 0.8V above GND will disable the device. The device will be enabled when the ENABLE signal is 2V above GND.

Output Drive Capability

The maximum output current for the ISL59832 is ±50mA. Maximum reliability is maintained if the output current never exceeds ±50mA, after which the electro-migration limit of the process will be exceeded and the part will be damaged. This limit is set by the design of the internal metal interconnections.

Driving Capacitive Loads and Cables

The ISL59832, internally-compensated to drive 75Ω cables, will drive 10pF loads in parallel with 150Ω or 75Ω with less than 1.3dB of peaking.

Power Dissipation

With the high output drive capability of the ISL59832, it is possible to exceed the +150°C absolute maximum junction temperature under certain load current conditions. Therefore, it is important to calculate the maximum junction temperature for an application to determine if load conditions or package types need to be modified to assure operation of the amplifier in a safe operating area.

The maximum power dissipation allowed in a package is determined according to Equation 1:

$$PD_{MAX} = \frac{T_{JMAX} - T_{AMAX}}{\Theta_{JA}} \quad \text{(EQ. 1)}$$

Where:

T_{JMAX} = Maximum junction temperature

T_{AMAX} = Maximum ambient temperature

Θ_{JA} = Thermal resistance of the package

The maximum power dissipation actually produced by an IC is the total quiescent supply current times the total power supply voltage, plus the power in the IC due to the load, or:

for sourcing:

$$PD_{MAX} = V_S \times I_{SMAX} + (V_S - V_{OUT}i) \times \frac{V_{OUT}i}{R_L i} \quad \text{(EQ. 2)}$$

for sinking:

$$PD_{MAX} = V_S \times I_{SMAX} + (V_{OUT}i - V_S) \times I_{LOAD}i \quad \text{(EQ. 3)}$$

Where:

V_S = Supply voltage

I_{SMAX} = Maximum quiescent supply current

V_{OUT} = Maximum output voltage of the application

R_{LOAD} = Load resistance tied to ground

I_{LOAD} = Load current

i = Number of output channels

By setting Equation 1 equal to Equation 2 and 3, we can solve for the output current and R_{LOAD} values needed to avoid exceeding the maximum junction temperature.

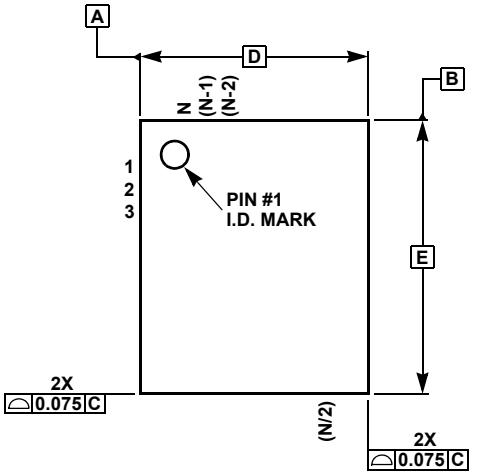
Power Supply Bypassing and Printed Circuit Board Layout

As with any high frequency device, a good printed circuit board layout is necessary for optimum performance. Strip line design techniques are recommended for the input and output signal traces to help control the characteristic impedance. Furthermore, the characteristic impedance of the traces should be 75Ω. Trace lengths should be as short as possible between the output pin and the series 75Ω resistor. The power supply pin must be well bypassed to reduce the risk of oscillation. For normal single supply operation, a single 4.7µF tantalum capacitor in parallel with a 0.1µF ceramic capacitor from V_S and V_{CP} to GND will suffice.

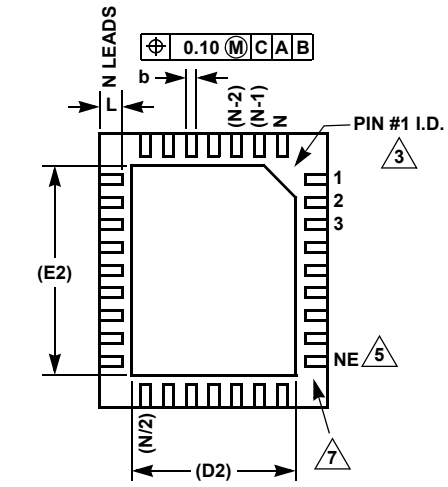
The AC performance of this circuit depends greatly on the care taken in designing the PC board. The following are recommendations to achieve optimum high frequency performance from your PC board.

- Use low inductance components, such as chip resistors and chip capacitors whenever possible.
- Minimize signal trace lengths. Trace inductance and capacitance can easily limit circuit performance. Avoid sharp corners; use rounded corners when possible. Vias in the signal lines add inductance at high frequency and should be avoided. PCB traces longer than 1" begin to exhibit transmission line characteristics with signal rise/fall times of 1ns or less. To maintain frequency performance with longer traces, use striplines.
- Match channel-to-channel analog I/O trace lengths and layout symmetry. This will minimize propagation delay mismatches.
- Route all signal I/O lines over continuous ground planes (i.e. no split planes or PCB gaps under these lines).
- Place termination resistors in their optimum location as close to the device as possible.
- Use good quality connectors and cables, matching cable types and keeping cable lengths to a minimum when testing.
- Place flying and output capacitor as close to the device as possible for the charge pump.
- Decouple well, using a minimum of 2 power supply decoupling capacitors, placed as close to the device as possible. Avoid vias between the capacitor and the device because vias adds unwanted inductance. Larger caps may be farther away. When vias are required in a layout, they should be routed as far away from the device as possible.

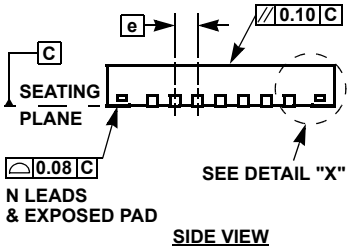
QFN (Quad Flat No-Lead) Package Family



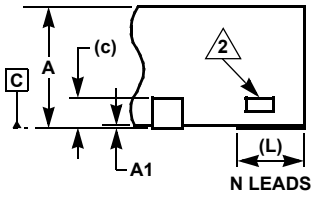
TOP VIEW



BOTTOM VIEW



SIDE VIEW



DETAIL X

MDP0046

QFN (QUAD FLAT NO-LEAD) PACKAGE FAMILY
(COMPLIANT TO JEDEC MO-220)

SYMBOL	MILLIMETERS				TOLERANCE	NOTES
	QFN44	QFN38	QFN32			
A	0.90	0.90	0.90	0.90	±0.10	-
A1	0.02	0.02	0.02	0.02	+0.03/-0.02	-
b	0.25	0.25	0.23	0.22	±0.02	-
c	0.20	0.20	0.20	0.20	Reference	-
D	7.00	5.00	8.00	5.00	Basic	-
D2	5.10	3.80	5.80	3.60/2.48	Reference	8
E	7.00	7.00	8.00	6.00	Basic	-
E2	5.10	5.80	5.80	4.60/3.40	Reference	8
e	0.50	0.50	0.80	0.50	Basic	-
L	0.55	0.40	0.53	0.50	±0.05	-
N	44	38	32	32	Reference	4
ND	11	7	8	7	Reference	6
NE	11	12	8	9	Reference	5

SYMBOL	MILLIMETERS					TOLER-ANCE	NOTES
	QFN28	QFN24	QFN20		QFN16		
A	0.90	0.90	0.90	0.90	0.90	±0.10	-
A1	0.02	0.02	0.02	0.02	0.02	+0.03/ -0.02	-
b	0.25	0.25	0.30	0.25	0.33	±0.02	-
c	0.20	0.20	0.20	0.20	0.20	Reference	-
D	4.00	4.00	5.00	4.00	4.00	Basic	-
D2	2.65	2.80	3.70	2.70	2.40	Reference	-
E	5.00	5.00	5.00	4.00	4.00	Basic	-
E2	3.65	3.80	3.70	2.70	2.40	Reference	-
e	0.50	0.50	0.65	0.50	0.65	Basic	-
L	0.40	0.40	0.40	0.40	0.60	±0.05	-
N	28	24	20	20	16	Reference	4
ND	6	5	5	5	4	Reference	6
NE	8	7	5	5	4	Reference	5

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NOTES:

1. Dimensioning and tolerancing per ASME Y14.5M-1994.
2. Tiebar view shown is a non-functional feature.
3. Bottom-side pin #1 I.D. is a diepad chamfer as shown.
4. N is the total number of terminals on the device.
5. NE is the number of terminals on the “E” side of the package (or Y-direction).
6. ND is the number of terminals on the “D” side of the package (or X-direction). ND = (N/2)-NE.
7. Inward end of terminal may be square or circular in shape with radius (b/2) as shown.
8. If two values are listed, multiple exposed pad options are available. Refer to device-specific datasheet.