

Precision 2.50V, 1.08µ-Watt, High Precision FGA™ Voltage References

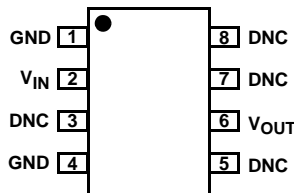
The ISL60007 FGA™ voltage references are extremely low power, very high precision analog voltage references fabricated in Intersil's proprietary Floating Gate Analog technology. The ISL60007 features low supply voltage operation at ultra-low 400nA operating current resulting in typical 1.08µW power consumption.

In addition, the ISL60007 family features guaranteed initial accuracy as low as ±0.5mV, temperature coefficients as tight as 3ppm/°C and long-term stability of 10ppm/√1kHrs.

The initial accuracy and thermal stability performance of the ISL60007 family plus the low power consumption eliminates the need to compromise accuracy and thermal stability for reduced power consumption making it an ideal high resolution, low power data conversion system.

Pinout

ISL60007 (8 LD SOIC)
TOP VIEW



Pin Descriptions

PIN NAME	DESCRIPTION
GND	Ground Connection
V _{IN}	Power Supply Input Connection
V _{OUT}	Voltage Reference Output Connection
DNC	Do Not Connect; Internal Connection - Must Be Left Floating

Ordering Information

PART NUMBER	PART MARKING	V _{OUT} OPTION	GRADE	TEMP. RANGE (°C)	PACKAGE	PKG. DWG. #
ISL60007BIB825	60007BI 25	2.500V	±0.5mV, 3ppm/°C	-40 to +85	8 Ld SOIC	MDP0027
ISL60007BIB825Z (Note)	60007BI Z25	2.500V	±0.5mV, 3ppm/°C	-40 to +85	8 Ld SOIC (Pb-free)	MDP0027
ISL60007CIB825	60007CI 25	2.500V	±0.5mV, 5ppm/°C	-40 to +85	8 Ld SOIC	MDP0027
ISL60007CIB825Z (Note)	60007CI Z25	2.500V	±0.5mV, 5ppm/°C	-40 to +85	8 Ld SOIC (Pb-free)	MDP0027
ISL60007DIB825	60007DI 25	2.500V	±1.0mV, 10ppm/°C	-40 to +85	8 Ld SOIC	MDP0027
ISL60007DIB825Z (Note)	60007DI Z25	2.500V	±1.0mV, 10ppm/°C	-40 to +85	8 Ld SOIC (Pb-free)	MDP0027

*Add "-TK" suffix for tape and reel.

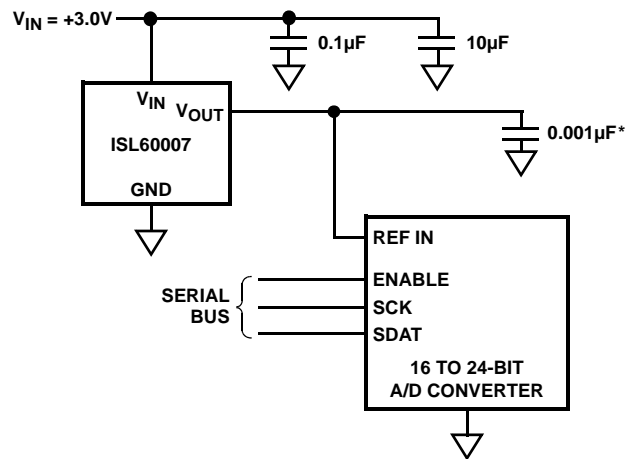
NOTE: Intersil Pb-free plus anneal products employ special Pb-free material sets; molding compounds/die attach materials and 100% matte tin plate termination finish, which are RoHS compliant and compatible with both SnPb and Pb-free soldering operations. Intersil Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020.

Features

- Reference Voltage 2.50V
- Absolute Initial Accuracy Options. . . . ±0.5mV, & ±1.0mV
- 1.08µW typical Power Consumption
- Supply Voltage Range 2.7V to 5.5V
- Ultra-Low Supply Current. 400nA
- Low Temperature Coefficient Options 3ppm/°C, 5ppm/°C, & 10ppm/°C
- Long Term Stability. 10ppm/√1kHrs
- 7mA Source & Sink Current
- ESD Protection. 5kV (Human Body Model)
- Standard 8 Ld SOIC Packaging
- Temperature Range -40°C to +85°C
- Pb-Free Plus Anneal Available (RoHS Compliant)

Applications

- High Resolution A/Ds & D/As
- Digital Meters
- Bar Code Scanners
- Mobile Communications
- PDA's and Notebooks
- Battery Management Systems
- Medical Systems

Typical Application

*Also see Figure 17 in Applications Information.

Absolute Maximum Ratings

Storage Temperature Range -65°C to +125°C
 Max Voltage V_{IN} to Gnd. -0.5V to +6.5V
 Max Voltage V_{OUT} to Gnd (10s) -0.5V to +3.50V
 Voltage on "DNC" Pins. No connections permitted to these pins.
 Lead Temperature, Soldering (10s) +225°C

Recommended Operating Conditions

Temperature Range (Industrial) -40°C to 85°C

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

Electrical Specifications Operating Conditions: $V_{IN} = 3.0V$, $I_{OUT} = 0mA$, $C_{OUT} = 0.001\mu F$, $T_A = -40$ to $+85^\circ C$, Unless Otherwise Specified.

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
2.500V OUTPUT VOLTAGE						
V_{OUT}	Output Voltage			2.500		V
V_{OA}	V_{OUT} Accuracy @ $T_A = 25^\circ C$	ISL60007B25	-0.5		+0.5	mV
		ISL60007C25	-0.5		+0.5	mV
		ISL60007D25	-1.0		+1.0	mV
TC V_{OUT}	Output Voltage Temperature Coefficient (Note 1)	ISL60007B25			3	ppm/ $^\circ C$
		ISL60007C25			5	ppm/ $^\circ C$
		ISL60007D25			10	ppm/ $^\circ C$
V_{IN}	Input Voltage Range		2.7		5.5	V
I_{IN}	Supply Current			400	800	nA
$\Delta V_{OUT}/\Delta V_{IN}$	Line Regulation	$+2.7V \leq V_{IN} \leq +5.5V$		30	200	$\mu V/V$
$\Delta V_{OUT}/\Delta I_{OUT}$	Load Regulation	Sourcing: $0mA \leq I_{OUT} \leq 7mA$		15	50	$\mu V/mA$
		Sinking: $-7mA \leq I_{OUT} \leq 0mA$		50	150	$\mu V/mA$
$\Delta V_{OUT}/\Delta t$	Long Term Stability (Note 4)	$T_A = 25^\circ C$		10		ppm/ $\sqrt{1kHrs}$
$\Delta V_{OUT}/\Delta T_A$	Thermal Hysteresis (Note 2)	$\Delta T_A = 125^\circ C$		50		ppm
I_{SC}	Short Circuit Current (Note 3)	$T_A = 25^\circ C$, V_{OUT} tied to Gnd		40	80	mA
V_N	Output Voltage Noise	$0.1Hz \leq f \leq 10Hz$		30		μV_{p-p}

NOTES:

- Over the specified temperature range. Temperature coefficient is measured by the box method whereby the change in V_{OUT} is divided by the temperature range; in this case, $-40^\circ C$ to $+85^\circ C = 125^\circ C$.
- Thermal Hysteresis is the change in V_{OUT} measured @ $T_A = 25^\circ C$ after temperature cycling over a specified range, ΔT_A . V_{OUT} is read initially at $T_A = 25^\circ C$ for the device under test. The device is temperature cycled and a second V_{OUT} measurement is taken at $25^\circ C$. The difference between the initial V_{OUT} reading and the second V_{OUT} reading is then expressed in ppm. For $\Delta T_A = 125^\circ C$, the device under test is cycled from $+25^\circ C$ to $+85^\circ C$ to $-40^\circ C$ to $+25^\circ C$.
- Guaranteed by device characterization and/or correlation to other device tests.
- FGA voltage reference long term drift is a logarithmic characteristic. Changes that occur after the first few hundred hours of operation are significantly smaller with time, asymptotically approaching zero beyond 1000 hours. Because of this decreasing characteristic, long term drift is specified in ppm/ $\sqrt{1kHrs}$.

Typical Performance Curves, 2.5V Reference

$V_{IN} = 3.0V$, $I_{OUT} = 0mA$, $T_A = 25^\circ C$
Unless Otherwise Specified

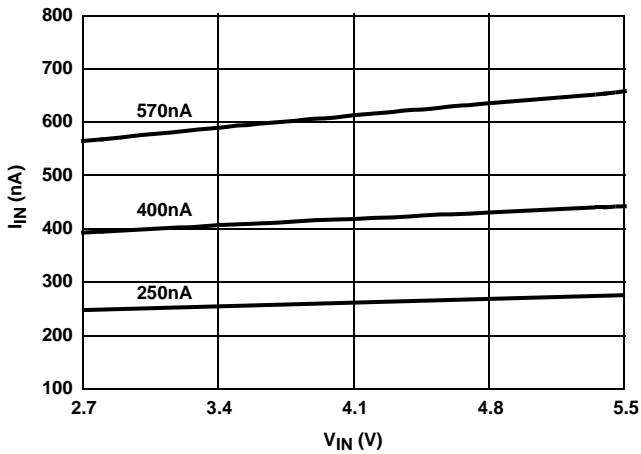


FIGURE 1. I_{IN} vs V_{IN} - 3 UNITS

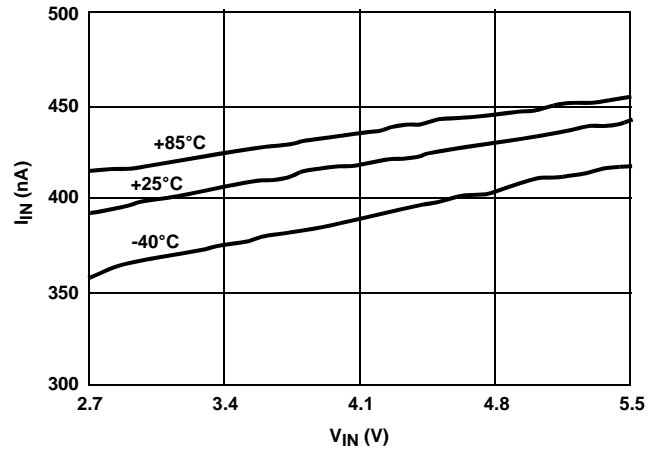


FIGURE 2. I_{IN} vs V_{IN} - 3 TEMPS

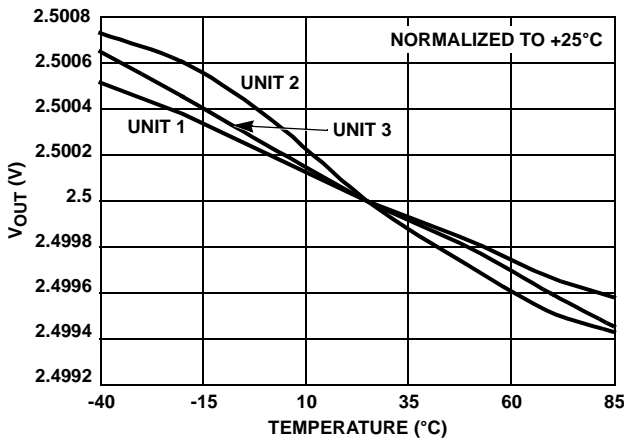


FIGURE 3. V_{OUT} vs TEMP - 3 UNITS

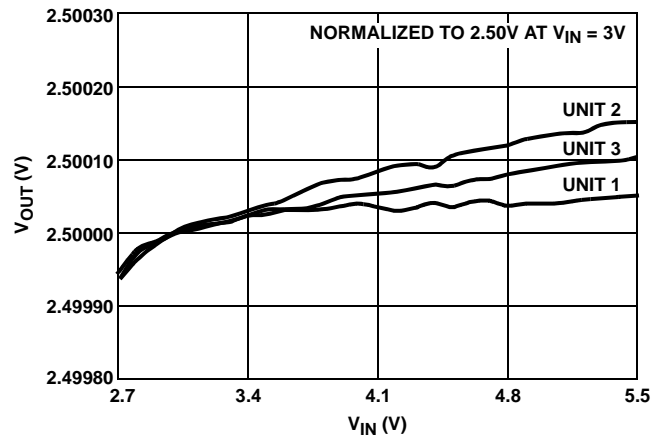


FIGURE 4. LINE REGULATION - 3 UNITS

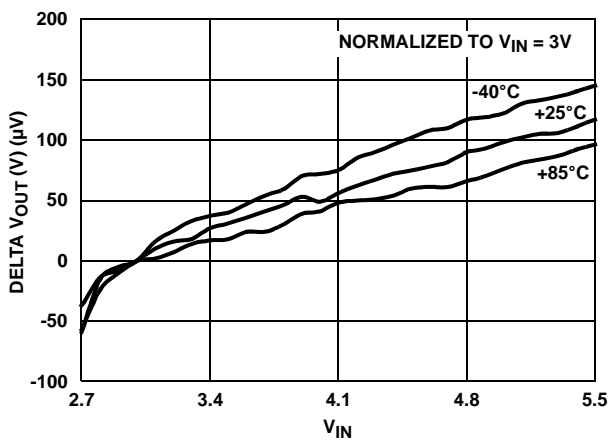


FIGURE 5. LINE REGULATION - 3 TEMPS

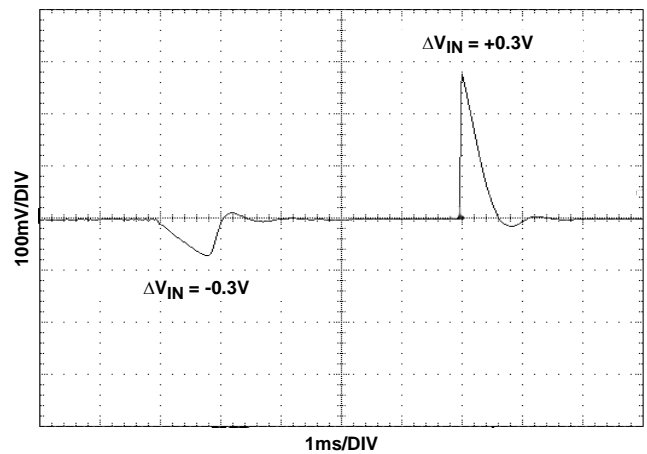


FIGURE 6. LINE TRANSIENT RESPONSE, $C_L = 0nF$

Typical Performance Curves, 2.5V Reference

$V_{IN} = 3.0V$, $I_{OUT} = 0mA$, $T_A = 25^\circ C$
 Unless Otherwise Specified (Continued)

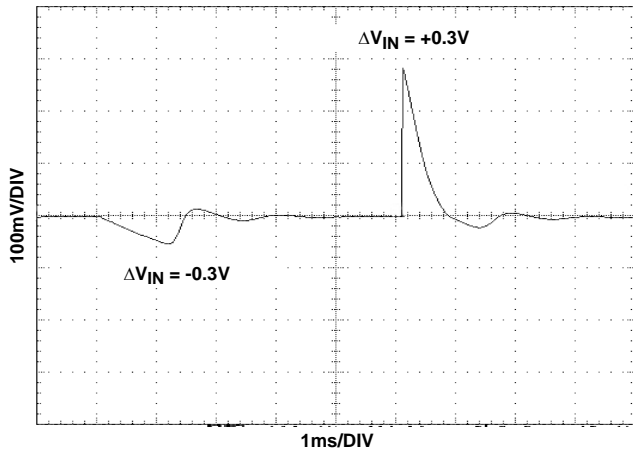


FIGURE 7. LINE TRANSIENT RESPONSE, $C_L = 1nF$

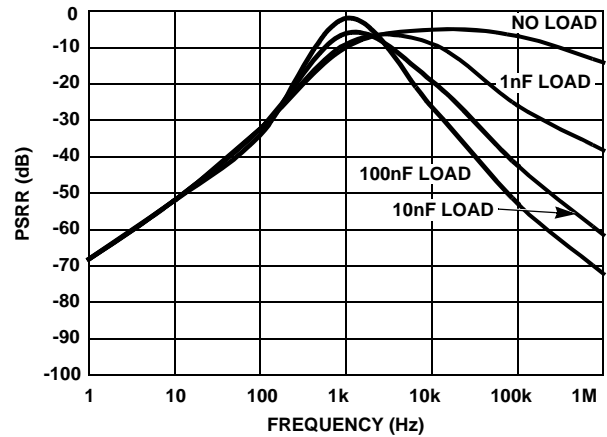


FIGURE 8. PSRR vs f vs C_L

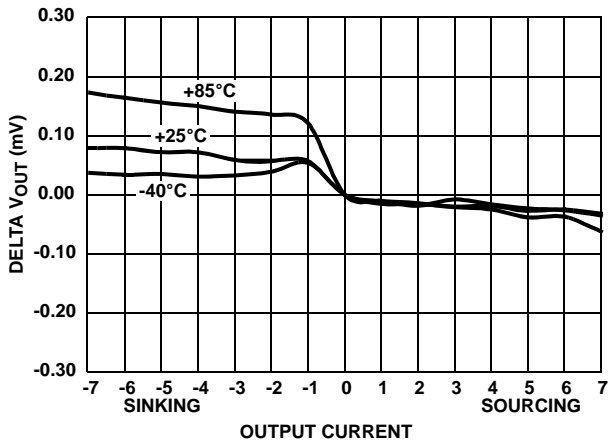


FIGURE 9. LOAD REGULATION vs TEMP

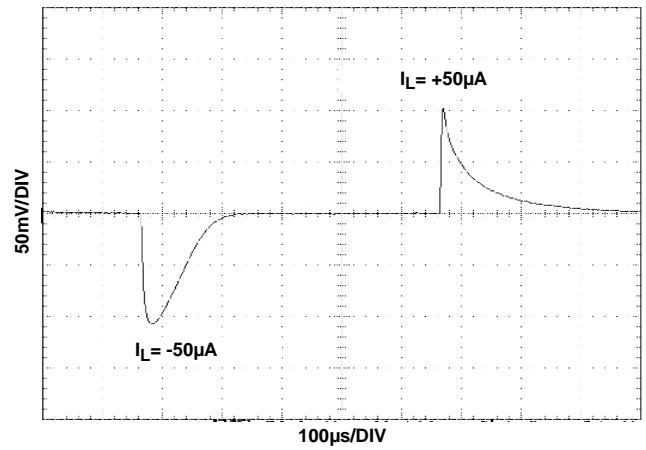


FIGURE 10. LOAD TRANSIENT RESPONSE @ $I_L = 50\mu A$, $C_L = 1nF$

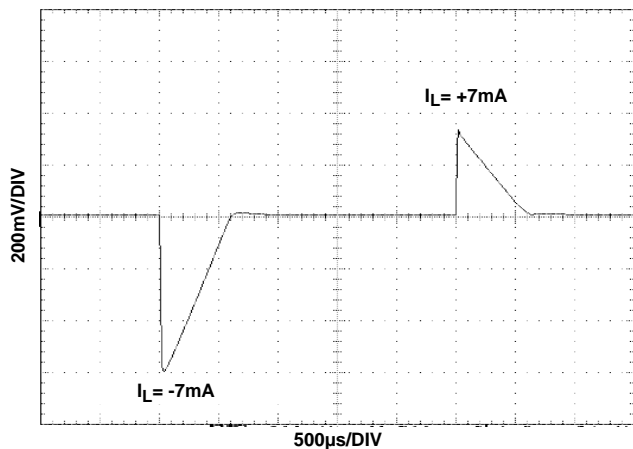


FIGURE 11. LOAD TRANSIENT RESPONSE @ $I_L = 7mA$, $C_L = 1nF$

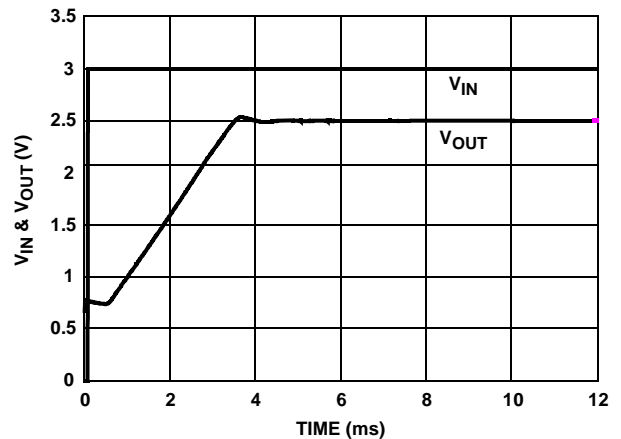


FIGURE 12. TURN-ON TIME @ $T_A = 25^\circ C$

Typical Performance Curves, 2.5V Reference

$V_{IN} = 3.0V$, $I_{OUT} = 0mA$, $T_A = 25^\circ C$
 Unless Otherwise Specified (Continued)

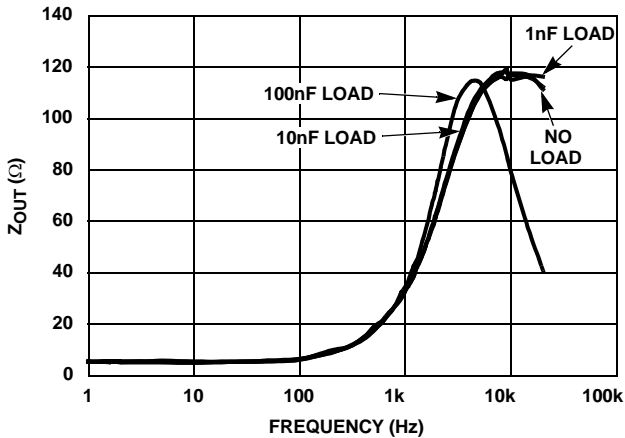


FIGURE 13. Z_{OUT} vs f vs C_L

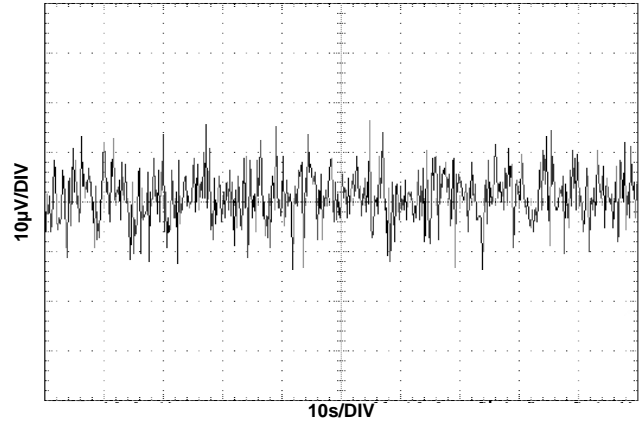


FIGURE 14. V_{OUT} NOISE

Applications Information

FGA Technology

The ISL60007 series of voltage references use the floating gate technology to create references with very low drift and supply current. Essentially the charge stored on a floating gate cell is set precisely in manufacturing. The reference voltage output itself is a buffered version of the floating gate voltage. The resulting reference device has excellent characteristics which are unique in the industry: very low temperature drift, high initial accuracy, and almost zero supply current. Also, the reference voltage itself is not limited by voltage bandgaps or zener settings, so a wide range of reference voltages can be programmed (standard voltage settings are provided, but customer-specific voltages are available).

The process used for these reference devices is a floating gate CMOS process, and the amplifier circuitry uses CMOS transistors for amplifier and output transistor circuitry. While providing excellent accuracy, there are limitations in output noise level and load regulation due to the MOS device characteristics. These limitations are addressed with circuit techniques discussed in other sections.

Nanopower Operation

Reference devices achieve their highest accuracy when powered up continuously, and after initial stabilization has taken place. This drift can be eliminated by leaving the power on continuously.

The ISL60007 is the first high precision voltage reference with ultra low power consumption that makes it possible to leave power on continuously in battery operated circuits. The ISL60007 consumes extremely low supply current due to the proprietary FGA technology. Supply current at room temperature is typically 400nA which is 1 to 2 orders of magnitude lower than competitive devices. Application

circuits using battery power will benefit greatly from having an accurate, stable reference which essentially presents no load to the battery.

In particular, battery powered data converter circuits that would normally require the entire circuit to be disabled when not in use can remain powered up between conversions as shown in Figure 15. Data acquisition circuits providing 12 to 24 bits of accuracy can operate with the reference device continuously biased with no power penalty, providing the highest accuracy and lowest possible long term drift.

Other reference devices consuming higher supply currents will need to be disabled in between conversions to conserve battery capacity. Absolute accuracy will suffer as the device is biased and requires time to settle to its final value, or, may not actually settle to a final value as power on time may be short.

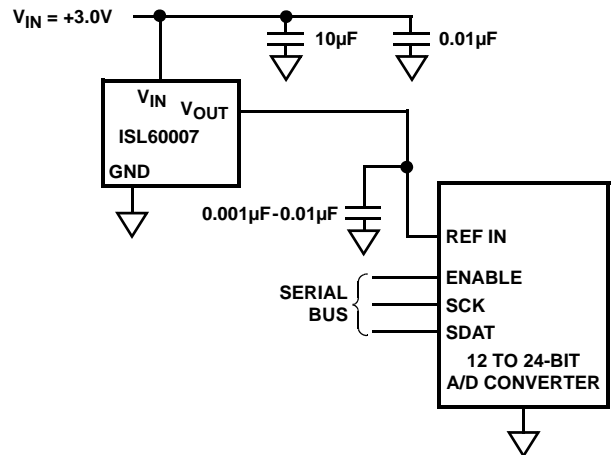


FIGURE 15.

Board Mounting Considerations

For applications requiring the highest accuracy, board mounting location should be reviewed. Placing the device in areas subject to slight twisting can cause degradation of the accuracy of the reference voltage due to die stresses. It is normally best to place the device near the edge of a board, or the shortest side, as the axis of bending is most limited at that location. Obviously mounting the device on flexprint or extremely thin PC material will likewise cause loss of reference accuracy.

Noise Performance and Reduction

The output noise voltage in a 0.1Hz to 10Hz bandwidth is typically $30\mu\text{V}_{\text{P-P}}$. This is shown in the plot in the Typical Performance Curves. The noise measurement is made with a bandpass filter made of a 1 pole high-pass filter with a corner frequency at 0.1Hz and a 2-pole low-pass filter with a corner frequency at 12.6Hz to create a filter with a 9.9Hz bandwidth. Noise in the 10kHz to 1MHz bandwidth is approximately $400\mu\text{V}_{\text{P-P}}$ with no capacitance on the output, as shown in Figure 16. These noise measurements are made with a 2 decade bandpass filter made of a 1 pole high-pass filter with a corner frequency at 1/10 of the center frequency and 1-pole low-pass filter with a corner frequency at 10 times the center frequency. Figure 16 also shows the noise in the 10kHz to 1MHz band can be reduced to about $50\mu\text{V}_{\text{P-P}}$ using a $0.001\mu\text{F}$ capacitor on the output. Noise in the 1kHz to 100kHz band can be further reduced using a $0.1\mu\text{F}$ capacitor on the output, but noise in the 1Hz to 100Hz band increases due to instability of the very low power amplifier with a $0.1\mu\text{F}$ capacitance load. For load capacitances above $0.001\mu\text{F}$ the noise reduction network shown in Figure 17 is recommended. This network reduces noise significantly over the full bandwidth. As shown in Figure 16, noise is reduced to less than $40\mu\text{V}_{\text{P-P}}$ from 1Hz to 1MHz using this network with a $0.01\mu\text{F}$ capacitor and a $2\text{k}\Omega$ resistor in series with a $10\mu\text{F}$ capacitor.

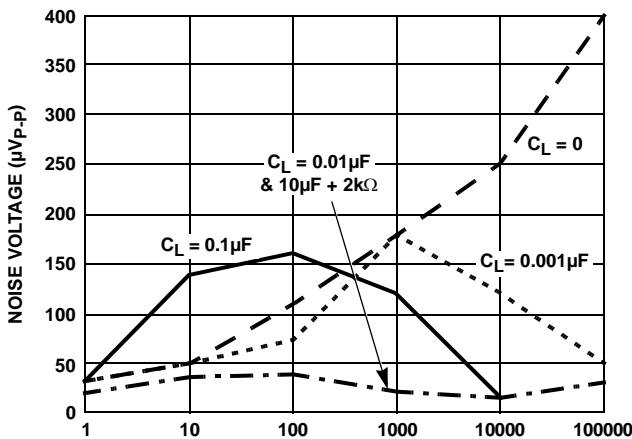


FIGURE 16. NOISE REDUCTION

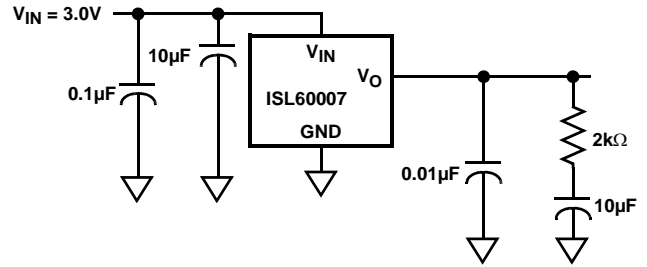


FIGURE 17.

Turn-On Time

The ISL60007 devices operate with ultra-low supply current and thus the time to bias up internal circuitry to final values will be longer than with references that require higher current. Normal turn-on time is typically 4ms. This is shown in Figure 18. Since devices can vary in supply current down to 250nA, turn-on time can last up to about 6ms. Care should be taken in system design to include this delay before measurements or conversions are started.

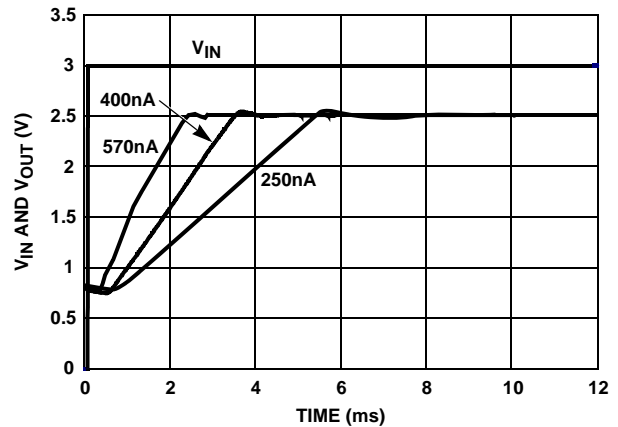


FIGURE 18. TURN-ON TIME (+25°C)

Temperature Coefficient

The limits stated for temperature coefficient (tempco) are governed by the method of measurement. The overwhelming standard for specifying the temperature drift of a reference is to measure the reference voltage at two temperatures, take the total variation, $(V_{\text{HIGH}} - V_{\text{LOW}})$, and divide by the temperature extremes of measurement $(T_{\text{HIGH}} - T_{\text{LOW}})$. The result is divided by the nominal reference voltage (at $T = 25^\circ\text{C}$) and multiplied by 10^6 to yield ppm/ $^\circ\text{C}$. This is the "Box" method for specifying temperature coefficient.

Typical Application Circuits

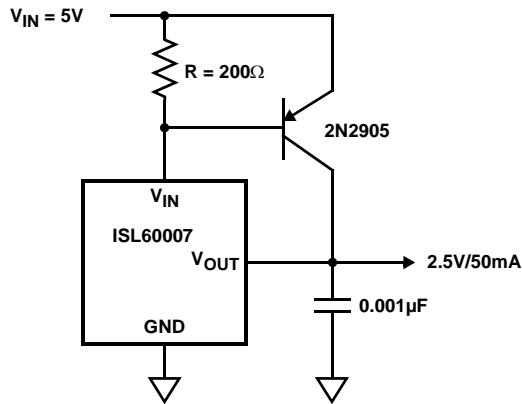


FIGURE 19. PRECISION 2.5V, 50mA REFERENCE

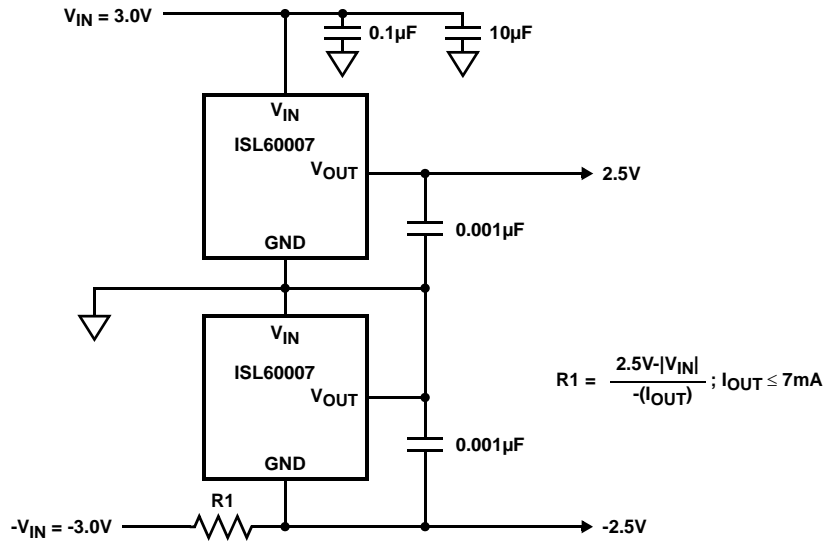


FIGURE 20. ±2.5V DUAL OUTPUT, HIGH ACCURACY REFERENCE

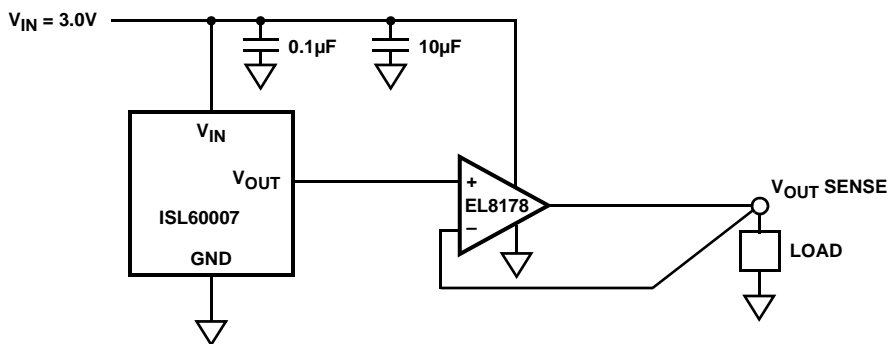
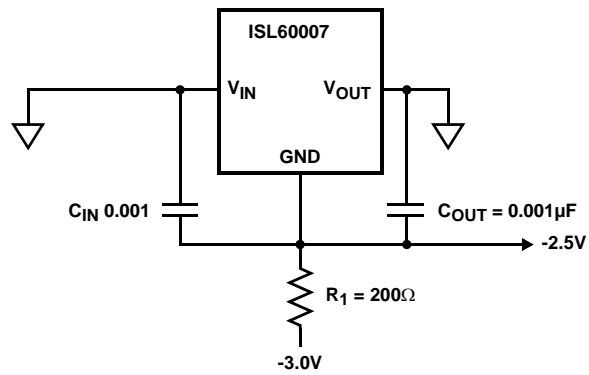


FIGURE 21. KELVIN SENSED LOAD

Typical Application Circuits (Continued)



R₁ LIMITS MAX LOAD CURRENT
with R₁ = 200Ω; I_{LOAD MAX} = 2.5mA
 $R_1 = \frac{2.5V - |V_{IN}|}{-(I_{OUT})}$; I_{OUT} ≤ 7mA

FIGURE 22. NEGATIVE VOLTAGE REFERENCE

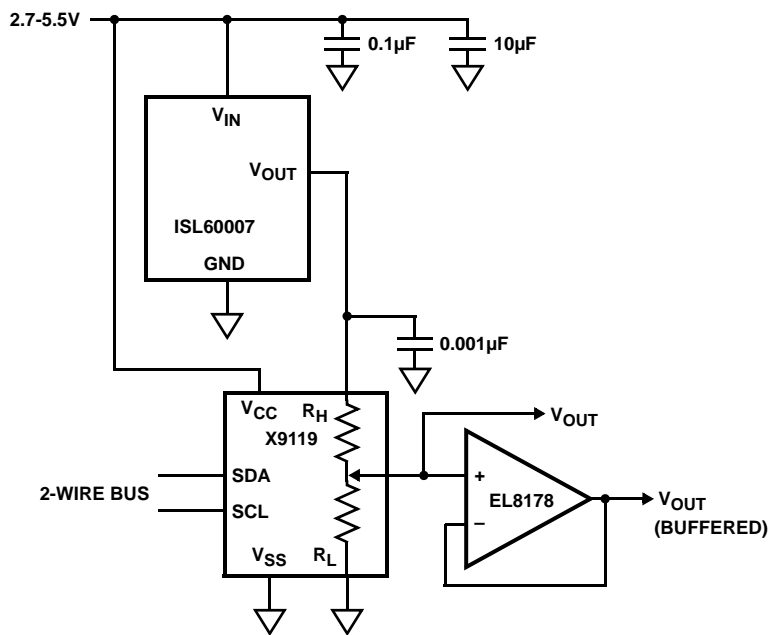
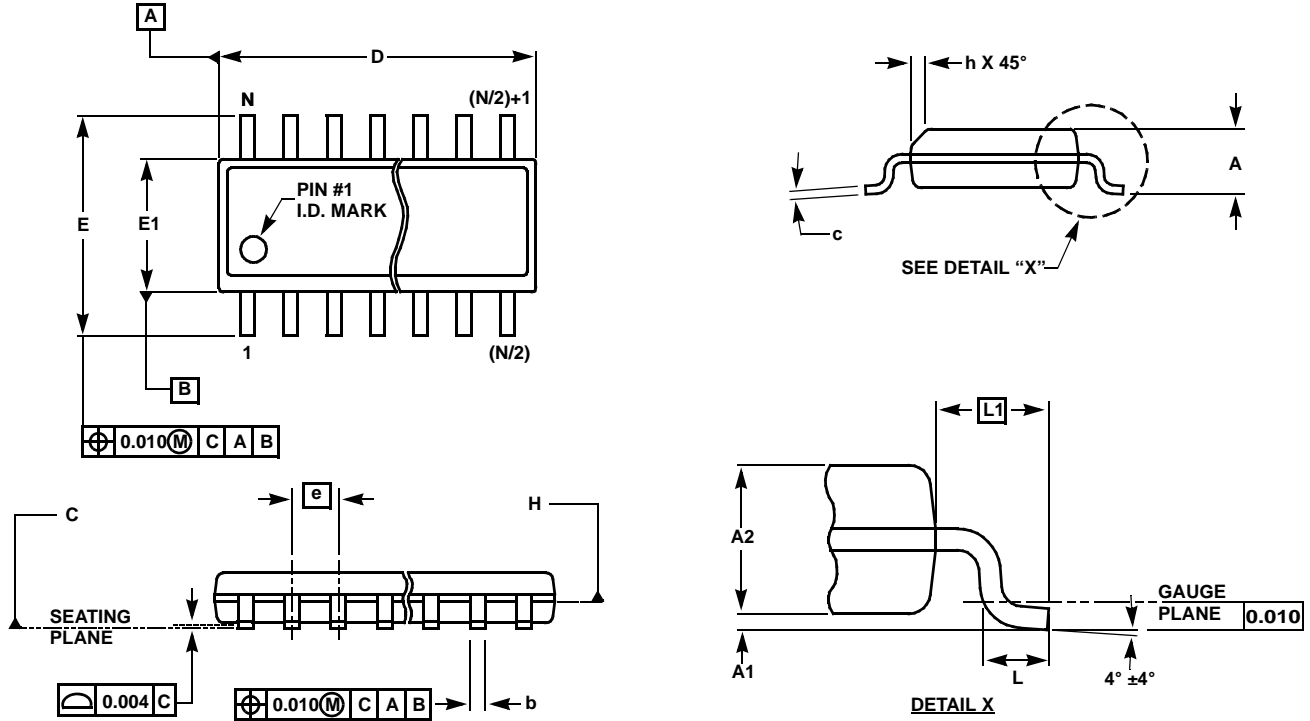


FIGURE 23. 2.5V FULL SCALE LOW-DRIFT 10-BIT ADJUSTABLE VOLTAGE SOURCE

Small Outline Package Family (SO)



MDP0027

SMALL OUTLINE PACKAGE FAMILY (SO)

SYMBOL	SO-8	SO-14	SO16 (0.150")	SO16 (0.300") (SOL-16)	SO20 (SOL-20)	SO24 (SOL-24)	SO28 (SOL-28)	TOLERANCE	NOTES
A	0.068	0.068	0.068	0.104	0.104	0.104	0.104	MAX	-
A1	0.006	0.006	0.006	0.007	0.007	0.007	0.007	± 0.003	-
A2	0.057	0.057	0.057	0.092	0.092	0.092	0.092	± 0.002	-
b	0.017	0.017	0.017	0.017	0.017	0.017	0.017	± 0.003	-
c	0.009	0.009	0.009	0.011	0.011	0.011	0.011	± 0.001	-
D	0.193	0.341	0.390	0.406	0.504	0.606	0.704	± 0.004	1, 3
E	0.236	0.236	0.236	0.406	0.406	0.406	0.406	± 0.008	-
E1	0.154	0.154	0.154	0.295	0.295	0.295	0.295	± 0.004	2, 3
e	0.050	0.050	0.050	0.050	0.050	0.050	0.050	Basic	-
L	0.025	0.025	0.025	0.030	0.030	0.030	0.030	± 0.009	-
L1	0.041	0.041	0.041	0.056	0.056	0.056	0.056	Basic	-
h	0.013	0.013	0.013	0.020	0.020	0.020	0.020	Reference	-
N	8	14	16	16	20	24	28	Reference	-

Rev. L 2/01

NOTES:

1. Plastic or metal protrusions of 0.006" maximum per side are not included.
2. Plastic interlead protrusions of 0.010" maximum per side are not included.
3. Dimensions "D" and "E1" are measured at Datum Plane "H".
4. Dimensioning and tolerancing per ASME Y14.5M-1994

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